Personal System/2®
Model P70
Technical Reference

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Preface

The Technical Reference library is intended for those who develop hardware and software products for IBM Personal Computers and IBM Personal System/2. Users should understand computer architecture and programming concepts.

This technical reference provides hardware and software interface information for the IBM Personal System/2 Model P70 and should be used with the following publications:

IBM Personal System/2 Hardware Interface Technical Reference

IBM Personal System/2 and Personal Computer BIOS Interface Technical Reference

This manual consists of the following sections:

Section 1, "System Overview," describes the system, features, and specifications.

Section 2, "Programmable Option Select," describes the registers used for configuration.

Section 3, "System Board," describes the system-specific hardware implementations.

Section 4, "Video Subsystem," describes the function of the plasma display and the display adapter card.

Warning: The term "Reserved" describes certain signals, bits, and registers that should not be changed. Use of reserved areas can cause compatibility problems, loss of data, or permanent damage to the hardware. When the contents of a register are changed, the state of the reserved bits must be preserved. When possible, read the register first and change only the bits that must be changed.

For information about components or devices not described in this manual, refer to the *Hardware Interface Technical Reference.* Information about diskette drives, fixed disk drives, adapters, and external options are in separate option technical references.

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Section 1. System Overview

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Description

The IBM Personal System/2 Model P70 is a self-contained, portable computer system with a built-in keyboard and a built-in plasma display. It is equipped with one diskette drive and one fixed disk drive. And it can support one external storage device additionally.

Programs identify the type by reading the model and submodel bytes. The model and submodel byte for this system is hex F8 and 0B, respectively. Interrupt hex 15, function code (AH) = hex C0, returns the model and submodel bytes and BIOS revision code.

Refer to the *IBM Personal System/2 and Personal Computer BIOS Interface Technical Reference* for a listing of other systems, and check the supplements section for updates to that listing.

System Board Features

The following figure lists the system board devices and features. The *Hardware Interface Technical Reference* describes devices common to PS/2 products by type number.

Device	Type	Features
Microprocessor	---	80386 32-bit address and 32-bit data interface
System Timers	1	Channel 0 – System timer Channel 2 – Tone generation for speaker Channel 3 – Watchdog timer
ROM Subsystem	---	128KB (KB = 1024 bytes)
RAM Subsystem	---	System board, 4 to 8MB (MB = 1,048,576 bytes) Expandable on the channel
CMOS RAM Subsystem	---	64-byte CMOS RAM with real-time clock/calendar 2KB CMOS RAM extension Battery backup
Audio Subsystem	1	Driven by: - System-timer channel 2 - The 'audio sum node' signal.
DMA Controller	1	Eight independent DMA channels Single or burst transfers and read verification
Interrupt Controller	1	16 levels of system interrupts Interrupts are level-sensitive
Keyboard/Auxiliary Device Controller	1	Keyboard connector Auxiliary device connector Password security
Diskette Drive Controller	1	Supports: - 720KB formatted diskette density - 1.44MB formatted diskette density. Auxiliary connector for an external storage device
Serial Controller	2	RS-232C interface Programmable as serial port 1 or 2 FIFO mode and character mode
Parallel Controller	1	Programmable as parallel port 1, 2, or 3 Supports bidirectional input and output
Micro Channel	---	Two channel connectors: - One 16-bit connector for half-length adapter card - One 32-bit connector with matched-memory extension.
Math Coprocessor Socket	---	Supports 80387 math coprocessor Same clock speed as the system microprocessor
Power Supply	1	100 to 240 Vac support

Figure 1-1. System Board Devices and Features

System Board Block Diagram

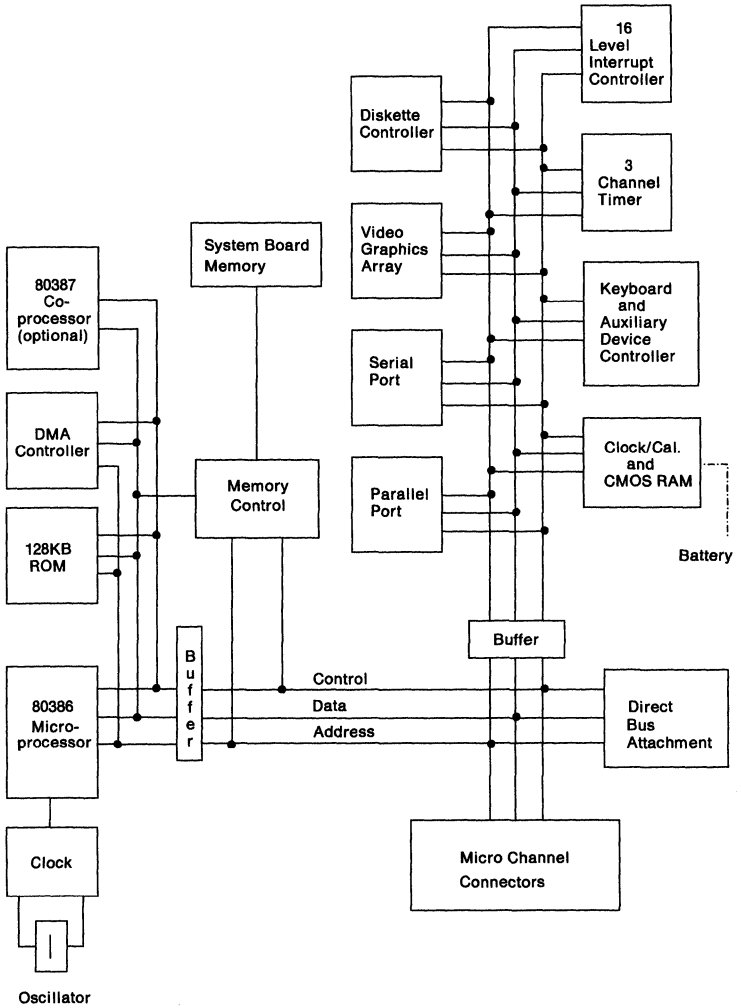


Figure 1-2. System Board

Note: Additional memory can be added in any of the 32-bit Micro Channel connectors. However, the total amount of memory installed should not exceed the 16MB addressing limit of the DMA controller.

System Board I/O Address Map

Hex Addresses	Device
0000 - 001F	DMA Controller (0–3)
0020, 0021	Interrupt Controller (Master)
0040, 0042 - 0044, 0047	System Timers
0060	Keyboard, Auxiliary Device
0061	System Control Port B
0064	Keyboard, Auxiliary Device
0070, 0071	RT/CMOS and NMI Mask
0081 - 0083, 0087	DMA Page Registers (0–3)
0089 - 008B, 008F	DMA Page Registers (4–7)
0090	Central Arbitration Control Point
0091	Card Selected Feedback Register
0092	System Control Port A
0094	System Board Enable/Setup Register
0096	Adapter Enable/Setup Register
00A0 - 00A1	Interrupt Controller (Slave)
00C0 - 00DF	DMA Controller (4–7)
00E0, 00E1	Memory Encoding Registers
00F0 - 00FF	Math Coprocessor
0100 - 0107	Programmable Option Select
0278 - 027B	Parallel Port 3
02F8 - 02FF	Serial Port 2 (RS-232C)
0378 - 037B	Parallel Port 2
03B4, 03B5, 03BA	Video Subsystem
03BC - 03BF	Parallel Port 1
03C0 - 03C5	Video Subsystem
03C6 - 03C9	Video DAC
03CA, 03CC, 03CE, 03CF	Video Subsystem
03D4, 03D5, 03DA	Video Subsystem
03F0 - 03F7	Diskette Drive Controller
03F8 - 03FF	Serial Port 1 (RS-232C)
3510 - 3518	Fixed Disk Drive Controller

Figure 1-3. System Board I/O Address Map

Specifications

Device	Number of Waits	Cycle Time (ns)
Microprocessor (20 MHz – 50 ns Clock):		
Access to System Board RAM: *		
Memory Read (Page Hit)	0	100
Memory Read (Page Miss)	2	200
Memory Write (Page Hit)	1	150
Memory Write (Page Miss)	2	200
Access to Channel:		
Default Transfer Cycle	2	200
Extended Transfer Cycle	4	300
Refresh Rate (Typically performed every 15.1 μs)		500 (min)
Bus Master Access to System Board RAM		300 (min)
DMA Controller (10 MHz – 100 ns Clock):		
Single Transfer: 300 + I/O Access + Memory Access		
Burst Transfers: 300 + (I/O Access + Memory Access)N **		
System Board Memory Access		300
Default Transfer Cycle		200
Extended Transfer Cycle		300

* Adapters installed in the channel should not rely on monitoring system board memory accesses because channel memory control signals may not be present during these accesses.

** N is the number of transfers in the burst.

Figure 1-4. Performance Specifications

Size:	
Width	465 mm (18.3 in)
Depth	126 mm (5.0 in)
Height	306.3 mm (12.1 in)
Air Temperature:	
System On	10.0 to 35.0°C (50 to 95°F)
System Off	5.0 to 60.0°C (41 to 140°F)
Humidity:	
System On	20% to 80%
System Off	5% to 95%
Maximum Altitude	2133.6 m (7000 ft)
Heat Output	150 W
Acoustical Readings	
See Figure 1-6 on page 1-9	
Electrical:	
Power Supply Input:	
Low Range	90 (min) - 137 (max) Vac
High Range	180 (min) - 264 (max) Vac
Maximum Current Draw :	
Low Range	4.0 A
High Range	2.0 A
Frequency	50 ± 3Hz/60 ± 3Hz
Electromagnetic Compatibility	FCC Class B / VCCI Class 2 / GOP

Figure 1-5. Physical Specifications

Description	L_{WAd} in bels Operate	Idle	L_{pAm} in dB Operate	Idle	$<L_{pA}>_m$ in dB Operate	Idle
Model P70	5.2	5.0	45	40	39	37

Notes:

L_{WAd} is the declared sound power level for the random sample of machines.

L_{pAm} is the mean value of the A-weighted sound pressure levels at the operator position (if any) for the random sample of machines.

$<L_{pA}>_m$ is the mean value of the A-weighted sound pressure levels at the one-meter positions for the random sample of machines.

These measurements are preliminary data and subject to change.

Figure 1-6. Acoustical Readings

Dimensions for Micro Channel adapter

The system board provides channel connectors to support the following types of adapters.

- 8 or 16 bit MC adapter slot (half-length)
- 8, 16, or 32 bit MC adapter slot (full-length)

The following figures show the dimensions of the half-length adapter card, it's retainer and the associated mounting hardware. The other dimensions (ie. connector dimensions, holder dimensions) are as same as the standard size (full-length) adapter card's dimensions which are described in the "Hardware Interface Technical Reference".

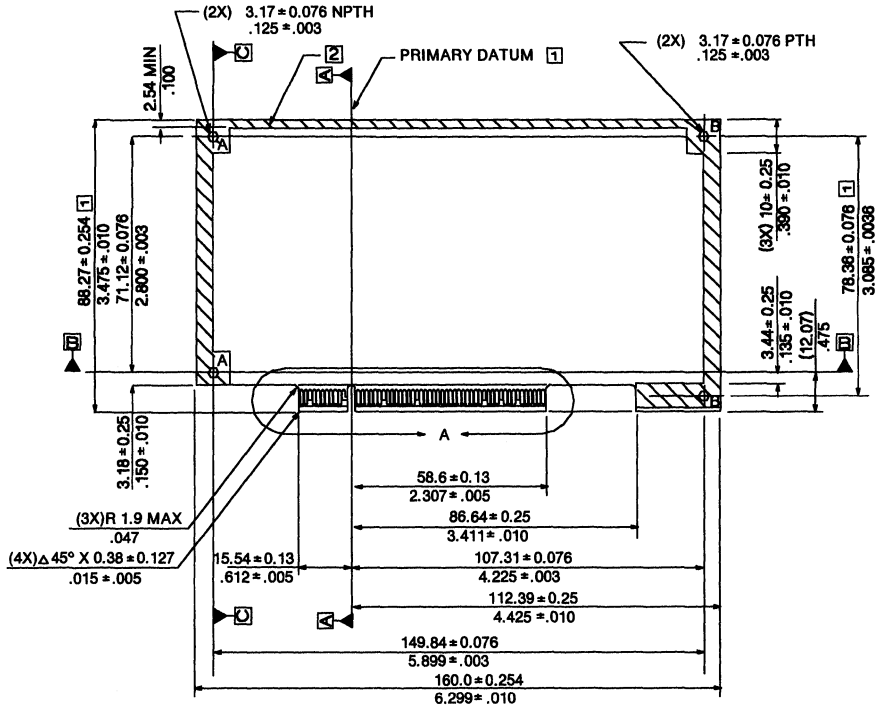


Figure 1-7. Adapter Dimensions (8 or 16-bit)

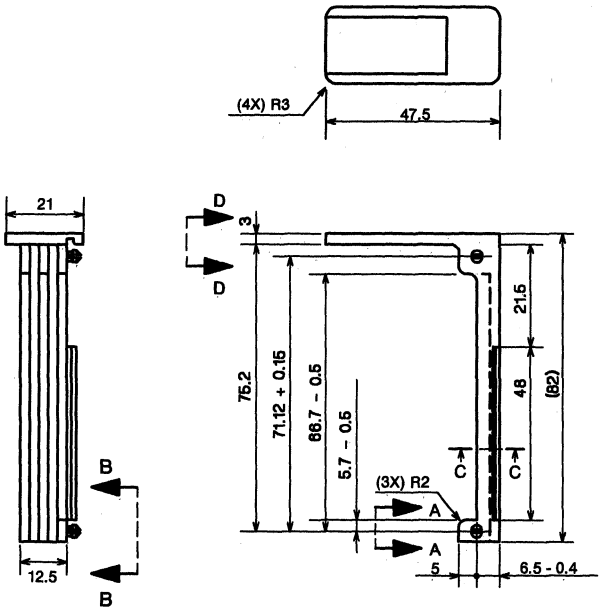
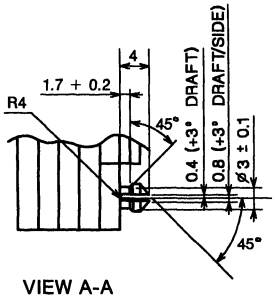
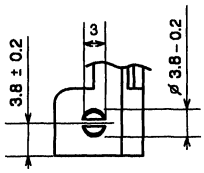


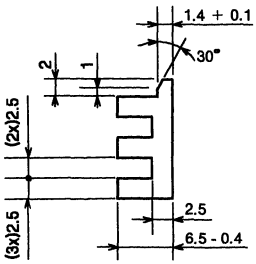
Figure 1-8 (Part 1 of 2). Adapter Retainer



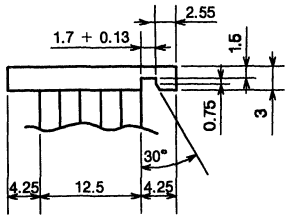
VIEW A-A



VIEW B-B

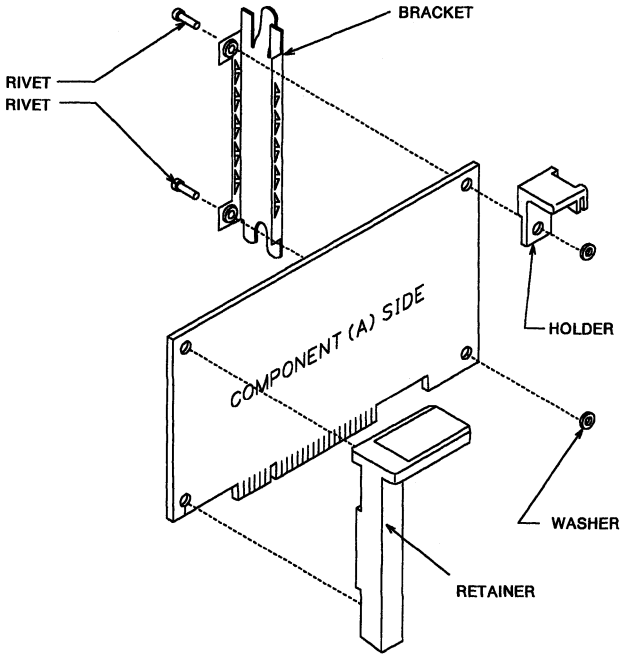


SECTION C-C



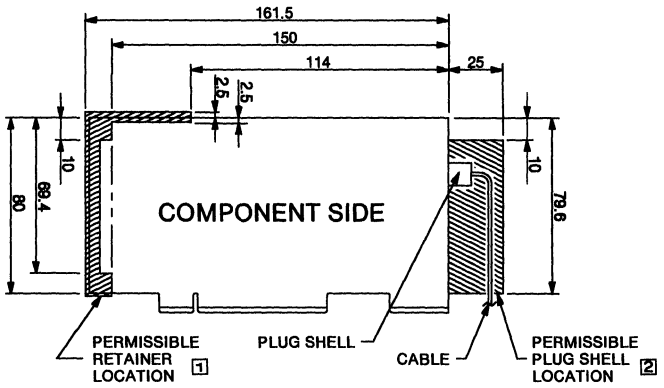
VIEW D-D

Figure 1-8 (Part 2 of 2). Adapter Retainer



MATERIALS:
HOLDER AND RETAINER - POLYCARBONATE UL 94 V-0
BRACKET - AISI TYPE 302 1/4 HARD STAINLESS STEEL

Figure 1-9. Typical Adapter Assembly



1 Permissible Retainer height to be 17mm max. on the component side.

2 Plug Cable to be bent by 90° in the shaded area.

Figure 1-10. Permissive Areas (Harf-Lenght Adapter)

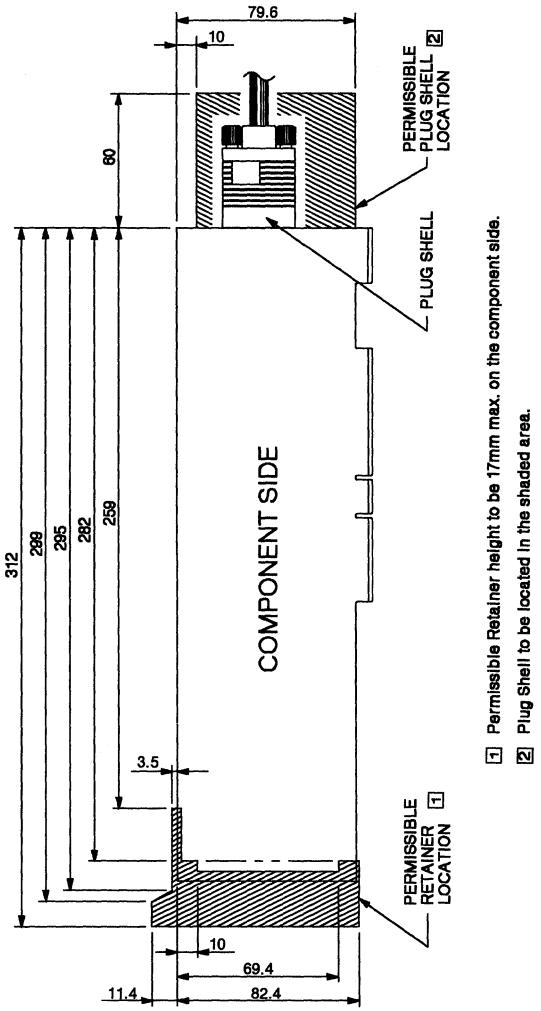


Figure 1-11. Permissive Areas (Full-Lenght Adapter)

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Notes:

Description

Programmable Option Select (POS) eliminates the need for switches by replacing their function with programmable registers. This section describes the POS information used on the Model P70 system boards. For additional POS information, refer to the *Hardware Interface Technical Reference.*

Warning:

- IBM recommends that programmable options be set only through the System Configuration utilities. Directly setting the POS registers or CMOS RAM POS parameters can result in multiple assignment of the same system resource, improper operation of the feature, loss of data, or possible damage to the hardware.
- Application programs should not use the adapter identification (ID) unless absolutely necessary. Compatibility problems can result.
- If an adapter and the system board are in setup mode at the same time, bus contention will occur, no useful programming can take place, and damage to the hardware can occur.
- After setup operations are complete, the Adapter Enable/Setup register (hex 0096) should be set to hex 00, and the System Board Enable/Setup register (hex 0094) should be set to hex FF.
- The channel reset bit (bit 7) in the Adapter Enable/Setup register must be 0 to program the adapters.
- The system board does not support 16-bit I/O operations to 8-bit POS registers. Using 16-bit I/O instructions on 8-bit POS registers will cause erroneous data to be written to or read from the registers. Only 8-bit transfers are supported for setup operations.

Setup functions respond to I/O addresses hex 0100 through 0107 only when their unique setup signal is active. The following precautions must be taken before setting individual bits in the POS registers.

Video Subsystem Setup:

- The Adapter Enable/Setup register (hex 0096) must be set to hex 0B to setup the Video Subsystem.
- Bit 7 in the System Board Enable/Setup register (hex 0094) must be set to 1 to avoid driving a 'setup' signal to system board functions.

Adapter Setup:

- Bit 3 in the Adapter Enable/Setup register must be set to 1 to allow adapter setup.
- Bit 7 in the System Board Enable/Setup register must be set to 1 to avoid driving a 'setup' signal to a system board function.

System Board Setup:

- Bit 7 in the System Board Enable/Setup register must be set to 0 to allow setup of other system board functions.
- Bit 3 in the Adapter Enable/Setup register must be set to 0 to avoid driving a 'setup' signal to an adapter.

POS Address Map

The following figure shows the organization of the I/O address space used by POS. Bit 0 of POS Register 2 and bits 6 and 7 of POS Register 5 are fixed. All other bits in POS Registers 2 through 5 are free-form.

Address (Hex)	Function
0094	System Board Enable/Setup Register
0096	Adapter Enable/Setup Register
0100	POS Register 0—Adapter Identification Byte (Low Byte)
0101	POS Register 1—Adapter Identification Byte (High Byte)
0102	POS Register 2—Option Select Data Byte 1 Bit 0 is Card Enable.
0103	POS Register 3—Option Select Data Byte 2
0104	POS Register 4—Option Select Data Byte 3
0105	POS Register 5—Option Select Data Byte 4 Bit 7 is the channel check active indicator Bit 6 is the channel check status-available indicator
0106	POS Register 6—Subaddress Extension (Low Byte)
0107	POS Register 7—Subaddress Extension (High Byte)

Figure 2-1. POS I/O Address Map

Card Selected Feedback

When an adapter is addressed, it responds by setting the '-card selected feedback' signal (-CD SFDBK) to active. -CD SFDBK is derived from the address decode and driven by a totem pole driver. It is latched by the system board and can be read through the Card Selected Feedback register at address hex 0091. Diagnostic and automatic configuration programs use this signal to verify the operation of an adapter at a given address or DMA port. This signal must not be active during a setup cycle.

The Card Selected Feedback register is a read-only register at address hex 0091. It allows programs to monitor -CD SFDBK and thereby determine if the video subsystem, system board I/O, or an adapter is addressed and functioning.

Bit	Function
7 - 1	Reserved
0	-Card Selected Feedback

Figure 2-2. Card Selected Feedback Register (Hex 0091)

Bits 7 - 1 Reserved.

Bit 0 This bit is set to 1 whenever -CD SFDBK was active on a previous cycle or whenever the system board I/O functions (diskette drive, serial, or parallel interfaces) are accessed by an I/O cycle. Reading this register resets the bit to 0.

System Board Setup

The integrated I/O functions on the system board use POS information during setup. The diskette drive controller, serial port, and parallel port are treated as a single device. The video subsystem is also an integrated part of the system board, however, POS treats it as a separate device. The System Board Enable/Setup register is used to place the system board or the video subsystem into the setup mode.

System Board Enable/Setup Register (Hex 0094)

This is a read/write register; all bits in this register default to 1 (enabled).

Bit	Function
7	Enable/-Setup System Board Functions
6 - 0	Reserved

Figure 2-3. System Board Enable/Setup Register (Hex 0094)

Bit 7 When this bit is set to 0, various system board I/O functions are placed in the setup mode. The diskette drive controller, serial port, and parallel port are controlled through System Board POS Register 2 (hex 0102). The POS information for memory is in System Board POS Register 3 (hex 0103).

When this bit is set to 1, the system board function is enabled.

Bits 6 - 0 Reserved.

System Board POS Register 2 (Hex 0102)

When the system board is in the setup mode, the diskette drive controller, serial port, and parallel port are controlled by this read/write register. Reading this register returns the current state of these system board functions.

Bit	Function
7	Disable Parallel Port Extended Mode
6, 5	Parallel Port Select
4	Enable Parallel Port
3	Serial Port Select
2	Enable Serial Port
1	Enable Diskette Drive Interface
0	Enable System Board

Figure 2-4. System Board POS Register 2 (Hex 0102)

Bit 7 When set to 0, this bit allows the parallel port to be configured as an 8-bit, parallel, bidirectional interface. When set to 1, this bit disables the bidirectional mode. This bit is set to 0 at power-on and POST sets it to 1.

Bits 6, 5 These bits select the configuration of the system board parallel port.

Bits 6 5	Assignment	Hex Address	Interrupt Level
0 0	Parallel 1	03BC - 03BF	7
0 1	Parallel 2	0378 - 037B	7
1 0	Parallel 3	0278 - 027B	7
1 1	Reserved	----------	-

Figure 2-5. Parallel Port Select Bits

Bit 4 When this bit and bit 0 are set to 1, the system board parallel port is enabled.

Bit 3 When set to 1, this bit sets the system board serial port as Serial 1 (addresses hex 03F8 through 03FF), which uses interrupt level 4. When set to 0, this bit sets the serial port as Serial 2 (addresses hex 02F8 through 02FF), which uses interrupt level 3.

Bit 2 When this bit and bit 0 are set to 1, the system board serial port is enabled.

Bit 1 When this bit and bit 0 are set to 1, the diskette drive interface is enabled.

Bit 0 When set to 1, this bit allows bits 4, 2, and 1 to enable and disable their respective devices. When set to 0, this bit disables the diskette drive interface, system board serial port, and system board parallel port, regardless of the state of bits 4, 2, and 1.

System Board POS Register 3 (Hex 0103)

This read-only register is accessed while the system board is in the setup mode. It contains information about the presence and type of memory card installed in each system board connector. The memory connectors are numbered 1-2-3-4 from top to bottom as viewed from the rear of the system.

Bit	Function
7	Reserved
6	2MB Card, Connector 3
5	-Card Present, Connector 3
4	Reserved
3	2MB Card, Connector 2
2	-Card Present, Connector 2
1	2MB Card, Connector 1
0	-Card Present, Connector 1

Figure 2-6. System Board POS Register 3 (Hex 0103)

Bits 7, 4 These bits are reserved.

Bits 6, 3, 1 Each bit indicates the type of memory card installed in the connector indicated. When set to 1, the bit indicates that the card installed is a 2MB memory card.

Bits 5, 2, 0 When set to 0, each bit indicates that a memory card is installed in the connector indicated.

System Board POS Register 4 (Hex 0104)

This read-only register is used in the same way as the POS register 3 (hex 0103).

Bit	Function
7 - 4	Reserved
3	2MB Card, Connector 4
2	-Card Present, Connector 4
1 - 0	Reserved

Figure 2-7. System Board POS Register 4 (Hex 0104)

Bits 7 - 4 These bits are reserved, and must be 1.

Bit 3 This bit indicates the type of memory installed in connector 4. When set to 1, this bit indicates that the card installed is the 2MB memory card.

Bit 2 When set to 0, this bit indicates that a memory card is installed in connector 4.

Bits 1 - 0 These bits are reserved, and must be 1.

Adapter Enable/Setup Register (Hex 0096)

The Adapter Enable/Setup register selects the connector to be configured.

Bit	Symbol
7	Channel Reset
6 - 4	Reserved
3	Card Setup Enable
2 - 0	Channel Select 2 - 0

Figure 2-8. Adapter Enable/Setup Register (Hex 0096)

Bit 7 When set to 1, this bit activates the 'channel reset' signal to all connectors.

Bits 6 - 4 These bits are reserved.

Bit 3 When set to 1, this bit enables the '-card setup' signal selected by bits 2 through 0.

Bits 2 - 0 These bits are the address bits for the '-card setup' signal. Connectors 1 through 2 are addressed as 0 through 1, respectively. The fixed disk connector is addressed as 2, and the piasma display adapter connector is addressed as 3. When bit 3 is set to 1, these bits select the connector that is put into setup.

Each channel connector has a unique '-card setup' signal (-CD SETUP) associated with it. This signal is used to put the adapters in the setup mode, which allows access to the POS registers. The individual connectors are selected through the Adapter Enable/Setup register. Setup information is then read from or written to the selected adapter through I/O addresses hex 0100 through 0107.

Notes:

1. -CD SETUP only goes active when an operation is performed in the I/O address range hex 0100 through 0107.
2. The status of port hex 0096 can be read by software. However, when the port is read, bits 6, 5, and 4 are set to 1.

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Notes:

Description

This section describes the math coprocessor, channel differences, memory subsystems, and miscellaneous system ports and connectors for the Model P70. For additional information about these and other topics, refer to the *Hardware Interface Technical Reference*.

80387 Math Coprocessor

The 20 MHz 80387 Math Coprocessor is matched to the speed of the system microprocessor and operate in the synchronous mode.

Micro Channel

This section describes the implementation of the Micro Channel architecture on Model P70 systems. For general Micro Channel information, refer to the *Hardware Interface Technical Reference*.

Matched-Memory Cycles

The 32-bit channel connector has a matched-memory extension. The system microprocessor activates the '-matched memory cycle' signal (-MMC) when it does a memory access. This allows the Model P70 to support the same memory adapter design as the PS/2 Model 80 system board.

Although a memory adapter can respond to -MMC active by driving the '-matched memory cycle request' signal (-MMCR) active, the Model P70 system board ignores -MMCR and performs a default cycle if the 'channel ready' signal (CD CHRDY) is driven active, or a synchronous-extended cycle if CD CHRDY is inactive. The Model P70 also drives the '-matched memory cycle command' signal active at the same time as the '-command' signal.

Central Arbiter

The central arbitration control point gives intelligent subsystems on the channel the ability to share and control the system. It allows burst data transfers and prioritization of control between devices. This arbiter supports up to 16 arbitrating devices.

Arbitration Bus Priority Assignments

The following figure shows the assignment of arbitration levels. The functions with the lowest arbitration level have the highest priority.

ARB Level	Primary Assignment
-2	Memory Refresh
-1	NMI
0	DMA Channel 0 (Programmable to any arbitration level)
1	DMA Channel 1
2	DMA Channel 2
3	DMA Channel 3
4	DMA Channel 4 (Programmable to any arbitration level)
5	DMA Channel 5
6	DMA Channel 6
7	DMA Channel 7
8 - E	Available
F	System Microprocessor

Figure 3-1. Arbitration Bus Priority Assignments

Note: Devices designed for arbitration level 0 or 1 should have limited bandwidth or short bursts so diskette overruns can be prevented or recovered by retry operations. The diskette drive controller, on arbitration level 2, can be held inactive by devices on levels 0 and 1, by a refresh operation, and by the previous controlling master. The diskette drive controller should not be held inactive for more than 12 microseconds to prevent overrun.

NMI service is executed at a priority level higher than 0, called -1. Memory refresh is prioritized at -2, two levels higher than 0. Levels -1 and -2 are reached on the system board only, while the 'arbitrate/-grant' signal is in the arbitrate state.

When the central arbitration control point receives a level -1 request (NMI, a system-board internal signal), it activates -PREEMPT, waits for

the end of transfer, and then places ARB/-GNT in the arbitrate state, which denies channel activity to arbitrating devices. The central arbitration control point gives the grant to the level -1 request, and holds ARB/-GNT in the arbitrate state until the operation is complete and the NMI is reset.

Central Arbiter Programming

The central arbitration control point provides access to programmable options through the Arbitration register, which is accessed at I/O address hex 0090. The bits are defined differently for read and write operations, as shown in the following figures.

Bit	Definition
7	Enable System Microprocessor Cycle
6	Arbitration Mask
5	Enable Extended Arbitration
4 - 0	Reserved

Figure 3-2. Arbitration Register, Write to Hex 0090

Bit	Definition
7	Enable System Microprocessor Cycle
6	Arbitration Masked by NMI
5	Bus Time-out
4	Reserved
3 - 0	Value of Arbitration Bus During Previous Grant State

Figure 3-3. Arbitration Register, Read Hex 0090

Bit 7 Setting this bit to 1 enables system microprocessor cycles during arbitration cycles. This bit can be set to 0 if an arbitrating device requires total control of the channel bandwidth. This bit is set to 0 by a system reset.

Reading this bit as a 1 indicates system microprocessor cycles are enabled during arbitration.

Bit 6 Setting this bit to 1 causes the central arbitration control point to enter the arbitration state. The system microprocessor controls the channel until this bit is reset to 0. This bit is set to 0 by a system reset.

Reading this bit as a 1 indicates that an NMI has occurred and has masked arbitration.

Warning: This bit should be set to 1 only by diagnostic routines and system error-recovery routines.

Bit 5 Setting this bit to 1 enables extended arbitration. The minimum arbitration cycle is 300 nanoseconds; this bit extends that minimum cycle to 600 nanoseconds. This bit is set to 0 during a system reset.

Reading this bit as a 1 indicates that a bus time-out has occurred, and resets bit 6 in this register to 0.

Bit 4 This bit is reserved and should be 0.

Bits 3 - 0 These bits are undefined for a write operation and should be set to 0.

Reading these bits returns the arbitration level of the arbiter controlling the channel during the most recent grant state. This information allows the system microprocessor to determine the arbitration level of the device that caused a bus time-out.

Diskette Drive and Fixed Disk Connectors

The system board has a 2- by 17-pin connector for one internal diskette drive, a 30-pin connector for external diskette drive, and a 2- by 36-pin connector for internal fixed disk drive.

The internal diskette drive connector passes control and data signals between the internal diskette drive and the diskette drive controller on the system board. Micro Channel signals necessary for fixed disk operations are present on the fixed disk connector. The external diskette drive attaches to the 30-pin connector, which passes the necessary signals from the diskette drive controller.

When in the setup mode, the fixed disk is addressed as channel connector 3 through the Adapter Enable/Setup register. For more information about this register, see "POS Information" in the *Hardware Interface Technical Reference*. For more POS information about the fixed disk drive, refer to the technical reference for that drive.

Internal Diskette Drive Connector

The following figure shows the signal assignment and pin numbering for the internal diskette drive connector on the system board. The internal diskette drive connector is a 2- by 17-pin connector that is numbered with the odd numbers on the top.

Pin	I/O	Signal	Pin	I/O	Signal
1	I	-2nd Drive Installed	2	O	-High Density Select
3	O	+5 Vdc	4	N/A	Reserved
5	N/A	Ground	6	O	+12Vdc
7	N/A	Signal Ground	8	I	-Index
9	N/A	Signal Ground	10	N/A	Reserved
11	N/A	Signal Ground	12	O	-Drive Select
13	N/A	Ground	14	N/A	Reserved
15	N/A	Signal Ground	16	O	-Motor Enable
17	N/A	Signal Ground	18	O	-Direction In
19	N/A	Signal Ground	20	O	-Step
21	N/A	Signal Ground	22	O	-Write Data
23	N/A	Signal Ground	24	O	-Write Enable
25	N/A	Signal Ground	26	I	-Track 0

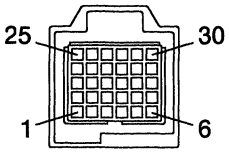
Figure 3-4 (Part 1 of 2). Internal Diskette Drive Connector

Pin	I/O	Signal	Pin	I/O	Signal
27	N/A	Signal Ground	28	I	-Write Protect
29	N/A	Signal Ground	30	I	-Read Data
31	N/A	Signal Ground	32	O	-Head 1 Select
33	N/A	Signal Ground	34	I	-Diskette Change

Figure 3-4 (Part 2 of 2). Internal Diskette Drive Connector

External Storage Device Connector

The following figure shows the signal assignment and pin numbering for the external storage device connector on the system board. This external storage device connector is a 30-pin connector located at the rear of the system unit. The system can support an external diskette drive through this connector.



Pin	I/O	Signal	Pin	I/O	Signal
1	N/A	Ground	2	I	-Second Drive Installed
3	N/A	Ground	4	O	-Reduced Write Current
5	N/A	Ground	6	N/A	Reserved
7	N/A	Ground	8	I	-Index
9	O	-Motor On 1	10	O	-Drive Select 1
11	N/A	Reserved	12	N/A	Reserved
13	N/A	Ground	14	O	-Direction
15	N/A	Ground	16	O	-Step
17	N/A	Ground	18	O	-Write Data
19	N/A	Ground	20	O	-Write Gate
21	N/A	Ground	22	I	-Track 00
23	N/A	Ground	24	I	-Write Protect
25	N/A	Ground	26	I	-Read Data
27	N/A	Ground	28	O	-Side 1 Select
29	N/A	Ground	30	I	-Diskette Change

Figure 3-5. External Storage Device Connector

Fixed Disk Drive Connector

The following figure shows the signal assignment and pin numbering for the fixed disk drive connector on the adapter. The fixed disk drive connector is a 2- by 36-pin connector. Side A of the connector is the top and Side B is the bottom.

Side A			Side B		
Pin	**I/O**	**Signal**	**Pin**	**I/O**	**Signal**
1	O	-CD SETUP	1	O	A15
2	O	A13	2	O	A14
3	N/A	Ground	3	N/A	Ground
4	O	A11	4	N/A	Reserved
5	O	A10	5	N/A	Ground
6	O	A09	6	O	A12
7	O	+5 Vdc	7	O	-CMD
8	O	A08	8	I	-CD SFDBK
9	O	A07	9	N/A	Ground
10	O	A06	10	I/O	D01
11	N/A	Ground	11	I/O	D03
12	O	A05	12	I/O	D04
13	O	A04	13	N/A	Ground
14	O	A03	14	O	CHRESET
15	O	+5 Vdc	15	I/O	D08
16	O	A02	16	I/O	D09
17	O	A01	17	N/A	Ground
18	O	A00	18	I/O	D12
19	O	+12 Vdc	19	I/O	D14
20	O	-ADL	20	I/O	D15
21	I	-PREEMPT	21	N/A	Ground
22	I	-BURST	22	I/O	D00
23	O	+5 Vdc	23	I/O	D02
24	I	ARB 00	24	I/O	D05
25	I	ARB 01	25	N/A	Ground
26	I	ARB 02	26	I/O	D06
27	N/A	+12 Vdc	27	I/O	D07
28	I	ARB 03	28	I/O	D10
29	O	ARB/-GNT	29	N/A	Ground
30	O	-TC	30	I/O	D11
31	N/A	+5 Vdc	31	I/O	D13
32	O	-S0	32	O	-SBHE
33	O	-S1	33	N/A	Ground
34	O	M/-IO	34	I	-CD DS 16
35	N/A	Ground	35	I	-IRQ 14
36	I	CD CHRDY	36	N/A	Ground

Figure 3-6. Fixed Disk Connector

Memory

Model P70 systems use the following types of memory:

- Read-only memory (ROM)
- Random access memory (RAM)
- Real-time Clock and CMOS RAM.

Read-Only Memory Subsystem

The ROM subsystem consists of 128KB in a 64Kb by 16-bit arrangement. ROM is active at power-on at address space hex 000E0000 to 000FFFFF. After POST ensures the proper operation of system memory, the ROM code is copied to RAM at the same address space, and ROM is disabled. ROM is assigned the top of the first and last 1MB of address space (000E0000 and FFFE0000).

ROM or RAM access at address space hex 000E0000 to 000FFFFF is controlled by the ROMEN bit in Memory Encoding Register 1 (hex 00E1). When enabled, ROM is not parity-checked and operates with four 50-nanosecond wait states.

Random Access Memory Subsystem

The RAM subsystem on the system board starts at address hex 00000000 of the address space. Memory is attached to the system board by four connectors. The RAM subsystem is 36 bits wide: 32 data bits and 4 parity bits. One parity bit is generated for each byte of data written. During a read operation, one parity bit is checked for each byte of data read by the device controlling the bus.

The Model P70 enables and disables memory in 1MB blocks. Each 1MB block must start on a 1MB boundary. Because 128KB of I/O ROM, and 128KB of video memory are mapped within the first 1MB address space, an overflow is created from the first 1MB of RAM installed in the system. The first 1MB of RAM can be split at either 512KB or 640KB; the memory from the split to the start of the RAM that contains the ROM code is called the *split memory block*. This split memory block can be disabled, or it can be remapped to the first address following the last 1MB of memory. Split memory block remapping and disabling are controlled by the memory encoding registers.

Note: Additional memory can be added in either of the 32-bit Micro Channel connectors. The total amount of memory installed should not exceed the 16MB addressing limit of the DMA controller.

Error Recovery

If POST detects a memory error in the first 512KB of memory, the first physical 1MB block of memory is deactivated. The addresses assigned to the deactivated block are reassigned to the second physical block of system board memory (the first 1MB of system memory must reside in connector 1 or 2). If 1MB of valid memory cannot be allocated from connector 1 or 2, the system cannot recover from the error. The first 1MB of memory address space cannot be assigned to memory on the channel.

POST does not deactivate a memory block if an error is detected in the second 512KB of that block. If an error is detected in that area of memory, the 1MB block containing the error can be deactivated and have its addresses reassigned by running the customer-level memory diagnostics program on the Reference Diskette supplied with the system. Once a block of memory is deactivated, it is ignored by POST on subsequent power-ons.

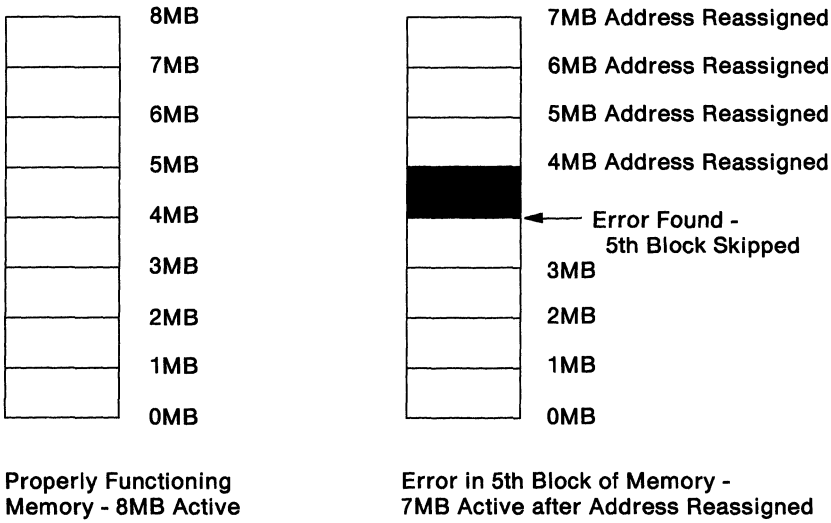


Figure 3-7. Memory Error Address Reassignment

Memory Subsystem Control

These read/write registers define and control the ROM and RAM subsystems.

Memory Encoding Register 1 (Hex 00E1)

This register determines how the first 1MB of memory is addressed and is used with Memory Encoding Register 2 to determine the amount of system board memory enabled.

Bit	Function
7	-Card 2 EN2
6	-Card 2 EN1
5	-Card 1 EN2
4	-Card 1 EN1
3	-ENSPLIT
2	-640
1	ROMEN
0	-ENPLRPCH

Figure 3-8. Memory Encoding Register 1

Bits 7, 6 These bits define system board memory in connector 2. When they are set to 0, bit 6 enables the first 1MB block and bit 7 enables the second 1MB block.

Bits 5, 4 These bits define system board memory in connector 1. When they are set to 0, bit 4 enables the first 1MB block and bit 5 enables the second 1MB block.

Bit 3 This bit determines whether the split-memory block is assigned addresses or is disabled. The top 128KB of the first 1MB is always mapped into the ROM address space and the code in ROM is copied into this space.

When this bit is set to 0, the split-memory block is enabled. The split-memory block size is dependent on the value of the 640 bit. Its address is determined in Memory Encoding Register 2. When this bit is set to 1, the split-memory block is disabled.

Note: If the total system memory is equal to or greater than 16MB, the split-memory block cannot be used.

Bit 2 This bit determines where the first active 1MB of memory is split.

When this bit is set to 0, the system maps 640KB of the first 1MB to address hex 00000000 to 0009FFFF. The split-memory block, 256KB, is mapped to the address specified in Memory Encoding register 2.

When this bit is set to 1, the system maps 512KB of the first 1MB to address hex 00000000 to 0007FFFF. The split-memory block, 384KB, is mapped to the address specified in the Memory Encoding register 2. The addresses hex 00080000 to 0009FFFF are unassigned.

Bit 1 This bit determines how addresses hex 000E0000 to 000FFFFF are assigned.

When this bit is set to 1, ROM is enabled and the read-access addresses are assigned to ROM; the write-access addresses are assigned to RAM. When this bit is set to 0, ROM is disabled and read addresses are assigned to RAM; the write addresses are disabled while ROM is disabled.

Note: When this bit is set to 1, system performance will be substantially slower because of 16-bit accesses to ROM and a longer cycle.

Bit 0 When set to 0, this bit enables parity checking of system board memory. To clear a parity error, this bit must be set to 1 and then to 0.

Memory Encoding Register 2 (Hex 00E0)

This register is used with Memory Encoding Register 1 to determine the amount of system board memory that is enabled. It also contains the address for the split-memory block.

Bit	Function
7	-Card 4 EN2
6	-Card 4 EN1
5	-Card 3 EN2
4	-Card 3 EN1
3	SPA23
2	SPA22
1	SPA21
0	SPA20

Figure 3-9. Memory Encoding Register 2

Bits 7, 6 These bits define the system board memory in connector 4. When they are set to 0, bit 6 enables the first 1MB block and bit 7 enables the second 1MB block.

Bits 5, 4 These bits define the system board memory in connector 3. When they are set to 0, bit 4 enables the first 1MB block and bit 5 enables the second 1MB block.

Bits 3 - 0 These bits define the starting address of the split-memory block. When split memory is enabled, these bits determine its starting address. The starting location can be at any 1MB boundary from 1MB to 15MB.

System Memory Maps

Memory is mapped by the Memory Encoding registers. The mapping results in either 512KB or 640KB of system board RAM starting at address hex 00000000. A 256-byte and 1KB portion and of this RAM is reserved as BIOS data areas. See the *IBM Personal System/2 and Personal Computer BIOS Interface Technical Reference* for details.

In the following figures, the variable *X* represents the number of 1MB blocks of system board memory starting at or above the hex 00100000 boundary. The variable *Y* represents the number of 1MB blocks of memory installed in the channel starting at or above the hex 00100000 boundary (*Y* = 0 to 15).

The following figure shows the memory mapping when:

Enable Split bit = 1
640 bit = 1
ROM enable bit = 1

Hex Range	Function
00000000 to 0007FFFF	512KB System Board RAM
00080000 to 0009FFFF	Not Used
000A0000 to 000BFFFF	128KB Video RAM
000C0000 to 000DFFFF	Channel ROM
000E0000 to 000FFFFF	128KB System Board ROM
00100000 to (00100000 + XMB)	XMB System Board RAM
(00100000 + XMB) to (00100000 + XMB + YMB)	YMB Channel RAM
(00100000 + XMB + YMB) to FFFDFFFF	Not Used
FFFE0000 to FFFFFFFF	128KB System Board ROM (Same as 000E0000 to 000FFFFF)

Figure 3-10. System Memory Map 1

The following figure shows the memory mapping when:

Enable Split bit = 1
640 bit = 0
ROM enable bit = 1

Hex Range	Function
00000000 to 0009FFFF	640KB System Board RAM
000A0000 to 000BFFFF	128KB Video RAM
000C0000 to 000DFFFF	Channel ROM
000E0000 to 000FFFFF	128KB System Board ROM
00100000 to (00100000 + *XMB*)	*XMB* System Board RAM
(00100000 + *XMB*) to (00100000 + *XMB* + *YMB*)	*YMB* Channel RAM
(00100000 + *XMB* + *YMB*) to FFFDFFFF	Not Used
FFFE0000 to FFFFFFFF	128KB System Board ROM (Same as 000E0000 to 000FFFFF)

Figure 3-11. System Memory Map 2

The following figure shows the memory mapping when:

Enable Split bit = 0
640 bit = 1
ROM enable bit = 1
Split address bits = 1 + *X* + *Y* (Total Range = 1 to 15).

Hex Range	Function
00000000 to 0007FFFF	512KB System Board RAM
00080000 to 0009FFFF	Not Used
000A0000 to 000BFFFF	128KB Video RAM
000C0000 to 000DFFFF	Channel ROM
000E0000 to 000FFFFF	128KB System Board ROM
00100000 to (00100000 + *XMB*)	*XMB* System Board RAM
(00100000 + *XMB*) to (00100000 + *XMB* + *YMB*)	*YMB* Channel RAM
(00100000 + *XMB* + *YMB*) to (00100000 + *XMB* + *YMB* +384KB − 1)	384KB System Board RAM
(00100000 + *XMB* + *YMB* + 384KB) to FFFDFFFF	Not Used
FFFE0000 to FFFFFFFF	128KB System Board ROM (Same as 000E0000 to 000FFFFF)

Figure 3-12. System Memory Map 3

The following figure shows the memory mapping when:

Enable Split bit = 0
640 bit = 0
ROM enable bit = 1
Split address bits = 1 + *X* + *Y* (Total Range = 1 to 15).

Hex Range	Function
00000000 to 0009FFFF	640KB System Board RAM
000A0000 to 000BFFFF	128KB Video RAM
000C0000 to 000DFFFF	Channel ROM
000E0000 to 000FFFFF	128KB System Board ROM
00100000 to (00100000 + *X*MB)	*X*MB System Board RAM
(00100000 + *X*MB) to (00100000 + *X*MB + *Y*MB)	*Y*MB Channel RAM
(00100000 + *X*MB + *Y*MB) to (00100000 + *X*MB + *Y*MB + 256KB − 1)	256KB System Board RAM
(00100000 + *X*MB + *Y*MB + 256KB) to FFFDFFFF	Not Used
FFFE0000 to FFFFFFFF	128KB System Board ROM (Same as 000E0000 to 000FFFFF)

Figure 3-13. System Memory Map 4

The following figure shows the memory mapping when:

Enable Split bit = 1
640 bit = 1
ROM enable bit = 0

Hex Range	Function
00000000 to 0007FFFF	512KB System Board RAM
00008000 to 0009FFFF	Not Used
000A0000 to 000BFFFF	128KB Video RAM
000C0000 to 000DFFFF	Channel ROM
000E0000 to 000FFFFF	128KB System Board ROM mapped to RAM
00100000 to (00100000 + *X*MB)	*X*MB System Board RAM
(00100000 + *X*MB) to (00100000 + *X*MB + *Y*MB)	*Y*MB Channel RAM
(00100000 + *X*MB + *Y*MB) to FFFDFFFF	Not Used
FFFE0000 to FFFFFFFF	128KB System Board ROM

Figure 3-14. System Memory Map 5

The following figure shows the memory mapping when:

Enable Split bit = 1
640 bit = 0
ROM enable bit = 0

Hex Range	Function
00000000 to 0009FFFF	640KB System Board RAM
000A0000 to 000BFFFF	128KB Video RAM
000C0000 to 000DFFFF	Channel ROM
000E0000 to 000FFFFF	128KB System Board ROM mapped to RAM
00100000 to (00100000 + *X*MB)	*X*MB System Board RAM
(00100000 + *X*MB) to (00100000 + *X*MB + *Y*MB)	*Y*MB Channel RAM
(00100000 + *X*MB + *Y*MB) to FFFDFFFF	Not Used
FFFE0000 to FFFFFFFF	128KB System Board ROM

Figure 3-15. System Memory Map 6

The following figure shows the memory mapping when:

Enable Split bit = 0
640 bit = 1
ROM enable bit = 0
Split address bits = 1 + *X* + *Y* (Total Range = 1 to 15).

Hex Range	Function
00000000 to 0007FFFF	512KB System Board RAM
00080000 to 0009FFFF	Not Used
000A0000 to 000BFFFF	128KB Video RAM
000C0000 to 000DFFFF	Channel ROM
000E0000 to 000FFFFF	128KB System Board ROM mapped to RAM
00100000 to (00100000 + *X*MB)	*X*MB System Board RAM
(00100000 + *X*MB) to (00100000 + *X*MB + *Y*MB)	*Y*MB Channel RAM
(00100000 + *X*MB + *Y*MB) to (00100000 + *X*MB + *Y*MB + 384KB − 1)	384KB of First 1MB at Split Address
(00100000 + *X*MB + *Y*MB + 384KB) to FFFDFFFF	Not Used
FFFE0000 to FFFFFFFF	128KB System Board ROM

Figure 3-16. System Memory Map 7

The following figure shows the memory mapping when:

Enable Split bit = 0
640 bit = 0
ROM enable bit = 0
Split address bits = 1 + *X* + *Y* (Total Range = 1 to 15).

Hex Range	**Function**
00000000 to 0009FFFF	640KB System Board RAM
000A0000 to 000BFFFF	128KB Video RAM
000C0000 to 000DFFFF	Channel ROM
000E0000 to 000FFFFF	128K System Board ROM mapped to RAM
00100000 to (00100000 + *X*MB)	*X*MB System Board RAM
(00100000 + *X*MB) to (00100000 + *X*MB + *Y*MB)	*Y*MB Channel RAM
(00100000 + *X*MB + *Y*MB) to (00100000 + *X*MB + *Y*MB + 256KB-1)	256KB of First 1MB at Split Address
(00100000 + *X*MB + *Y*MB + 256KB) to FFFDFFFF	Not Used
FFFE0000 to FFFFFFFF	128KB System Board ROM (Same as 000E0000 to 000FFFFF)

Figure 3-17. System Memory Map 8

System Board Memory Connectors

The system board has four 72-pin memory connectors that support the 2MB memory cards. The four connectors are numbered 1-2-3-4 from the top of the system. Memory-refresh requests typically occur once every 15 microseconds.

The following figure shows the pin assignments for the 1- by 72-pin memory connectors.

Pin	I/O	Signal	Pin	I/O	Signal
1	N/A	Ground	37	I/O	Parity Data 1
2	I/O	Data 0	38	I/O	Parity Data 3
3	I/O	Data 16	39	N/A	Ground
4	I/O	Data 1	40	O	Column Address Strobe 0
5	I/O	Data 17	41	O	Column Address Strobe 2
6	I/O	Data 2	42	O	Column Address Strobe 3
7	I/O	Data 18	43	O	Column Address Strobe 1
8	I/O	Data 3	44	O	Row Address Strobe 0
9	I/O	Data 19	45	O	Row Address Strobe 1
10	O	+5 Vdc	46	O	Block Select 1
11	O	-Column Address Strobe P	47	O	Write Enable
12	O	Address 0	48	N/A	Reserved
13	O	Address 1	49	I/O	Data 8
14	O	Address 2	50	I/O	Data 24
15	O	Address 3	51	I/O	Data 9
16	O	Address 4	52	I/O	Data 25
17	O	Address 5	53	I/O	Data 10
18	O	Address 6	54	I/O	Data 26
19	N/A	Reserved	55	I/O	Data 11
20	I/O	Data 4	56	I/O	Data 27
21	I/O	Data 20	57	I/O	Data 12
22	I/O	Data 5	58	I/O	Data 28
23	I/O	Data 21	59	O	+5 Vdc
24	I/O	Data 6	60	I/O	Data 29
25	I/O	Data 22	61	I/O	Data 13
26	I/O	Data 7	62	I/O	Data 30
27	I/O	Data 23	63	I/O	Data 14
28	O	Address 7	64	I/O	Data 31
29	O	Block Select 0	65	I/O	Data 15

Figure 3-18 (Part 1 of 2). System Board Memory Connector

Pin	I/O	Signal	Pin	I/O	Signal
30	O	+5 Vdc	66	O	Block Select 2
31	O	Address 8	67	I	Presence Detect 0
32	N/A	Reserved	68	I	Presence Detect 1
33	O	Row Address Strobe 3	69	I	Presence Detect 2
34	O	Row Address Strobe 2	70	I	Presence Detect 3
35	I/O	Parity Data 2	71	O	Block Select 3
36	I/O	Parity Data 0	72	N/A	Ground

Figure 3-18 (Part 2 of 2). System Board Memory Connector

The 'presence detect' signals are used by the system to determine memory card size and memory speed. The pins are either connected to ground (G) or not connected (N). The following table shows those combinations supported by Model P70.

	Presence Detect Signals			
Card Type	**0**	**1**	**2**	**3**
2 MB Memory at 85 ns	N	G	N	G

Figure 3-19. Presence Detect Encoding

Real-Time Clock/Complementary Metal-Oxide Semiconductor RAM

The real-time clock/complementary metal-oxide semiconductor RAM (RT/CMOS) chip contains the real-time clock and 64 bytes of CMOS RAM. The internal clock circuitry uses 14 bytes of this memory, and the rest is allocated to configuration and system status information.

In addition to the 64 bytes of CMOS RAM, a 2KB CMOS RAM extension is provided for configuration and other system information.

A 6-Vdc lithium battery maintains voltage to the RT/CMOS RAM and 2KB CMOS RAM extension when the power supply is not in operation.

The following figure shows the RT/CMOS RAM bytes and their addresses.

Address (Hex)	RT/CMOS RAM Bytes
000 - 00D	Real-Time Clock Bytes
00E	Diagnostic Status Byte
00F	Shutdown Status Byte
010	Diskette Drive Type Byte
011	First Fixed Disk Drive Type Byte
012	Reserved
013	Reserved
014	Equipment Byte
015 - 016	Low and High Base Memory Bytes
017 - 018	Low and High Expansion Memory Bytes
019 - 031	Reserved
032 - 033	Configuration CRC Bytes
034 - 036	Reserved
037	Date Century Byte
038 - 03F	Reserved

Figure 3-20. RT/CMOS RAM Address Map

RT/CMOS Address Register and NMI Mask (Hex 0070)

This register is used in conjunction with the port at hex 0071 to read and write the RT/CMOS RAM bytes.

Bit	Function
7	NMI Mask
6	Reserved
5 - 0	RT/CMOS RAM Address

Figure 3-21. RT/CMOS Address Register and NMI Mask (Hex 0070)

Warning: The operation following a write to hex 0070 should access port hex 0071; otherwise intermittent malfunctions and unreliable operation of the RT/CMOS RAM can occur.

Bit 7 When this bit is set to 1, the NMI is masked off (the NMI is disabled). This bit is set to 1 by a power-on reset. This is a write-only bit.

Bit 6 Reserved.

Bits 5 - 0 These bits are used to select RT/CMOS RAM addresses.

RT/CMOS Data Register (Hex 0071)

This port is used in conjunction with the address register at hex 0070 to read and write the RT/CMOS RAM bytes.

Bit	Function
7 - 0	RT/CMOS Data

Figure 3-22. RT/CMOS Data Register (Hex 0071)

RT/CMOS RAM I/O Operations

During I/O operations to the RT/CMOS RAM addresses, interrupts should be masked to prevent other interrupt routines from changing the CMOS Address register before data is read or written. After I/O operations, the RT/CMOS and NMI Mask register (hex 0070) should be left pointing to Status Register D (hex 00D).

Warning: The operation following a write to hex 0070 should access hex 0071; otherwise intermittent malfunctions and unreliable operation of the RT/CMOS RAM can occur.

The following steps are required to perform I/O operations to the RT/CMOS RAM addresses:

1. Write the RT/CMOS RAM address to the RT/CMOS and NMI Mask register (hex 0070).
2. Write the data to address hex 0071.

Reading RT/CMOS RAM requires the following steps:

1. Write the RT/CMOS RAM address to the RT/CMOS and NMI Mask register (hex 0070).
2. Read the data from address hex 0071.

Real-Time Clock Bytes (Hex 000-00D)

Bit definitions and addresses for the real-time clock bytes are shown in the following figure.

Address (Hex)	Function	Byte Number
000	Seconds	0
001	Second Alarm	1
002	Minutes	2
003	Minute Alarm	3
004	Hours	4
005	Hour Alarm	5
006	Day of Week	6
007	Date of Month	7
008	Month	8
009	Year	9
00A	Status Register A	10
00B	Status Register B	11
00C	Status Register C	12
00D	Status Register D	13

Figure 3-23. Real-Time Clock Bytes

Note: The Setup program initializes status registers A, B, C, and D when the time and date are set. Interrupt hex 1A is the BIOS interface to read and set the time and date and it initializes the register the same way as the Setup program.

Status Register A (Hex 00A)

Bit	Function
7	Update in Progress
6 - 4	22-Stage Divider
3 - 0	Rate Selection Bits

Figure 3-24. Status Register A

Bit 7 When set to 1, this bit indicates the time-update cycle is in progress. When set to 0, it indicates the current date and time can be read.

Bits 6 - 4 These three divider-selection bits identify which time-base frequency is being used. The system initializes these bits to binary 010, which selects a 32.768 kHz time base. This is the only value supported by the system for proper time-keeping.

Bits 3 - 0 These bits allow the selection of a divider output frequency. The system initializes the rate selection bits to a binary 0110, which selects a 1.024 kHz square-wave output frequency and a 976.562-microsecond periodic interrupt rate.

Status Register B (Hex 00B)

Bit	Function
7	Set
6	Periodic Interrupt Enable
5	Alarm Interrupt Enable
4	Update-Ended Interrupt Enabled
3	Square Wave Enabled
2	Date Mode
1	24-Hour Mode
0	Daylight Savings Enabled

Figure 3-25. Status Register B

Bit 7 When set to 0, this bit updates the cycle, normally by advancing the counts at a rate of one per second. When set to 1, this bit immediately ends any update cycle in progress, and the program can initialize the 14 time bytes without any further updates occurring until this bit is set to 0.

Bit 6 This bit is a read/write bit that allows an interrupt to occur at a rate specified by the rate and divider bits in Status Register A. When set to 1, this bit enables the interrupt. The system initializes this bit to 0.

Bit 5 When set to 1, this bit enables the alarm interrupt. The system initializes this bit to 0.

Bit 4 When set to 1, this bit enables the update-ended interrupt. The system initializes this bit to 0.

Bit 3 When set to 1, this bit enables the square-wave frequency as set by the rate-selection bits in Status Register A. The system initializes this bit to 0.

Bit 2 This bit indicates if the time-and-date calendar updates use binary or binary-coded-decimal (BCD) formats. When set to 1, this bit indicates a binary format. The system initializes this bit to 0.

Bit 1 This bit establishes if the hours byte is in the 24-hour or 12-hour mode. When set to 1, this bit indicates the 24-hour mode. The system initializes this bit to 1.

Bit 0 When set to 1, this bit enables the daylight savings time mode. When set to 0, it disables the mode, and the clock reverts to standard time. The system initializes this bit to 0.

Status Register C (Hex 00C)

Bit	Function
7	Interrupt Request Flag
6	Periodic Interrupt Flag
5	Alarm Interrupt Flag
4	Update-Ended Interrupt Flag
3 - 0	Reserved

Figure 3-26. Status Register C

Note: Interrupts are enabled by bits 6, 5, and 4 in Status Register B.

Bit 7 This bit is used in conjunction with bits 6, 5, and 4. When set to 1, this bit indicates that an interrupt has occurred; bits 6, 5, and 4 indicate the type of interrupt.

Bit 6 When set to 1, this bit indicates that a periodic interrupt occurred.

Bit 5 When set to 1, this bit indicates that an alarm interrupt occurred.

Bit 4 When set to 1, this bit indicates that an update-ended interrupt occurred.

Bits 3 - 0 Reserved.

Status Register D (Hex 00D)

Bit	Function
7	Valid RAM
6 - 0	Reserved

Figure 3-27. Status Register D

Bit 7 This read-only bit monitors the power-sense pin. A low state of this pin indicates a loss of power to the real-time clock (dead battery). When set to 1, this bit indicates that the real-time clock has power. When set to 0, it indicates that the real-time clock has lost power.

Bits 6 - 0 Reserved.

CMOS RAM Configuration

The following shows the bit definitions for the CMOS RAM configuration bytes.

Diagnostic Status Byte (Hex 00E)

Bit	Function
7	Real-Time Clock Chip Power
6	Configuration Record and Checksum Status
5	Incorrect Configuration
4	Memory Size Miscompare
3	Fixed Disk Controller/Drive C Initialization Status
2	Time Status Indicator
1	Adapter Configuration Miscompare
0	Adapter ID Time-Out

Figure 3-28. Diagnostic Status Byte

Bit 7 When set to 1, this bit indicates the real-time clock chip lost power.

Bit 6 When this bit is set to 1, the checksum is incorrect.

Bit 5 This is a check, at power-on time, of the Equipment byte. When set to 1, the configuration information is incorrect. Power-on checks require that at least one diskette drive be installed (bit 0 of the Equipment byte, hex 014, is set to 1).

Bit 4 When set to 1, this bit indicates the power-on check determined that the memory size is not the same as in the configuration record.

Bit 3 When set to 1, this bit indicates that the controller or drive C failed initialization, which prevents the system from attempting a power-on reset.

Bit 2 When set to 0, this bit indicates the time is valid. When set to 1, this bit indicates the time is invalid.

Bit 1 This bit indicates if the installed adapters match the configuration information. When this bit is set to 1, the adapters do not match the configuration information.

Bit 0 When set to 1, this bit indicates a time-out occurred while an adapter ID was being read.

Shutdown Status Byte (Hex 00F): This byte is defined by the power-on diagnostic programs.

Diskette Drive Type Byte (Hex 010): This byte indicates the type of diskette drive installed.

Bit	Function
7 - 4	First Diskette Drive Type
3 - 0	Second Diskette Drive Type

Figure 3-29. Diskette Drive Type Byte

Bits 7 - 4 These bits indicate the first diskette drive type, as shown in the following figure.

Bits 7 6 5 4	Function
0 0 0 0	No drive present
0 0 0 1	Double-sided diskette drive (48 tracks per inch, 360KB)
0 0 1 1	High-capacity diskette drive (720KB)
0 1 0 0	High-density diskette drive (1.44MB)

Note: All combinations that are not shown are reserved.

Figure 3-30. Diskette Drive Type Byte (Bits 7 - 4)

Bits 3 - 0 These bits indicate the second diskette drive type, as shown in the following figure.

Bits 3 2 1 0	Function
0 0 0 0	No drive present
0 0 0 1	Double-sided diskette drive (48 tracks per inch, 360KB)
0 0 1 1	High-capacity diskette drive (720KB)
0 1 0 0	High-density diskette drive (1.44MB)

Note: All combinations that are not shown are reserved.

Figure 3-31. Diskette Drive Type Byte (Bits 3 - 0)

First Fixed Disk Drive Type Byte (Hex 011): This byte defines the type of the first fixed disk drive (drive C). Hex 00 indicates that a fixed disk drive is *not* installed.

Note: For more information about fixed disk drive types, refer to the *IBM Personal System/2 and Personal Computer BIOS Interface Technical Reference*.

Reserved Byte (Hex 013): This byte is reserved.

Equipment Byte (Hex 014): The equipment byte defines the basic equipment in the system for the power-on diagnostic tests.

Bit	Function
7, 6	Number of Diskette Drives
5, 4	Display Operating Mode
3, 2	Reserved
1	Math Coprocessor Presence
0	Diskette Drive Presence

Figure 3-32. Equipment Byte

Bits 7, 6 These bits indicate the number of diskette drives installed, as shown in the following figure.

Bits 7 6	Number of Diskette Drives
0 0	One Drive
0 1	Two Drives
1 0	Reserved
1 1	Reserved

Figure 3-33. Equipment Byte (Bits 7, 6)

Bits 5, 4 These bits indicate the operating mode of the display attached to the video port, as shown in the following figure.

Bits 5 4	Display Operating Mode
0 0	Reserved
0 1	40-Column Mode
1 0	80-Column Mode
1 1	Monochrome Mode

Figure 3-34. Equipment Byte (Bits 5, 4)

Bits 3, 2 Reserved.

Bit 1 When set to 1, this bit indicates that a math coprocessor is installed.

Bit 0 When set to 1, this bit indicates that a diskette drive is installed.

Low and High Base Memory Bytes (Hex 015 and 016): These bytes define the amount of memory below the 640KB address space.

The value from these bytes represents the number of 1KB blocks of base memory. For example, hex 0280 is equal to 640KB. The low byte is hex 15; the high byte is hex 16.

Low and High Expansion Memory Bytes (Hex 017 and 018): These bytes define the amount of memory above the 1MB address space.

The hexadecimal values in these bytes represent the number of 1KB blocks of expansion memory. For example, hex 0800 is equal to 2048KB. The low byte is hex 17; the high byte is hex 18.

Reserved Bytes (Hex 019 through 031): These bytes are reserved.

Configuration CRC Bytes (Hex 032 and 033): These bytes contain the cyclic-redundancy-check data for bytes hex 010 through hex 031 of the 64-byte CMOS RAM. The low byte is hex 33; the high byte is hex 32.

Reserved Bytes (Hex 034 through 036): These bytes are reserved.

Date Century Byte (Hex 037): Bits 7 through 0 of this byte contain the BCD value for the century. Refer to the *IBM Personal System/2 and Personal Computer BIOS Interface Technical Reference* for information about reading and setting this byte.

Reserved Bytes (Hex 038 through 03F): These bytes are reserved.

Miscellaneous System Functions

Nonmaskable Interrupt

The nonmaskable interrupt (NMI) signals the system microprocessor that a parity error, a channel check, a system channel time-out, or a system Watchdog time-out has occurred. The NMI stops all arbitration on the bus until bit 6 of the Arbitration register (I/O address hex 0090) is set to 0. This can result in lost data or an overrun error on some I/O devices. The NMI masks all other interrupts and the IRET instruction restores the interrupt flag to the state it was in prior to the interrupt. A system reset causes a reset of the NMI.

Nonmaskable interrupt requests from system board parity and channel check are subject to mask control with the NMI mask bit in the RT/CMOS Address register. The Watchdog Timer and system channel time-out are not masked by this bit. (See "RT/CMOS Address Register and NMI Mask (Hex 0070)" on page 3-25). The power-on default of the NMI mask is 1 (NMI disabled). Prior to enabling the NMI after a power-on reset, the parity check and channel check state are initialized by the POST.

Warning: The operation following a write to hex 0070 should access port hex 0071; otherwise intermittent malfunctions and unreliable operation of the RT/CMOS RAM can occur.

System Control Port B (Hex 0061)

Bit definitions for the read and write functions of this port are shown in the following figures.

Bit	Function
7	Reset Timer 0 Output Latch (IRQ0)
6 - 4	Reserved
3	Enable Channel Check
2	Enable Parity Check
1	Speaker Data Enable
0	Timer 2 Gate to Speaker

Figure 3-35. System Control Port B (Write)

Bit	Function
7	Parity Check
6	Channel Check
5	Timer 2 Output
4	Toggles with Each Refresh Request
3	Enable Channel Check
2	Enable Parity Check
1	Speaker Data Enable
0	Timer 2 Gate to Speaker

Figure 3-36. System Control Port B (Read)

Bit 7 Setting this bit to 1 resets IRQ0. Reading this bit as a 1 indicates a parity check has occurred.

Bit 6 Reading this bit as a 1 indicates a channel check has occurred.

Bit 5 This bit indicates the condition of the timer/counter 2 'output' signal.

Bit 4 This bit toggles for each refresh request.

Bit 3 Setting this bit to 0 enables channel check. This bit is set to 1 during a power-on reset.

Bit 2 Setting this bit to 0 enables parity check. This bit is set to 1 during a power-on reset.

Bit 1 Setting this bit to 1 enables speaker data.

Bit 0 Setting this bit to 1 enables the timer 2 gate.

System Control Port A (Hex 0092)

Bit	Function
7, 6	Fixed-Disk Activity Light
5	Reserved
4	Watchdog Timer Status
3	Security Lock Latch
2	Reserved = 0
1	Alternate Gate A20
0	Alternate Hot Reset

Figure 3-37. System Control Port A

Bits 7, 6 These bits control the fixed-disk activity light. Setting either bit to 1 turns the fixed-disk activity light on. Setting both bits to 0 turns the light off. The power-on reset condition of each bit is 0.

Bit 5 Reserved.

Bit 4 This read-only bit indicates the Watchdog Timer status. When this bit is set to 1, a Watchdog time-out has occurred. For more information about the Watchdog Timer, refer to the *Hardware Interface Technical Reference*.

Bit 3 This bit provides the security lock for the secured area of RT/CMOS. Setting this bit to 1 electrically locks the 8-byte, power-on password. Once this bit is set by POST, it can only be cleared by turning the system off.

Bit 2 Reserved.

Bit 1 This bit is used to enable the 'address 20' signal (A20) when the microprocessor is in the real address mode. When this bit is set to 0, A20 cannot be used in real mode addressing. This bit is set to 0 during a system reset.

Bit 0 This bit provides an alternate method of resetting the system microprocessor. This alternate method supports operating systems requiring faster operation than was provided on the IBM Personal Computer AT®. Resetting the system microprocessor is used to switch the microprocessor from the protected mode to the real address mode. The alternate reset takes 13.4 microseconds.

This bit is set to 0 either by a system reset or a Write operation. When a Write operation changes this bit from 0 to 1, the alternate reset pin is pulsed high for 100 to 125 nanoseconds. The reset occurs after a minimum delay of 6.72 microseconds. While the reset is occurring, the latch remains set so that POST can read this bit. If the bit is 0, POST assumes the system was just powered on. If the bit is 1, POST assumes a switch from the protected mode to the real mode has taken place.

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Power-On Password

RT/CMOS RAM has 8 bytes reserved for the power-on password and its check character. The 8 bytes are initialized to hex 00. The microprocessor can only access these bytes during power-on self-test (POST). After POST is completed, if a power-on password is installed, the password bytes are locked and cannot be accessed by a program. A power-on password can be from 1 to 7 characters.

During power-on password installation, the password (1 to 7 keyboard scan codes), is stored in the security space.

Power-on password installation is a function of a program contained on the Reference diskette. Once the power-on password utility has been installed, the password can be changed only during the POST. When the new power-on password is installed, changed, or removed, the password is not visible on the display.

The system unit cover can be physically locked to prevent unauthorized access to the battery. This helps prevent unauthorized battery removal and loss of power-on password and configuration information.

For information about the keyboard password, see the "Keyboard and Auxiliary Device Controller" section in the *Hardware Interface Technical Reference*.

Hardware Compatibility

The Model P70 maintains many of the interfaces used by the IBM Personal Computer AT. In most cases command and status organization of these interfaces is maintained.

The functional interfaces for the Model P70 are compatible with the following interfaces:

- The Intel[1] 8259 interrupt controllers (without edge triggering).
- The Intel 8253 timers driven from 1.193 MHz (timer 0 and 2 only).
- The Intel 8237 DMA controller-address/transfer counters, page registers and status fields only. The Command and Request registers are not supported. The rotate and mask functions are not supported. The Mode register is partially supported.
- The NS16450 serial port.
- The Intel 8088, 8086, and 80286 microprocessors.
- The Intel 8272 diskette drive controller.
- The Motorola[2] MC146818 Time of Day Clock command and status (CMOS reorganized).
- The Intel 8042 keyboard port at address hex 0060.
- Display modes supported by the IBM Monochrome Display and Printer Adapter, the IBM Color/Graphics Monitor Adapter, and the IBM Enhanced Graphics Adapter.

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1 Intel is a trademark of the Intel Corporation.

2 Motorola is a trademark of Motorola, Inc.

- The parallel printer ports (Parallel 1, Parallel 2, and Parallel 3) in compatibility mode.
- Generally compatible with the Intel 80287 and 8087 math coprocessors.
- The plasma display operates identically to IBM 8503 Monochrome Display, with the following exception. 9-PEL wide fonts are not supported on the plasma display because the display is limited to 640 total PELs.

Section 4. Video Subsystem

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Notes:

Description

Model P70 is equipped with a plasma display which is controlled by the plasma display adapter. The plasma display works as a monochrome display. In addition, the plasma display adapter also has the VGA and DAC section so that a PS/2 display can be attached to the Model P70 without any other additional adapter.

Note: When an external PS/2 display is attached, the plasma display does not display unless the Reference Diskette is in use.

Plasma Display

The plasma display is a flat panel monochrome display. Each PEL can display 16 gray scales.

The specification is the following.

Screen size : 211.2 x 158.4 mm (8.31 x 6.24 inch)
Resolution : 640 x 480 PEL

Plasma Display Adapter

Overview

The plasma display adapter card is plugged in the 16-bit channel connecter on the system board. This 16-bit channel connecter contains all signals on the 16-bit micro channel plus some additional signals necessary for the plasma display adapter. Notice that the connecter does not have the video extension.

The plasma display controller (PDC) emulates the PS/2 8503 monochrome display. Half-toning technology is used to implement mode hex 13, and distinctive-mapping is used on the remaining modes.

This adapter has the following three sections.

- **VGA:** Video Graphics Array
- **DAC:** Digital-to-Analog Converter
- **PDC:** Plasma Display Controller

Following is the block diagram of the plasma display adapter.

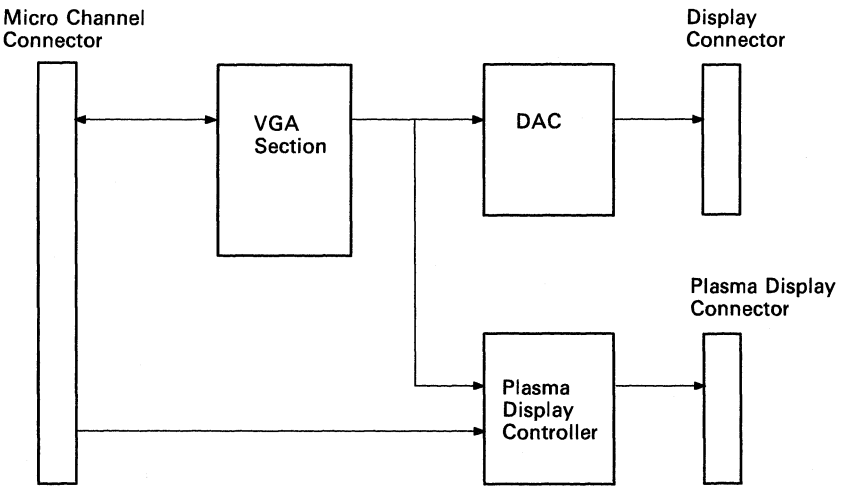


Figure 4-1. Block Diagram

Video Mode

The plasma display adapter supports the following modes. A/N modes (0+, 1+, 2+, 3+, 7, 7+) with 9-dot width font are supported only for the external PS/2 display. A/N modes (0#, 1#, 2#, 3#, 7*, 7#) are used only for the plasma display.

Mode (Hex)	Type	Colors (Shades)	Alpha Format	Buffer Start	Box Size	Max. Pgs.	Vert. Freq.	PELs
0, 1	A/N	16	40 x 25	B8000	8 x 8	8	70 Hz	320 x 200
0*, 1*	A/N	16	40 x 25	B8000	8 x 14	8	70 Hz	320 x 350
0+, 1+	A/N	16	40 x 25	B8000	9 x 16	8	70 Hz	360 x 400
0#, 1#	A/N	16	40 x 25	B8000	8 x 16	8	70 Hz	320 x 400
2, 3	A/N	16	80 x 25	B8000	8 x 8	8	70 Hz	640 x 200
2*, 3*	A/N	16	80 x 25	B8000	8 x 14	8	70 Hz	640 x 350
2+, 3+	A/N	16	80 x 25	B8000	9 x 16	8	70 Hz	720 x 400
2#, 3#	A/N	16	80 x 25	B8000	8 x 16	8	70 Hz	640 x 400
4, 5	APA	4	40 x 25	B8000	8 x 8	1	70 Hz	320 x 200
6	APA	2	80 x 25	B8000	8 x 8	1	70 Hz	640 x 200
7	A/N	-	80 x 25	B0000	9 x 14	8	70 Hz	720 x 350
7*	A/N	-	80 x 25	B0000	8 x 14	8	70 Hz	640 x 350
7+	A/N	-	80 x 25	B0000	9 x 16	8	70 Hz	720 x 400
7#	A/N	-	80 x 25	B0000	8 x 16	8	70 Hz	640 x 400
D	APA	16	40 x 25	A0000	8 x 8	8	70 Hz	320 x 200
E	APA	16	80 x 25	A0000	8 x 8	4	70 Hz	640 x 200
F	APA	-	80 x 25	A0000	8 x 14	2	70 Hz	640 x 350
10	APA	16	80 x 25	A0000	8 x 14	2	70 Hz	640 x 350
11	APA	2	80 x 30	A0000	8 x 16	1	60 Hz	640 x 480
12	APA	16	80 x 30	A0000	8 x 16	1	60 Hz	640 x 480
13	APA	256(64)	40 x 25	A0000	8 x 8	1	70 Hz	320 x 200

Figure 4-2. BIOS Video Modes

Note: The border screen is not supported for the plasma display.

Programming Considerations

To prevent "tearing" of the screen image, an application reading data from or writing data to the DAC color registers should ensure that the BLANK input to the DAC is only asserted during the retrace intervals. This can be accomplished by restricting data transfers to 20 DAC entries during the retrace interval. Use VGA Input Status Register 1 to determine when retrace is occurring.

For more information about the DAC and the registers, refer to the "Video Subsystem" section of the *IBM Personal System/2 Hardware Interface Technical Reference.*

Auto-dim function

The plasma display has an auto-dim function. It automatically turns the plasma display off after the specified period since the last keystroke. Any keystroke returns the plasma display on.

A desired value for the period can be specified approximately in the range 1 to 120 minutes during the system configuration by the backup copy of the reference diskette.

Note: For German models, the background intensity of the screen is selectable. The background intensity does not affect the auto-dim function.

The auto-dim logic is integrated in the PDC on the adapter card. (See Figure 4-3.)

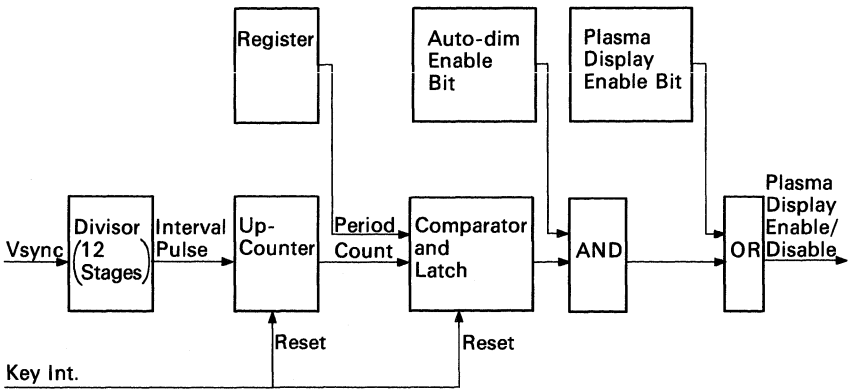


Figure 4-3. Auto-Dim Block Diagram

The sequence of auto-dim operation is as follows. (See Figure 4-3.)

1. During the system configuration, plasma display may be enabled (PDP ENABLE bit is set) and a value corresponding to the specified period is stored.
2. When the auto-dim function is enabled, the AUTO-DIM ENABLE bit is set by POST (Power-on Self Test).

3. The up-counter increases each minute with a interval pulse derived from the VSYNC (Vertical Synchronization) signal.
4. The comparator compares the count and the value specified for the period, then the result is latched.
5. The result is gated twice into the plasma display.
   If the AUTO-DIM ENABLE bit is set and the count has reached the matching value, the plasma display is disabled and the up-counter is reset. Otherwise, nothing is performed.
6. Go to step 3.

Distinctive-mapping

The plasma display controller has unique distinctive-mapping hardware for use in video modes hex 0 to hex 12. This is a transparent technique to ensure that the plasma display will correctly show the shades requested from an application.

This mapping hardware will take the output of the color registers and identify which 16 shades are currently in use by the application. It then assigns a corresponding brightness level for the plasma display and also makes sure each application color will have 1 of 16 distinct plasma display brightness levels. Colors that would be very similar on a CRT will be adjusted to a unique brightness level on the plasma display. The relative brightness positions are maintained during this process.

The result is a better image on the plasma display even when applications adjust the palette and color registers. The distinctive-mapping operation occurs during the vertical retrace interval and is automatic and transparent to the application.

If applications adjust the color registers, BIOS is recommended. The IBM PS/2 Monochrome Display 8503 and the plasma display use the DAC color registers for only the green output. BIOS will make the appropriate weighted sum from the red, green, and blue register values for use with any IBM PS/2 display. For more information, refer to the *IBM Personal System/2 and Personal Computer BIOS Interface Technical Reference*.

Half-toning (Dithering)

The plasma display can display 16 gray scales in each PEL, but the PS/2 8503 monochrome display identifies up to 64 gray scales in mode hex 13. The plasma display emulates 64 gray patterns with half-toning technology.

In the half-toning method, contiguous 2 x 2 PELs are treated as one logical dot because the resolution in mode hex 13 is 320 x 200 dots while the physical resolution is 640 x 400 PELs. The four PELs of 16 gray scales result in 64 gray patterns.

Connectors and Signals

The plasma display adapter has three connectors.

- Plasma display adapter connector to the system board
- Plasma Display connector to the plasma display
- Display connector to the external PS/2 display

Plasma display adapter connector

The following figure shows the signal assignment of the plasma display adapter connector. The connector contains the same signal set as of the 16-bit micro channel connector except two pins; the pin B04 does not provide the signal 14.3MHz OSC and the pin B45 is assigned with the signal -KEYSTROKE for the plasma display.

Pin	Signal	Pin	Signal
B01	AUDIO GND	A01	-CD SETUP
B02	AUDIO	A02	MADE 24
B03	GND	A03	GND
B04	Reserved	A04	A 11
B05	GND	A05	A 10
B06	A 23	A06	A 09
B07	A 22	A07	+5Vdc
B08	A 21	A08	A 08
B09	GND	A09	A 07
B10	A 20	A10	A 06
B11	A 19	A11	+5Vdc
B12	A 18	A12	A 05

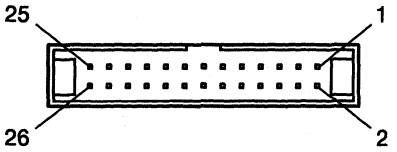
Figure 4-4 (Part 1 of 2). Plasma Display Adapter Connector

Pin	Signal	Pin	Signal
B13	GND	A13	A 04
B14	A 17	A14	A 03
B15	A 16	A15	+5Vdc
B16	A 15	A16	A 02
B17	GND	A17	A 01
B18	A 14	A18	A 00
B19	A 13	A19	+12Vdc
B20	A 12	A20	-ADL
B21	GND	A21	-PREEMPT
B22	-IRQ 09	A22	-BURST
B23	-IRQ 03	A23	-12Vdc
B24	-IRQ 04	A24	ARB 00
B25	GND	A25	ARB 01
B26	-IRQ 05	A26	ARB 02
B27	-IRQ 06	A27	-12Vdc
B28	-IRQ 07	A28	ARB 03
B29	GND	A29	ARB/-GNT
B30	Reserved	A30	-TC
B31	Reserved	A31	+5Vdc
B32	-CHCK	A32	-S0
B33	GND	A33	-S1
B34	-CMD	A34	M/-IO
B35	CHRDYRTN	A35	+12Vdc
B36	-CD SFDBK	A36	CD CHRDY
B37	GND	A37	D 00
B38	D 01	A38	D 02
B39	D 03	A39	+5Vdc
B40	D 04	A40	D 05
B41	GND	A41	D 06
B42	CHRESET	A42	D 07
B43	Reserved	A43	GND
B44	Reserved	A44	-DS 16 RTN
B45	-KEYSTROKE	A45	-REFRESH
B46	KEY	A46	KEY
B47	KEY	A47	KEY
B48	D 08	A48	+5Vdc
B49	D 09	A49	D 10
B50	GND	A50	D 11
B51	D 12	A51	D 13
B52	D 14	A52	+12Vdc
B53	D 15	A53	Reserved
B54	GND	A54	-SBHE
B55	-IRQ 10	A55	-CD DS 16
B56	-IRQ 11	A56	+5Vdc
B57	-IRQ 12	A57	-IRQ 14
B58	GND	A58	-IRQ 15

Figure 4-4 (Part 2 of 2). Plasma Display Adapter Connector

Plasma display connector

The hardware interface to the plasma display uses a 26-pin connector. The following figure shows the signal assignment.



Pin	I/O	Signal	Pin	I/O	Signal
1	O	-Vsync	2	N/A	Ground
3	O	-Hsync	4	N/A	Ground
5	O	-Data 0	6	N/A	Ground
7	O	-Data 1	8	N/A	Ground
9	O	-Data 2	10	N/A	Ground
11	O	-Data 3	12	N/A	Ground
13	O	-Display Timing	14	N/A	Ground
15	O	-Dot Clock	16	N/A	Ground
17	O	+Disable	18	N/A	Ground
19	O	-Blanking	20	N/A	Ground
21	O	-Gamma Compensation	22	O	-Background Intensity
23	N/A	Ground	24	N/A	Ground
25	N/A	Ground	26	N/A	Ground

Figure 4-5. Plasma Display Connector

Display connector

The hardware interface to the external display uses the standard PS/2 display connector. For more information, refer to "Hardware Interface Technical Reference".

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IBM Personal System/2 Model P70 Supplement

This supplement contains programming considerations that apply to the BIOS section of the *IBM Personal System/2 and IBM Personal Computer BIOS Interface Technical Reference.*

This information should be used in addition to the material covered in the above manual.

File this page behind the "Supplements" tab in the *IBM Personal System/2 and Personal Computer BIOS Interface Technical Reference.*

System Identification

- Model Byte : F8
- Submodel Byte : 0B
- Revision Level : 00

Programming Considerations for BIOS

The model P70 is fully compatible with the BIOS and ABIOS in other Personal System/2 products. Changes and enhancements are noted below.

Warning: To prevent "tearing" of the screen image, an application reading data from or writing data to the DAC color registers should ensure that the BLANK input to the DAC is only asserted during the retrace intervals. This can be accomplished by restricting data transfers to 20 DAC entries during the retrace interval. Use VGA Input Status Register 1 to determine when retrace is occurring.

For more information about the DAC and the registers, refer to the "Video Subsystem" section of the *IBM Personal System/2 Hardware Interface Technical Reference.*

Interrupt 10H - Video

(AH) = 00H - Set Mode: (AL) - Requested video mode

The following table lists hardware specific video mode characteristics:

Mode (Hex)	Type	Colors	Alpha Format	Buffer Start	Box Size	Max. Pgs.	Vert. Freq.	PELs
0, 1	A/N	16	40 x 25	B8000	8 x 8	8	70 Hz	320 x 200
0*, 1*	A/N	16	40 x 25	B8000	8 x 14	8	70 Hz	320 x 350
0+, 1+	A/N	16	40 x 25	B8000	9 x 16	8	70 Hz	360 x 400
0#, 1#	A/N	16	40 x 25	B8000	8 x 16	8	70 Hz	320 x 400
2, 3	A/N	16	80 x 25	B8000	8 x 8	8	70 Hz	640 x 200
2*, 3*	A/N	16	80 x 25	B8000	8 x 14	8	70 Hz	640 x 350
2+, 3+	A/N	16	80 x 25	B8000	9 x 16	8	70 Hz	720 x 400
2#, 3#	A/N	16	80 x 25	B8000	8 x 16	8	70 Hz	640 x 400
4, 5	APA	4	40 x 25	B8000	8 x 8	1	70 Hz	320 x 200
6	APA	2	80 x 25	B8000	8 x 8	1	70 Hz	640 x 200
7	A/N	-	80 x 25	B0000	9 x 14	8	70 Hz	720 x 350
7*	A/N	-	80 x 25	B0000	8 x 14	8	70 Hz	640 x 350
7+	A/N	-	80 x 25	B0000	9 x 16	8	70 Hz	720 x 400
7#	A/N	-	80 x 25	B0000	8 x 16	8	70 Hz	640 x 400
D	APA	16	40 x 25	A0000	8 x 8	8	70 Hz	320 x 200
E	APA	16	80 x 25	A0000	8 x 8	4	70 Hz	640 x 200
F	APA	-	80 x 25	A0000	8 x 14	2	70 Hz	640 x 350
10	APA	16	80 x 25	A0000	8 x 14	2	70 Hz	640 x 350
11	APA	2	80 x 30	A0000	8 x 16	1	60 Hz	640 x 480
12	APA	16	80 x 30	A0000	8 x 16	1	60 Hz	640 x 480
13	APA	256	40 x 25	A0000	8 x 8	1	70 Hz	320 x 200

Figure 1. Hardware Specific Video Mode Characteristics

Notes:

1. Personal System/2 Model P70

   a. The Plasma Display Panel works as an analog monochrome display.

   b. When an external display is not attached, A/N 8 bit fonts only are available in modes 0#, 1#, 2#, 3#, 7#, and 7*.

   c. The power-on default mode is 7# when an external PS/2 color display is not attached.

   d. The power-on default mode is 3+ when an external PS/2 color display is attached.

(AH) =1BH - Return Functionality/State Information: For the Personal System/2 Model P70:

```
(DI+2DH) byte - Miscellanious state information
              Bit 7 - Reserved
              Bit 6 = 1 - Plasma display active
                      (Without 9 dot width font)
              Bit 5 = 0 - Background intensity
                    = 1 - Blinking
              Bit 4 = 1 - Cursor emulation active
                      (Always 0 for Personal System/2 Model
              Bit 3 = 1 - Mode set default palette loading disable
              Bit 2 = 1 - Monochrome display attached
              Bit 1 = 1 - Summing active
              Bit 0 = 1 - All modes on all displays active
                      (Always 0 for Personal System/2 Model 30)
```

Notes:

1. When the bit 6 is set to 1, the screen modes with 9-dot width font are not available. They are 0+, 1+, 2+, 3+, 7 and 7+.
2. If one of those modes is requested, BIOS automatically sets it to a mode with 8-dot width font. They are 0#, 1#, 2#, 3#, 7#, and 7*.

Video Supplement

This supplement contains programming considerations that apply to the Advanced BIOS section of the *IBM Personal System/2 and IBM Personal Computer BIOS Interface Technical Reference.*

This information should be used in addition to the material covered in the Advanced BIOS (ABIOS) section of the above manual.

Programming Considerations

The following are the model P70 video functions.

03H - Read Device Parameters

This function returns parameters that indicate the current video state.

Service Specific Output

SIZE	OFFSET	DESCRIPTION
Byte	+1B	Reserved
Byte	+1C	Number of scan lines on the screen 00H - 200 scan lines 01H - 350 scan lines 02H - 400 scan lines 03H - 480 scan lines 04H to FFH - Reserved
Word	+1E	Video mode setting
Word	+20	Type of monitor attached Bits 15 to 2 - Reserved Bit 1 - Plasma display 0 - Inactive 1 - Active Bit 0 - Color vs Monochrome 0 - Color display 1 - Monochrome display
Word	+22	Character height (bytes/character)
Word	+24	Character block specifier Bits 15 to 12 - Reserved Bits 11 to 8 - Character block select A Bits 7 to 4 - Reserved Bits 3 to 0 - Character block select B
Word	+2A	Size of data buffer required for the Return ROM Fonts function in bytes.
Word	+2E	Size of save/restore buffer header in bytes.
Word	+30	Size of save/restore hardware state in bytes.
Word	+32	Size of save/restore device block state in bytes.
Word	+34	Size of save/restore DAC state in bytes.

Notes:

1. When offset +20 bit 1 is set to 1, the screen modes with 9-dot width font are not available. They are 0+, 1+, 2+, 3+, 7 and 7+.
2. If one of those modes is requested, BIOS automatically sets it to a mode with 8-dot width font. They are 0#, 1#, 2#, 3#, 7#, and 7*.

Notes: