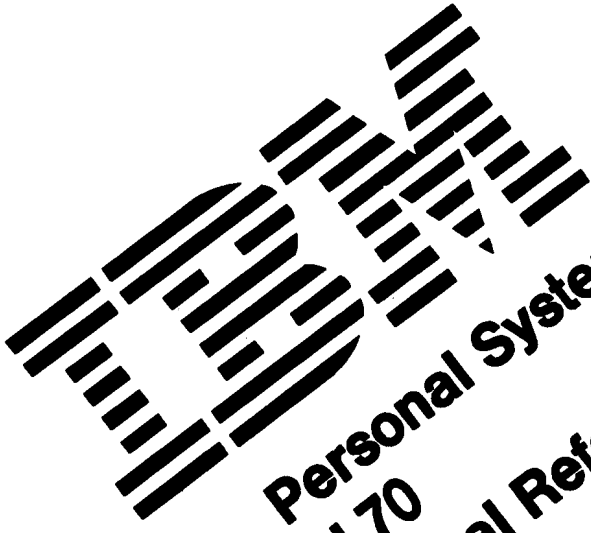

Personal System/2
Model 70
Technical Reference

Fourth Edition (October 1990)

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Preface

This technical reference contains hardware and software interface information specific to the IBM Personal System/2 Model 70 computer. It is intended for those who develop hardware and software products for these systems. Users should understand computer architecture and programming concepts.

This publication consists of the following sections:

Section 1, "System Overview," describes the system, features, and specifications.

Section 2, "Programmable Option Select," describes the registers used for configuration.

Section 3, "System Board," describes the system-specific hardware implementations.

This technical reference should be used with the following publications:

IBM Personal System/2 Hardware Interface Technical Reference — Architectures

IBM Personal System/2 Hardware Interface Technical Reference — Common Interfaces

IBM Personal System/2 and Personal Computer BIOS Interface Technical Reference

These publications contain additional information on many of the subjects discussed in this technical reference.

Warning: The term "Reserved" describes certain signals, bits, and registers that should not be changed. Use of reserved areas can cause compatibility problems, loss of data, or permanent damage to the hardware. When the contents of a register are changed, the state of the reserved bits must be preserved. When possible, read the register first and change only the bits that must be changed.

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Notes:

Description

The IBM* Personal System/2* Model 70 computer is a self-contained, desktop computer that features the Micro Channel* architecture. This system can support two diskette drives and one internal fixed disk drive and comes with a keyboard.

A system can have either a Type 1, Type 2, Type 3, or Type 4 system board. The major differences among the four system boards are system clock speed, component layout, and memory. In addition, the Type 3 and Type 4 system boards have the following features.

The Type 3 system board:

- Uses a two-way, set-associative, store-through, 64KB (KB = 1,024 bytes) cache for instructions and data.
- Has the microprocessor, math coprocessor, cache, and cache controller mounted on a processor card that attaches to the system board.
- Has four connectors for system board memory.

The Type 4 system board:

- Uses the Intel 80486 microprocessor, which includes an internal 8KB, 4-way set-associative cache and an internal numeric coprocessor on a processor card.
- Has four connectors for system board memory.

* IBM, Personal System/2, and Micro Channel are trademarks of the International Business Machines Corporation.

Programs identify the type of system board by reading the model and submodel bytes. Interrupt hex 15, function code (AH) = hex C0, returns the model and submodel bytes. The following table shows these bytes, system board types, and system clock speeds.

Model Byte	Submodel Byte	System Board	System Clock/Microprocessor
F8	09	Type 1	16 MHz/80386
F8	04	Type 2	20 MHz/80386
F8	0D	Type 3	25 MHz/80386
F8	1B	Type 4	25 MHz/80486

Figure 1-1. Model and Submodel Bytes

Refer to the *IBM Personal System/2 and Personal Computer BIOS Interface Technical Reference* for a listing of other systems, and check the supplements section for updates to that listing.

System Board Features

The following tables list the system board devices and features. The *Hardware Interface Technical Reference* manuals describe devices common to PS/2* products by type number.

* PS/2 is a trademark of the International Business Machines Corporation.

Device	Type	Features
Microprocessor	---	80386 32-bit address and 32-bit data interface
System Timers	1	Channel 0 – System timer Channel 2 – Tone generation for speaker Channel 3 – Watchdog timer
ROM Subsystem	---	128KB (KB = 1024 bytes)
RAM Subsystem	---	1 to 6MB on the system board (MB = 1,048,576 bytes) Expandable on the channel
CMOS RAM Subsystem	---	64-byte CMOS RAM with real-time clock/calendar 2KB CMOS RAM extension Battery backup
Video Subsystem	1	Auxiliary connector on the channel Analog output 256KB video memory
Audio Subsystem	1	Driven by: - System-timer channel 2 - The 'audio sum node' signal.
DMA Controller	1	Eight independent DMA channels Single or burst transfers and read verification
Interrupt Controller	1	16 levels of system interrupts Interrupts are level-sensitive
Keyboard/Auxiliary Device Controller	1, 2	Keyboard connector Auxiliary device connector Password security
Diskette Drive Controller	1	Supports: - 720KB formatted diskette density - 1.44MB formatted diskette density
Serial Controller	2	RS-232C interface Programmable as serial port 1 or 2 FIFO mode and character mode
Parallel Controller	1	Programmable as parallel port 1, 2, or 3 Supports bidirectional input and output
Micro Channel	---	Three channel connectors for Type 3 adapters : - One 16-bit connector with an auxiliary video extension - Two 32-bit connectors with matched-memory extension
Math Coprocessor Socket	---	Supports 80387 Math Coprocessor Same clock speed as the system microprocessor
Power Supply	1	110 and 220 Vac support

Figure 1-2. System Board Devices and Features – Types 1 and 2

Device	Type	Features
Microprocessor	---	80386 32-bit address and 32-bit data interface
Microprocessor Cache	---	82385 Cache Controller 64KB of static-RAM cache
System Timers	1	Channel 0 – System timer Channel 2 – Tone generation for speaker Channel 3 – Watchdog timer
ROM Subsystem	---	128KB
RAM Subsystem	---	2 to 8MB on the system board Expandable on the channel
CMOS RAM Subsystem	---	64-byte CMOS RAM with real-time clock/calendar 2KB CMOS RAM extension Battery backup
Video Subsystem	1	Auxiliary connector on the channel Analog output 256KB video memory
Audio Subsystem	1	Driven by: - System-timer channel 2 - The 'audio sum node' signal
DMA Controller	1	Eight independent DMA channels Single or burst transfers and read verification
Interrupt Controller	1	16 levels of system interrupts Interrupts are level-sensitive
Keyboard/Auxiliary Device Controller	1	Keyboard connector Auxiliary device connector Password security
Diskette Drive Controller	1	Supports: - 720KB formatted diskette density - 1.44MB formatted diskette density
Serial Controller	2	RS-232C interface Programmable as serial port 1 or 2 FIFO mode and character mode
Parallel Controller	1	Programmable as parallel port 1, 2, or 3 Supports bidirectional input and output
Micro Channel	---	Three channel connectors for Type 3 adapters: - One 16-bit connector with an auxiliary video extension - Two 32-bit connectors with matched-memory extension.
Math Coprocessor Socket	---	Supports 80387 Math Coprocessor Same clock speed as the system microprocessor

Figure 1-3. System Board Devices and Features – Type 3

Device	Type	Features
Microprocessor	---	80486 at 25 MHz 32-bit address and 32-bit data interface
Microprocessor Cache	---	8KB internal cache 4-way set associative
Math Coprocessor	---	Internal floating point coprocessor 80387 compatible No optional math coprocessor
System Timers	1	Channel 0 – System timer Channel 2 – Tone generation for speaker Channel 3 – Watchdog timer
ROM Subsystem	---	128KB
RAM Subsystem	---	2 to 8MB on the system board Expandable on the channel
CMOS RAM Subsystem	---	64-byte CMOS RAM with real-time clock/calendar 2KB CMOS RAM extension Battery backup
Video Subsystem	1	Auxiliary connector on the channel Analog output 256KB video memory
Audio Subsystem	1	Driven by: - System-timer channel 2 - The 'audio sum node' signal
DMA Controller	1	Eight independent DMA channels Single or burst transfers and read verification
Interrupt Controller	1	16 levels of system interrupts Interrupts are level-sensitive
Keyboard/Auxiliary Device Controller	1	Keyboard connector Auxiliary device connector Password security
Diskette Drive Controller	1	Supports: - 720KB formatted diskette density - 1.44MB formatted diskette density
Serial Controller	2	RS-232C interface Programmable as serial port 1 or 2 FIFO mode and character mode
Parallel Controller	1	Programmable as parallel port 1, 2, or 3 Supports bidirectional input and output
Micro Channel	---	Three channel connectors for Type 3 adapters: - One 16-bit connector with an auxiliary video extension - Two 32-bit connectors with matched-memory extension

Figure 1-4. System Board Devices and Features – Type 4

System Board I/O Address Map

Hex Addresses	Device
0000 - 001F	DMA Controller (0 – 3)
0020, 0021	Interrupt Controller (Master)
0040, 0042 - 0044, 0047	System Timers
0060	Keyboard, Auxiliary Device
0061	System Control Port B
0064	Keyboard, Auxiliary Device
0070, 0071	RT/CMOS and NMI Mask
0081 - 0083, 0087	DMA Page Registers (0 – 3)
0089 - 008B, 008F	DMA Page Registers (4 – 7)
0090	Central Arbitration Control Point
0091	Card Selected Feedback Register
0092	System Control Port A
0094	System Board Enable/Setup Register
0096	Adapter Enable/Setup Register
00A0 - 00A1	Interrupt Controller (Slave)
00C0 - 00DF	DMA Controller (4 – 7)
00E0 - 00E2	Memory Encoding Registers
00F0 - 00FF	Math Coprocessor
0100 - 0107	Programmable Option Select
01F0 - 01F8	Fixed Disk Drive Controller
0278 - 027B	Parallel Port 3
02F8 - 02FF	Serial Port 2 (RS-232C)
0378 - 037B	Parallel Port 2
03B4, 03B5, 03BA	Video Subsystem
03BC - 03BF	Parallel Port 1
03C0 - 03C5	Video Subsystem
03C6 - 03C9	Video DAC
03CA, 03CC, 03CE, 03CF	Video Subsystem
03D4, 03D5, 03DA	Video Subsystem
03F0 - 03F7	Diskette Drive Controller
03F8 - 03FF	Serial Port 1 (RS-232C)

Figure 1-5. System Board I/O Address Map

Specifications

Device	Number of Waits	Cycle Time (ns)
Microprocessor (16 MHz – 62.5 ns Clock):		
Access to System Board RAM: *		
Memory Read (Page Hit)	0	125
Memory Read (Page Miss)	2	250
Memory Write (Page Hit)	1	187.5
Memory Write (Page Miss)	2	250
Access to Channel:		
Default Transfer Cycle	2	250
Synchronous Extended Transfer Cycle	4	375
Refresh Rate (Typically performed every 15.1 μs)		625 (min)
Bus Master Access to System Board RAM		300 (min)
DMA Controller (8 MHz – 125 ns Clock):		
Single Transfer: 375 + I/O Access + Memory Access		
Burst Transfers: 375 + (I/O Access + Memory Access)N **		
System Board Memory Access		375
Default Transfer Cycle		250
Synchronous Extended Transfer Cycle		375

* Adapters installed in the channel should not rely on monitoring system board memory accesses because channel memory control signals may not be present during these accesses.

** N is the number of transfers in the burst.

Figure 1-6. Performance Specifications – Type 1

Device	Number of Waits	Cycle Time (ns)
Microprocessor (20 MHz – 50 ns Clock):		
Access to System Board RAM: *		
Memory Read (Page Hit)	0	100
Memory Read (Page Miss)	2	200
Memory Write (Page Hit)	1	150
Memory Write (Page Miss)	2	200
Access to Channel:		
Default Transfer Cycle	2	200
Synchronous Extended Transfer Cycle	4	300
Refresh Rate (Typically performed every 15.1 μs)		500 (min)
Bus Master Access to System Board RAM		300 (min)
DMA Controller (10 MHz – 100 ns Clock):		
Single Transfer: 300 + I/O Access + Memory Access		
Burst Transfers: 300 + (I/O Access + Memory Access)N **		
System Board Memory Access		300
Default Transfer Cycle		200
Synchronous Extended Transfer Cycle		300

* Adapters installed in the channel should not rely on monitoring system board memory accesses because channel memory control signals may not be present during these accesses.

** N is the number of transfers in the burst.

Figure 1-7. Performance Specifications – Type 2

Device	Number of Waits	Cycle Time (ns)
Microprocessor (25 MHz – 40 ns Clock):		
Access to System Board RAM: *		
Memory Read (Cache Hit)	0	80
Memory Write (Cache Hit)	0	80**
Memory Read (Cache Miss, Page Hit)	0 - 2	80 - 160
Memory Write (Cache Miss, Page Hit)	1	80**
Memory Read (Cache Miss, Page Miss)	3 - 5	200 - 280
Memory Write (Cache Miss, Page Miss)	0	80**
Access to Channel:		
Default Transfer Cycle	4	240
Synchronous Extended Transfer Cycle	7	360
Refresh Rate (Typically performed every 15.1 μs)		600 (min)
Bus Master Access to System Board RAM		300 (min)
DMA Controller (10 MHz – 100 ns Clock):		
Single Transfer: 300 + I/O Access + Memory Access		
Burst Transfers: 300 + (I/O Access + Memory Access)N ***		
System Board Memory Access		300
Default Transfer Cycle		200
Synchronous Extended Transfer Cycle		300

* Adapters installed in the channel should not rely on monitoring system board memory accesses because channel memory control signals may not be present during these accesses.

** The write operation is buffered outside the microprocessor. Additional time is required if another write operation or read operation with a cache-miss occurs before the write operation is completed.

*** N is the number of transfers in the burst.

Figure 1-8. Performance Specifications – Type 3

Device	Number of Waits	Cycle Time (ns)
Microprocessor (25 MHz – 40 ns Clock):		
Internal 80486 Cache Hits: *		
Access to System Board RAM: *		
Memory Read	0	40
Memory Write	0	40**
Memory Read (Page Hit)		400***
Memory Write (Page Hit)	4	240**
Memory Read (Page Miss)		520***
Memory Write (Page Miss)	5	280**
Access to Channel:		
Default Transfer Cycle	6	320
Synchronous Extended Transfer Cycle	9	440
Refresh Rate (Typically performed every 15.1 μs)		200 (min)
Bus Master Access to System Board RAM		300 (min)
DMA Controller (10 MHz – 100 ns Clock):		
Single Transfer: 300 + I/O Access + Memory Access		
Burst Transfers: 300 + (I/O Access + Memory Access)N ****		
System Board Memory Access		300
Default Transfer Cycle		200
Synchronous Extended Transfer Cycle		300

* Adapters installed in the channel should not rely on monitoring system board memory accesses because channel memory control signals may not be present during these accesses.

** The memory write is buffered internally. The 80486 contains a four-deep write-through buffer (refer to the Intel specifications for more information). Additional time is required if another write operation or a read operation with a cache-miss occurs before the write operation is completed.

*** The 80486 bus cycle is nonpipelined, and always fetches a 16-byte line from cacheable memory space. The number of clock cycles for memory read with a cache miss:

- If page hit on first access, 4–2–2–2
- If page miss on first access, 7–2–2–2.

**** N is the number of transfers in the burst.

Figure 1-9. Performance Specifications – Type 4

Size:	
Width	360 mm (14.1 in)
Depth	420 mm (16.5 in)
Height	140 mm (5.5 in)
Weight	9.55 kg (21 lb)
Cables:	
Power Cable	1.8 m (6 ft)
Keyboard Cable	1.8 m (6 ft)
Air Temperature:	
System On	15.6 to 32.2°C (60 to 90°F)
System Off	10.0 to 43.0°C (50 to 110°F)
Humidity:	
System On	8% to 80%
System Off	8% to 80%
Maximum Altitude	2133.6 m (7000 ft)
Heat Output	215 Watts (735 BTUs per hour)
Acoustical Readings	(See Figure 1-11 on page 1-14)
Electrical Input:	
Input Voltage (Range is automatically selected; sinewave input is required):	
Low Range	90 (min) – 137 (max) Vac
High Range	180 (min) – 265 (max)Vac
Frequency:	
Low Range	47 (min) – 53 (max) Hz
High Range	57 (min) – 63 (max) Hz
Input in Kilovolt-Ampere (kVA):	
Minimum configuration (as shipped by IBM)	0.13 kVA
Maximum configuration	0.36 kVA
Electromagnetic Compatibility	
FCC Class B	

Figure 1-10. Physical Specifications

Description	L_{WAd} in bels		L_{pAm} in dB		$<L_{pA}>_m$ in dB	
	Operate	Idle	Operate	Idle	Operate	Idle
Model 70	5.3	5.3	43	43	40	40

Notes:

L_{WAd} is the declared sound power level for the random sample of machines.

L_{pAm} is the mean value of the A-weighted sound pressure levels at the operator position (if any) for the random sample of machines.

$<L_{pA}>_m$ is the mean value of the A-weighted sound pressure levels at the one-meter positions for the random sample of machines.

All measurements made in accordance with ANSI S12.10, and reported in conformance with ISO DIS 9296.

The measurements are preliminary data and subject to change.

Figure 1-11. Acoustical Readings

Power Supply

The power supply requires a sineware input and converts the ac input voltage to three dc output voltages. The power supply provides power for the following:

- System board
- Channel adapters
- Internal diskette drives
- Internal fixed disk drive
- Auxiliary device
- Keyboard.

The power switch and one light-emitting diode (LED) are on the front of the system unit. The power supply is operating when the LED is lit.

Outputs

The power supply provides separate voltage sources for the system board and the drives. The system-board voltages are +5 Vdc, +12 Vdc, and −12 Vdc. The drive voltages are +5 Vdc and +12 Vdc. The following is a list of the approximate power provided for system components.

System Component	Maximum Current	
	+12 Vdc	+5 Vdc
Auxiliary Device	None	300 mA
Keyboard	None	275 mA

Figure 1-12. Component Maximum Current

The following are the load currents allowed for each channel connector.

Supply Voltage	16-Bit Connector Maximum Current	32-Bit Connector Maximum Current
+ 5.0 Vdc	1.6 A	2.0 A
+12.0 Vdc	0.175 A	0.175 A
−12.0 Vdc	0.040 A	0.040 A

Figure 1-13. Channel Load Current

The formulas used to determine the power requirements and the voltage regulation tolerances are in the Micro Channel adapter design information in the *Hardware Interface Technical Reference - Architectures* manual.

Output Protection

A short circuit placed on any dc output (between outputs or between an output and dc return) latches all dc outputs into a shutdown state with no damage to the power supply.

If an overvoltage fault occurs (internal to the power supply), the power supply latches all dc outputs into a shutdown state before any output exceeds 130% of its nominal value.

If either of these shutdown states is actuated, the power supply returns to normal operation only after the fault has been removed and the power switch has been turned off for at least ten seconds.

Voltage Sequencing

At power-on time, the output voltages track within 50 milliseconds of each other when measured at the 50% points.

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Notes:

Description

Programmable Option Select (POS) eliminates the need for switches by replacing their function with programmable registers. This section describes the POS information used on the Model 70 system boards. For additional POS information, refer to the Hardware Interface Technical Reference Micro Channel architecture information.

Warning:

- IBM recommends that programmable options be set only through the System Configuration utilities. Directly setting the POS registers or CMOS RAM POS parameters can result in multiple assignment of the same system resource, improper operation of the feature, loss of data, or possible damage to the hardware.
- Application programs should not use the adapter identification (ID) unless absolutely necessary. Compatibility problems can result.
- If an adapter and the system board are in setup mode at the same time, bus contention will occur, no useful programming can take place, and damage to the hardware can occur.
- After setup operations are complete, the Adapter Enable/Setup register (hex 0096) should be set to hex 00, and the System Board Enable/Setup register (hex 0094) should be set to hex FF.
- Bit 7 (channel reset) in the Adapter Enable/Setup register must be 0 to program the adapters.
- Only 8-bit instructions are supported for setup operations. Using 32- or 16-bit I/O instructions on 8-bit POS registers will cause erroneous data to be written or read.

Setup functions respond to I/O addresses hex 0100 through 0107 only when their unique setup signal is active. The following precautions must be taken before setting individual bits in the POS registers.

System Board Video Subsystem Setup:

- Bit 5 in the System Board Enable/Setup register (hex 0094) must be set to 0 to place the system board video into the setup mode.
- Bit 3 in the Adapter Enable/Setup register (hex 0096) must be set to 0 to avoid driving a 'setup' signal to an adapter.
- Bit 7 in the System Board Enable/Setup register must be set to 1 to avoid driving a 'setup' signal to other system board functions.

Adapter Setup:

- Bit 3 in the Adapter Enable/Setup register must be set to 1 to allow adapter setup.
- Bit 5 in the System Board Enable/Setup register must be set to 1 to avoid driving a 'setup' signal to the Video Subsystem.
- Bit 7 in the System Board Enable/Setup register must be set to 1 to avoid driving a 'setup' signal to a system board function.

Other System Board Setup:

- Bit 7 in the System Board Enable/Setup register must be set to 0 to allow setup of other system board functions.
- Bit 3 in the Adapter Enable/Setup register must be set to 0 to avoid driving a 'setup' signal to an adapter.
- Bit 5 in the System Board Enable/Setup register must be set to 1 to avoid driving a 'setup' signal to the Video Subsystem.

POS Address Map

The following table shows the organization of the I/O address space used by POS. Bit 0 of POS Register 2 and bits 6 and 7 of POS Register 5 are fixed. All other bits in POS Registers 2 through 5 are free-form.

Address (Hex)	Function
0094	System Board Enable/Setup Register
0096	Adapter Enable/Setup Register
0100	POS Register 0—Adapter Identification Byte (Low Byte)
0101	POS Register 1—Adapter Identification Byte (High Byte)
0102	POS Register 2—Option Select Data Byte 1 Bit 0 is Card Enable.
0103	POS Register 3—Option Select Data Byte 2
0104	POS Register 4—Option Select Data Byte 3
0105	POS Register 5—Option Select Data Byte 4 Bit 7 is the channel check active indicator Bit 6 is the channel check status-available indicator
0106	POS Register 6—Reserved
0107	POS Register 7—Reserved

Figure 2-1. POS I/O Address Map

Card Selected Feedback

When an adapter is addressed, it responds by setting the '-card selected feedback' signal (-CD SFDBK) to active. -CD SFDBK is derived from the address decode and driven by a totem pole driver. It is latched by the system board and can be read through the Card Selected Feedback register at address hex 0091. Diagnostic and automatic configuration programs use this signal to verify the operation of an adapter at a given address or DMA port. This signal must not be active during a setup cycle.

The Card Selected Feedback register is a read-only register at address hex 0091. It allows programs to monitor -CD SFDBK and thereby determine if the video subsystem, system board I/O, or an adapter is addressed and functioning.

Bit	Function
7 - 1	Reserved
0	-Card Selected Feedback

Figure 2-2. Card Selected Feedback Register (Hex 0091)

Bits 7 - 1 These bits are reserved.

Bit 0 This bit is set to 1 whenever -CD SFDBK was active on a previous cycle or whenever the system board I/O functions (diskette drive, serial, or parallel interfaces) are accessed by an I/O cycle. Reading this register resets the bit to 0.

System Board Setup

The integrated I/O functions on the system board use POS information during setup. The diskette drive controller, serial port, and parallel port are treated as a single device. The video subsystem is also an integrated part of the system board; however, POS treats it as a separate device. The System Board Enable/Setup register is used to place the system board or the video subsystem into the setup mode.

System Board Enable/Setup Register (Hex 0094)

This is a read/write register; all bits in this register default to 1 (enabled).

Bit	Function
7	Enable/-Setup System Board Functions
6	Reserved
5	Enable/-Setup Video Subsystem
4 - 0	Reserved

Figure 2-3. System Board Enable/Setup Register (Hex 0094)

Bit 7 When this bit is set to 0, various system board I/O functions are placed in the setup mode. The diskette drive controller, serial port, and parallel port are controlled through System Board POS Register 2 (hex 0102).

When this bit is set to 1, the system board function is enabled.

Bit 6 This bit is reserved.

Bit 5 When this bit is set to 0, the video subsystem is placed in the setup mode and controlled through POS Register 2 (hex 0102). When set to 1, and bit 0 in hex 0102 is set to 1, video is enabled.

Bit 0 of POS Register 2 is the video enable bit. When this bit is set to 0, the video subsystem does not respond to commands, addresses, or data. If video is being generated when the video enable bit is set to 0, the output is still generated. For information on BIOS calls to enable or disable the video, see the *IBM Personal System/2 and Personal Computer BIOS Interface Technical Reference.*

Note: When video is disabled, access to the video DAC registers is disabled.

Bits 4 - 0 These bits are reserved.

System Board POS Register 2 (Hex 0102)

When the system board is in the setup mode, the diskette drive controller, serial port, and parallel port are controlled by this read/write register. Reading this register returns the current state of these system board functions.

Bit	Function
7	Disable Parallel Port Extended Mode
6, 5	Parallel Port Select
4	Enable Parallel Port
3	Serial Port Select
2	Enable Serial Port
1	Enable Diskette Drive Interface
0	Enable System Board

Figure 2-4. System Board POS Register 2 (Hex 0102)

Bit 7 When set to 0, this bit allows the parallel port to be configured as an 8-bit, parallel, bidirectional interface. When set to 1, this bit disables the bidirectional mode. This bit is set to 0 at power-on and POST sets it to 1.

Bits 6, 5 These bits select the configuration of the system board parallel port.

Bits 6 5	Assignment	Hex Address	Interrupt Level
0 0	Parallel 1	03BC - 03BF	7
0 1	Parallel 2	0378 - 037B	7
1 0	Parallel 3	0278 - 027B	7
1 1	Reserved	----------	-

Figure 2-5. Parallel Port Select Bits

Bit 4 When this bit and bit 0 are set to 1, the system board parallel port is enabled.

Bit 3 When set to 1, this bit sets the system board serial port as Serial 1 (addresses hex 03F8 through 03FF), which uses interrupt level 4. When set to 0, this bit sets the serial port as Serial 2 (addresses hex 02F8 through 02FF), which uses interrupt level 3.

Bit 2 When this bit and bit 0 are set to 1, the system board serial port is enabled.

Bit 1 When this bit and bit 0 are set to 1, the diskette drive interface is enabled.

Bit 0 When set to 1, this bit allows bits 4, 2, and 1 to enable and disable their respective devices. When set to 0, this bit disables the diskette drive interface, system board serial port, and system board parallel port, regardless of the state of bits 4, 2, and 1.

System Board POS Register 3 (Hex 0103) – Types 1 and 2

This port contains information about the presence and type of memory card installed in each system board memory connector of Type 1 and Type 2 system boards.

How this information is stored and retrieved depends on whether the port is read-only or read/write. To determine the type of port, with a memory card in connector 1, set bit 2 of port hex 103 to 1, and then read port hex 103. If bit 0 of this byte is 0, the port is read-only (connector 1 card present); if bit 0 is 1, the port is read/write (the reserved bit is read as 1).

POS Register 3 as a Read-Only Port
For these systems, the memory connectors are numbered from left to right as viewed from the front of the system.

Bit	Function
7	Reserved
6	2MB/-1MB Card, Connector 3
5	-Card Present, Connector 3
4	Reserved
3	2MB/-1MB Card, Connector 2
2	-Card Present, Connector 2
1	2MB/-1MB Card, Connector 1
0	-Card Present, Connector 1

Figure 2-6. System Board POS Register 3 (Read-Only) – Types 1 and 2

Bits 7, 4 These bits are reserved.

Bits 6, 3, 1 Each bit indicates the type of memory card installed. When set to 1, the bit indicates that the card is a 2MB memory card. When set to 0, the bit indicates that the card is a 1MB memory card.

Bits 5, 2, 0 When set to 0, each bit indicates that a memory card is installed.

POS Register 3 as a Read/Write Port

For these systems, the memory connectors are numbered from right to left as viewed from the front of the system.

Bit	Function
7 - 3	Reserved
2	-Connector 1 and 2
1, 0	Reserved

Figure 2-7. System Board POS Register 3 (Write-Access) — Types 1 and 2

Bits 7 - 3 These bits are reserved.

Bit 2 This bit selects the connector information returned when port hex 0103 is read. When this bit is set to 0, the information for connectors 1 and 2 is shown. This bit is write only.

Bits 1, 0 These bits are reserved.

Bits	Function
7 - 4	Presence Detect 3 - 0, Connector 1
3 - 0	Presence Detect 3 - 0, Connector 2

Figure 2-8. Read Port with Bit 2 Set to 0

When bit 2 is set to 1, connector 3 information is shown.

Bits	Function
7 - 4	Presence Detect 3 - 0, Connector 3
3 - 0	Reserved

Figure 2-9. Read Port with Bit 2 Set to 1

Each set of four bits shows the state of the presence detect signals for that connector (see Figure 2-12 on page 2-14 for more information).

System Board POS Register 3 (Hex 0103) – Types 3 and 4

On the Type 3 and Type 4 system boards, two read-only registers, POS register 3 and POS register 4, contain information about the type of memory on the system board. The memory connectors are numbered from left to right as viewed from the front of the system. (See Figure 2-12 on page 2-14 for information on the signals.)

Bit	Function
7	AND of Presence Detect 3
6	Presence Detect 0, Connector 3
5	Presence Detect 2, Connector 3
4	Reserved
3	Presence Detect 0, Connector 2
2	Presence Detect 2, Connector 2
1	Presence Detect 0, Connector 1
0	Presence Detect 2, Connector 1

Figure 2-10. System Board POS Register 3 (Hex 0103) – Types 3 and 4

Bits 7 This bit is the AND of the 'presence detect 3' signal for all connectors. This bit is 1 if the proper memory cards are installed.

Bits 6, 3, 1 Each bit indicates the state of the 'presence detect 0' signal.

Bits 5, 2, 0 Each bit indicates the state of the 'presence detect 2' signal.

Bit 4 This bit is reserved.

System Board POS Register 4 (Hex 0104) – Types 3 and 4

On the Type 3 and Type 4 system boards, this read-only register and POS Register 3 contain information about the type of memory on the system boards.

Bit	Function
7	Presence Detect 1, Connector 4
6	Presence Detect 1, Connector 3
5	Presence Detect 1, Connector 2
4	Presence Detect 1, Connector 1
3, 2	Cache ID bits
1	Presence Detect 0, Connector 4
0	Presence Detect 2, Connector 4

Figure 2-11. System Board POS Register 4 (Hex 0104) – Types 3 and 4

Bits 7 - 4 These bits indicate the state of the 'presence detect 1' signal.

Bits 3, 2 These bits describe the processor card. Both bits are set to binary 00 on the Type 3 system board, indicating a 64KB cache with a 80386 microprocessor operating at 25 MHz. The cache ID bits are set to binary 01 on the Type 4 system board, indicating a 80486 microprocessor operating at 25 MHz.

Bit 1 This bit indicates the state of the 'presence detect 0' signal.

Bit 0 This bit indicates the state of the 'presence detect 2' signal.

Memory Presence Detect

The presence detect signals are used by the system to determine size and speed of memory on the memory card. The pins are either connected to ground or not connected.

A set of four bits shows the state of all presence detect signals for a specific memory connector; the bit is 0 when the signal is grounded. The following table shows the information indicated by these bits and the system board types that support each memory card. All combinations not shown are reserved.

Presence Detect 3	2	1	0	Function	System Board
0	0	1	0	1MB 100-ns Memory	Type 1
0	0	0	1	2MB 100-ns Memory	Type 1
0	1	1	0	1MB 85-ns Memory	Types 1 and 2
0	1	0	1	2MB 85-ns Memory	Types 1 and 2
1	0	0	1	2MB 80-ns Memory	Types 3 and 4

Figure 2-12. Presence Detect Bits

Adapter Enable/Setup Register (Hex 0096)

This read/write register selects the connector to be configured.

Bit	Symbol
7	Channel Reset
6 - 4	Reserved
3	Card Setup Enable
2 - 0	Channel Select 2 - 0

Figure 2-13. Adapter Enable/Setup Register (Hex 0096)

Bit 7 When set to 1, this bit activates the 'channel reset' signal to all connectors.

Bits 6 - 4 These bits are reserved.

Bit 3 When set to 1, this bit enables the '-card setup' signal selected by bits 2 through 0.

Bits 2 - 0 These bits are the address bits for the '-card setup' signal. Connectors 1 through 3 are addressed as 0 through 2, respectively, and the fixed disk connector is addressed as 3. When bit 3 is set to 1, these bits select the connector that is put into setup mode.

Each channel connector has a unique '-card setup' signal (-CD SETUP) associated with it. This signal is used to put the adapters in the setup mode, which allows access to the POS registers. The individual connectors are selected through the Adapter Enable/Setup register. Setup information is then read from or written to the selected adapter through I/O addresses hex 0100 through 0107.

Notes:

1. -CD SETUP goes active only when an operation is performed in the I/O address range hex 0100 through 0107.
2. The status of port hex 0096 can be read by software. However, when the port is read, bits 6, 5, and 4 are set to 1.

Notes:

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Description

This section describes the math coprocessor, channel differences, memory subsystems, and miscellaneous system ports and connectors for the Model 70. Additional information on these topics can be found in the *Hardware Interface Technical Reference* listed in the preface of this manual.

80387 Math Coprocessor

The 80387 Math Coprocessors are matched to the speed of the system microprocessor and operate in the synchronous mode. The different speed coprocessors are not interchangeable; their logical operation is the same.

The microprocessor on the Type 4 system board incorporates the 80387 Math Coprocessor. Programs written for the 80387 Math Coprocessor will run without modifications.

Micro Channel Implementation

This section describes the implementation of the Micro Channel architecture on Model 70 systems. Refer to the Hardware Interface Technical Reference Micro Channel information for more information.

Exception Reporting

Exceptions should be reported using the asynchronous channel check procedure. The synchronous channel check procedure is not supported.

Matched-Memory

Each 32-bit channel connector has a matched-memory extension. The system microprocessor activates the '-matched memory cycle' signal (-MMC) when it does a memory access. This allows the Model 70 to support the same memory adapter design as the PS/2 Model 80 system board.

Although a memory adapter can respond to -MMC active by driving the '-matched memory cycle request' signal (-MMCR) active, the

Model 70 system board ignores -MMCR and performs a default cycle if the 'channel ready' signal (CD CHRDY) is active, or a synchronous-extended cycle if CD CHRDY is inactive. The Model 70 also drives the '-matched memory cycle command' signal active at the same time as the '-command' signal.

Matched-Memory Extension

This extension to the 32-bit Micro Channel connector provides the signals necessary to accommodate matched-memory cycles.

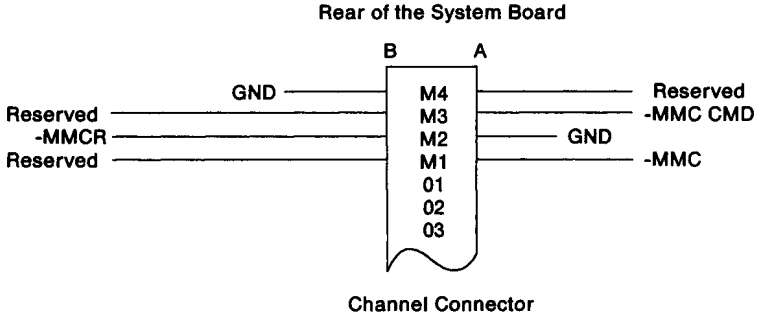

Figure 3-1. Matched-Memory Extension Voltage and Signal Assignments

Signal Descriptions

The following are descriptions of the matched-memory signals.

-MMC: -Matched Memory Cycle: This signal is driven by the system board logic to indicate to the channel slaves that the system microprocessor is the controlling master and is able to run a matched-memory cycle. -MMC is driven by a tri-state driver that can sink 24 milliamps.

-MMCR: -Matched Memory Cycle Request: This is a bus cycle control input signal. A 16- or 32-bit channel slave drives -MMCR to request a matched-memory cycle available on the system bus. This signal is driven active from an address decode and MEMORY/-IO signal.

If -MMCR is driven active by an 8-bit channel slave, or if it is driven active by a 16- or 32-bit channel slave during a cycle other than a microprocessor bus cycle, a default transfer cycle is run and -MMCR is not honored. CD CHRDY is used to extend the matched-memory cycle, as needed. The 'address latch' signal (-ADL) and -CMD remain inactive for the entire matched-memory cycle.

Only the system microprocessor can drive matched-memory cycles. This signal is wired separately to each of the 32-bit channel connectors on the system board and ORed by the system logic. This signal is driven by a totem-pole driver that can sink 6 milliamps.

-MMC CMD: -Matched Memory Cycle Command: This output signal to the bus is generated for system microprocessor bus cycles only. It is used during a matched-memory cycle to define when the data on the bus is valid. The trailing edge of this signal indicates the end of the matched-memory cycle. As with -CMD, this signal indicates the time that the data is valid on the bus, and indicates when to latch the data from the bus or stop driving the data onto the bus. -MMC CMD is driven by a tri-state driver that can sink 24 milliamps.

Central Arbiter

The central arbitration control point gives intelligent subsystems on the channel the ability to share and control the system. It allows burst data transfers and prioritization of control between devices. This arbiter supports up to 16 arbitrating devices.

Arbitration Bus Priority Assignments

The following table shows the assignment of arbitration levels. The functions with the lowest arbitration level have the highest priority.

ARB Level	Primary Assignment
-2	Memory Refresh
-1	NMI
0	DMA Channel 0 (Programmable to any arbitration level)
1	DMA Channel 1
2	DMA Channel 2
3	DMA Channel 3
4	DMA Channel 4 (Programmable to any arbitration level)
5	DMA Channel 5
6	DMA Channel 6
7	DMA Channel 7
8 - E	Available
F	System Microprocessor

Figure 3-2. Arbitration Bus Priority Assignments

Note: Devices designed for arbitration level 0 or 1 should have limited bandwidth or short bursts so diskette overruns can be prevented or recovered by retry operations. The diskette drive controller, on arbitration level 2, can be held inactive by devices on levels 0 and 1, by a refresh operation, and by the previous controlling master. The diskette drive controller should not be held inactive for more than 12 microseconds to prevent overrun.

Nonmaskable interrupt (NMI) service is executed at a priority level higher than 0, called -1. Memory refresh is prioritized at -2, two levels higher than 0. Levels -1 and -2 are reached on the system board only, while the 'arbitrate/-grant' signal is in the arbitrate state.

When the central arbitration control point receives a level -1 request (NMI, a system-board internal signal), it activates -PREEMPT, waits for the end of transfer, and then places ARB/-GNT in the arbitrate state, which denies channel activity to arbitrating devices. The central arbitration control point gives the grant to the level -1 request, and holds ARB/-GNT in the arbitrate state until the operation is complete and the NMI is reset.

Central Arbiter Programming

The central arbitration control point provides access to programmable options through the Arbitration register, which is accessed at I/O address hex 0090. The bits are defined differently for read and write operations, as shown in the following tables.

Bit	Definition
7	Enable System Microprocessor Cycle
6	Arbitration Mask
5	Enable Extended Arbitration
4 - 0	Reserved

Figure 3-3. Arbitration Register (Hex 0090) — Write

Bit	Definition
7	Enable System Microprocessor Cycle
6	Arbitration Masked by NMI
5	Bus Time-out
4	Reserved
3 - 0	Value of Arbitration Bus During Previous Grant State

Figure 3-4. Arbitration Register (Hex 0090) — Read

Bit 7 Setting this bit to 1 enables system microprocessor cycles during arbitration cycles. This bit can be set to 0 if an arbitrating device requires total control of the channel bandwidth. This bit is set to 0 by a system reset.

Reading this bit as a 1 indicates system microprocessor cycles are enabled during arbitration.

Bit 6 Setting this bit to 1 causes the central arbitration control point to enter the arbitration state. The system microprocessor controls the channel until this bit is reset to 0. This bit is set to 0 by a system reset.

Reading this bit as a 1 indicates that an NMI has occurred and has masked arbitration.

Warning: This bit should be set to 1 only by diagnostic routines and system error-recovery routines.

Bit 5 Setting this bit to 1 enables extended arbitration. The minimum arbitration cycle is 300 nanoseconds; this bit extends that minimum cycle to 600 nanoseconds. This bit is set to 0 during a system reset.

Reading this bit as a 1 indicates that a bus time-out has occurred, and resets bit 6 in this register to 0.

Bit 4 This bit is reserved and should be 0.

Bits 3 - 0 These bits are undefined for a write operation and should be set to 0.

Reading these bits returns the arbitration level of the arbiter controlling the channel during the most recent grant state. This information allows the system microprocessor to determine the arbitration level of the device that caused a bus time-out.

Diskette Drive and Fixed Disk Connectors

The system board has a 2- by 56-pin connector that provides direct bus attachment for two diskette drives and one fixed disk through the fixed disk and diskette drive adapter.

For the diskette drives, this adapter passes control and data signals between the diskette drive controller on the system board and the drives. For the fixed disk drive, the adapter provides a path for the Micro Channel signals necessary for fixed disk operations. It also provides the power required for fixed disk and diskette drive operations.

When in the setup mode, the fixed disk drive is addressed as channel connector 4 through the Adapter Enable/Setup register. For more information about this register, see the POS information in the *Hardware Interface Technical Reference*. For more POS information about the fixed disk drive, refer to the technical reference for that drive.

Direct Bus Attachment Connector

The following figure shows the signal assignments and pin numbers for the 2- by 56-pin system board connector.

Side B			Side A		
Pin	I/O	Signal	Pin	I/O	Signal
1	O	-High Density Select	1	I	-2nd Drive Installed
2	O	+12 Vdc	2	O	+12 Vdc
3	O	+12 Vdc	3	O	+12 Vdc
4	O	+5 Vdc	4	I	CD CHRDY
5	I	-Index	5	O	M/-IO
6	O	-Motor Enable 1	6	N/A	Ground
7	O	-Drive Select 0	7	O	-S1
8	N/A	Ground	8	O	+5 Vdc
9	O	-Drive Select 1	9	O	-S0
10	O	-Motor Enable 0	10	N/A	Ground
11	O	-Direction In	11	N/A	Reserved
12	N/A	Ground	12	O	-TC
13	O	-Step	13	O	ARB/-GNT
14	O	-Write Data	14	N/A	Ground
15	O	-Write Enable	15	I/O	ARB 03
16	N/A	Frame Ground	16	I/O	ARB 02
17	I	-Track 0	17	I/O	ARB 01
18	I	-Write Protect	18	N/A	Frame Ground
19	I	-Read Data	19	N/A	Reserved
20	O	-Head 1 Select	20	I/O	ARB 00
21	I	-Diskette Change	21	I	-BURST
22	I	-IRQ 14	22	N/A	Ground
23	I	-CD DS 16	23	I	-PREEMPT
24	N/A	Ground	24	O	+5 Vdc
25	O	-SBHE	25	O	-ADL
26	I/O	D13	26	N/A	Ground
27	O	+12 Vdc	27	O	+12 Vdc
28	I/O	D11	28	O	A00
29	I/O	D10	29	O	A01
30	I/O	D07	30	N/A	Ground
31	I/O	D06	31	O	A02
32	N/A	Ground	32	O	+5 Vdc
33	I/O	D05	33	O	A03
34	I/O	D02	34	N/A	Ground
35	O	+12 Vdc	35	O	+12 Vdc
36	I/O	D00	36	O	A04
37	I/O	D15	37	O	A05
38	I/O	D14	38	N/A	Ground
39	I/O	D12	39	O	A06
40	N/A	Ground	40	O	+5 Vdc
41	I/O	D09	41	O	A07
42	I/O	D08	42	N/A	Ground
43	O	CHRESET	43	N/A	Reserved
44	O	+5 Vdc	44	N/A	Reserved
45	I/O	D04	45	O	A08
46	N/A	Key	46	N/A	Key

Figure 3-5 (Part 1 of 2). Direct Bus Attachment

Side B			Side A		
Pin	**I/O**	**Signal**	**Pin**	**I/O**	**Signal**
47	N/A	Key	47	N/A	Key
48	N/A	Ground	48	O	+5 Vdc
49	I/O	D03	49	O	A09
50	I/O	D01	50	N/A	Ground
51	I	-CD SFDBK	51	O	A10
52	N/A	Ground	52	O	+5 Vdc
53	O	-CMD	53	O	A11
54	O	A12	54	N/A	Ground
55	O	14.3 MHz Osc	55	O	A13
56	N/A	Ground	56	O	+5 Vdc
57	O	A14	57	O	-CD SETUP
58	O	A15	58	N/A	Ground

Figure 3-5 (Part 2 of 2). Direct Bus Attachment

Diskette Drive Connectors

The following figure shows the signal assignments and pin numbers for the 2- by 20-pin diskette drive connectors on the adapter.

Pin	I/O	Signal	Pin	I/O	Signal
1	I	-2nd Drive Installed	2	O	-High Density Select
3	N/A	Reserved	4	N/A	Reserved
5	N/A	Ground	6	N/A	Reserved
7	N/A	Signal Ground	8	I	-Index
9	N/A	Signal Ground	10	N/A	Reserved
11	N/A	Signal Ground	12	O	-Drive Select
13	N/A	Ground	14	N/A	Reserved
15	N/A	Signal Ground	16	O	-Motor Enable
17	N/A	Signal Ground	18	O	-Direction In
19	N/A	Signal Ground	20	O	-Step
21	N/A	Signal Ground	22	O	-Write Data
23	N/A	Signal Ground	24	O	-Write Enable
25	N/A	Signal Ground	26	I	-Track 0
27	N/A	Signal Ground	28	I	-Write Protect
29	N/A	Signal Ground	30	I	-Read Data
31	N/A	Signal Ground	32	O	-Head 1 Select
33	N/A	Signal Ground	34	I	-Diskette Change
35	N/A	Frame Ground	36	N/A	Frame Ground
37	N/A	Ground	38	O	+5 Vdc
39	N/A	Ground	40	O	+12 Vdc

Figure 3-6. Diskette Drive Connectors

Fixed Disk Drive Connector

The following figure shows the signal assignment and pin numbering for the fixed disk drive connector on the adapter. The fixed disk drive connector is a 2- by 36-pin connector. Side A of the connector is the top and Side B is the bottom.

Side B			Side A		
Pin	**I/O**	**Signal**	**Pin**	**I/O**	**Signal**
1	I	-CD SETUP	1	O	A15
2	N/A	A13	2	O	A14
3	N/A	Ground	3	N/A	Ground
4	N/A	A11	4	O	14.3 MHz Osc
5	N/A	A10	5	N/A	Ground
6	N/A	A09	6	O	A12
7	N/A	+5 Vdc	7	O	-CMD
8	N/A	A08	8	I	-CD SFDBK
9	N/A	A07	9	N/A	Ground
10	N/A	A06	10	I/O	D01
11	N/A	Ground	11	I/O	D03
12	N/A	A05	12	I/O	D04
13	N/A	A04	13	N/A	Ground
14	N/A	A03	14	O	CHRESET
15	N/A	+5 Vdc	15	I/O	D08
16	N/A	A02	16	I/O	D09
17	N/A	A01	17	N/A	Ground
18	N/A	A00	18	I/O	D12
19	N/A	+12 Vdc	19	I/O	D14
20	N/A	-ADL	20	I/O	D15
21	N/A	-PREEMPT	21	N/A	Ground
22	N/A	-BURST	22	I/O	D00
23	N/A	+5 Vdc	23	I/O	D02
24	N/A	ARB 00	24	I/O	D05
25	N/A	ARB 01	25	N/A	Ground
26	N/A	ARB 02	26	I/O	D06
27	N/A	+12 Vdc	27	I/O	D07
28	N/A	ARB 03	28	I/O	D10
29	N/A	ARB/-GNT	29	N/A	Ground
30	N/A	-TC	30	I/O	D11
31	N/A	+5 Vdc	31	I/O	D13
32	N/A	-S0	32	O	-SBHE
33	N/A	-S1	33	N/A	Ground
34	N/A	M/-IO	34	I	-CD DS 16
35	N/A	Ground	35	I	-IRQ 14
36	N/A	CD CHRDY	36	N/A	Ground

Figure 3-7. Fixed Disk Drive Connector

Memory

Model 70 systems use the following types of memory:

- Read-only memory (ROM)
- Random access memory (RAM)
- Real-time Clock and CMOS RAM.

Read-Only Memory Subsystem

The ROM subsystem consists of 128KB. At power-on, ROM is active in two address spaces: hex 000E0000 to 000FFFFF and hex FFFE0000 to FFFFFFFF. After POST (power-on self test) ensures the proper operation of system memory, the ROM code is copied to RAM. ROM is then disabled, and the RAM responds to the ROM addresses. This RAM is write protected.

CAUTION:
Although this RAM is write protected, writing to this space can cause unpredictable results on systems with cache.

ROM or RAM access at address space hex 000E0000 to 000FFFFF is controlled by the ROMEN bit in Memory Encoding Register 1 (hex 00E1). When enabled, ROM is not parity-checked and operates with a minimum of 200-nanoseconds in wait states.

For the Type 3 and Type 4 system boards, the address space hex 000E0000 to 000FFFFF is not cached if ROM is enabled, and is cached if ROM is disabled.

Warning: On systems with a cache, writing to the ROM address space with the ROM enable bit set to 0 (bit 1 address hex 00E1) might produce unpredictable results, including parity errors or problems with cache integrity.

Random Access Memory Subsystem

The RAM subsystem on the system board starts at address hex 00000000 of the address space. The RAM subsystem is 36 bits wide: 32 data bits and 4 parity bits. One parity bit is generated for each byte of data written. During a read operation, one parity bit is checked for each byte of data read by the device controlling the bus.

The Model 70 enables and disables memory in 1MB blocks. Each 1MB block must start on a 1MB boundary. Because 128KB of I/O ROM, and 128KB of video memory are mapped within the first 1MB address space, an overflow is created from the first 1MB of RAM installed in the system. The first 1MB of RAM can be split at either 512KB or 640KB; the memory from the split to the start of the RAM that contains the ROM code is called the *split memory block*. This split memory block can be disabled, or it can be remapped to the first address following the last 1MB of memory. Split memory block remapping and disabling are controlled by the memory encoding registers.

Notes:

1. Additional memory can be added in either of the 32-bit Micro Channel connectors. However, the total amount of memory installed should not exceed the 16MB addressing limit of the DMA controller.
2. For the Type 3 and Type 4 system boards, system memory must be 32-bits wide (nonsystem memory can be any width).

System and Nonsystem Memory

Two basic types of memory can be assigned addresses within the memory address space: system memory and nonsystem memory.

System memory is memory that is managed and allocated by the primary operating system. It remains assigned to and fixed in the 4GB (GB = 1,073,741,824 bytes) physical address space, and its contents can be accessed or modified only by an independent master (bus master, system microprocessor, or DMA controller).

Nonsystem memory is memory that is not managed or allocated by the primary operating system. It is made up of memory-mapped I/O devices, memory on an adapter that can be directly modified by the adapter, or memory that can be relocated within the address space, such as bank switched and EMS (expanded memory specifications). Nonsystem memory should not be mapped into microprocessor's cacheable address space.

Memory Caching

The following figure is the memory map for the first 32MB of address space on Type 3 and Type 4 system boards and shows which addresses can be used with the cache. On these system boards, the address space from 32MB to the end of the second GB is not usable. The third and fourth GB are not mapped into the cache, but can be used, especially for nonsystem memory.

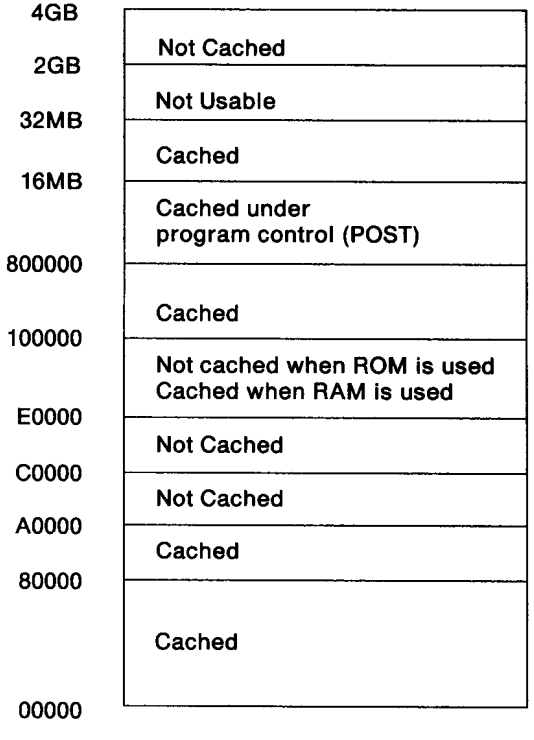

Figure 3-8. Mapping of the First 32MB Segment

Within the first 16MB of address space, all system memory above 1MB must be one contiguous sum starting at the 1MB boundary. If nonsystem memory is present, it should be assigned addresses starting at 16MB and counting down. Do not assign addresses below 8MB to nonsystem memory.

If nonsystem memory exists between 8MB and 16MB, caching for that 8MB block must be disabled even if system memory is also located there. Setup routines must be aware of the existence and location of nonsystem memory so that POST can properly control the caching of the second 8MB.

In the 16MB to 4GB address space, system memory can be contiguously placed from 16MB up to 32MB and can be cached. If nonsystem memory is located within the 16MB to 4GB address space, it should be assigned addresses starting at 4GB and counting down, allowing space for system ROM.

Error Recovery

If POST detects a memory error in the first 512KB of memory, the first physical 1MB block of memory is deactivated. The addresses assigned to the deactivated block are reassigned to the second physical block of system board memory (the first 1MB of system memory must reside in connector 1 or 2). If 1MB of valid memory cannot be allocated from connector 1 or 2, the system cannot recover from the error. The first 1MB of memory address space cannot be assigned to memory on the channel.

POST does not deactivate a memory block if an error is detected in the second 512KB of that block. If an error is detected in that area of memory, the 1MB block containing the error can be deactivated and have its addresses reassigned by running the customer-level memory diagnostics program on the Reference Diskette supplied with the system. Once a block of memory is deactivated, it is ignored by POST on subsequent power-ons.

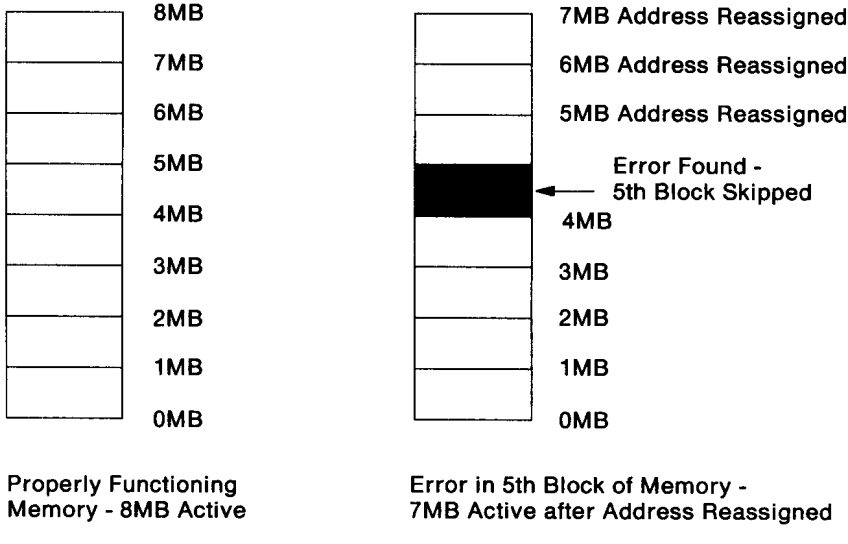

Figure 3-9. Memory Error Address Reassignment

Memory Subsystem Control

These read/write registers define and control the ROM and RAM subsystems.

Memory Encoding Register 1 (Hex 00E1)

This register determines how the first 1MB of memory is addressed and is used with Memory Encoding Register 2 to determine the amount of system board memory enabled.

Bit	Function
7	-Card 2 EN2
6	-Card 2 EN1
5	-Card 1 EN2
4	-Card 1 EN1
3	-ENSPLIT
2	-640
1	ROMEN
0	-ENPLRPCH

Figure 3-10. Memory Encoding Register 1 (Hex 00E1)

Bits 7, 6 These bits define system board memory in connector 2. When they are set to 0, bit 6 enables the first 1MB block and bit 7 enables the second 1MB block.

Bits 5, 4 These bits define system board memory in connector 1. When they are set to 0, bit 4 enables the first 1MB block and bit 5 enables the second 1MB block.

Bit 3 This bit determines if the split-memory block is assigned addresses or is disabled. The top 128KB of the first 1MB is always mapped into the ROM address space and the code in ROM is copied into this space.

When this bit is set to 0, the split-memory block is enabled. The split-memory block size is dependent on the value of the 640 bit. Its address is determined in Memory Encoding Register 2. When this bit is set to 1, the split-memory block is disabled.

Note: If the total system memory is equal to or greater than 16MB, the split-memory block cannot be used.

Bit 2 This bit determines where the first active 1MB of memory is split.

Note: Because the memory below 640KB is always cached, this bit is always set to 0 for Type 3 and Type 4 system boards.

When this bit is set to 0, the system maps 640KB of the first 1MB to address hex 00000000 to 0009FFFF. The split-memory block, 256KB, is mapped to the address specified in Memory Encoding Register 2.

When this bit is set to 1, the system maps 512KB of the first 1MB to address hex 00000000 to 0007FFFF. The split-memory block, 384KB, is mapped to the address specified in Memory Encoding Register 2. The addresses hex 00080000 to 0009FFFF are unassigned.

Bit 1 This bit determines how addresses hex 000E0000 to 000FFFFF are assigned.

When this bit is set to 1, ROM is enabled and the read-access addresses are assigned to ROM; the write-access addresses are assigned to RAM. When this bit is set to 0, ROM is disabled and read addresses are assigned to RAM; the write addresses are disabled while ROM is disabled.

Note: When this bit is set to 1, system performance will be substantially slower because of 16-bit accesses to ROM and a longer cycle.

Bit 0 When set to 0, this bit enables parity checking of system board memory. For compatibility with other systems, enabling and disabling of parity checking should be done through System Control Port B at address hex 0061 (see "System Control Port B (Hex 0061)" on page 3-43).

Memory Encoding Register 2 (Hex 00E0)

This register is used with Memory Encoding Register 1 to determine the amount of system board memory that is enabled. It also contains the address for the split-memory block.

Bit	Function
7	-Card 4 EN2
6	-Card 4 EN1
5	-Card 3 EN2
4	-Card 3 EN1
3	SPA23
2	SPA22
1	SPA21
0	SPA20

Figure 3-11. Memory Encoding Register 2 (Hex 00E0)

Bits 7, 6 These bits are used on the Type 3 system board only. They define the system board memory in connector 4. When set to 0, bit 6 enables the first 1MB block and bit 7 enables the second 1MB block. For Type 1 and Type 2 system boards, these bits must be set to 1.

Bits 5, 4 These bits define the system board memory in connector 3. When they are set to 0, bit 4 enables the first 1MB block and bit 5 enables the second 1MB block.

Bits 3 - 0 These bits define the starting address of the split-memory block. When split memory is enabled, these bits determine its starting address. The starting location can be at any 1MB boundary from 1MB to 15MB.

Memory Encoding Register 3 (Hex 00E2) – Types 3 and 4

This read/write register is used by the Type 3 and Type 4 system boards only and provides control of the cache memory.

Bit	Function
7	Reserved
6	-Preempt Enable
5	-Cache Flush
4	Lock
3	Reserved
2	-Cache 2nd 8MB
1	Reserved
0	-Enable Cache

Figure 3-12. Memory Encoding Register 3 (Hex 00E2) – Types 3 and 4

Bit 7 This bit is reserved.

Bit 6 This bit controls the preempt support for the system microprocessor. When this bit is set to 1, preempting is disabled. When this bit is set to 0, system logic activates the '-preempt' signal when the system microprocessor accesses a memory location not satisfied in the cache (cache miss).

Bit 5 See the description of bit 0.

Bit 4 On the Type 3 system board, this bit controls if locked-access operations from the system microprocessor can or cannot be cache hits.

If this bit is set to 0, all locked-access operations are treated as cache misses. If this bit is set to 1, locked-access operations can be cache hits.

This bit is not used on the Type 4 system board.

Bit 3 This bit is reserved.

Bit 2 This bit determines if the second 8MB of memory is cached or not. When the bit is set to 0, the second 8MB is cached.

Note: Before disabling the caching of the second 8MB, disable and flush the cache.

Bit 1 This bit is reserved.

Bit 0 This bit and bit 5 work together to control the state of the cache. These bits must always be modified in the same I/O instruction.

For Type 3, these bits must always be written in the sequence shown below and always be opposite polarities. The following describes their control.

1. Bit 5=0 and Bit 0=1 for the disabled/flushed state.
2. Bit 5=1 and Bit 0=0 for the enabled state.

For the Type 4 system board, these bits work together to control the state of the cache; either disabled, disabled and flushed, or enabled. These bits must always be written in the sequence shown below for the Type 4 system board.

1. Bit 5=0 and Bit 0=1 for the disabled/flushed state.
2. Bit 5=1 and Bit 0=1 for the disabled state.
3. Bit 5=1 and Bit 0=0 for the enabled state.

Notes:

1. Refer to the 80486 specification microprocessor section for information on CR0, which must also be set to enable the 80486 internal 8KB cache.
2. The cache must be disabled and flushed before enabling ROM or disabling the caching of the second 8MB.

System Memory Maps

Memory is mapped by the Memory Encoding registers. The mapping results in either 512KB or 640KB of system board RAM starting at address hex 00000000 (system boards Type 3 and Type 4 do not support the split at 512KB). A 256-byte and 1KB portion of this RAM are reserved as BIOS data areas. See the *IBM Personal System/2 and Personal Computer BIOS Interface Technical Reference* for details.

In the following tables, the variable *X* represents the number of 1MB blocks of system board memory starting at or above the hex 00100000 boundary. The variable *Y* represents the number of 1MB blocks of memory installed in the channel starting at or above the hex 00100000 boundary (*Y* = 0 to 15).

The following table shows the memory mapping when:

Enable Split bit = 1
640 bit = 1
ROM enable bit = 1.

Hex Range	Function
00000000 to 0007FFFF	512KB System Board RAM
00080000 to 0009FFFF	Not Used
000A0000 to 000BFFFF	128KB Video RAM
000C0000 to 000DFFFF	Channel ROM
000E0000 to 000FFFFF	128KB System Board ROM
00100000 to (00100000 + *X*MB)	*X*MB System Board RAM
(00100000 + *X*MB) to (00100000 + *X*MB + *Y*MB)	*Y*MB Channel RAM
(00100000 + *X*MB + *Y*MB) to FFFDFFFF	Not Used
FFFE0000 to FFFFFFFF	128KB System Board ROM (Same as 000E0000 to 000FFFFF)

Figure 3-13. System Memory Map 1

The following table shows the memory mapping when:

Enable Split bit = 1
640 bit = 0
ROM enable bit = 1.

Hex Range	Function
00000000 to 0009FFFF	640KB System Board RAM
000A0000 to 000BFFFF	128KB Video RAM
000C0000 to 000DFFFF	Channel ROM
000E0000 to 000FFFFF	128KB System Board ROM
00100000 to (00100000 + XMB)	XMB System Board RAM
(00100000 + XMB) to (00100000 + XMB + YMB)	YMB Channel RAM
(00100000 + XMB + YMB) to FFFDFFFF	Not Used
FFFE0000 to FFFFFFFF	128KB System Board ROM (Same as 000E0000 to 000FFFFF)

Figure 3-14. System Memory Map 2

The following table shows the memory mapping when:

Enable Split bit = 0
640 bit = 1
ROM enable bit = 1
Split address bits = 1 + X + Y (Total range = 1 to 15).

Hex Range	Function
00000000 to 0007FFFF	512KB System Board RAM
00080000 to 0009FFFF	Not Used
000A0000 to 000BFFFF	128KB Video RAM
000C0000 to 000DFFFF	Channel ROM
000E0000 to 000FFFFF	128KB System Board ROM
00100000 to (00100000 + XMB)	XMB System Board RAM
(00100000 + XMB) to (00100000 + XMB + YMB)	YMB Channel RAM
(00100000 + XMB + YMB) to (00100000 + XMB + YMB +384KB)	384KB System Board RAM
(00100000 + XMB + YMB + 384KB) to FFFDFFFF	Not Used
FFFE0000 to FFFFFFFF	128KB System Board ROM (Same as 000E0000 to 000FFFFF)

Figure 3-15. System Memory Map 3

The following table shows the memory mapping when:

Enable Split bit = 0
640 bit = 0
ROM enable bit = 1
Split address bits = 1 + *X* + *Y* (Total range = 1 to 15).

Hex Range	Function
00000000 to 0009FFFF	640KB System Board RAM
000A0000 to 000BFFFF	128KB Video RAM
000C0000 to 000DFFFF	Channel ROM
000E0000 to 000FFFFF	128KB System Board ROM
00100000 to (00100000 + *X*MB)	*X*MB System Board RAM
(00100000 + *X*MB) to (00100000 + *X*MB + *Y*MB)	*Y*MB Channel RAM
(00100000 + *X*MB + *Y*MB) to (00100000 + *X*MB + *Y*MB + 256KB)	256KB System Board RAM
(00100000 + *X*MB + *Y*MB + 256KB) to FFFDFFFF	Not Used
FFFE0000 to FFFFFFFF	128KB System Board ROM (Same as 000E0000 to 000FFFFF)

Figure 3-16. System Memory Map 4

The following table shows the memory mapping when:

Enable Split bit = 1
640 bit = 1
ROM enable bit = 0.

Hex Range	Function
00000000 to 0007FFFF	512KB System Board RAM
00008000 to 0009FFFF	Not Used
000A0000 to 000BFFFF	128KB Video RAM
000C0000 to 000DFFFF	Channel ROM
000E0000 to 000FFFFF	128KB System Board ROM Mapped to RAM
00100000 to (00100000 + *X*MB)	*X*MB System Board RAM
(00100000 + *X*MB) to (00100000 + *X*MB + *Y*MB)	*Y*MB Channel RAM
(00100000 + *X*MB + *Y*MB) to FFFDFFFF	Not Used
FFFE0000 to FFFFFFFF	128KB System Board ROM

Figure 3-17. System Memory Map 5

The following table shows the memory mapping when:

Enable Split bit = 1
640 bit = 0
ROM enable bit = 0.

Hex Range	Function
00000000 to 0009FFFF	640KB System Board RAM
000A0000 to 000BFFFF	128KB Video RAM
000C0000 to 000DFFFF	Channel ROM
000E0000 to 000FFFFF	128KB System Board ROM Mapped to RAM
00100000 to (00100000 + XMB)	XMB System Board RAM
(00100000 + XMB) to (00100000 + XMB + YMB)	YMB Channel RAM
(00100000 + XMB + YMB) to FFFDFFFF	Not Used
FFFE0000 to FFFFFFFF	128KB System Board ROM

Figure 3-18. System Memory Map 6

The following table shows the memory mapping when:

Enable Split bit = 0
640 bit = 1
ROM enable bit = 0
Split address bits = 1 + *X* + *Y* (Total range = 1 to 15).

Hex Range	Function
00000000 to 0007FFFF	512KB System Board RAM
00080000 to 0009FFFF	Not Used
000A0000 to 000BFFFF	128KB Video RAM
000C0000 to 000DFFFF	Channel ROM
000E0000 to 000FFFFF	128KB System Board ROM Mapped to RAM
00100000 to (00100000 + XMB)	XMB System Board RAM
(00100000 + XMB) to (00100000 + XMB + YMB)	YMB Channel RAM
(00100000 + XMB + YMB) to (00100000 + XMB + YMB + 384KB)	384KB of First 1MB at Split Address
(00100000 + XMB + YMB + 384KB) to FFFDFFFF	Not Used
FFFE0000 to FFFFFFFF	128KB System Board ROM

Figure 3-19. System Memory Map 7

The following table shows the memory mapping when:

Enable Split bit = 0
640 bit = 0
ROM enable bit = 0
Split address bits = 1 + *X* + *Y* (Total range = 1 to 15).

Hex Range	Function
00000000 to 0009FFFF	640KB System Board RAM
000A0000 to 000BFFFF	128KB Video RAM
000C0000 to 000DFFFF	Channel ROM
000E0000 to 000FFFFF	128K System Board ROM Mapped to RAM
00100000 to (00100000 + *X*MB)	*X*MB System Board RAM
(00100000 + *X*MB) to (00100000 + *X*MB + *Y*MB)	*Y*MB Channel RAM
(00100000 + *X*MB + *Y*MB) to (00100000 + *X*MB + *Y*MB + 256KB-1)	256KB of First 1MB at Split Address
(00100000 + *X*MB + *Y*MB + 256KB) to FFFDFFFF	Not Used
FFFE0000 to FFFFFFFF	128KB System Board ROM (Same as 000E0000 to 000FFFFF)

Figure 3-20. System Memory Map 8

System Board Memory Connectors

The Type 1 and Type 2 system boards have three 72-pin memory connectors that support the 1MB and 2MB memory cards. The numbering of the connectors depends on the location. If the memory connectors are under the diskette drives, the connectors are numbered from left to right. If the connectors are under the fixed disk drive, the connectors are numbered from right to left.

The Type 3 and Type 4 system boards have four 72-pin memory connectors and only support the 2MB, 80-nanosecond memory card. The four connectors are numbered from the left as viewed from the front of the system.

The following figure shows the pin assignments for the 1- by 72-pin memory connectors. Refer to "Memory Presence Detect" on page 2-14 for decoding of the presence detect signal.

Pin	I/O	Signal	Pin	I/O	Signal
1	N/A	Ground	37	I/O	Parity Data 1
2	I/O	Data 0	38	I/O	Parity Data 3
3	I/O	Data 16	39	N/A	Ground
4	I/O	Data 1	40	O	Column Address Strobe 0
5	I/O	Data 17	41	O	Column Address Strobe 2
6	I/O	Data 2	42	O	Column Address Strobe 3
7	I/O	Data 18	43	O	Column Address Strobe 1
8	I/O	Data 3	44	O	Row Address Strobe 0
9	I/O	Data 19	45	O	Row Address Strobe 1
10	O	+5 Vdc	46	O	Block Select 1
11	O	-Column Address Strobe P	47	O	Write Enable
12	O	Address 0	48	N/A	Reserved
13	O	Address 1	49	I/O	Data 8
14	O	Address 2	50	I/O	Data 24
15	O	Address 3	51	I/O	Data 9
16	O	Address 4	52	I/O	Data 25
17	O	Address 5	53	I/O	Data 10
18	O	Address 6	54	I/O	Data 26
19	N/A	Reserved	55	I/O	Data 11
20	I/O	Data 4	56	I/O	Data 27
21	I/O	Data 20	57	I/O	Data 12
22	I/O	Data 5	58	I/O	Data 28
23	I/O	Data 21	59	O	+5 Vdc
24	I/O	Data 6	60	I/O	Data 29
25	I/O	Data 22	61	I/O	Data 13
26	I/O	Data 7	62	I/O	Data 30
27	I/O	Data 23	63	I/O	Data 14
28	O	Address 7	64	I/O	Data 31
29	O	Block Select 0	65	I/O	Data 15
30	O	+5 Vdc	66	O	Block Select 2
31	O	Address 8	67	I	Presence Detect 0
32	N/A	Reserved	68	I	Presence Detect 1
33	O	Row Address Strobe 3	69	I	Presence Detect 2
34	O	Row Address Strobe 2	70	I	Presence Detect 3
35	I/O	Parity Data 2	71	O	Block Select 3
36	I/O	Parity Data 0	72	N/A	Ground

Figure 3-21. System Board Memory Connector

Real-Time Clock/Complementary Metal-Oxide Semiconductor RAM

The real-time clock/complementary metal-oxide semiconductor RAM (RT/CMOS) chip contains the real-time clock and 64 bytes of CMOS RAM. The internal clock circuitry uses 14 bytes of this memory, and the rest is allocated to configuration and system status information.

In addition to the 64 bytes of CMOS RAM, a 2KB CMOS RAM extension is provided for configuration and other system information.

A battery maintains voltage to the RT/CMOS RAM and 2KB CMOS RAM extension when the power supply is not in operation.

The system cover can be locked to prevent battery removal and loss of password and configuration information.

The following table shows the RT/CMOS RAM bytes and their addresses.

Address (Hex)	RT/CMOS RAM Bytes
000 - 00D	Real-Time Clock Bytes
00E	Diagnostic Status Byte
00F	Shutdown Status Byte
010	Diskette Drive Type Byte
011	First Fixed Disk Drive Type Byte
012	Second Fixed Disk Drive Type Byte
013	Reserved
014	Equipment Byte
015 - 016	Low and High Base Memory Bytes
017 - 018	Low and High Expansion Memory Bytes
019 - 031	Reserved
032 - 033	Configuration CRC Bytes
034	Reserved
035 - 036	Low and High Useable Memory Bytes
037	Date Century Byte
038 - 03F	Reserved

Figure 3-22. RT/CMOS RAM Address Map

RT/CMOS Address Register and NMI Mask (Hex 0070)

This read/write register is used in conjunction with the port at hex 0071 to read and write the RT/CMOS RAM bytes.

Bit	Function
7	NMI Mask
6	Reserved
5 - 0	RT/CMOS RAM Address

Figure 3-23. RT/CMOS Address Register and NMI Mask (Hex 0070)

Warning: The operation following a write to hex 0070 must access port hex 0071; otherwise intermittent malfunctions and unreliable operation of the RT/CMOS RAM can occur.

Bit 7 When this bit is set to 1, the NMI is masked off (the NMI is disabled). This bit is set to 1 by a power-on reset. This is a write-only bit.

Bit 6 This bit is reserved.

Bits 5 - 0 These bits are used to select RT/CMOS RAM addresses.

RT/CMOS Data Register (Hex 0071)

This port is used in conjunction with the address register at hex 0070 to read and write the RT/CMOS RAM bytes.

Bit	Function
7 - 0	RT/CMOS Data

Figure 3-24. RT/CMOS Data Register (Hex 0071)

RT/CMOS RAM I/O Operations

During I/O operations to the RT/CMOS RAM addresses, interrupts should be masked to prevent other interrupt routines from changing the CMOS Address register before data is read or written. After I/O operations, the RT/CMOS and NMI Mask register (hex 0070) should be left pointing to Status Register D (hex 00D).

Warning: The operation following a write to hex 0070 must access hex 0071; otherwise intermittent malfunctions and unreliable operation of the RT/CMOS RAM can occur.

The following steps are required to perform I/O operations to the RT/CMOS RAM addresses:

1. Write the RT/CMOS RAM address to the RT/CMOS and NMI Mask register (hex 0070).
2. Write the data to address hex 0071.

Reading RT/CMOS RAM requires the following steps:

1. Write the RT/CMOS RAM address to the RT/CMOS and NMI Mask register (hex 0070).
2. Read the data from address hex 0071.

Real-Time Clock Bytes (Hex 000 - 00D)

Bit definitions and addresses for the real-time clock bytes are shown in the following table.

Address (Hex)	Function	Byte Number
000	Seconds	0
001	Second Alarm	1
002	Minutes	2
003	Minute Alarm	3
004	Hours	4
005	Hour Alarm	5
006	Day of Week	6
007	Date of Month	7
008	Month	8
009	Year	9
00A	Status Register A	10
00B	Status Register B	11
00C	Status Register C	12
00D	Status Register D	13

Figure 3-25. Real-Time Clock Bytes

Note: The Setup program initializes status registers A, B, C, and D when the time and date are set. Interrupt hex 1A is the BIOS interface to read and set the time and date. It initializes the register the same way as the Setup program.

Status Register A (Hex 00A)

Bit	Function
7	Update in Progress
6 - 4	22-Stage Divider
3 - 0	Rate Selection Bits

Figure 3-26. Status Register A

Bit 7 When set to 1, this bit indicates the time-update cycle is in progress. When set to 0, it indicates the current date and time can be read.

Bits 6 - 4 These three divider-selection bits identify which time-base frequency is being used. The system initializes these bits to binary 010, which selects a 32.768 kHz time base. This is the only value supported by the system for proper time-keeping.

Bits 3 - 0 These bits allow the selection of a divider output frequency. The system initializes the rate selection bits to a binary 0110, which selects a 1.024 kHz square-wave output frequency and a 976.562-microsecond periodic interrupt rate.

Status Register B (Hex 00B)

Bit	Function
7	Set
6	Periodic Interrupt Enable
5	Alarm Interrupt Enable
4	Update-Ended Interrupt Enable
3	Square Wave Enable
2	Date Mode
1	24-Hour Mode
0	Daylight Savings Enable

Figure 3-27. Status Register B

Bit 7 When set to 0, this bit updates the cycle, normally by advancing the counts at a rate of one per second. When set to 1, this bit immediately ends any update cycle in progress, and the program can initialize the 14 time bytes without any further updates occurring until this bit is set to 0.

Bit 6 This bit is a read/write bit that allows an interrupt to occur at a rate specified by the rate and divider bits in Status Register A. When set to 1, this bit enables the interrupt. The system initializes this bit to 0.

Bit 5 When set to 1, this bit enables the alarm interrupt. The system initializes this bit to 0.

Bit 4 When set to 1, this bit enables the update-ended interrupt. The system initializes this bit to 0.

Bit 3 When set to 1, this bit enables the square-wave frequency as set by the rate-selection bits in Status Register A. The system initializes this bit to 0.

Bit 2 This bit indicates if the time-and-date calendar updates use binary or binary-coded-decimal (BCD) formats. When set to 1, this bit indicates a binary format. The system initializes this bit to 0.

Bit 1 This bit establishes if the hours byte is in the 24-hour or 12-hour mode. When set to 1, this bit indicates the 24-hour mode. The system initializes this bit to 1.

Bit 0 When set to 1, this bit enables the daylight savings time mode. When set to 0, it disables the mode, and the clock reverts to standard time. The system initializes this bit to 0.

Status Register C (Hex 00C)

Bit	Function
7	Interrupt Request Flag
6	Periodic Interrupt Flag
5	Alarm Interrupt Flag
4	Update-Ended Interrupt Flag
3 - 0	Reserved

Figure 3-28. Status Register C

Note: Interrupts are enabled by bits 6, 5, and 4 in Status Register B.

Bit 7 This bit is used in conjunction with bits 6, 5, and 4. When set to 1, this bit indicates that an interrupt has occurred; bits 6, 5, and 4 indicate the type of interrupt.

Bit 6 When set to 1, this bit indicates that a periodic interrupt occurred.

Bit 5 When set to 1, this bit indicates that an alarm interrupt occurred.

Bit 4 When set to 1, this bit indicates that an update-ended interrupt occurred.

Bits 3 - 0 These bits are reserved.

Status Register D (Hex 00D)

Bit	Function
7	Valid RAM
6 - 0	Reserved

Figure 3-29. Status Register D

Bit 7 This read-only bit monitors the power-sense pin. A low state of this pin indicates a loss of power to the real-time clock (dead battery). When set to 1, this bit indicates that the real-time clock has power. When set to 0, it indicates that the real-time clock has lost power.

Bits 6 - 0 These bits are reserved.

CMOS RAM Configuration

The following figure shows the bit definitions for the CMOS RAM configuration bytes.

Diagnostic Status Byte (Hex 00E)

Bit	Function
7	Real-Time Clock Chip Power
6	Configuration Record and Checksum Status
5	Incorrect Configuration
4	Memory Size Miscompare
3	Fixed Disk Controller/Drive C Initialization Status
2	Time Status Indicator
1	Adapter Configuration Miscompare
0	Adapter ID Time-Out

Figure 3-30. Diagnostic Status Byte

Bit 7 When set to 1, this bit indicates the real-time clock chip lost power.

Bit 6 When this bit is set to 1, the checksum is incorrect.

Bit 5 This is a check, at power-on time, of the Equipment byte. When set to 1, the configuration information is incorrect. Power-on checks require that at least one diskette drive be installed (bit 0 of the Equipment byte, hex 014, is set to 1).

Bit 4 When set to 1, this bit indicates the power-on check determined that the memory size is not the same as in the configuration record.

Bit 3 When set to 1, this bit indicates that the controller or drive C failed initialization, which prevents the system from attempting a power-on reset.

Bit 2 When set to 0, this bit indicates the time is valid. When set to 1, this bit indicates the time is invalid.

Bit 1 This bit indicates if the installed adapters match the configuration information. When this bit is set to 1, the adapters do not match the configuration information.

Bit 0 When set to 1, this bit indicates a time-out occurred while an adapter ID was being read.

Shutdown Status Byte (Hex 00F): This byte is defined by the power-on diagnostic programs.

Diskette Drive Type Byte (Hex 010): This byte indicates the type of diskette drive installed.

Bit	Function
7 - 4	First Diskette Drive Type
3 - 0	Second Diskette Drive Type

Figure 3-31. Diskette Drive Type Byte

Bits 7 - 4 These bits indicate the first diskette drive type, as shown in the following table.

Bits 7 6 5 4	Function
0 0 0 0	No Drive Present
0 0 0 1	Double-sided Diskette Drive (48 tracks per inch, 360KB)
0 0 1 1	High-capacity Diskette Drive (720KB)
0 1 0 0	High-density Diskette Drive (1.44MB)

All combinations that are not shown are reserved.

Figure 3-32. Diskette Drive Type Byte (Bits 7 - 4)

Bits 3 - 0 These bits indicate the second diskette drive type, as shown in the following table.

Bits 3 2 1 0	Function
0 0 0 0	No Drive Present
0 0 0 1	Double-sided Diskette Drive (48 tracks per inch, 360KB)
0 0 1 1	High-capacity Diskette Drive (720KB)
0 1 0 0	High-density Diskette Drive (1.44MB)

All combinations that are not shown are reserved.

Figure 3-33. Diskette Drive Type Byte (Bits 3 - 0)

First Fixed Disk Drive Type Byte (Hex 011): This byte defines the type of the first fixed disk drive (drive C). Hex 00 indicates that a fixed disk drive is *not* installed.

Second Fixed Disk Drive Type Byte (Hex 012): This byte defines the type of the second fixed disk drive (drive D). Hex 00 indicates that a fixed disk drive is *not* installed.

Note: For more information about fixed disk drive types, refer to the *IBM Personal System/2 and Personal Computer BIOS Interface Technical Reference*.

Reserved Byte (Hex 013): This byte is reserved.

Equipment Byte (Hex 014): The equipment byte, for the power-on diagnostic tests, defines the basic equipment in the system.

Bit	Function
7, 6	Number of Diskette Drives
5, 4	Display Operating Mode
3, 2	Reserved
1	Math Coprocessor Presence
0	Diskette Drive Presence

Figure 3-34. Equipment Byte

Bits 7, 6 These bits indicate the number of diskette drives installed, as shown in the following table.

Bits 7 6	Number of Diskette Drives
0 0	One Drive
0 1	Two Drives
1 0	Reserved
1 1	Reserved

Figure 3-35. Equipment Byte (Bits 7, 6)

Bits 5, 4 These bits indicate the operating mode of the display attached to the video port, as shown in the following table.

Bits 5 4	Display Operating Mode
0 0	Reserved
0 1	40-Column Mode
1 0	80-Column Mode
1 1	Monochrome Mode

Figure 3-36. Equipment Byte (Bits 5, 4)

Bits 3, 2 These bits are reserved.

Bit 1 When set to 1, this bit indicates that a math coprocessor is installed.

Bit 0 When set to 1, this bit indicates that a diskette drive is installed.

Low and High Base Memory Bytes (Hex 015 and 016): These bytes define the amount of memory below the 640KB address space.

The value from these bytes represents the number of 1KB blocks of base memory. For example, hex 0280 is equal to 640KB. The low byte is hex 15; the high byte is hex 16.

Low and High Expansion Memory Bytes (Hex 017 and 018): These bytes define the amount of memory above the 1MB address space.

The value from these bytes represents the number of 1KB blocks of expansion memory. For example, hex 0800 is equal to 2048KB. The low byte is hex 17; the high byte is hex 18.

Reserved Bytes (Hex 019 through 031): These bytes are reserved.

Configuration CRC Bytes (Hex 032 and 033): These bytes contain the cyclic-redundancy-check (CRC) data for bytes hex 010 through hex 031 of the 64-byte CMOS RAM. The low byte is hex 33; the high byte is hex 32.

Reserved Byte (Hex 034): This byte is reserved.

Low and High Useable Memory Bytes (Hex 035 and 036): These bytes define the total amount of useable memory above the 1MB address space.

The hexadecimal values in these bytes represent the number of 1KB blocks of useable memory. For example, hex 0800 is equal to 2048KB. The low byte is hex 35; the high byte is hex 36.

Date Century Byte (Hex 037): Bits 7 through 0 of this byte contain the BCD value for the century. Refer to the *IBM Personal System/2 and Personal Computer BIOS Interface Technical Reference* for information about reading and setting this byte.

Reserved Bytes (Hex 038 through 03F): These bytes are reserved.

Miscellaneous System Functions

Nonmaskable Interrupt

The nonmaskable interrupt (NMI) signals the system microprocessor that a parity error, a channel check, a system channel time-out, or a system Watchdog time-out has occurred. The NMI stops all arbitration on the bus until bit 6 of the Arbitration register (I/O address hex 0090) is set to 0. This can result in lost data or an overrun error on some I/O devices. The NMI masks all other interrupts and the IRET instruction restores the interrupt flag to the state it was in prior to the interrupt. A system reset causes a reset of the NMI.

Nonmaskable interrupt requests caused by system board parity checks or channel checks are subject to mask control by the NMI mask bit in the RT/CMOS Address register. The Watchdog Timer and system channel time-out are not masked by this bit. (See "RT/CMOS Address Register and NMI Mask (Hex 0070)" on page 3-32). The power-on default of the NMI mask is 1 (NMI disabled). Prior to enabling the NMI after a power-on reset, the parity check and channel check state are initialized by the POST.

Warning: The operation following a write to hex 0070 must access port hex 0071; otherwise intermittent malfunctions and unreliable operation of the RT/CMOS RAM can occur.

System Control Port B (Hex 0061)

Bit definitions for the read and write functions of this port are shown in the following tables.

Bit	Function
7	Reset Timer 0 Output Latch (IRQ0)
6 - 4	Reserved
3	Enable Channel Check
2	Enable Parity Check
1	Speaker Data Enable
0	Timer 2 Gate to Speaker

Figure 3-37. System Control Port B (Write)

Bit	Function
7	Parity Check
6	Channel Check
5	Timer 2 Output
4	Toggles with Each Refresh Request
3	Enable Channel Check
2	Enable Parity Check
1	Speaker Data Enable
0	Timer 2 Gate to Speaker

Figure 3-38. System Control Port B (Read)

Bit 7 Setting this bit to 1 resets IRQ0. Reading this bit as a 1 indicates a parity check has occurred.

Bit 6 Reading this bit as a 1 indicates a channel check has occurred.

Bit 5 This bit indicates the condition of the timer/counter 2 'output' signal.

Bit 4 This bit toggles for each refresh request.

Bit 3 Setting this bit to 0 enables channel check. Setting this bit is set to 1 during a power-on reset. Setting this bit to 1 disables channel check and clears the channel check latch.

Bit 2 Setting this bit to 0 enables parity check. This bit is set to 1 during a power-on reset. To clear a parity error, set this bit to 1 and then to 0.

Bit 1 Setting this bit to 1 enables speaker data.

Bit 0 Setting this bit to 1 enables the timer 2 gate.

System Control Port A (Hex 0092)

Bit	Function
7, 6	Fixed-Disk Activity Light
5	Reserved
4	Watchdog Timer Status
3	Security Lock Latch
2	Reserved
1	Alternate Gate A20
0	Alternate Hot Reset

Figure 3-39. System Control Port A

Bits 7, 6 These bits control the fixed-disk activity light. Setting either bit to 1 turns the fixed-disk activity light on. Setting both bits to 0 turns the light off. The power-on reset condition of each bit is 0.

Bit 5 This bit is reserved.

Bit 4 This read-only bit indicates the Watchdog Timer status. When this bit is set to 1, a Watchdog time-out has occurred. The Hardware Interface Technical Reference manuals contain more information about the Watchdog Timer.

Bit 3 This bit provides the security lock for the secured area of RT/CMOS. Setting this bit to 1 electrically locks the 8-byte, power-on password. Once this bit is set by POST, it can only be cleared by turning the system off.

Bit 2 This bit is reserved.

Bit 1 This bit is ORed with bit 1 in the keyboard output port to enable the 'address 20' signal (A20). When both bits are set to 0, A20 is disabled and set to 0. This bit is set to 0 during a system reset. (See the Keyboard and Auxiliary Device Controller section in the *Hardware Interface Technical Reference*.)

Bit 0 This bit provides an alternate method of resetting the system microprocessor. This alternate method supports operating systems requiring faster operation than was provided on the IBM Personal Computer AT*. Resetting the system microprocessor is used to switch the microprocessor from the protected mode to the real address mode. The alternate reset takes 13.4 microseconds.

This bit is set to 0 either by a system reset or a Write operation. When a Write operation changes this bit from 0 to 1, the alternate reset pin is pulsed high for 100 to 125 nanoseconds. The reset occurs after a minimum delay of 6.72 microseconds. While the reset is occurring, the latch remains set so that POST can read this bit. If the bit is 0, POST assumes the system was just powered on. If the bit is 1, POST assumes a switch from the protected mode to the real mode has taken place.

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* Personal Computer AT is a trademark of the International Business Machines Corporation.

Power-On Password

RT/CMOS RAM has eight bytes reserved for the power-on password and its check character. The eight bytes are initialized to hex 00. The microprocessor can only access these bytes during power-on self-test (POST). After POST is completed, if a power-on password is installed, the password bytes are locked and cannot be accessed by a program. A power-on password can be from 1 to 7 characters.

During power-on password installation, the password (1 to 7 keyboard scan codes), is stored in the security space.

Power-on password installation is a function of a program contained on the Reference Diskette. Once the power-on password utility has been installed, the password can be changed only during POST (power-on self-test). When the new power-on password is installed, changed, or removed, the password is not visible on the display.

The system unit cover can be physically locked to prevent unauthorized access to the battery. This helps prevent unauthorized battery removal and loss of power-on password and configuration information.

For information about the keyboard password, see the Keyboard and Auxiliary Device Controller section in the *Hardware Interface Technical Reference.*

Hardware Compatibility

The Model 70 maintains many of the interfaces used by the IBM Personal Computer AT. In most cases, command and status organization of these interfaces is maintained.

The functional interfaces for the Model 70 are compatible with the following interfaces:

- The Intel** 8259 interrupt controllers (without edge triggering).
- The Intel 8253 timers driven from 1.193 MHz (timer 0 and 2 only).
- The Intel 8237 DMA controller address/transfer counters, page registers and status fields only. The Command and Request registers are not supported. The rotate and mask functions are not supported. The Mode register is partially supported.
- The NS16450 serial port.
- The Intel 8088, 8086, and 80286 microprocessors.
- The Intel 8272 diskette drive controller.
- The Motorola** MC146818 Time of Day Clock command and status (CMOS reorganized).
- The Intel 8042 keyboard port at address hex 0060.
- Display modes supported by the IBM Monochrome Display and Printer Adapter, the IBM Color/Graphics Monitor Adapter, and the IBM Enhanced Graphics Adapter.
- The parallel printer ports (Parallel 1, Parallel 2, and Parallel 3) in compatibility mode.
- Generally compatible with the Intel 80287 and 8087 Math Coprocessors.

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Error Codes

POST returns a message in the form of a number to indicate the type of test that failed. The following table gives the failure by error code. For information on unlisted error codes, contact Developer Assistance at 1-800-IBM-7763 (this number is for developers who are registered with IBM).

Error Number	Error Indication
101	Interrupt Failure
102	Timer Failure
103	Timer Interrupt Failure
104	Protected Mode Failure
105	Keyboard Controller Command Failure
107	Hot NMI Test
108	Timer Bus Test
109	Memory Select
110	System Board Parity
111	I/O Parity
112	Watchdog Timeout
113	DMA Arbitration Timeout
114	External ROM Checksum
160	System Board ID Not Recognized
161	Bad Battery or Configuration
162	CMOS Checksum or Adapter ID Mismatch
163	Date and Time Not Set
164	Memory Size Mismatch
165	Adapter ID Mismatch
166	Card Busy
167	System Clock Not Updating
201	Memory Miscompare or Parity
202	Memory Address Line Error (Address Line 00 - 15)
203	Memory Address Line Error (Address Line 16 - 31)
211	Memory Base 64KB on System Board Failed
215	Memory Base 64KB on Daughter/SIP 2 Failed
216	Memory Base 64KB on Daughter/SIP 1 Failed

Figure 3-40 (Part 1 of 2). POST Error Message Table

Error Number	Error Indication
221	ROM to RAM Copy
225	Wrong Speed Memory on System Board
301	Keyboard Interface
303	Keyboard or System Board
304	Keyboard Clock Failure
305	Keyboard +5V Error
601	Diskette Drive or Controller
602	Diskette Boot Record
1101	Async Error
2401	System Board Video
8601	Mouse Timeout
8602	Mouse Interface
8603	Mouse Interrupt
10480	Drive C Seek Failure
10481	Drive D Seek Failure
10482	Drive Failed Controller Test
10483	Drive Controller Failed to Reset
10490	Drive C Read Failure
10491	Drive D Read Failure
12901	Failed Processor Portion of Processor Board Test (Type 3 and Type 4)
12902	Failed Cache Portion of Processor Board Test (Type 3 and Type 4)
12903	Failed Math Coprocessor Portion of Processor Board Test (Type 4)

Figure 3-40 (Part 2 of 2). POST Error Message Table

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