VT20C18 • VT20C19

2,048 × 8 SRAM

FEATURES

- High-speed access and cycle times: 20, 25, and 35 ns
- Fast output enable control
- Fast chip select option (VT20C19)
- Automatic power-down when deselected (VT20C18)
- CMOS process for low power:
  - 600 mW (typical) active
  - 35 mW (typical) standby (VT20C18)
  - 100 μW (typical) CMOS standby (VT20C18)
- Highly reliable six-transistor memory cell
- All pins capable of withstanding electrostatic discharge greater than 2,000 V
- 24-lead, 300 mil plastic DIP, SOG and SOJ packages

DESCRIPTION

The VT20C18 and VT20C19 are high-speed static RAMs (SRAMs) that are organized as 2,048 words by 8 bits. They were developed in conjunction with VISIC Inc., and are fabricated using an advanced 1.5 micron CMOS process. These devices offer very high performance and reliability, as well as low power, making them suitable for use in high-performance cache memory, writeable control store and high-speed data buffer applications.

The VT20C18, with automatic power-down, offers standby current of only 7 mA (typical) when deselected. The VT20C19 offers a fast chip select option that provides data access in only 10 ns.

For easy memory expansion, both devices have active-LOW chip enable ($\overline{E}$), output enable ($\overline{G}$) and write enable ($\overline{W}$) signals, as well as three-state outputs. The VT20C18 and VT20C19 are packaged in 300-mil DIPs with industry-standard pinouts, but offer higher speeds for increased system performance.

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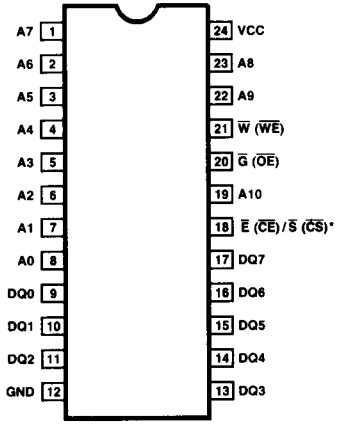
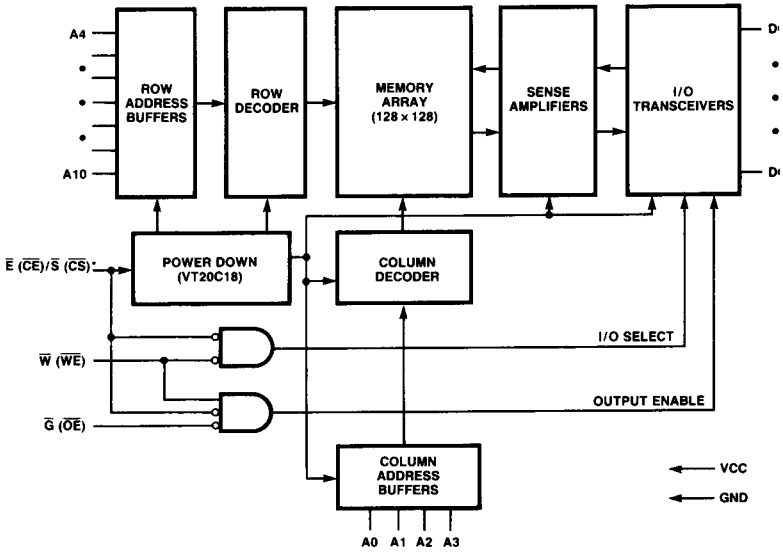
PIN DIAGRAM

VT20C18 • VT20C19



BLOCK DIAGRAM



PIN NAMES

A0–A10	Address Inputs
DQ0–DQ7	Data Inputs/Outputs
$\overline{E}$ ($\overline{CE}$)/$\overline{S}$ ($\overline{CS}$)*	Chip Enable/Chip Select*
$\overline{W}$ ($\overline{WE}$)	Write Enable
$\overline{G}$ ($\overline{OE}$)	Output Enable
VCC	Power (5 V)
GND	Ground (0 V)

*VT20C19 only.

ABSOLUTE MAXIMUM RATINGS

Voltage on VCC Relative to GND	−1 V to +7 V
Voltage on Any Pin Relative to GND	−2 V to VCC +1 V
Storage Temperature	−65°C to +150°C
Short Circuit Current (Each Output)	30 mA
Static Discharge Voltage	>2000 V
Latch-Up Current (TA = 0°C to +70°C)	>200 mA

Stresses above those listed may cause permanent damage to the device. These are stress ratings only, and functional operation of the device under these or any conditions above those indicated in this data sheet is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DC CHARACTERISTICS TA = 0°C to +70°C, VCC = 5 V ±10%, Note 1

Symbol	Parameter		Min	Typ	Max	Unit	Conditions
VIL	Input LOW Voltage		−1.0		0.8	V	Note 2
VIH	Input HIGH Voltage		2.2		VCC +1	V	Note 3
VOL	Output LOW Voltage				0.4	V	IOUT = 8.0 mA (each output)
VOH	Output HIGH Voltage		2.4			V	IOUT = −4.0 mA (each output)
ILI	Input Leakage Current		−10		10	μA	VIN = VCC to GND
IIOL	Input/Output Leakage Current		−10		10	μA	VIN = VCC to GND
ICC	VCC Current, Active	VT20C18/19-20			150	mA	$\overline{E}$ = VIL, outputs are open-load
		VT20C18/19-25			135	mA	
		VT20C18/19-35			120	mA	
ISB1	VCC Current, Standby	VT20C18-20			15	mA	$\overline{E} \geq$ VIH
		VT20C18-25			10	mA	
		VT20C18-35			10	mA	
ISB2	VCC Current, CMOS Standby	VT20C18-20			2	mA	$\overline{E} \geq$ VCC −0.2 V
		VT20C18-25			100	μA	
		VT20C18-35			100	μA	

CAPACITANCE TA = 25°C, f = 1 MHz (sampled only)

Symbol	Parameter	Typ	Max	Unit
CI/O	Combined I/O Capacitance	7	10	pF
CIN	Input Capacitance	7	10	pF

AC TEST CONDITIONS

Input Voltage Levels	0 V to 3 V
Input Rise and Fall Times	5 ns
Input Reference Levels	1.5 V
Output Reference Levels	1.5 V
Output Load	Figures 1a and 1b

AC TESTING LOAD CIRCUIT

FIGURE 1a. OUTPUT LOAD CIRCUIT A

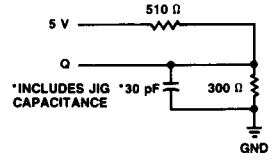
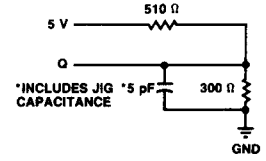


FIGURE 1b. OUTPUT LOAD CIRCUIT B



Notes:

1. Operation across the temperature range is guaranteed with 400 linear feet per minute of air flow.
2. VIL min is −2.0 V for pulse widths of less than 20 ns.
3. All input pins are diode-clamped to VCC. Some testers may not have enough drive capability to reach the maximum input voltage.

TIMING CHARACTERISTICS $T_A = 0°C$ to $+70°C$, $V_{CC} = 5\ V \pm 10\%$

READ CYCLE

Symbol	Parameter		VT20C18/19-20 Min	VT20C18/19-20 Max	VT20C18/19-25 Min	VT20C18/19-25 Max	VT20C18/19-35 Min	VT20C18/19-35 Max	Unit
tRC	Read Cycle Time		20		25		35		ns
tAA	Address Access Time			20		25		35	ns
tOH	Output Hold Time from Address Change		5		5		5		ns
tEA	$\overline{E}$ LOW to Output Valid	VT20C18		20		25		35	ns
		VT20C19		10		12		15	ns
tGA	$\overline{G}$ LOW to Output Valid			10		10		10	ns
tLZG	$\overline{G}$ LOW to Output Low Z		0		0		0		ns
tHZG	$\overline{G}$ HIGH to Output High Z (Output Load Figure 1b)			10		10		15	ns
tLZE	$\overline{E}$ LOW to Output Low Z		3		3		3		ns
tHZE	$\overline{E}$ HIGH to Output High Z (Output Load Figure 1b)			10		15		15	ns
tPU	$\overline{E}$ LOW to Power-Up (VT20C18)		0		0		0		ns
tPD	$\overline{E}$ HIGH to Power-Down (VT20C18)			15		15		15	ns

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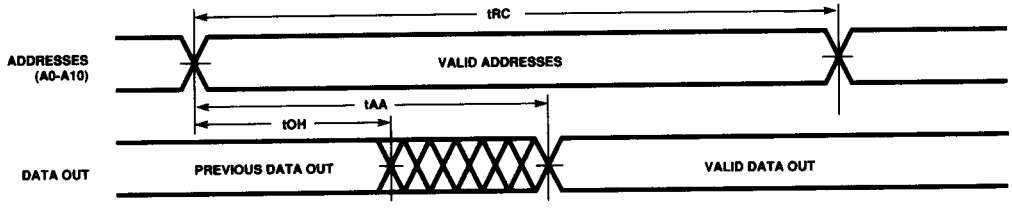
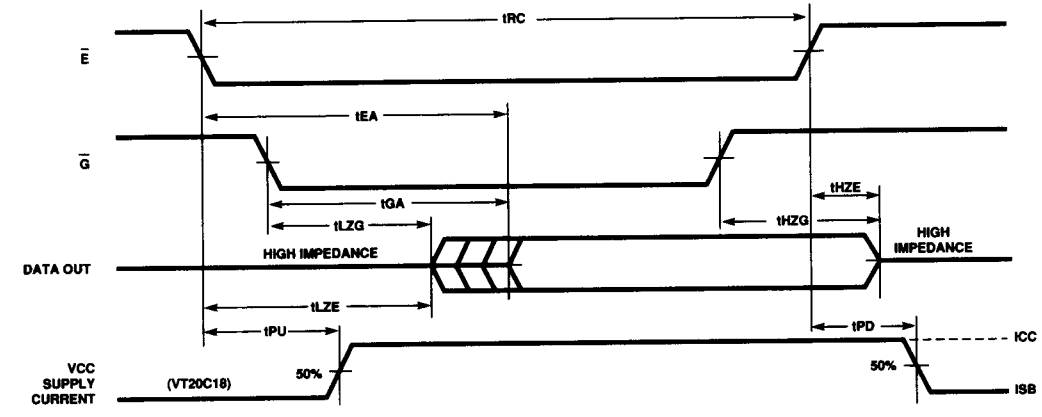
TIMING DIAGRAMS

READ CYCLE NO. 1 ($\overline{W}$ = VIH; $\overline{G}$, $\overline{E}$ = VIL)



READ CYCLE NO. 2 ($\overline{W}$ = VIH), Note 1



Note:
1. Address valid prior to or coincident with $\overline{E}$ transition LOW.

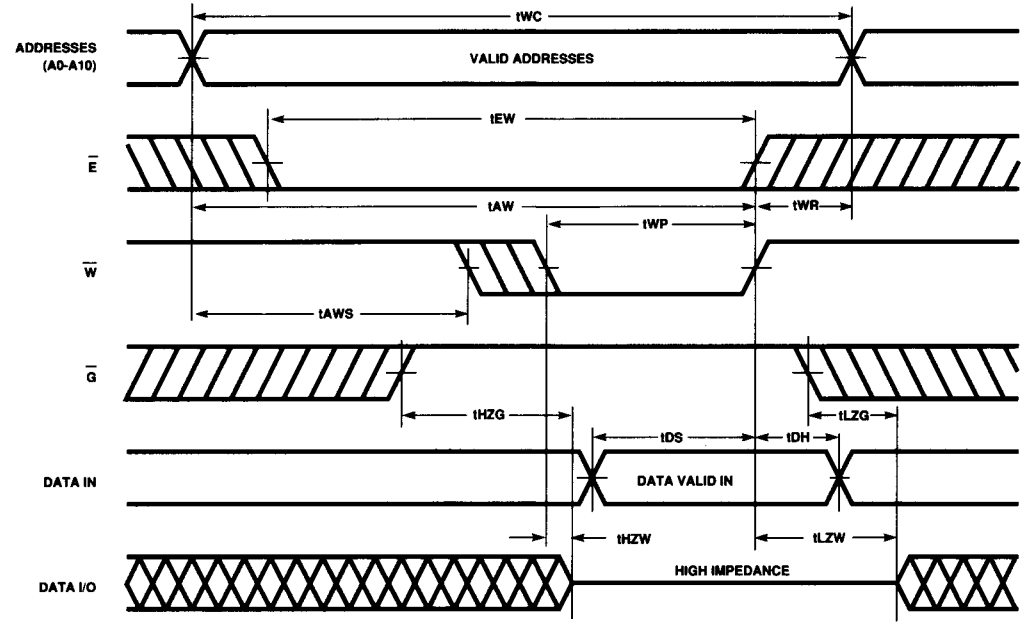
TIMING CHARACTERISTICS TA = 0°C to +70°C, VCC = 5 V ± 10%, Note 1

WRITE CYCLE

Symbol	Parameter	VT20C18/19-20		VT20C18/19-25		VT20C18/19-35		Unit
		Min	Max	Min	Max	Min	Max	
tWC	Write Cycle Time	20		25		35		ns
tEW	$\overline{E}$ LOW to Write End	20		25		30		ns
tAW	Address Set-Up Time to Write End	15		20		30		ns
tWR	Address Hold Time from Write End	0		0		0		ns
tAWS	Address Set-Up to Write Start	0		0		0		ns
tWP	$\overline{W}$ Pulse Width	15		20		25		ns
tDS	Data In Set-Up Time to Write End	10		12		15		ns
tDH	Data In Hold Time After Write End	0		0		0		ns
tHZW	$\overline{W}$ LOW to Output High Z (Output Load Figure 1b)		10		10		15	ns
tLZW	$\overline{W}$ HIGH to Output Low Z	0		0		0		ns
tHZG	$\overline{G}$ HIGH to Output High Z (Output Load Figure 1b)		10		15		15	ns
tLZG	$\overline{G}$ LOW to Output Low Z	0		0		0		ns

TIMING DIAGRAMS

WRITE CYCLE NO. 1 ($\overline{W}$ Controlled), Notes 2 and 3

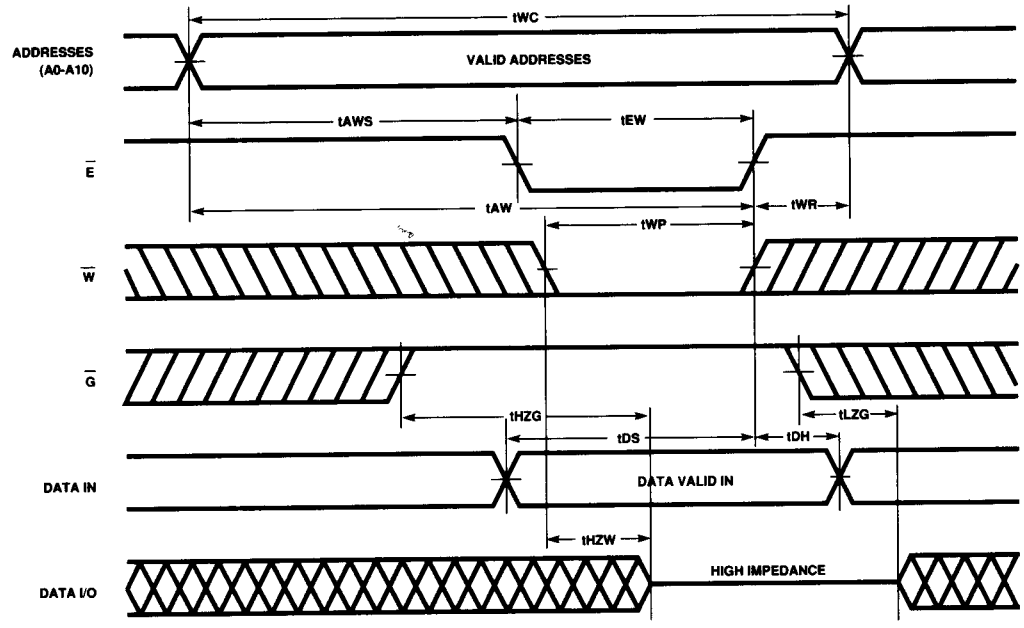


Notes:

1. All timing parameters were measured with output load Figure 1a unless otherwise noted.
2. Both $\overline{E}$ and $\overline{W}$ must be LOW to initiate a write. Either signal can terminate a write by going HIGH; thus, data set-up and hold are referenced to the rising edge of $\overline{E}$ or $\overline{W}$, whichever occurs first.
3. If $\overline{OE}$ is low during a $\overline{WE}$ controlled write cycle, the write pulse width must be the larger of the tWP or (tHZW + tDS) to allow the I/O drivers to turn off and data to be placed on the bus for the required tDS. If $\overline{OE}$ is high during a $\overline{WE}$ controlled write cycle, this requirement does not apply and the write pulse can be as short as the specified tWP.

TIMING DIAGRAM (Cont.)

WRITE CYCLE NO. 2 ($\overline{E}$ Controlled), Notes 1 and 2



Notes:

1. Both $\overline{E}$ and $\overline{W}$ must be LOW to initiate a write. Either signal can terminate a write by going HIGH; thus, data set-up and hold are referenced to the rising edge of $\overline{E}$ or $\overline{W}$, whichever occurs first.
2. If $\overline{E}$ goes HIGH simultaneously with $\overline{W}$ HIGH, the output remains in a high-impedance state.