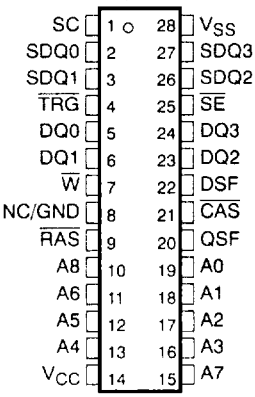
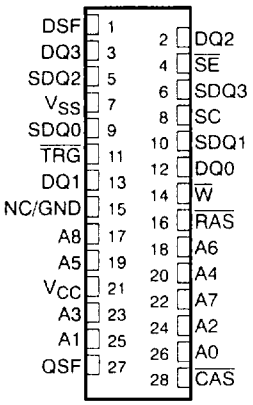
This Data Sheet Is Applicable to All TMS44C251s Symbolized With Revision "I" and Subsequent Revisions as Described on Page 8-71.

- **DRAM: 262 144 Words × 4 Bits**
  SAM: 512 Words × 4 Bits
- **Dual Port Accessibility — Simultaneous and Asynchronous Access from the DRAM and SAM Ports**
- **Bidirectional Data Transfer Function Between the DRAM and the Serial Data Register**
- **4 × 4-Block Write Feature for Fast Area Fill Operations. As Many as Four Memory Address Locations Written Per Cycle From an On-Chip Color Register**
- **Write-Per-Bit Feature for Selective Write to Each RAM I/O. Two Write-Per-Bit Modes to Simplify System Design**
- **Enhanced Page Mode Operation for Faster Access**
- **$\overline{CAS}$-Before-$\overline{RAS}$ and Hidden Refresh Modes**
- **RAM Output Enable Allows Direct Connection of DQ and Address Lines to Simplify System Design**
- **Long Refresh Period . . . Every 8 ms (Max)**
- **DRAM Port Is Compatible with the TMS44C256**
- **Up to 33 MHz Uninterrupted Serial Data Streams**
- **Split Serial Data Register for Simplified Realtime Register Reload**
- **3-State Serial I/Os Allow Easy Multiplexing of Video Data Streams**
- **512 Selectable Serial Register Starting Locations**
- **All Inputs and Outputs TTL Compatible**
- **Texas Instruments EPIC™ CMOS Process**

DZ Package† (Top View)



SD Package† (Top View)



†The packages shown here are for pinout reference only and are not drawn to scale.

PIN NOMENCLATURE

A0-A8	Address Inputs
$\overline{CAS}$	Column Enable
DQ0-DQ3	DRAM Data In-Out/Write Mask Bit
$\overline{SE}$	Serial Enable
$\overline{RAS}$	Row Enable
SC	Serial Data Clock
SDQ0-SDQ3	Serial Data In-Out
$\overline{TRG}$	Transfer Register/Q Output Enable
$\overline{W}$	Write Mask Select/Write Enable
DSF	Special Function Select
QSF	Split-Register Activity Status
V_{CC}	5-V Supply
V_{SS}	Ground
NC/GND	No Connect/Ground (Important: not connected to internally to V_{SS})

- **Performance Ranges:**

V_{CC} ± 5%

	ACCESS TIME ROW ADDRESS (MAX) $t_{a(R)}$	ACCESS TIME COLUMN ENABLE (MAX) $t_{a(C)}$	ACCESS TIME SERIAL DATA (MAX) $t_{a(SQ)}$	ACCESS TIME SERIAL ENABLE (MAX) $t_{a(SE)}$
TMS44C251-1	100 ns	25 ns	30 ns	20 ns

V_{CC} ± 10%

TMS44C251-10	100 ns	25 ns	30 ns	20 ns
TMS44C251-12	120 ns	30 ns	35 ns	25 ns

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description

The TMS44C251 multiport video RAM is a high speed, dual ported memory device. It consists of a dynamic random-access memory (DRAM) organized as 262 144 words of 4 bits each interfaced to a serial data register, or Serial Access Memory (SAM), organized as 512 words of 4 bits each. The TMS44C251 supports three basic types of operation: random access to and from the DRAM, serial access to and from the serial register, and bidirectional transfer of data between any row in the DRAM and the serial register. Except during transfer operations, the TMS44C251 can be accessed simultaneously and asynchronously from the DRAM and SAM ports. During transfer operations, the 512 columns of the DRAM are connected to the 512 positions in the serial data register. The 512 × 4 bit serial data register can be loaded from the memory row (transfer read), or else the contents of the 512 × 4 bit serial data register can be written to the memory row (transfer write).

The TMS44C251 is equipped with several features designed to provide higher system-level bandwidth and simplify design integration on both the DRAM and SAM ports. On the DRAM port, greater pixel draw rates can be achieved by the device's 4 × 4 Block Write mode. The Block Write mode allows four bits of data present in an on-chip color data register to be written to any combination of four adjacent column address locations. As many as 16 bits of data can be written to memory during each $\overline{\text{CAS}}$ cycle time. Also on the DRAM port, a write mask register provides a persistent write-per-bit mode without repeated mask loading.

On the serial register, or SAM port, the TMS44C251 offers a split-register transfer read (DRAM to SAM) option, which enables realtime register reload implementation for truly continuous serial data streams without critical timing requirements. The register is divided into a high half and a low half. While one half is being read out of the SAM port, the other half can be loaded from the memory array. This new realtime register reload implementation allows truly continuous serial data. For applications not requiring realtime register reload (for example, reloads done during CRT retrace periods), the single register mode of operation is retained to simplify design. The SAM can also be configured in input mode, accepting serial data from an external device. Once the serial register within the SAM is loaded, its contents can be transferred to the corresponding column positions in any row in memory in a single memory cycle.

The SAM port is designed for maximum performance. Data can be input to or accessed from the SAM at serial rates up to 33 MHz. During a split-register mode of operation, internal circuitry detects when the last bit position is accessed from the active half of the register and immediately transfers control to the opposite half. A separate open-drain output, designated QSF, is included to indicate which half of the serial register is active at any given time in the split register mode.

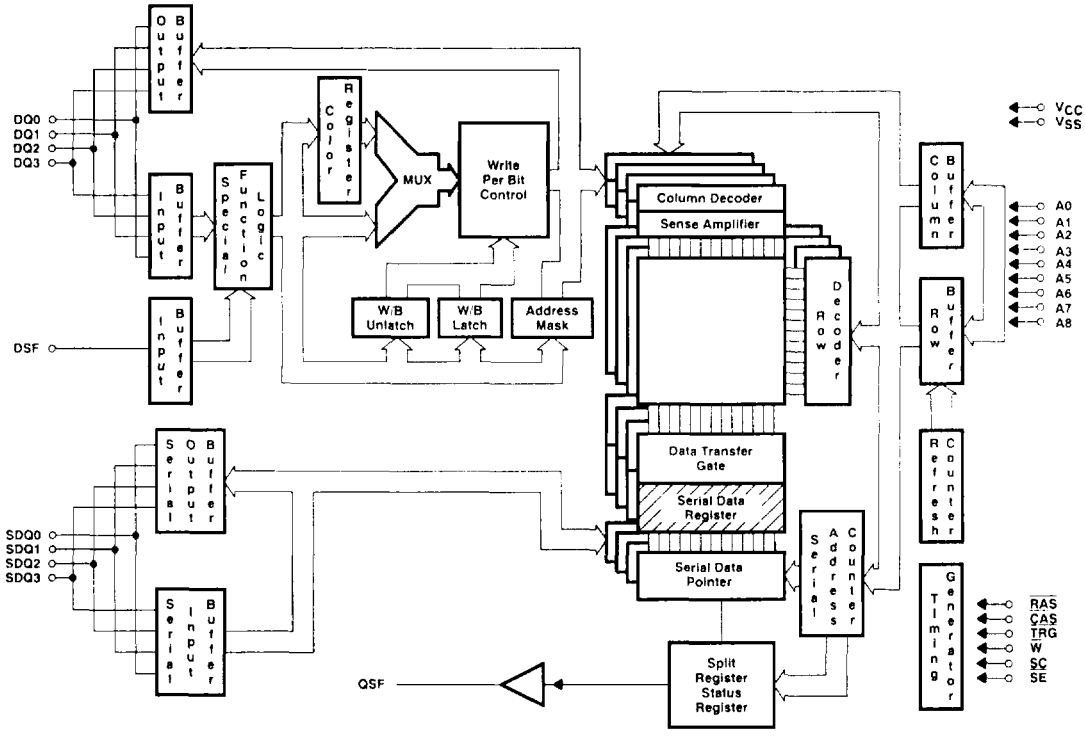
All inputs, outputs, and clock signals on the TMS44C251 are compatible with Series 74 TTL. All address lines and data-in are latched on-chip to simplify system design. All data-outs are unlatched to allow greater system flexibility.

The TMS44C251 employs state-of-the-art Texas Instruments EPIC™ scaled-CMOS, double-level polysilicon/polycide gate technology for very high performance combined with low cost and improved reliability.

The TMS44C251 is offered in a 28-pin small-outline J-lead package (DZ suffix) for direct surface mounting in rows on 400-mil (5,08-mm) centers. It is also offered in a 400-mil, 28-pin zig-zag in-line package (SD suffix). Both packages are characterized for operation from 0°C to 70°C (L suffix).

The TMS44C251 and other Multiport Video RAMs are supported by a broad line of graphics processor and control devices from Texas Instruments, including the TMS34020 Graphics System Processor.

functional block diagram



Detailed Pin Description vs Operational Mode

PIN	DRAM	TRANSFER	SAM
A0-A8	Row, Column Address	Row, Tap Address	
$\overline{CAS}$	Column Enable, Output Enable	Tap Address Strobe	
DQi	DRAM Data I/O, Write Mask Bits		
DSF	Block Write Enable	Split-Register Enable	
	Persistent Write-per-Bit Enable	Alternate Write Transfer Enable	
	Color Register Load Enable		
	Write-per-Bit Mask Load Enable		
$\overline{RAS}$	Row Enable	Row Enable	
$\overline{SE}$		Serial-In Mode Enable	Serial Enable
SC			Serial Clock
SDQi			Serial Data I/O
$\overline{TRG}$	Q Output Enable	Transfer Enable	
$\overline{W}$	Write Enable, Write-per-Bit Select	Transfer Write Enable	
QSF			Split Register Active Status
V_{CC}	5-V Supply (typical)		
V_{SS}	Device Ground		
NC/GND	Make No External Connection or Tie to System Ground		

operation

random-access operation

Refer to Table 1, Function Table, for Random-Access and Transfer Operations. Random-access operations are denoted by the designator "R" and transfer operations are denoted by a "T".

transfer register select and DQ enable ($\overline{TRG}$)

The $\overline{TRG}$ pin selects either register or random-access operation as $\overline{RAS}$ falls. For the random-access (DRAM) mode, $\overline{TRG}$ must be held high as $\overline{RAS}$ falls. Asserting $\overline{TRG}$ high as $\overline{RAS}$ falls causes the 512 storage elements of each data register to remain disconnected from the corresponding 512-bit lines of the memory array. (Asserting $\overline{TRG}$ low as $\overline{RAS}$ falls connects the 512-bit positions in the serial register to the bit lines and indicates that a transfer will occur between the data registers and the selected memory row. See "Transfer Operation" for details.)

During random-access operations, $\overline{TRG}$ also functions as an output enable for the random (Q) outputs. Whenever $\overline{TRG}$ is held high, the Q outputs are in the high-impedance state to prevent an overlap between the address and DRAM data. This organization allows the connection of the address lines to the data I/O lines but prohibits the use of the early write cycle. It also allows read-modify-write cycles to be performed by providing a three-state condition to the common I/O pins so that write data can be driven onto the pins after output read data has been externally latched.

address (A0 through A8)

Eighteen address bits are required to decode 1 of 262 144 storage cell locations. Nine row address bits are set up on pins A0 through A8 and latched onto the chip on the falling edge of $\overline{RAS}$. Then, the nine column address bits are set up on pins A0 through A8 and latched onto the chip on the falling edge of $\overline{CAS}$. All addresses must be stable on or before the falling edges of $\overline{RAS}$ and $\overline{CAS}$.

$\overline{RAS}$ and $\overline{CAS}$ address strobes and device control clocks

$\overline{RAS}$ is a control input that latches the states of the row address, $\overline{W}$, $\overline{TRG}$, $\overline{SE}$, $\overline{CAS}$, and DSF onto the chip to invoke the various DRAM and Transfer functions of the TMS44C251. $\overline{RAS}$ is similar to a chip enable in that it activates the sense amplifiers as well as the row decoder. $\overline{CAS}$ is a control input that latches the states of the column address and DSF to control various DRAM and Transfer functions. $\overline{CAS}$ also acts as an output enable for the DRAM output pins.

special function select (DSF)

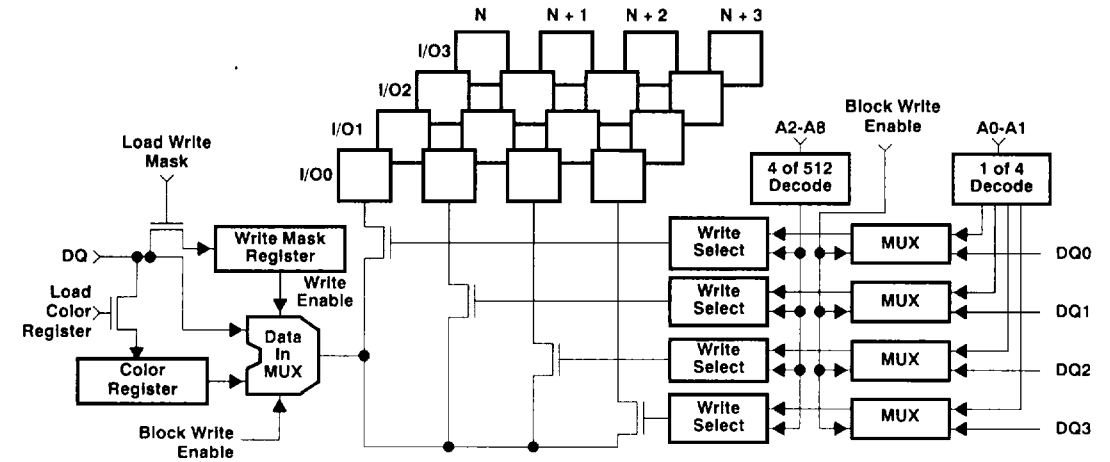
The Special Function Select input is latched on the falling edges of $\overline{RAS}$ and $\overline{CAS}$, similarly to an address, and serves four functions. First, during write cycles DSF invokes persistent write-per-bit operation. If $\overline{TRG}$ is high, $\overline{W}$ is low, and DSF is low on the falling edge of $\overline{RAS}$, the write mask will be reloaded with the data present on the DQ pins. If DSF is high, the mask will not be reloaded but will retain the data from the last mask reload cycle.

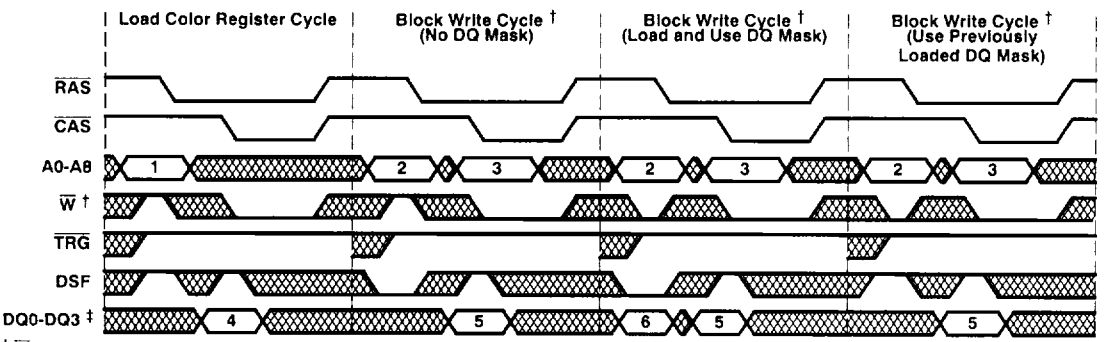
Second, DSF is used to change the internally stored write-per-bit mask register (or write mask) via the load write mask cycle. The data present on the DQ pins when $\overline{W}$ falls is written to the write mask rather than to the addressed memory location. See "Delayed Write Cycle Timing" and the accompanying "Write Cycle State Table" in the timing diagram section. Once the write mask is loaded, it can be used on subsequent masked write-per-bit cycles. This feature allows systems with a common address and data bus to use the write-per-bit feature, eliminating the time needed for multiplexing the write mask and input data on the data bus.

Third, DSF is used to load an on-chip four-bit data, or "color", register via the Load Color Register cycle. The contents of this register can subsequently be written to any combination of four adjacent column memory locations using the 4 × 4-Block Write feature. The load color register cycle is performed using normal write cycle timing except that DSF is held high on the falling edges of $\overline{RAS}$ and $\overline{CAS}$. Once the color register is loaded, it retains data until power is lost or until another load color register cycle is performed.

After loading the color register, the block write cycle can be enabled by holding DSF high on the falling edge of $\overline{CAS}$. During block write cycles, only the seven most significant column addresses (A2-A8) are latched on the falling edge of $\overline{CAS}$. The two least significant addresses (A0-A1) are replaced by the four DQ bits, which are also latched on the later of $\overline{CAS}$ or $\overline{W}$ falling. These four bits are used as an address mask and indicate which of the four column address locations addressed by A2-A8 will be written with the contents of the color register during the write cycle, and which ones will not. DQ0 enables a write to column address A1 is low, A0 is low; DQ1 enables a write to A1 is low, A0 is high; DQ2 enables a write to A1 is high, A0 is low; and DQ3 enables a write to A1 is high, A0 is high. A logic high level enables a write and a logic low level disables the write. A maximum of 16 bits can be written to memory during each $\overline{CAS}$ cycle (see Figure 1, Block Write Diagram).

Fourth, the DSF pin is used to invoke the split-register transfer and serial access operation, described in the sections "Transfer Operation" and "Serial Operation".





† $\overline{W}$ must be low during the Block Write Cycle.

‡ DQ0-DQ3 ($\overline{CAS}$) are latched on the later of $\overline{W}$ or $\overline{CAS}$ falling edge. DQ0-DQ3 ($\overline{RAS}$) are latched on $\overline{RAS}$ falling edge

Legend:

1. Refresh Address
2. Row Address
3. Block Address (A2-A8)
4. Color Register Data
5. Column Mask Data
6. DQ Mask Data

= Don't Care

Figure 1. Block Write Diagram

write enable, write-per-bit enable ($\overline{W}$)

The $\overline{W}$ pin enables data to be written to the DRAM and is also used to select the DRAM write-per-bit mode of operation. A logic level high on the $\overline{W}$ input selects the read mode and a logic low level selects the write mode. In an early write cycle, $\overline{W}$ is brought low before $\overline{CAS}$, and the DRAM output pins (DQ) remain in the high-impedance state for the entire cycle. During DRAM write cycles, holding $\overline{W}$ low on the falling edge of $\overline{RAS}$ will invoke the write-per-bit operation. Two modes of write-per-bit operation are supported.

Case 1. If DSF is low on the falling edge of $\overline{RAS}$, the write mask is reloaded. Accordingly, a four-bit binary code (the write-per-bit mask) is input to the device via the random DQ pins and is latched on the falling edge of $\overline{RAS}$. The write-per-bit mask selects which of the four random I/Os are written and which are not. After $\overline{RAS}$ has latched the write mask on-chip, input data is driven onto the DQ pins and is latched on the falling edge of the later of $\overline{CAS}$ or $\overline{W}$. If a low was strobed into a particular I/O pin on the falling edge of $\overline{RAS}$, data will not be written to that I/O. If a high was strobed into a particular I/O pin on the falling edge of $\overline{RAS}$, data will be written to that I/O.

Case 2. If DSF is high on the falling edge of $\overline{RAS}$, the mask is not reloaded from the DQ pins but instead retains the value stored during the last write-per-bit mask reload. This mode of operation is known as Persistent Write-per-Bit, since the write-per-bit mask is persistent over an arbitrary number of cycles.

See the corresponding timing diagrams for details.

IMPORTANT: The write-per-bit operation is invoked only if $\overline{W}$ is held low on the falling edge of $\overline{RAS}$. If $\overline{W}$ is held high on the falling edge of $\overline{RAS}$, write-per-bit is not enabled and the write operation is identical to that of standard × 4 DRAMs.

data I/O (DQ0-DQ3)

DRAM data is written during a write or read-modify-write cycle. The falling edge of $\overline{W}$ strobes data into the on-chip data latches. In an early write cycle, $\overline{W}$ is brought low prior to $\overline{CAS}$ and the data is strobed in by $\overline{CAS}$ with data setup and hold times referenced to this signal. In a delayed write or read-modify-write cycle, $\overline{CAS}$ will already be low. Thus, the data will be strobed-in by $\overline{W}$ with data setup and hold times referenced to this signal.

The three-state output buffers provide direct TTL compatibility (no pullup resistors required) with a fanout of two Series 74 TTL loads. Data-out is the same polarity as data-in. The outputs are in the high impedance (floating) state as long as $\overline{CAS}$ or $\overline{TRG}$ is held high. Data will not appear at the outputs until after both $\overline{CAS}$ and $\overline{TRG}$ have been brought low. Once the outputs are valid, they remain valid while $\overline{CAS}$ and $\overline{TRG}$ are low. $\overline{CAS}$ or $\overline{TRG}$ going high returns the outputs to a high-impedance state. In an early write cycle, the outputs are always in the high-impedance state. In a register transfer operation (memory to register or register to memory), the outputs remain in the high-impedance state for the entire cycle.

enhanced page mode

Unlike conventional page-mode DRAMs, the column-address buffers in this device are activated on the falling edge of $\overline{RAS}$. The buffers act as transparent or flow-through latches while $\overline{CAS}$ is high. The falling edge of $\overline{CAS}$ latches the column addresses. This feature allows theTMS44C251 to operate at a higher data bandwidth than conventional page-mode parts, since data retrieval begins as soon as column address is valid rather than when $\overline{CAS}$ transitions low. This performance improvement is referred to as *enhanced page mode*. Valid column address may be presented immediately after row address hold time has been satisfied, usually well in advance of the falling edge of $\overline{CAS}$. In this case, data is obtained after $t_{a(C)}$ max (access time from $\overline{CAS}$ low), if $t_{a(CA)}$ max (access time from column address) has been satisfied. In the event that column addresses for the next page cycle are valid at the time $\overline{CAS}$ goes high, access time for the next cycle is determined by the later occurrence of $t_{a(C)}$ or $t_{a(CP)}$ (access time from rising edge of $\overline{CAS}$).

Enhanced page mode operation allows faster memory access by keeping the same row address while selecting random column addresses. The time for row address setup, row address hold, and address multiplex is thus eliminated, and a memory cycle time reduction of up to 3 × can be achieved, compared to minimum $\overline{RAS}$ cycle times. The maximum number of columns that may be accessed is determined by the maximum $\overline{RAS}$ low time and page mode cycle time used. The TMS44C251 allows a full page (512 cycles) of information to be accessed in read, write, or read-modify-write mode during a single $\overline{RAS}$ low period using relatively conservative page mode cycle times.

During write-per-bit operations, the DQ pins are used to load the write-per-bit mask register using either mode of write-per-bit operation described above under the $\overline{W}$ pin description.

During block write operations, the DQ pins are used to load the on-chip color register during the load color register cycle and are also used as a write enable during block write cycles.

refresh

A refresh operation must be performed to each row at least once every eight milliseconds to retain data. Since the output buffer is in the high-impedance state (unless $\overline{CAS}$ is applied), the $\overline{RAS}$-only refresh sequence avoids any output during refresh. Strobing each of the 512 row addresses with $\overline{RAS}$ causes all bits in each row to be refreshed. $\overline{CAS}$ can remain high (inactive) for this refresh sequence to conserve power.

$\overline{CAS}$-before-$\overline{RAS}$ refresh

$\overline{CAS}$-before-$\overline{RAS}$ refresh is accomplished by bringing $\overline{CAS}$ low earlier than $\overline{RAS}$. The external row address is ignored and the refresh address is generated internally.

NC/GND

This pin is reserved for the manufacturer's test operation. It is an input and should be tied to system ground or left floating for proper device operation.

IMPORTANT: NC/GND is not connected internally to V_{SS}.

Table 1. Function Table

TYPE†	RAS FALL					CAS FALL	ADDRESS		DQ0-3		FUNCTION
	CAS	TRG	W¶	DSF	SE	DSF	RAS	CAS	RAS	CAS‡ W	
R	L	X§	X	X	X	X	X	X	X	X	CAS-Before-RAS Refresh
T	H	L	L	X	L	X	Row Addr	Tap Point	X	X	Register to Memory Transfer (Transfer Write)
T	H	L	L	H	X	X	Row Addr	Tap Point	X	X	Alternate Transfer Write (Independent of SE)
T	H	L	L	L	H	X	Refresh Addr	Tap Point	X	X	Serial Write-Mode Enable (Pseudo-Transfer Write)
T	H	L	H	L	X	X	Row Addr	Tap Point	X	X	Memory To Register Transfer (Transfer Read)
T	H	L	H	H	X	X	Row Addr	Tap Point	X	X	Split Register Transfer Read (Must Reload Tap)
R	H	H	L	L	X	L	Row Addr	Col Addr	Write Mask	Valid Data	Load and Use Write Mask, Write Data to DRAM
R	H	H	L	L	X	H	Row Addr	Col A2-A8	Write Mask	Addr Mask	Load and Use Write Mask, Block Write to DRAM
R	H	H	L	H	X	L	Row Addr	Col Addr	X	Valid Data	Persistent Write-per-Bit, Write Data to DRAM
R	H	H	L	H	X	H	Row Addr	Col A2-A8	X	Addr Mask	Persistent Write-per-Bit, Block Write to DRAM
R	H	H	H	L	X	L	Row Addr	Col Addr	X	Valid Data	Normal DRAM Read/Write (Non-Masked)
R	H	H	H	L	X	H	Row Addr	Col A2-A8	X	Addr Mask	Block Write to DRAM (Non-Masked)
R	H	H	H	H	X	L	Refresh Addr	X	X	Write Mask	Load Write Mask
R	H	H	H	H	X	H	Refresh Addr	X	X	Color Data	Load Color Register

† R = Random access operation; T = Transfer operation.
‡ DQ0-3 are latched on the later of W or CAS falling edge.
§ X = Don't care.
¶ In persistent write-per-bit function, W must be high during the refresh cycles.
Addr Mask = 1; write to address location enabled.
Write Mask = 1; write to I/O enabled.

random port to serial port interface

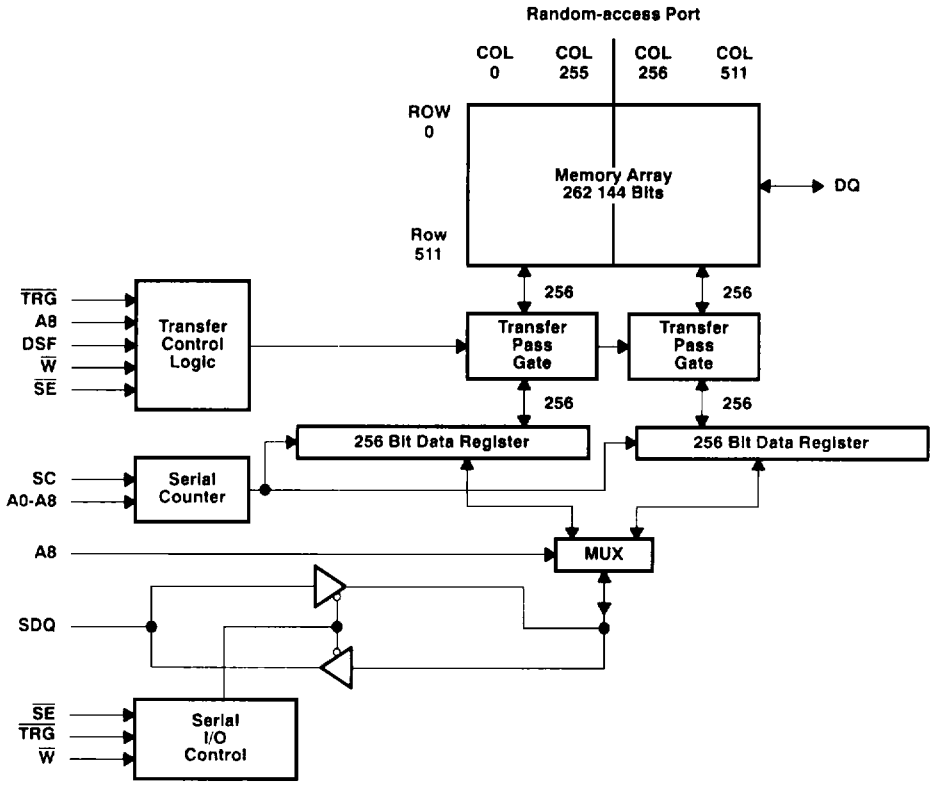


Figure 2. Block Diagram Showing One Random and One Serial I/O Interface

random-address space to serial-address space mapping

The 512 bits in each of the four data registers of the SAM are connected to the 512 column locations of each of the four random I/Os. Data can be accessed in or out of the SAM starting at any of the 512 data bit locations. This start location is selected by addresses A0 through A8 on the falling edge of $\overline{CAS}$ during any transfer cycle. The SAM is accessed starting from the selected start address, proceeding from the lowest to the highest significant bits. After the most significant bit position (511) is accessed, the serial counter wraps around such that bit 0 is accessed on the next clock pulse. The selected start address is stored and used for all subsequent transfer cycles until $\overline{CAS}$ is again brought low during any transfer cycle. Thus, the start address can be set once and $\overline{CAS}$ held high during all subsequent transfer cycles and the start address point will not change regardless of data present on A0 through A8.

split-register mode random-address to serial address-space mapping

In split-register transfer operations, the serial data register is split into halves, the low half containing bits 0 through 255 and the high half containing bits 256 through 511. When a split-register transfer cycle is performed, the tap address must be strobed in on the falling edge of $\overline{CAS}$. The most significant column address bit (A8) determines which register half will be reloaded from the memory array. The eight remaining column address bits (A0-A7) are used to select the SAM starting location for the register half selected by A8.

To insure proper operation when using the split-register read transfer feature, a non-split-register transfer must precede any split-register sequence. The serial start address must be supplied for every split-register transfer. (See Split Register Operating Sequence on page 8-69.)

transfer operations

As illustrated in Table 1, the TMS44C251 supports five basic transfer modes of operation:

1. Normal Write Transfer (SAM to DRAM)
2. Alternate Write Transfer (independent of the state of $\overline{SE}$)
3. Pseudo Write Transfer (Switches serial port from serial-out mode to serial-in mode. No actual data transfer takes place between the DRAM and the SAM.)
4. Normal Read Transfer (Transfer entire contents of DRAM to SAM)
5. Split-Register Read Transfer (Divides the SAM into a high and a low half. Only one half is transferred to the SAM while the other half is read from the serial I/O port.)

NOTES: A. All transfer write operations will switch the SDQ pins into the input (write) mode. Before data can be clocked into the serial port via the SDQ pins and SC serial clock, it is necessary to switch the SDQ pins into input mode via a previous transfer write operation.

B. *Pseudo Transfer Write Mode* has the same meaning as the term "Write Mode Control Cycle" as used in some VRAM data sheets. Both modes, or control cycles, serve to switch the direction of the SDQs without an actual data transfer taking place.

C. All transfer read operations will switch the SDQ pins into the output (read) operation

D. All transfer read operations and the pseudo transfer write operation perform a memory refresh on the selected row.

Table 2. Transfer Operation Logic

$\overline{TRG}$	$\overline{W}$	$\overline{SE}$	DSF	MODE
L	L	L	X	Register to memory (write) transfer, serial write mode enable
L	L	X	H	Alternate register to memory transfer, serial write mode enable
L	L	H	L	Pseudo write transfer, serial write mode enable
L	H	X	L	Memory to register (read) transfer
L	H	X	H	Split-register read transfer

NOTE: Above logic states are assumed valid on the falling edge of $\overline{RAS}$.

transfer register select ($\overline{TRG}$)

Transfer operations between the memory array and the data registers are invoked by bringing $\overline{TRG}$ low before $\overline{RAS}$ falls. The states of $\overline{W}$, $\overline{SE}$, and DSF, which are also latched on the falling edge of $\overline{RAS}$, determine which transfer operation will be invoked. (See Table 2.)

During read transfer cycles, $\overline{TRG}$ going high causes the addressed row of data to be transferred into the data register. Although the previous data in the data register is overwritten, the last bit of data appearing at SDQ before $\overline{TRG}$ goes high will remain valid until the first positive transition of SC after $\overline{TRG}$ goes high. The data at SDQ will then switch to new data beginning from the selected start, or *tap*, position.

transfer write enable ($\overline{W}$)

In any transfer operation, the state of $\overline{W}$ while $\overline{RAS}$ falls determines whether a read or write transfer will occur. To invoke any of the three possible write transfer operations, modes 1, 2, or 3 above, $\overline{W}$ must be low when $\overline{RAS}$ falls. If $\overline{W}$ is high when $\overline{RAS}$ falls, the transfer operation will be a read transfer (mode 4 or 5 above).

serial enable ($\overline{SE}$)

The serial enable pin has two functions, one that controls the transfer operations and one that controls the serial access operation.

For transfer operation, $\overline{SE}$ is latched together with DSF on the falling edge of $\overline{RAS}$ during any transfer write operation, i.e. when $\overline{TRG}$ and $\overline{W}$ are low when $\overline{RAS}$ falls (see Table 2):

- If $\overline{SE}$ is low at that time, a regular transfer write operation will occur.
- If $\overline{SE}$ is high and DSF is low at that time, a pseudo write transfer will occur, i.e. the SDQ pins will be switched from output to input mode without any data transfer from register to memory.
- If DSF is high, then an alternate register to memory transfer will occur, i.e. the state of $\overline{SE}$ is don't care.

column enable ($\overline{CAS}$)

If $\overline{CAS}$ is brought low during a transfer cycle, the address present on the pins A0 through A8 will become the new register start location. If $\overline{CAS}$ is held high during a control cycle, the previous tap address will be retained from the last transfer cycle in which $\overline{CAS}$ went low to set the tap address.

addresses (A0 through A8)

Nine address bits are required to select one of the 512 possible rows involved in the transfer of data to or from the data registers. The states of A0-A8 are latched on the fallling edge of $\overline{RAS}$ to select one of 512 rows for the transfer operation.

If $\overline{CAS}$ makes a high-to-low transition during any transfer cycle, the 9-bit address present on A0-A8 selects one of the 512 possible positions in the SAM from which the first serial data will be read or into which the first serial data will be written. This is also referred to as *setting the tap point*. During the very first transfer cycle, the tap point must be set. In subsequent transfer cycles, $\overline{CAS}$ need not go low, in which case the previously set tap point will be used.

In the split-register transfer mode, the most significant column address bit (A8) selects which half of the register will be reloaded from the memory array. The remaining eight addresses (A0-A7) determine the register starting location for the register to be reloaded.

special function input (DSF)

In the read transfer mode, holding DSF high on the falling edge of $\overline{RAS}$ selects the split-register mode transfer operation. This mode divides the serial data register into a high order half and a low order half; one active, and one inactive. When the cycle is initiated, a transfer occurs between the memory array and either the high half or the low half register, depending on the state of the most significant column address bit (A8) that is strobed in on the falling edge of $\overline{CAS}$. If A8 is high, the transfer is to the high half of the register. If A8 is low, the transfer is to the low half of the register. Use of the split-register mode read transfer feature allows on-the-fly read transfer operation without synchronizing $\overline{TRG}$ to the serial clock.

In the write transfer mode, holding DSF high on the falling edge of $\overline{RAS}$ permits use of an alternate mode of transfer write. This mode allows $\overline{SE}$ to be high on the falling edge of $\overline{RAS}$ without permitting a pseudo write transfer, with the serial port disabled during the entire transfer write cycle.

serial access operation

Refer to Table 2 for the following discussion on serial access operation.

serial clock (SC)

Data (SDQ) is accessed in or out of data registers on the rising edge of SC. The TMS44C251 is designed to work with a wide range of clock duty cycles to simplify system design. Since the data registers comprising the SAM are of static design, there are no SAM refresh requirements and there is no minimum SC clock operating frequency.

serial data input/output (SDQ0-SDQ3)

SD and SQ share a common I/O pin. Data is input to the device when $\overline{SE}$ is low during write mode, and data is output from the device when $\overline{SE}$ is low during read mode. The data in the SAM will be accessed in the direction from least significant bit to most significant bit. The data registers operate modulo 512. Thus, after bit 511 is accessed, the next bits to be accessed will be bits 00, 01, 02, and so on.

serial enable ($\overline{SE}$)

For serial access operation, $\overline{SE}$ enables or disables the SDQ pins. If the SDQ pins have been switched into input mode (write) by a previous transfer operation, $\overline{SE}$ high disables input and $\overline{SE}$ low enables input. If a previous transfer operation has switched the SDQ pins into output mode (read), $\overline{SE}$ high disables output and $\overline{SE}$ low enables output.

IMPORTANT NOTE: While $\overline{SE}$ is held high, the serial clock is NOT disabled. Thus, any SC pulses applied will increment the internal serial address counter regardless of the state of $\overline{SE}$. This ungated serial clock scheme minimizes access time of serial output from $\overline{SE}$ low since the serial clock input buffer and the serial address counter are not disabled by $\overline{SE}$.

QSF active status output for revision "I" and subsequent revision devices

During the split-register mode of serial access operation, QSF indicates which half of the serial register in the SAM is being accessed. If QSF is low, then the serial address pointer is accessing the lower (least significant) 256 bits of the SAM. If QSF is high, then the pointer is accessing the higher (most significant) 256 bits of the SAM. QSF changes state upon completing a transfer cycle, and the state of QSF is determined by the tap point loaded in that transfer cycle. QSF also changes state upon crossing the boundary between the two register halves in split-register mode. QSF is not an open-drain output pin.

QSF active status output for revision "H" devices

QSF is an open-drain output pin. During the split register mode of serial access operation, QSF indicates which half of the serial register in the SAM is being accessed. If QSF is low, then the serial address pointer is accessing the lower (least significant) 256 bits of the SAM. IF QSF is high, then the pointer is accessing the higher (most significant) 256 bits of the SAM.

QSF changes state upon crossing the boundary between the two register halves. When the SAM is not operating in split-register mode, the QSF output remains in the high-impedance state.

QSF is designed as an open drain output to allow OR-tying of QSF outputs from several chips. Thus, an external pullup resistor is required for the zero to one transition on QSF and the output rise time is determined by the load-capacitance and the value of the pullup resistor. The specification for QSF switching time assumes a pullup resistor of 820 ohms and a load capaticance of 50 picofarads illustrated as follows.

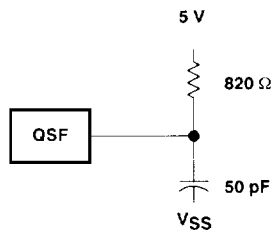


Figure 3. QSF Load Circuit (Revision "H" only)

power-up

To achieve proper device operation, an initial pause of 200 μs is required after power-up, followed by a minimum of eight $\overline{RAS}$ cycles or eight $\overline{CAS}$-before-$\overline{RAS}$ cycles, a memory-to-register transfer cycle, and two SC cycles.

absolute maximum ratings over operating free-air temperature†

Voltage on any pin except DQ and SDQ (see Note 1) ..... – 1 V to 7 V
Voltage on DQ and SDQ (see Note 1) ..... – 1 V to V_{CC} + 1
Voltage range on V_{CC} (see Note 1) ..... –1 V to 7 V
Short circuit output current (per output) ..... 50 mA
Power dissipation ..... 1 W
Operating free-air temperature range ..... 0°C to 70°C
Storage temperature range ..... – 65°C to 150°C

† Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions beyond those indicated in the "Recommended Operating Conditions" section of this specification is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values in this data sheet are with respect to V_{SS}.

recommended operating conditions

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	TMS44C251-1	4.75	5	5.25	V
		TMS44C251-10, TMS44C251-12	4.5	5	5.5	
V_{SS}	Supply voltage			0		V
V_{IH}	High-level input voltage		2.4		V_{CC}+1	V
V_{IL}	Low-level input voltage (see Note 2)		– 1		0.8	V
V_{OH}	High-level output voltage		2.4		V_{CC}	V
V_{OL}	Low-level output volage		– 1		0.4	V
T_A	Operating free-air temperature		0	25	70	°C

NOTE 2: The algebraic convention, where the more negative (less positive) limit is designated as minimum, is used in this data sheet for logic voltage levels only.

electrical characteristics over full ranges of recommended operating conditions

PARAMETER			TEST CONDITIONS	TMS44C251-1 TMS44C251-10		TMS44C251-12		UNIT
				MIN	MAX	MIN	MAX	
V_{OH}	High-level output voltage		I_{OH} = −2 mA	2.4		2.4		V
V_{OL}	Low-level output voltage		I_{OL} = 2 mA		0.4		0.4	V
I_L	Input leakage current	TMS44C251-10, TMS44C251-12	V_I = 0 to 5.8 V, V_{CC} = 5.5 V, All other pins = 0 to V_{CC}		±10		±10	μA
		TMS44C251-1	V_I = 0 to 5.55 V, V_{CC} = 5.25 V, All other pins = 0 to V_{CC}		±10		±10	μA
I_O	Output leakage current (see Note 3)	TMS44C251-10, TMS44C251-12	V_O = 0 to V_{CC}, V_{CC} = 5.5 V		±10		±10	μA
		TMS44C251-1	V_O = 0 to V_{CC}, V_{CC} = 5.25 V		±10		±10	μA

PARAMETER		SAM PORT	TMS44C251-1 TMS44C251-10		TMS44C251-12		UNIT
			MIN	MAX	MIN	MAX	
I_{CC1}	Operation current, $t_{c(RW)}$ = Minimum	Standby		90		80	mA
I_{CC1A}	$t_{c(SC)}$ = Minimum	Active		110		95	
I_{CC2}	Standby current, All clocks = V_{CC}	Standby		10		10	
I_{CC2A}	$t_{c(SC)}$ = Minimum	Active		35		35	
I_{CC3}	$\overline{RAS}$-only refresh current, $t_{c(RW)}$ = Minimum	Standby		90		80	
I_{CC3A}	$t_{c(SC)}$ = Minimum	Active		110		95	
I_{CC4}	Page mode current, $t_{c(P)}$ = Minimum	Standby		50		45	
I_{CC4A}	$t_{c(SC)}$ = Minimum	Active		60		55	
I_{CC5}	$\overline{CAS}$-before-$\overline{RAS}$ current, $t_{c(RW)}$ = Minimum	Standby		90		80	
I_{CC5A}	$t_{c(SC)}$ = Minimum	Active		110		95	
I_{CC6}	Data transfer current, $t_{c(RW)}$ = Minimum	Standby		90		80	
I_{CC6A}	$t_{c(SC)}$ = Minimum	Active		110		95	

NOTE 3: $\overline{SE}$ is disabled for SDQ output leakage tests.

capacitance over recommended ranges of supply voltage and operating free-air temperature, f = 1 MHz (see Note 4)

PARAMETER		MIN	MAX	UNIT
$C_{i(A)}$	Input capacitance, address inputs		6	pF
$C_{i(RC)}$	Input capacitance, strobe inputs		7	pF
$C_{i(W)}$	Input capacitance, write enable input		7	pF
$C_{i(SC)}$	Input capacitance, serial clock		7	pF
$C_{i(SE)}$	Input capacitance, serial enable		7	pF
$C_{i(DSF)}$	Input capacitance, special function		7	pF
$C_{i(TRG)}$	Input capacitance, transfer register input		7	pF
$C_{o(O)}$	Output capacitance, SDQ and DQ		7	pF
$C_{o(QSF)}$	Output capacitance, QSF		10	pF

NOTE 4: V_{CC} equal to 5 V ± 0.5 V for TMS44C251-10 and TMS44C251-12, 5 V ± 0.25 V for TMS44C251-1, and the bias on pins under test is 0 V.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (see Note 5)

PARAMETER		TEST CONDITIONS	ALT. SYMBOL	TMS44C251-1 TMS44C251-10		TMS44C251-12		UNIT
				MIN	MAX	MIN	MAX	
$t_{a(C)}$	Access time from $\overline{CAS}$	$t_{d(RLCL)}$ = MAX	t_{CAC}		25		25	ns
$t_{a(CA)}$	Access time from column address	$t_{d(RLCL)}$ = MAX	t_{AA}		50		25	ns
$t_{a(CP)}$	Access time from $\overline{CAS}$ high	$t_{d(RLCL)}$ = MAX	t_{CPA}		55		25	ns
$t_{a(R)}$	Access time from $\overline{RAS}$	$t_{d(RLCL)}$ = MAX	t_{RAC}		100		25	ns
$t_{a(G)}$	Access time of Q from $\overline{TRG}$ low		t_{OEA}		25		30	ns
$t_{a(SQ)}$	Access time of SQ from SC high	C_L = 30 pF	t_{SCA}		30		35	ns
$t_{a(SE)}$	Access time of SQ from $\overline{SE}$ low	C_L = 30 pF	t_{SEA}		20		25	ns
$t_{a(QSF)}$	Access time of QSF from SC low	C_L = 30 pF			60		60	ns
$t_{dis(CH)}$	Random output disable time from $\overline{CAS}$ high (See Note 6)	C_L = 100 pF	t_{OFF}	0	20	0	20	ns
$t_{dis(G)}$	Random output disable time from $\overline{TRG}$ high (See Note 6)	C_L = 100 pF	t_{OEZ}	0	20	0	20	ns
$t_{dis(SE)}$	Serial output disable time from $\overline{SE}$ high (See Note 6)	C_L = 30 pF	t_{SEZ}	0	20	0	20	ns

NOTES: 5. Switching times for RAM port output are measured with a load equivalent to 1TTL load and 100 pF, data out reference level is V_{OH}/V_{OL} = 2.4 V/0.8 V. Switching times for SAM port output are measured with a load equivalent to 1TTL load and 30 pF, serial data out reference level is V_{OH}/V_{OL} = 2 V/0.8 V.

6. $t_{dis(CH)}$, $t_{dis(G)}$, and $t_{dis(SE)}$ are specified when the output is no longer driven.

timing requirements over recommended ranges of supply voltage and operating free-air temperature †

		ALT. SYMBOL	TMS44C251-1 TMS44C251-10		TMS44C251-12		UNIT
			MIN	MAX	MIN	MAX	
$t_{c(rd)}$	Read cycle time (see Note 7)	t_{RC}	180		210		ns
$t_{c(W)}$	Write cycle time	t_{WC}	180		210		ns
$t_{c(rdW)}$	Read-modify-write cycle time	t_{RMW}	240		280		ns
$t_{c(P)}$	Page-mode read, write cycle time	t_{PC}	60		70		ns
$t_{c(RDWP)}$	Page-mode read-modify-write cycle time	t_{PRMW}	105		125		ns
$t_{c(TRD)}$	Transfer read cycle time	t_{RC}	180		210		ns
$t_{c(TW)}$	Transfer write cycle time	t_{WC}	180		210		ns
$t_{c(SC)}$	Serial clock cycle time (see Note 8)	t_{SCC}	30		35		ns
$t_{w(CH)}$	Pulse duration, $\overline{CAS}$ high	t_{CPN}	10		15		ns
$t_{w(CL)}$	Pulse duration, $\overline{CAS}$ low (see Note 9)	t_{CAS}	25	75 000	30	75 000	ns
$t_{w(RH)}$	Pulse duration, $\overline{RAS}$ high	t_{RP}	70		80		ns
$t_{w(RL)}$	Pulse duration, $\overline{RAS}$ low (see Note 10)	t_{RAS}	100	75 000	120	75 000	ns
$t_{w(WL)}$	Pulse duration, $\overline{W}$ low	t_{WP}	25		25		ns
$t_{w(TRG)}$	Pulse duration, $\overline{TRG}$ low		25		30		ns
$t_{w(SCH)}$	Pulse duration, SC high	t_{SC}	10		12		ns
$t_{w(SCL)}$	Pulse duration, SC low	t_{SCP}	10		12		ns
$t_{su(CA)}$	Column address setup time	t_{ASC}	0		0		ns
$t_{su(SFC)}$	DSF setup time before $\overline{CAS}$ low	t_{FSC}	0		0		ns
$t_{su(RA)}$	Row address setup time	t_{ASR}	0		0		ns
$t_{su(WMR)}$	$\overline{W}$ setup time before $\overline{RAS}$ low	t_{WSR}	0		0		ns
$t_{su(DQR)}$	DQ setup time before $\overline{RAS}$ low	t_{MS}	0		0		ns
$t_{su(TRG)}$	$\overline{TRG}$ setup time before $\overline{RAS}$ low	t_{THS}	0		0		ns
$t_{su(SE)}$	$\overline{SE}$ setup time before $\overline{RAS}$ low with $\overline{TRG}$ = $\overline{W}$ = low	t_{ESR}	0		0		ns
$t_{su(SFR)}$	DSF setup time before $\overline{RAS}$ low	t_{FSR}	0		0		ns
$t_{su(DCL)}$	Data setup time before $\overline{CAS}$ low	t_{DSC}	0		0		ns
$t_{su(DWL)}$	Data setup time before $\overline{W}$ low	t_{DSW}	0		0		ns
$t_{su(rd)}$	Read command setup time	t_{RCS}	0		0		ns
$t_{su(WCL)}$	Early write command setup time before $\overline{CAS}$ low	t_{WCS}	−5		−5		ns
$t_{su(WCH)}$	Write setup time before $\overline{CAS}$ high	t_{CWL}	25		30		ns
$t_{su(WRH)}$	Write setup time before $\overline{RAS}$ high	t_{RWL}	25		30		ns
$t_{su(SDS)}$	SD setup time before SC high	t_{SDS}	3		3		ns
$t_{h(CLCA)}$	Column address hold time after $\overline{CAS}$ low	t_{CAH}	20		20		ns
$t_{h(SFC)}$	DSF hold time after $\overline{CAS}$ low	t_{CFH}	20		20		ns
$t_{h(RA)}$	Row address hold time after $\overline{RAS}$ low	t_{RAH}	15		15		ns

Continued next page.

† Timing measurements are referenced to V_{IL} max and V_{IH} min.

NOTES: 7. All cycle times assume t_t = 5 ns.

8. For mid-line load, $t_{c(SC)}$ = 50 ns for Revision I and subsequent revisions; $t_{c(SC)}$ = 55 ns for Revision H only. For split-register, $t_{c(SC)}$ = 40 ns for Revision H only.
9. In a read-modify-write cycle, $t_{d(CLWL)}$ and $t_{su(WCH)}$ must be observed. Depending on the user's transition times, this may require additional $\overline{CAS}$ low time [$t_{w(CL)}$].
10. In a read-modify-write cycle, $t_{d(RLWL)}$ and $t_{su(WRH)}$ must be observed. Depending on the user's transition times, this may require additional $\overline{RAS}$ low time [$t_{w(RL)}$]

timing requirements over recommended ranges of supply voltage and operating free-air temperature (continued)†

		ALT. SYMBOL	TMS44C251-1 TMS44C251-10		TMS44C251-12		UNIT
			MIN	MAX	MIN	MAX	
$t_{h(TRG)}$	$\overline{TRG}$ hold time after $\overline{RAS}$ low	t_{THH}	15		15		ns
$t_{h(SE)}$	$\overline{SE}$ hold time after $\overline{RAS}$ low with $\overline{TRG}$ = $\overline{W}$ = low	t_{REH}	15		15		ns
$t_{h(RWM)}$	Write mask, transfer enable hold time after $\overline{RAS}$ low	t_{RWH}	15		15		ns
$t_{h(RDQ)}$	DQ hold time after $\overline{RAS}$ low (write mask operation)	t_{MH}	15		15		ns
$t_{h(SFR)}$	DSF hold time after $\overline{RAS}$ low	t_{RFH}	15		15		ns
$t_{h(RLCA)}$	Column address hold time after $\overline{RAS}$ low (see Note 10)	t_{AR}	45		45		ns
$t_{h(CLD)}$	Data hold time after $\overline{CAS}$ low	t_{DH}	20		25		ns
$t_{h(RLD)}$	Data hold time after $\overline{RAS}$ low (see Note 11)	t_{DHR}	45		50		ns
$t_{h(WLD)}$	Data hold time after $\overline{W}$ low	t_{DH}	20		25		ns
$t_{h(CHrd)}$	Read hold time after $\overline{CAS}$ (see Note 12)	t_{RCH}	0		0		ns
$t_{h(RHrd)}$	Read hold time after $\overline{RAS}$ (see Note 12)	t_{RRH}	10		10		ns
$t_{h(CLW)}$	Write hold time after $\overline{CAS}$ low	t_{WCH}	25		30		ns
$t_{h(RLW)}$	Write hold time after $\overline{RAS}$ low (see Note 11)	t_{WCR}	50		55		ns
$t_{h(WLG)}$	$\overline{TRG}$ hold time after $\overline{W}$ low (see Note 13)	t_{OEH}	25		30		ns
$t_{h(SDS)}$	SD hold time after SC high	t_{SDH}	5		5		ns
$t_{h(SHSQ)}$	SQ hold time after SC high	t_{SOH}	5		5		ns
$t_{d(RLCH)}$	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ high	t_{CSH}	100		120		ns
$t_{d(CHRL)}$	Delay time, $\overline{CAS}$ high to $\overline{RAS}$ low	t_{CRP}	0		0		ns
$t_{d(CLRH)}$	Delay time, $\overline{CAS}$ low to $\overline{RAS}$ high	t_{RSH}	25		30		ns
$t_{d(CLWL)}$	Delay time, $\overline{CAS}$ low to $\overline{W}$ low (see Notes 14 and 15)	t_{CWD}	55		65		ns
$t_{d(RLCL)}$	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ low (see Note 16)	t_{RCD}	25	75	25	90	ns
$t_{d(CARH)}$	Delay time, column address to $\overline{RAS}$ high	t_{RAL}	50		60		ns
$t_{d(RLWL)}$	Delay time, $\overline{RAS}$ low to $\overline{W}$ low (see Note 14)	t_{RWD}	130		155		ns
$t_{d(CAWL)}$	Delay time, column address to $\overline{W}$ low (see Note 14)	t_{AWD}	85		100		ns
$t_{d(RLCH)}$	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ high (see Note 17)	t_{CHR}	25		25		ns
$t_{d(CLRL)}$	Delay time, $\overline{CAS}$ low to $\overline{RAS}$ low (see Note 17)	t_{CSR}	10		10		ns
$t_{d(RHCL)}$	Delay time, $\overline{RAS}$ high to $\overline{CAS}$ low (see Note 17)	t_{RPC}	5		5		ns

Continued next page.

† Timing measurements are referenced to V_{IL} max and V_{IH} min.

NOTES: 10. In a read-modify-write cycle, $t_{d(RLWL)}$ and $t_{su(WRH)}$ must be observed. Depending on the user's transition times, this may require additional $\overline{RAS}$ low time [$t_{w(RL)}$].
11. The minimum value is measured when $t_{d(RLCL)}$ is set to $t_{d(RLCL)}$ min as a reference.
12. Either $t_{h(RHrd)}$ or $t_{h(CHrd)}$ must be satisfied for a read cycle.
13. Output Enable controlled write. Output remains in the high-impedance state for the entire cycle.
14. Read-modify-write operation only.
15. $\overline{TRG}$ must disable the output buffers prior to applying data to the DQ pins.
16. Maximum value specified only to guarantee $\overline{RAS}$ access time.
17. $\overline{CAS}$-before-$\overline{RAS}$ refresh operation only.

timing requirements over recommended ranges of supply voltage and operating free-air temperature (concluded)†

			ALT. SYMBOL	TMS44C251-1 TMS44C251-10		TMS44C251-12		UNIT
				MIN	MAX	MIN	MAX	
$t_{d(CLGH)}$	Delay time, $\overline{CAS}$ low to $\overline{TRG}$ high		t_{CTH}	25		35		ns
$t_{d(GHD)}$	Delay time, $\overline{TRG}$ high before data applied at DQ		t_{OED}	25		30		ns
$t_{d(RLTH)}$	Delay time, $\overline{RAS}$ low to $\overline{TRG}$ high	Early load	t_{RTH}	$t_{h(TRG)}$		$t_{h(TRG)}$		ns
		Mid-line load		85		90		
$t_{d(RLSH)}$	Delay time, $\overline{RAS}$ low to first SC high after $\overline{TRG}$ high (see Note 18)	Revision H	t_{RSD}	125		135		ns
		Revision I		105		115		
$t_{d(CLSH)}$	Delay time, $\overline{CAS}$ low to first SC high after $\overline{TRG}$ high (see Note 18)		t_{CSD}	35		40		ns
$t_{d(SCTR)}$	Delay time, SC high to $\overline{TRG}$ high (see Notes 18 and 19)		t_{TSL}	10		15		ns
$t_{d(THRH)}$	Delay time, $\overline{TRG}$ high to $\overline{RAS}$ high (see Note 18)		t_{TRD}	−10		−10		ns
$t_{d(SCRL)}$	Delay time, SC high to $\overline{RAS}$ low with $\overline{TRG}$ = $\overline{W}$ = low (see Notes 20 and 21)		t_{SRS}	10		10		ns
$t_{d(SCSE)}$	Delay time, SC high to $\overline{SE}$ high in serial input mode			20		20		ns
$t_{d(RHSC)}$	Delay time, $\overline{RAS}$ high to SC high (see Note 21)		t_{SRD}	25		30		ns
$t_{d(THRL)}$	Delay time, $\overline{TRG}$ high to $\overline{RAS}$ low (see Note 22)		t_{TRP}	$t_{w(RH)}$		$t_{w(RH)}$		ns
$t_{d(THSC)}$	Delay time, $\overline{TRG}$ high to SC high (see Note 22)	Revision H	t_{TSD}	35		40		ns
		Revision I		30		35		
$t_{d(THSC)}$	Delay time, $\overline{TRG}$ high to SC high (see Note 22)		t_{TSD}	35		40		ns
$t_{d(SESC)}$	Delay time, $\overline{SE}$ low to SC high (see Note 23)		t_{SWS}	10		15		ns
$t_{d(RHMS)}$	Delay time, $\overline{RAS}$ high to last (most significant) rising edge of SC before boundary switch during split read transfer cycles			25		30		ns
$t_{d(TPRL)}$	Delay time, first (TAP) rising edge of SC after boundary switch to $\overline{RAS}$ low during split read transfer cycles			20		25		ns
$t_{rf(MA)}$	Refresh time interval, memory		t_{REF}		8		8	ms
t_t	Transition time		t_T	3	50	3	50	ns

† Timing measurements are referenced to V_{IL} max and V_{IH} min.

NOTES: 18. Memory to register (read) transfer cycles only.

19. In a transfer read cycle, the state of SC when $\overline{TRG}$ rises is a Don't Care condition. However, to guarantee proper sequencing of the internal clock circuitry, there can be no positive transitions of SC for at least 10 ns prior to when $\overline{TRG}$ goes high.

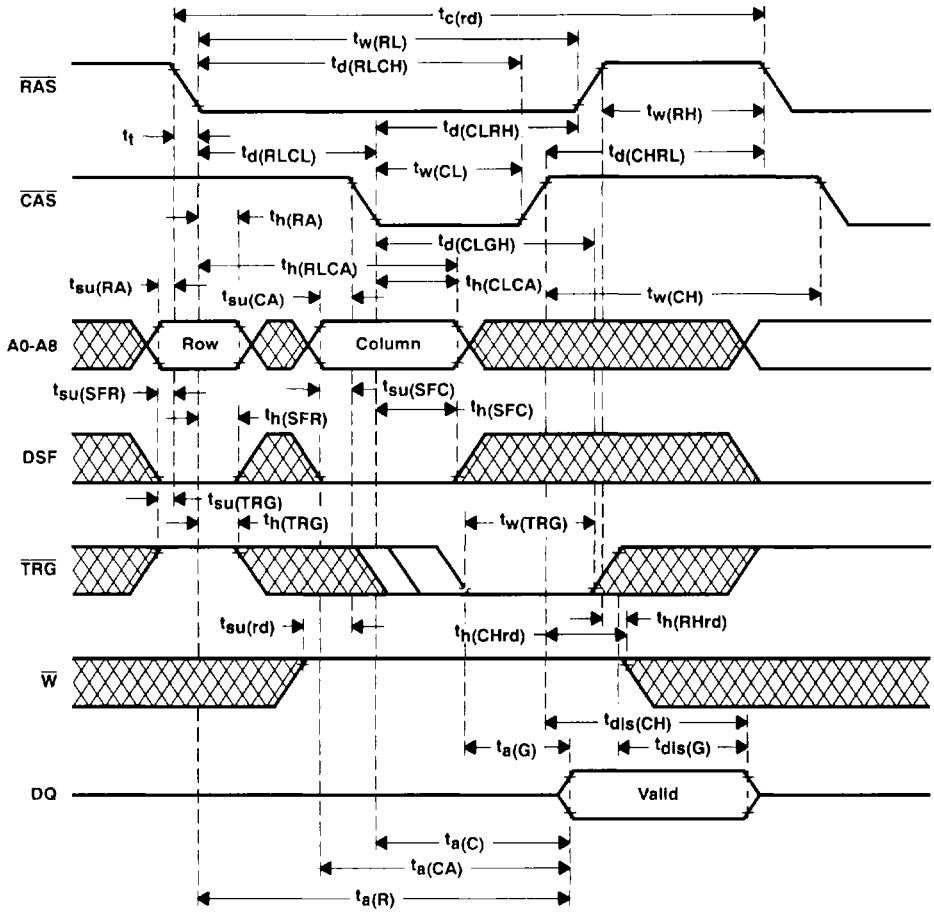
20. In a transfer write cycle, the state of SC when $\overline{RAS}$ falls is a Don't Care condition. However, to guarantee proper sequencing of the internal clock circuitry, there can be no positive transitions of SC for at least 10 ns prior to when $\overline{RAS}$ goes low.

21. Register to memory (write) transfer cycles only.

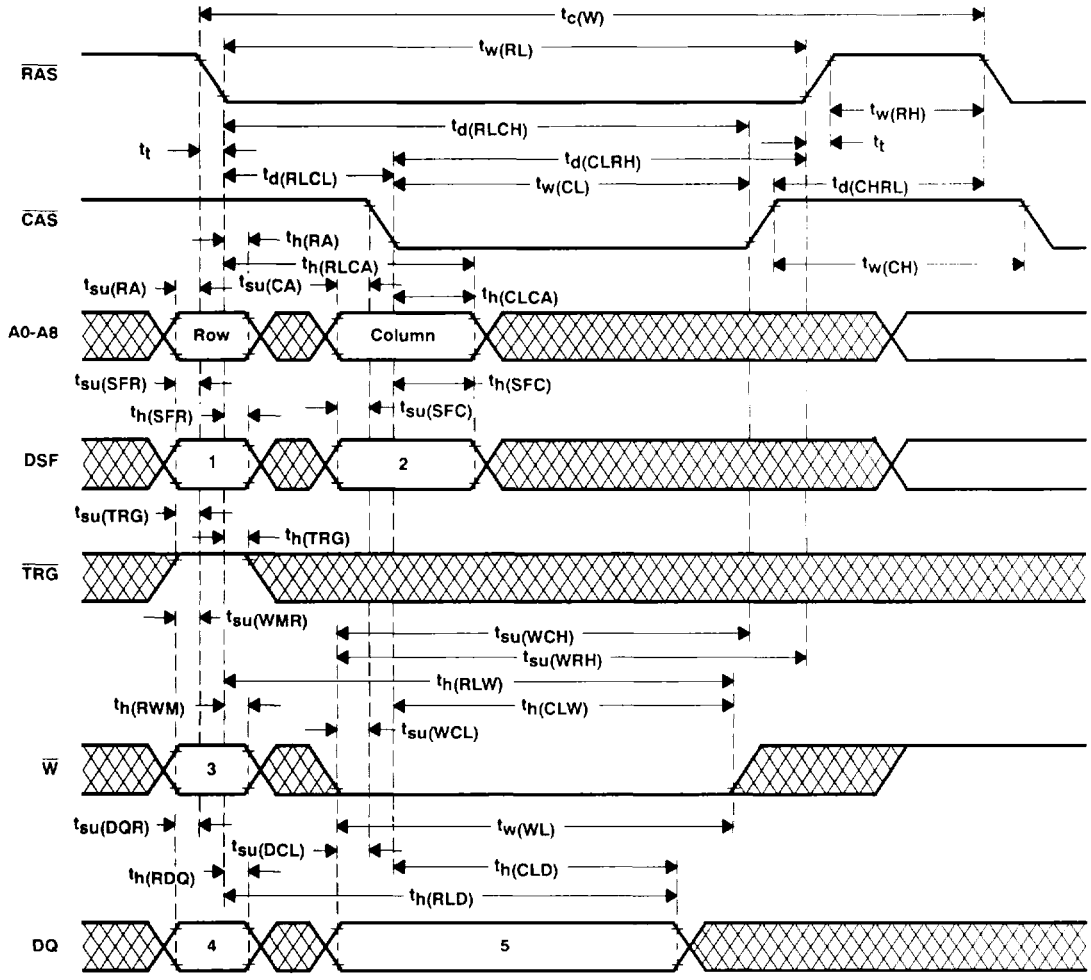
22. Memory to register (read) and register to memory (write) transfer cycles only.

23. Serial data-in cycles only.

read cycle timing

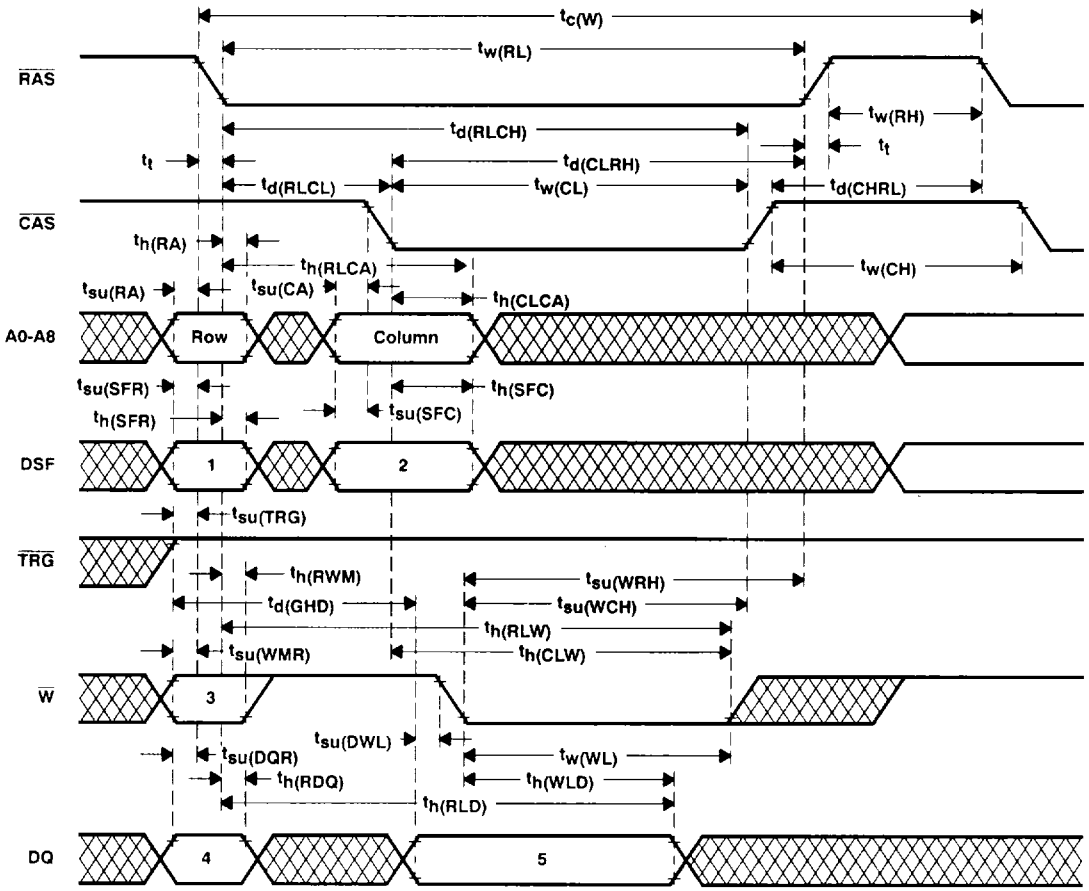


early write cycle timing



NOTE 24: See "Write Cycle State Table" for the logic state of "1", "2", "3", "4", and "5".

delayed write cycle timing

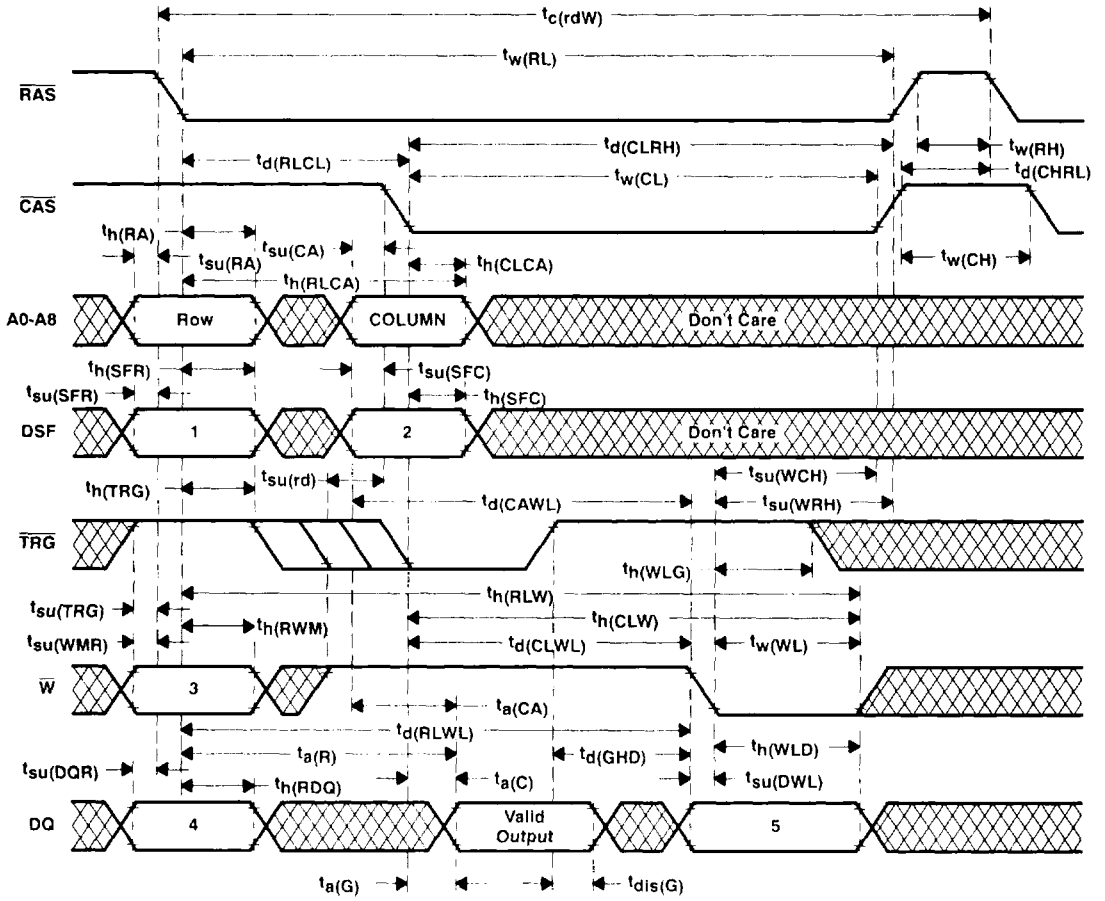


NOTE 24: See "Write Cycle State Table" for the logic state of "1", "2", "3", "4", and "5".

write cycle state table

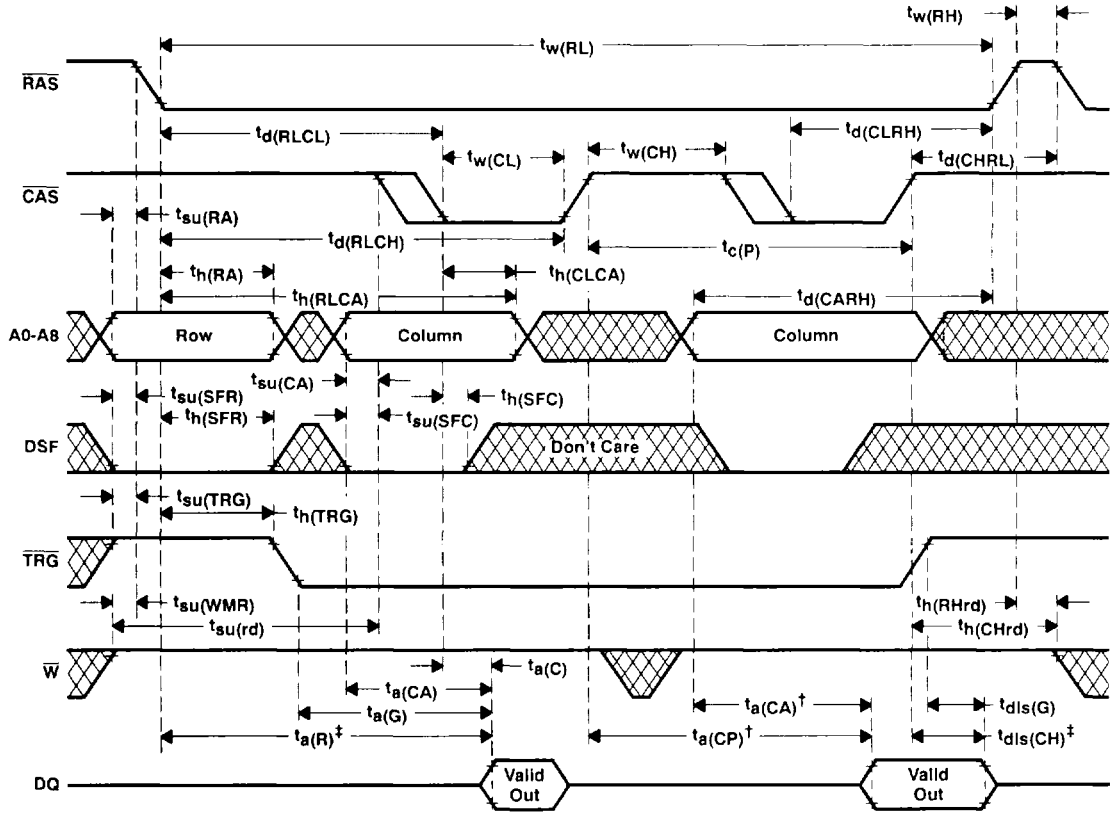
CYCLE	STATE				
	1	2	3	4	5
Write mask load/use write DQs to I/Os	L	L	L	Write Mask	Valid Data
Write mask load/use block write	L	H	L	Write Mask	Addr Mask
Use previous write mask, write DQs to I/Os	H	L	L	Don't Care	Valid Data
Use previous write mask, block write	H	H	L	Don't Care	Addr Mask
Load write mask on later of $\overline{W}$ fall and $\overline{CAS}$ fall	H	L	H	Don't Care	Write Mask
Load color register on later of $\overline{W}$ fall and $\overline{CAS}$ fall	H	H	H	Don't Care	Color Data
Write mask disabled, block write to all I/Os	L	H	H	Don't Care	Addr Mask
Normal early or late write operation	L	L	H	Don't Care	Valid Data

read-write/read-modify-write cycle timing



NOTE 25: See "Write Cycle State Table" for the logic state of "1", "2", "3", "4", and "5". Same logic as delayed write cycle.

enhanced page-mode read cycle timing

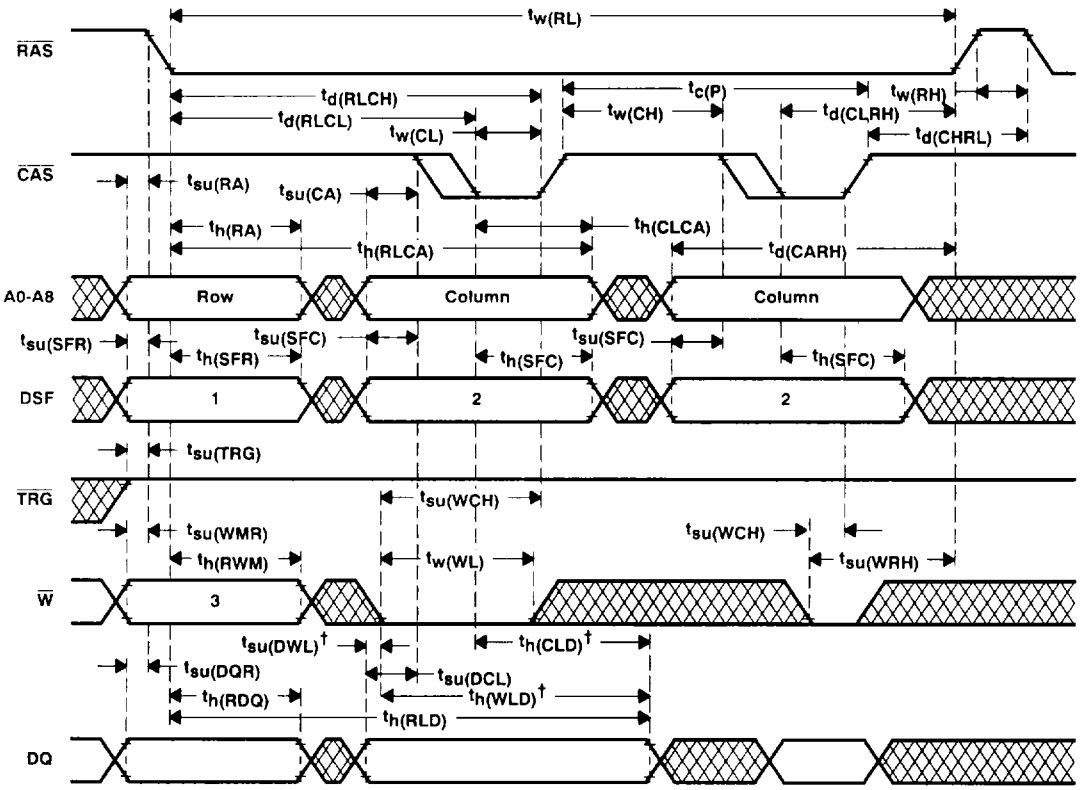


† Access time is $t_{a(CP)}$ or $t_{a(CA)}$ dependent.

‡ Output may go from high-impedance state to an invalid data state prior to the specified access time.

NOTE 26: A write cycle or a read-modify-write cycle can be mixed with the read cycles as long as the write and read-modify-write timing specifications are not violated and the proper polarity of DSF is selected on the falling edges of $\overline{RAS}$ and $\overline{CAS}$ to select the desired write mode (normal, block write, etc.)

enhanced page-mode write cycle timing

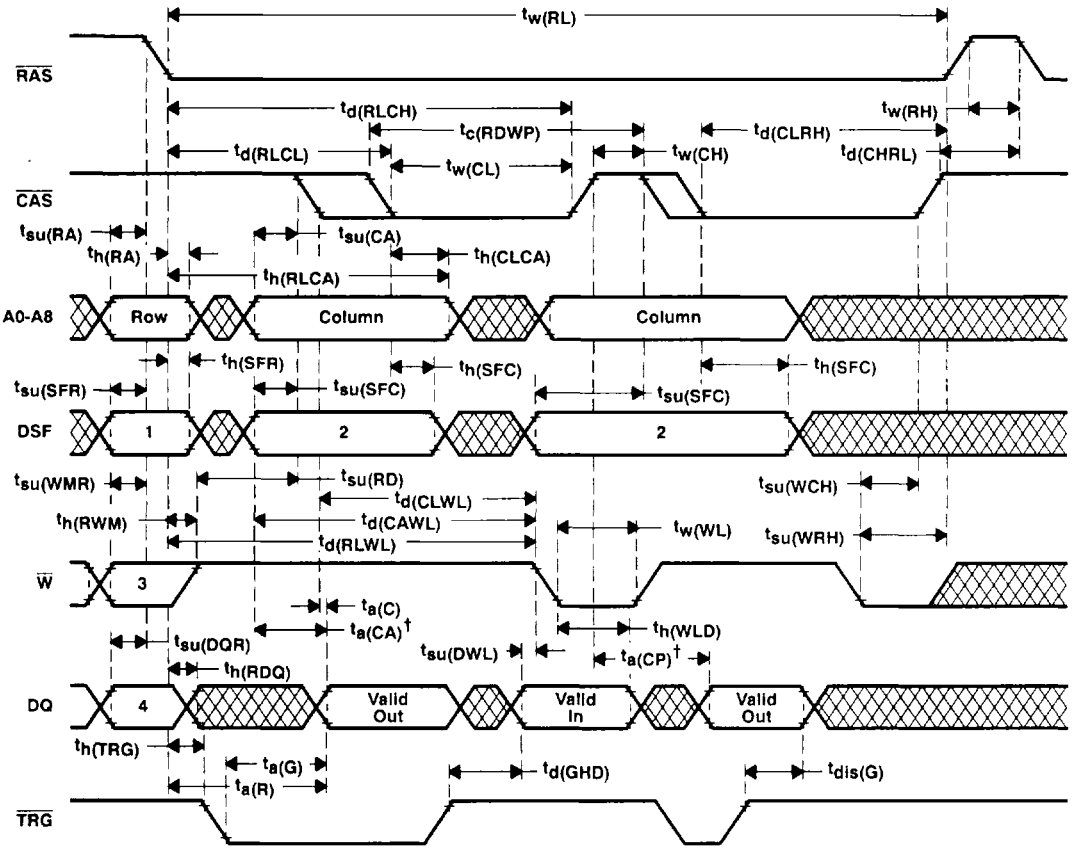


† Referenced to $\overline{CAS}$ or $\overline{W}$, whichever occurs last.

NOTES: 24. See "Write Cycle State Table" for the logic state of "1", "2", "3", "4", and "5".

27. A read cycle or a read-modify-write cycle can be intermixed with write cycles, observing read and read-modify-write timing specifications. $\overline{TRG}$ must remain high throughout the entire page-mode operation if the late write feature is used, to guarantee page-mode cycle time. If the early write cycle timing is used, the state of $\overline{TRG}$ is a Don't Care after the minimum period $t_{h(TRG)}$ from the falling edge of $\overline{RAS}$.

enhanced page-mode read-modify-write cycle timing

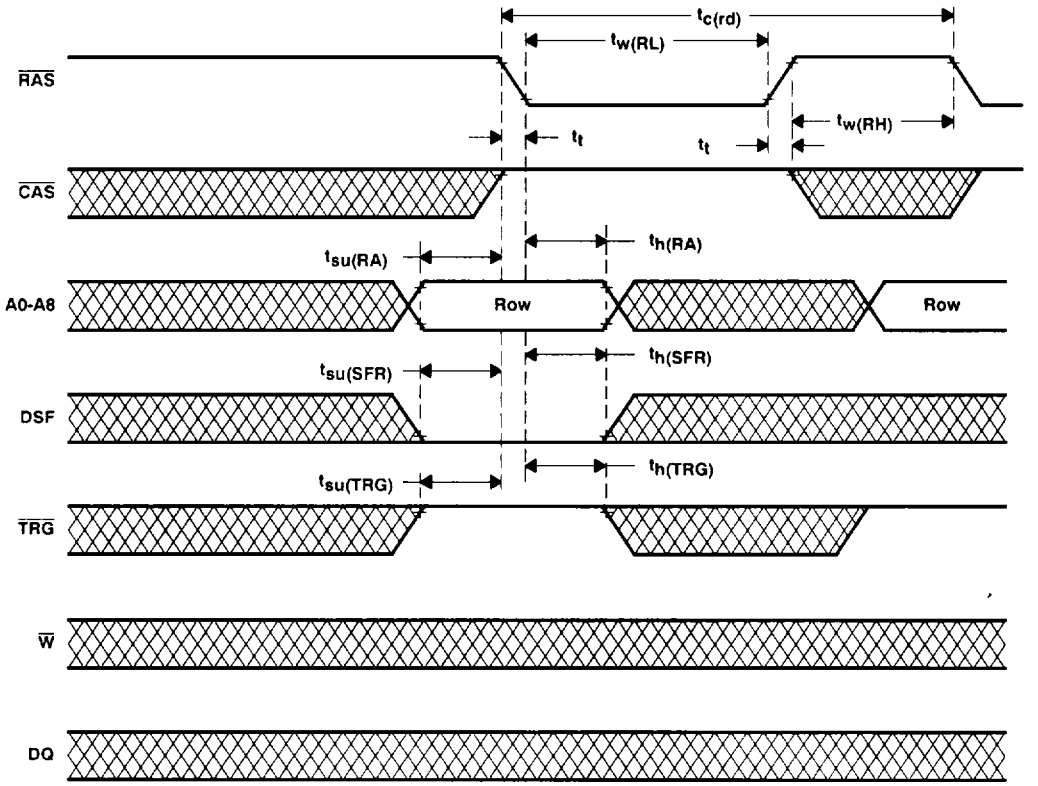


† Output may go from the high-impedance state to an invalid data state prior to the specified access time.

NOTES: 24. See "Write Cycle State Table" for the logic state of "1", "2", "3", "4", and "5".

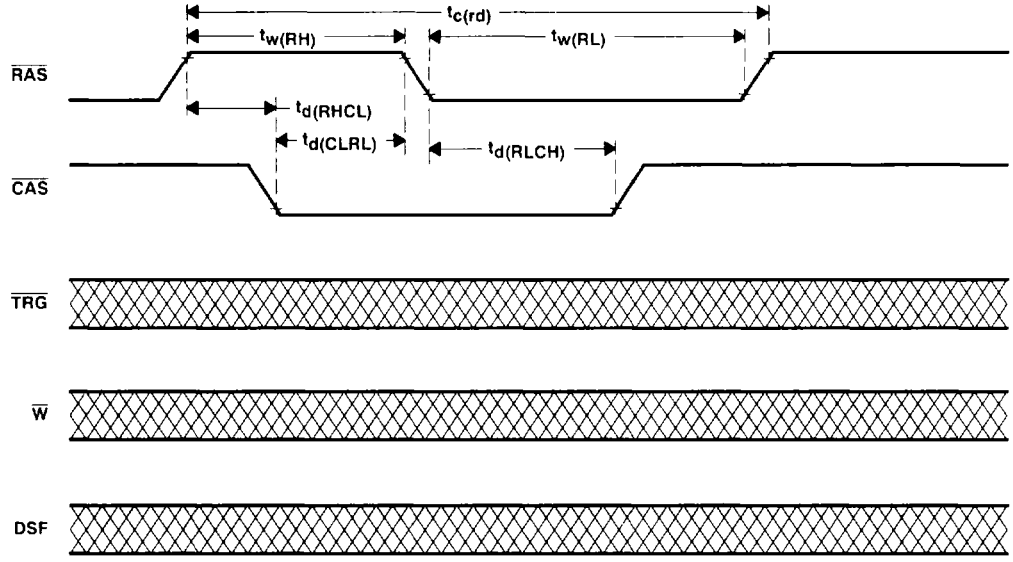
28. A read or a write cycle can be intermixed with read-modify-write cycles as long as the read and write timing specifications are not violated.

RAS-only refresh timing



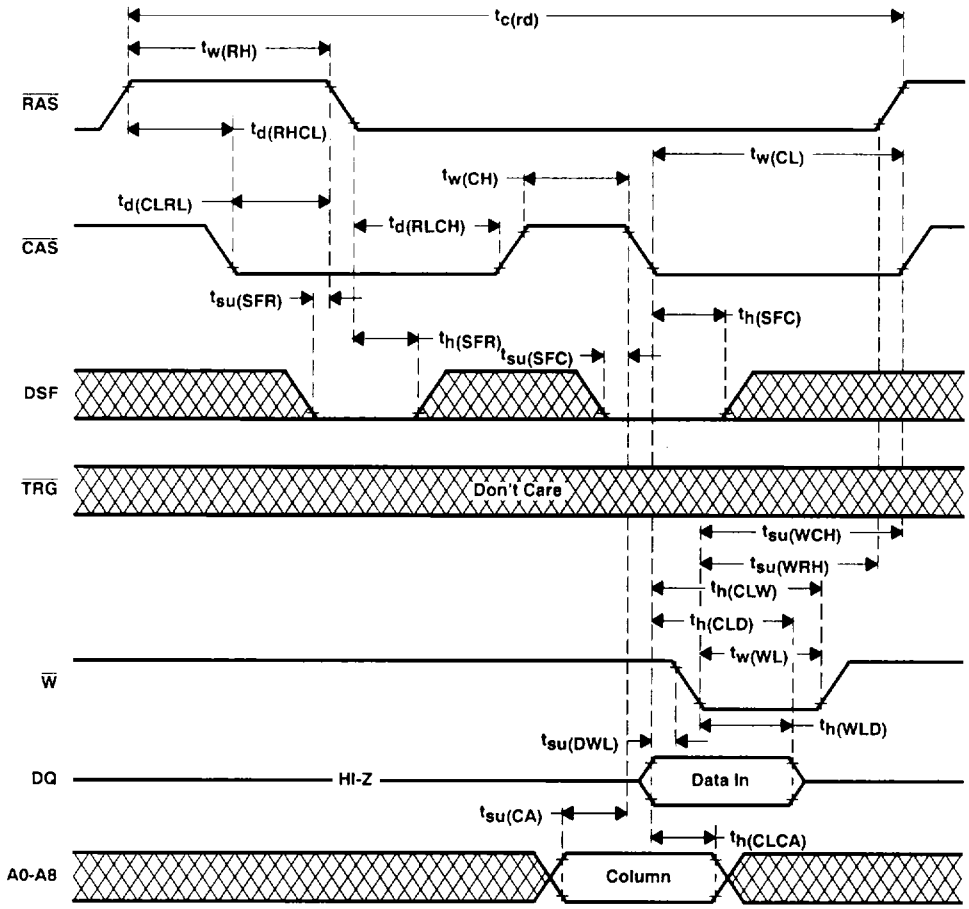
NOTE 29: In persistent write-per-bit function, W must be high during the refresh cycles

$\overline{CAS}$-before-$\overline{RAS}$ refresh

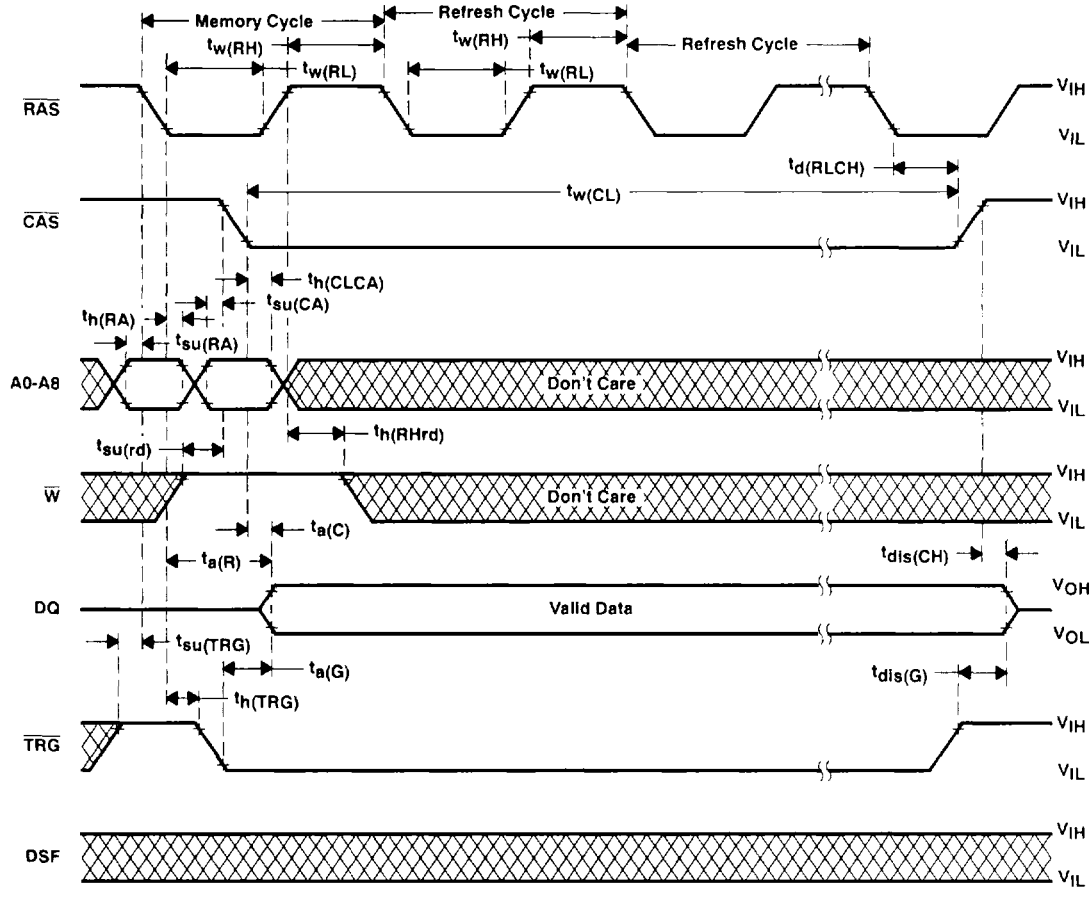


NOTE 29: In persistent write-per-bit function, $\overline{W}$ must be high during the refresh cycles.

CAS-before-RAS refresh counter test timing

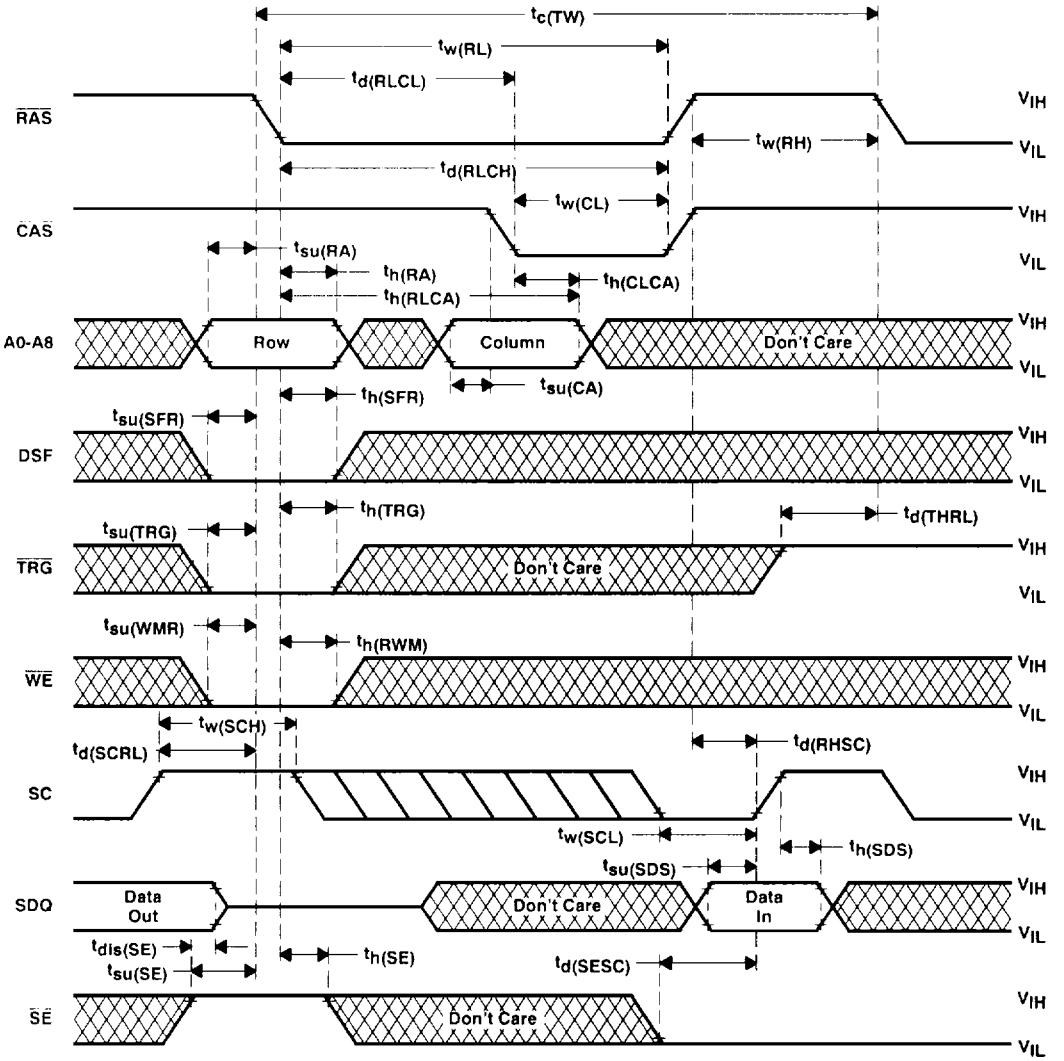


hidden refresh cycle timing



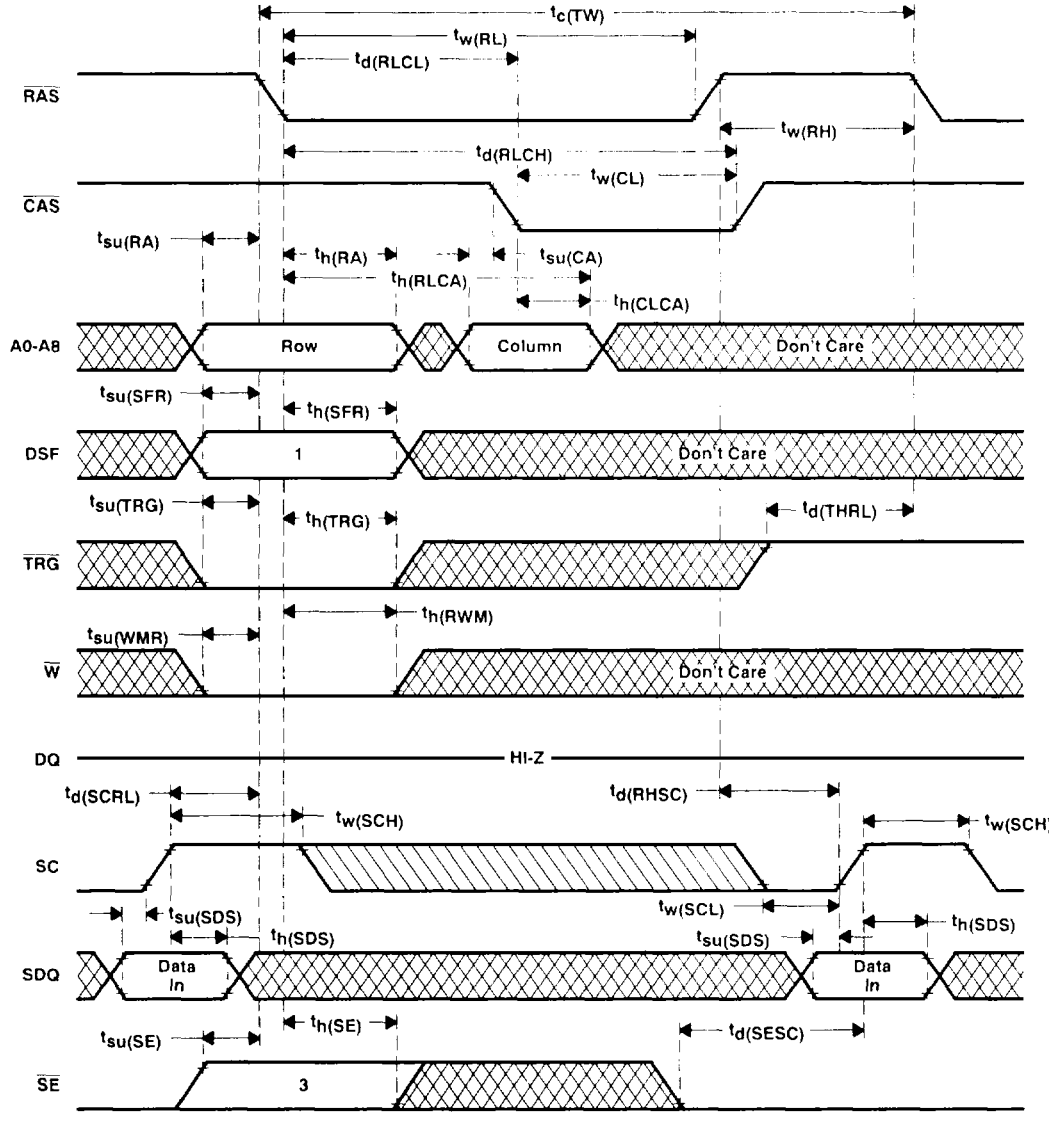
write-mode control pseudo write transfer timing

The write-mode control cycle is used to change the SDQs from the output mode to the input mode. This allows serial data to be written into the data register. The diagram below assumes that the device was originally in the serial read mode.



NOTES: 30. Random-mode Q outputs remain in the high-impedance state for the entire write-mode control.
31. $\overline{SE}$ must be high as $\overline{RAS}$ falls in order to perform a write-mode control cycle.

data register to memory timing, serial input enabled



NOTES: 32. Random mode Q outputs remain in the high-impedance state for the entire data register to memory transfer cycle. This cycle is used to transfer data from the data register to the memory array. Every one of the 512 locations in each data register is written into the corresponding 512 columns of the selected row. Data in the data register may proceed from a serial shift-in or from a parallel load from one of the memory array rows. The above diagram assumes that the device is in the serial write mode (i.e., SD is enabled by a previous write mode control cycle, thus allowing data to be shifted-in).

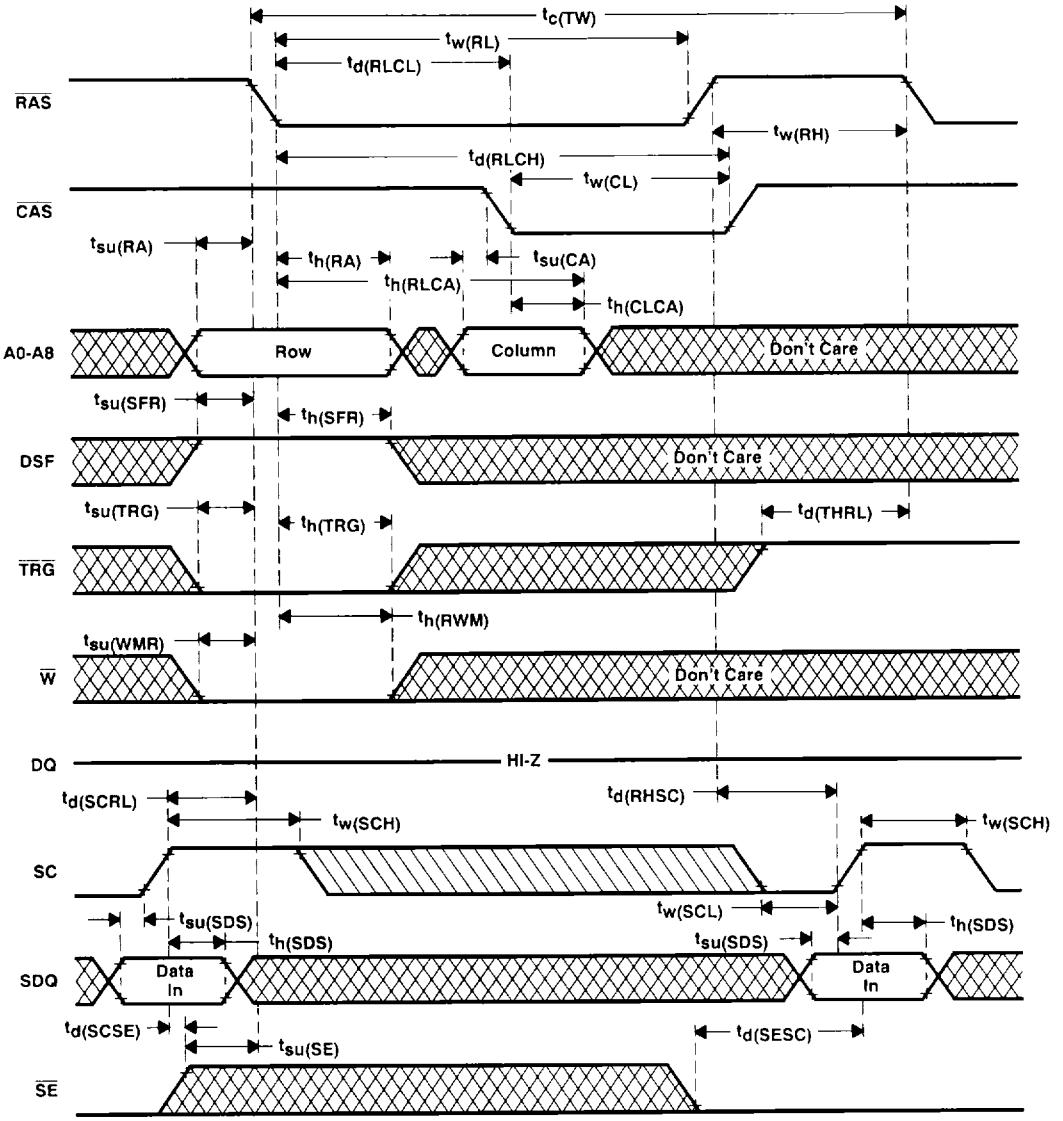
33. See "Register Transfer Function Table" for logic state of "1" and "3".

34. Successive transfer writes can be performed without serial clocks for applications requiring fast memory array clears.

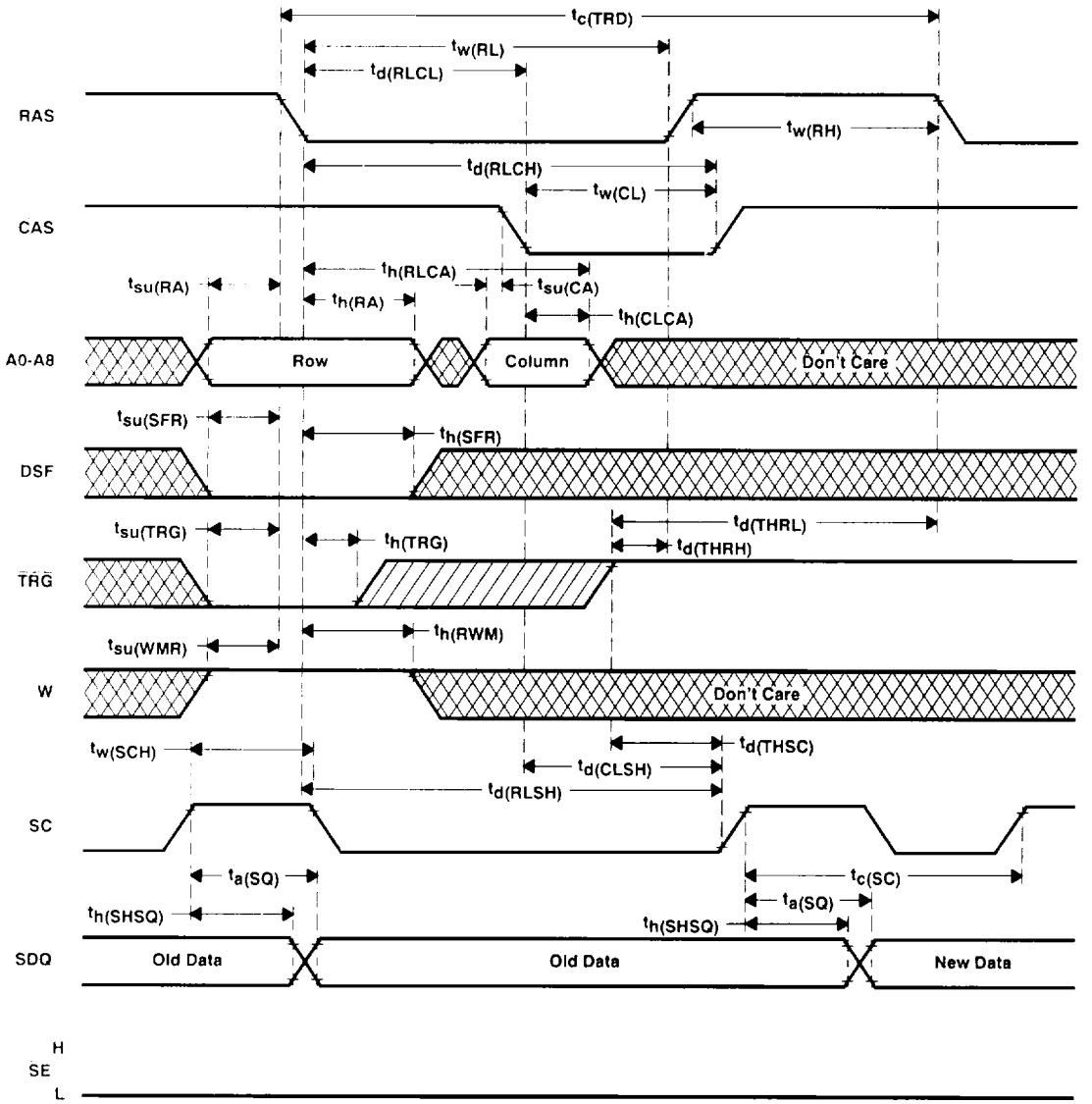
register transfer function table

FUNCTION	RAS FALL			
	$\overline{TRG}$	$\overline{W}$	DSF (1)	$\overline{SE}$ (3)
Register to memory transfer, serial input enabled, serial write mode enable	L	L	X	L
Register to memory transfer, alternate transfer write, serial write mode enable	L	L	H	X
Pseudo-transfer SDQ control, serial write mode enable	L	L	L	H
Memory to register transfer	L	H	L	X
Split-register transfer	L	H	H	X

alternate data register to memory timing



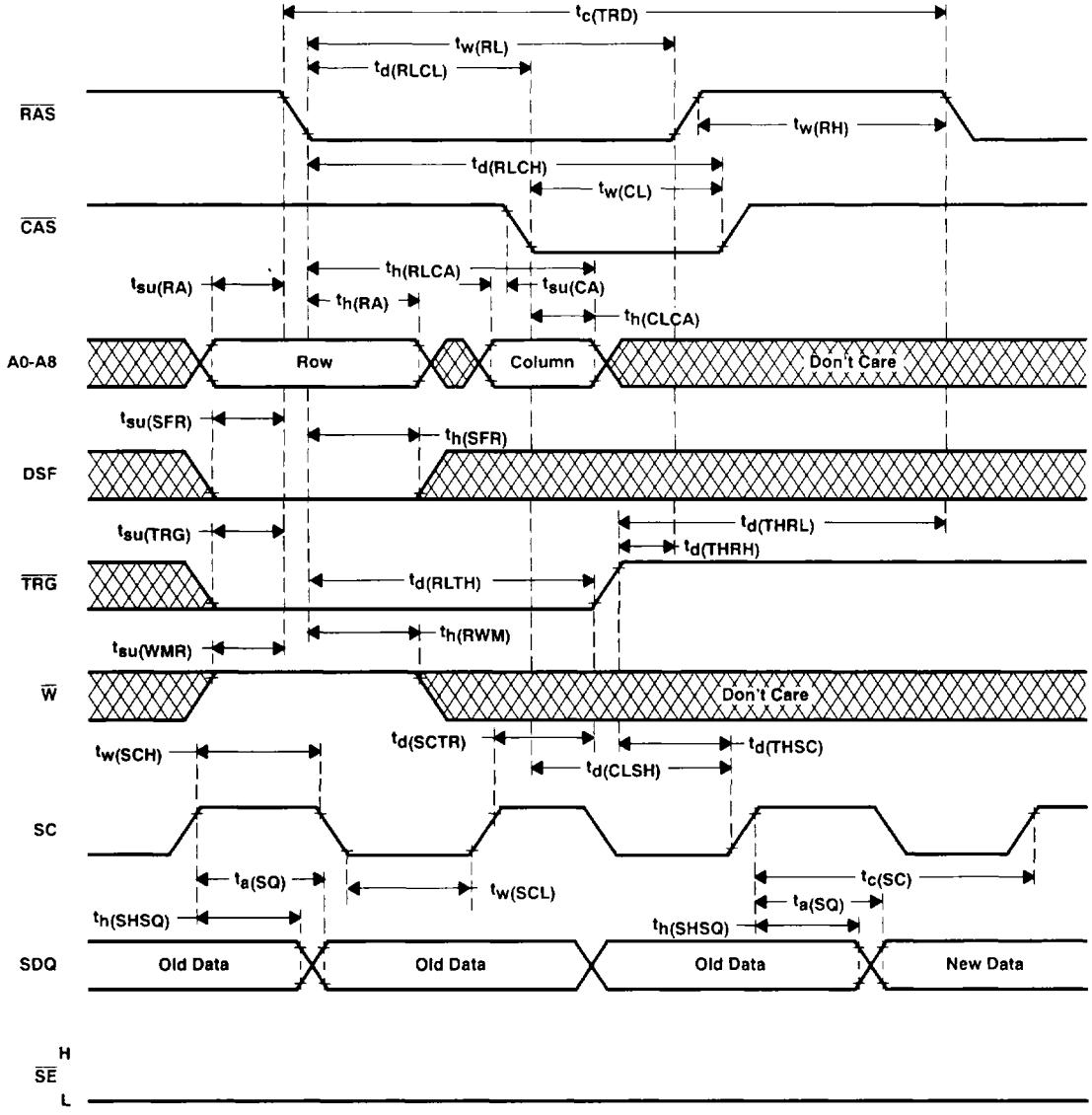
memory to data register transfer timing, early load operation



NOTES: 35. Random mode (Q outputs) remain in the high-impedance state for the entire memory to data register transfer cycle. The memory to data register transfer cycle is used to load the data registers in parallel from the memory array. The 512 locations in each data register are written into from the 512 corresponding columns of the selected row. The data that is transferred into the data registers may be either shifted out or transferred back into another row.

36. Once data is transferred into the data registers, the SAM is in the serial read mode (i.e., the SQ is enabled), thus allowing data to be shifted out of the registers. Also, the first bit to be read from the data register after $\overline{TRG}$ has gone high must be activated by a positive transition of SC.

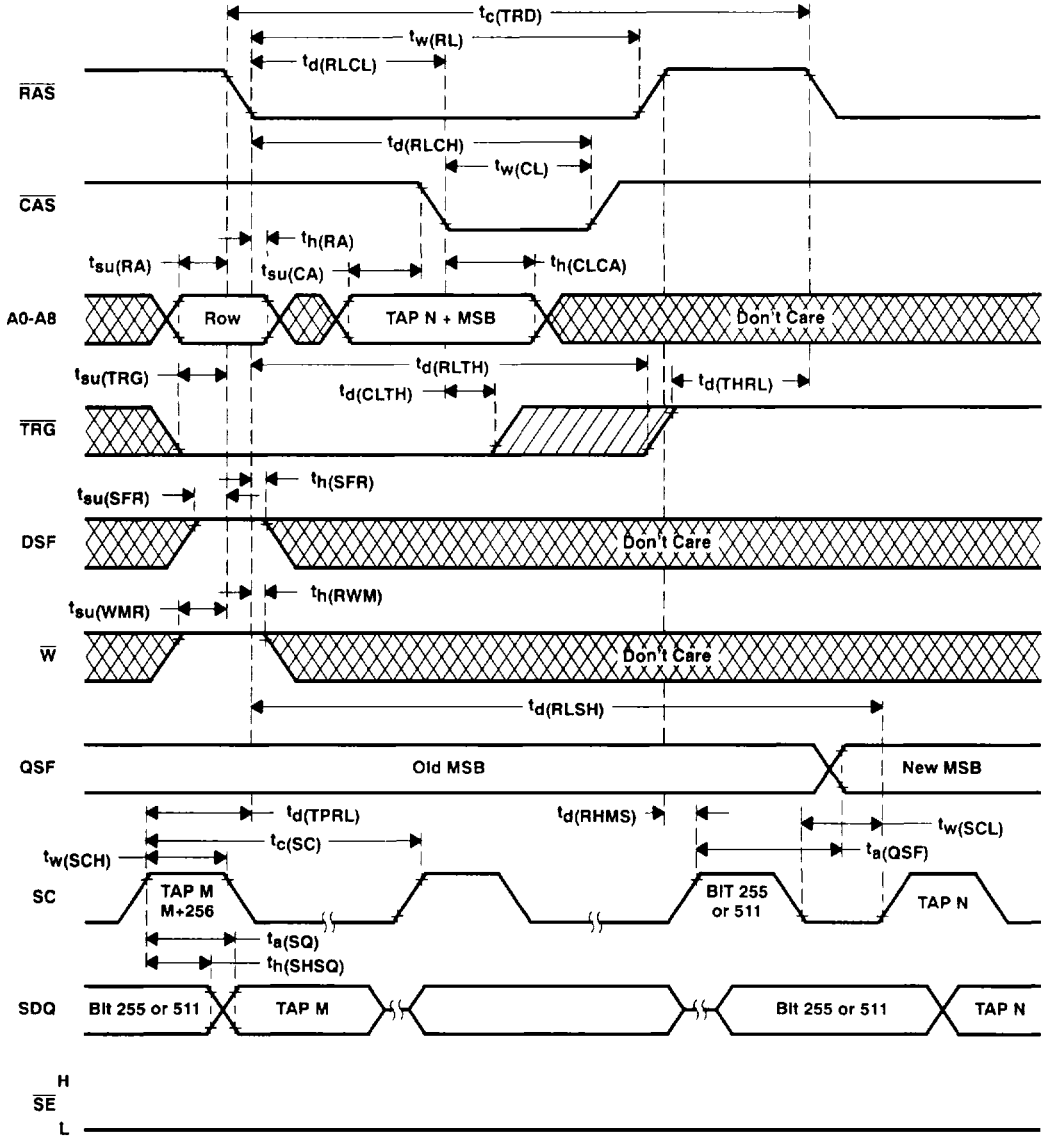
memory to data register transfer timing, mid-line load operation



NOTES: 35. Random mode (Q outputs) remain in the high-impedance state for the entire memory to data register transfer cycle. The memory to data register transfer cycle is used to load the data registers in parallel from the memory array. The 512 locations in each data register are written into from the 512 corresponding columns of the selected row. The data that is transferred into the data registers may be either shifted out or transferred back into another row.

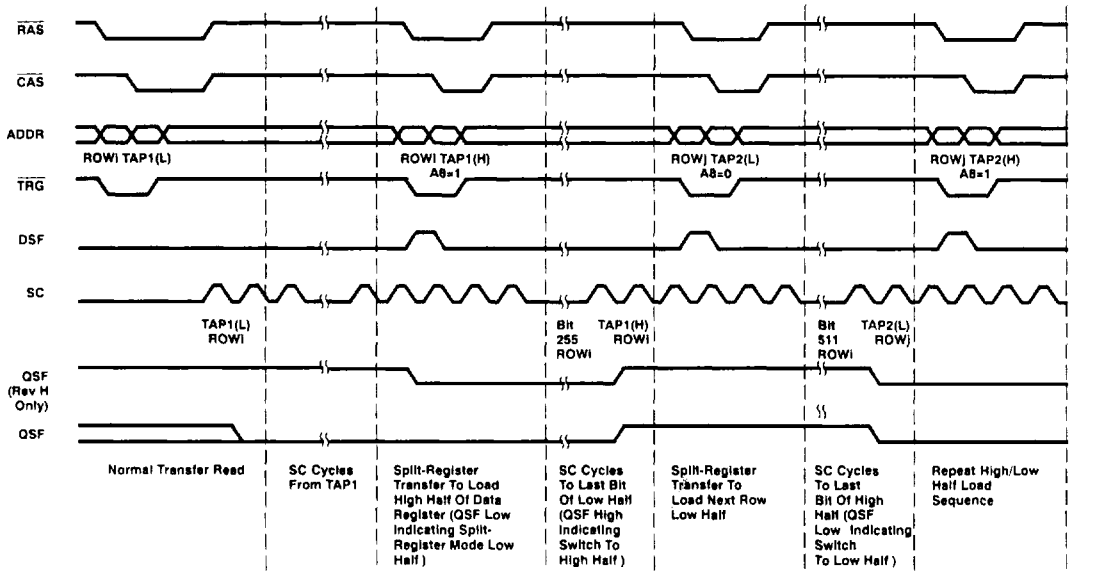
36. Once data is transferred into the data registers, the SAM is in the serial read mode (i.e., the SQ is enabled), thus allowing data to be shifted out of the registers. Also, the first bit to be read from the data register after $\overline{TRG}$ has gone high must be activated by a positive transition of SC.

split-register mode read transfer timing



NOTE 37: There must be a minimum of two SC clocks cycle between any two split-register reload cycles, and a minimum of one SC clock cycle between a transfer read cycle and a split-register cycle.

split-register operating sequence

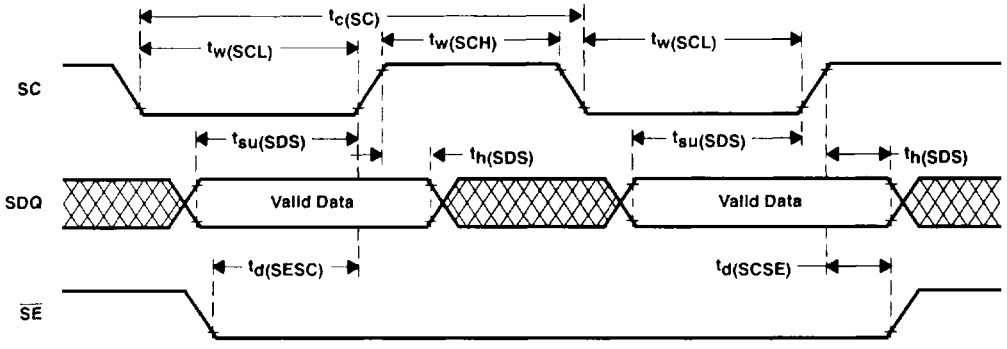


NOTES: 38. In the split-register mode, data can be transferred from different rows to the low and high halves of the data register.
39. When enabling or disabling the split-register mode, $t_{a(QSF)}$ is measured from $\overline{RAS}$ low in the transfer cycle.

application notes

1. In order to achieve proper split-register operation, a normal read transfer, followed by a minimum of one serial clock cycle should be performed before the first split-register transfer cycle. This is necessary to initialize the data register and the starting tap location. Serial access can then begin after the normal transfer cycle.
2. A split-register transfer into the inactive half is not allowed until $t_{d(TPRL)}$ is met. $t_{d(TPRL)}$ is the minimum delay time between the rising edge of the serial clock (SC) of the previously loaded tap point and the falling edge of $\overline{RAS}$ of the split-register transfer cycle into the inactive half.
3. After $t_{d(TPRL)}$ is met, the split-register transfer into the inactive half must also satisfy the $t_{d(RHMS)}$ condition. $t_{d(RHMS)}$ is the minimum delay time between the rising edge of $\overline{RAS}$ of the split-register transfer cycle into the inactive half and the rising edge of the last serial clock (SC 255 or 511) of the active half.

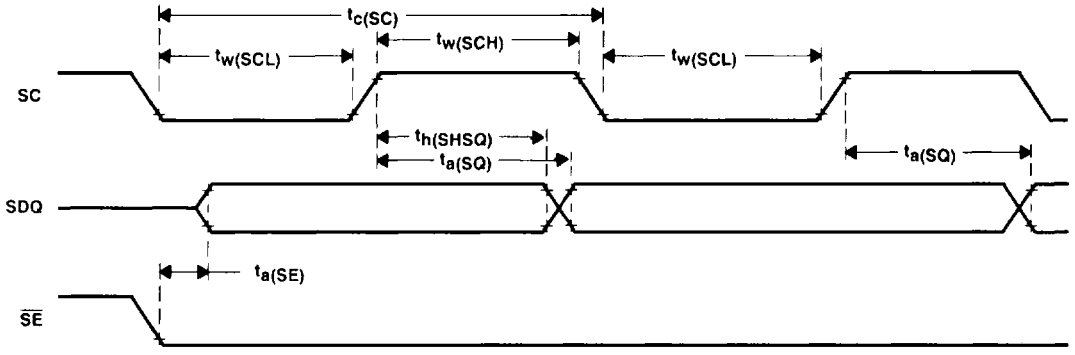
serial data-in timing



The serial data-in cycle is used to input serial data into the data registers. Before data can be written into the data registers via SD, the device must be put into the write mode by performing a write mode control (pseudo-transfer) or any transfer write cycle. A transfer read cycle is the only cycle that will take the device out of the write mode and put it into the read mode, thus disabling the input of data. Data will be written starting at the location specified by the input address loaded on the previous transfer cycle.

While accessing data in the serial data registers, the state of $\overline{TRG}$ is a Don't Care as long as $\overline{TRG}$ is held high when $\overline{RAS}$ goes low to prevent data transfers between memory and data registers.

serial data-out timing

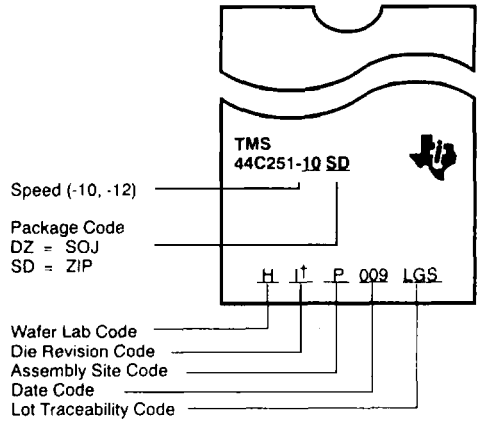


NOTES: 8. For mid-line load, $t_{c(SC)}$ = 50 ns for Revision I and subsequent revisions; $t_{c(SC)}$ = 55 ns for Revision H only. For split-register, $t_{c(SC)}$ = 40 ns for Revision H only.

40. While reading data through the serial data register, the state of $\overline{TRG}$ is a Don't Care as long as $\overline{TRG}$ is held high when $\overline{RAS}$ goes low. This is to avoid the initiation of a register to memory or memory to register data transfer operation.

The serial data-out cycle is used to read data out of the data registers. Before data can be read via SQ, the device must be put into the read mode by performing a transfer read cycle. Transfer write cycles occurring between the transfer read cycle and the subsequent shifting out of data will not take the device out of the read mode. But a write mode control cycle at that time will take the device out of the read mode and put it in the write mode, thus not allowing the reading of data.

device symbolization



† For information on Revision "H" devices, refer to page 8-43.