MC 9020

Micro Channel
Bus Master Interface Chip
for Intel 82596 Ethernet Controller

December 1991

T-52-33-55

Features

- Micro Channel Bus Master Interface for Intel 82596 Ethernet Controller
- Supports Micro Channel Streaming Data rates to 40 MBytes/sec
- BIOS PROM and Node ID PROM support
- Clock to 40 MHz
- Direct connect to System Bus of all Host Interface Control Signals
- Low power CMOS in 128 Pin Plastic QFP Package

General Description

The MC 9020 is designed to provide the most compact, inexpensive and highest performance Micro Channel bus interface for Bus Master adapter boards that use the Intel 82596 Ethernet Controller.

Use of the 90X0 series of chips minimizes hardware and software development costs and time because similar adapter hardware and driver designs can be used for either AT, EISA or Micro Channel applications.

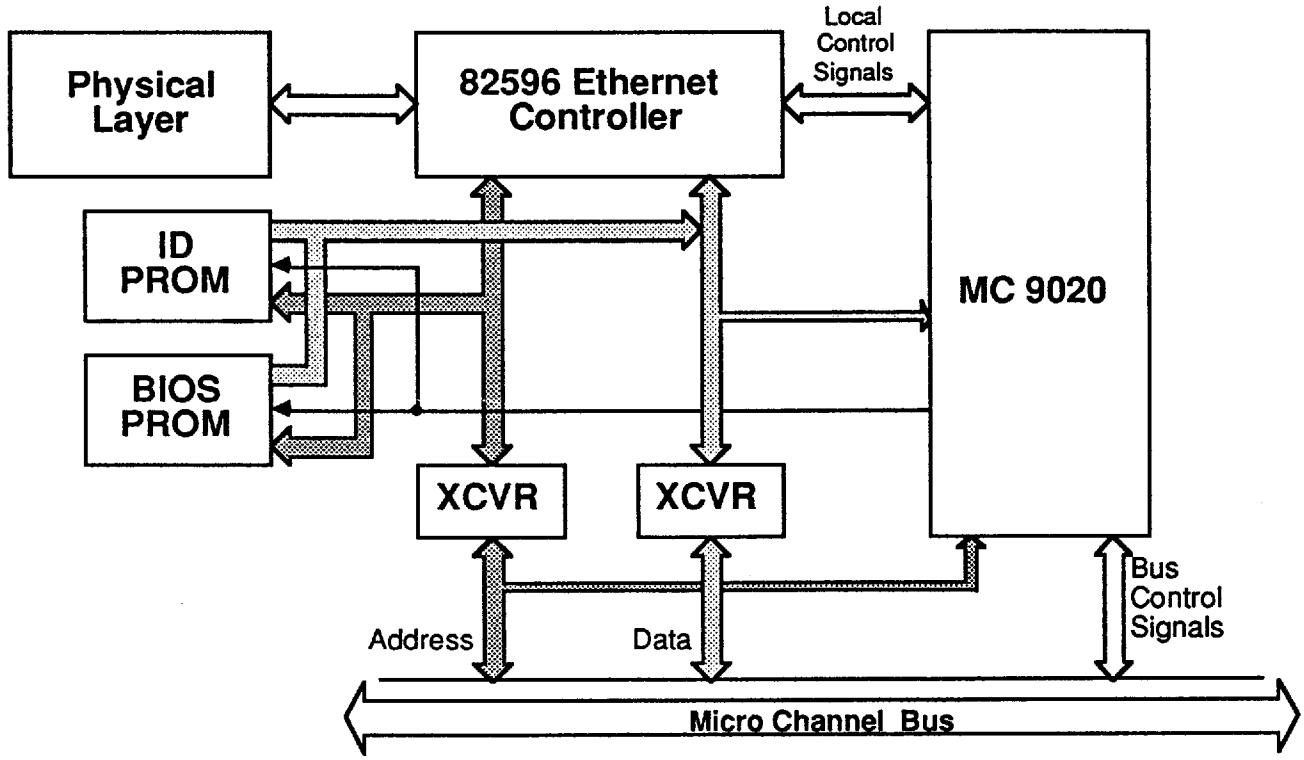

FIGURE 1. Typical Adapter Block Diagram

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SECTION 1 - INTRODUCTION

SIGNIFICANT CHANGES HAVE BEEN MADE TO DECEMBER 1990 UP TO NOVEMBER 1991 VERSIONS OF THE DATA SHEET. THE CHANGES ARE SUMMARIZED BELOW.

1. PINOUT CHANGES:

   -Pin 126 changed from TR32 to NC

   -Pin 62 Changed from -BS16 to LTR32

2. LAN BOARD CIRCUIT CHANGES (FIGURE 3):

   -Connect LTR32 to input of -244. Output of -244 is Micro Channel TR32

   -If Boot PROM is used on the board, M/-IO should connect to Micro Channel through a -243, gated by HOST/OWN. If Boot PROM is not on board, M/-IO may be connected directly to Micro Channel.

   -The -LBE3 output of the 82596 should be connected to the LBE3 input of the MC 9020 through an inverter.

   - The MC 9020 output LTR32 should be connected to the -BS16 input to the 82596 through an inverter.

3. POS REGISTER CHANGES:

   -POS 103 bit 6 polarity has been reversed.

   -Register 15 bit 7 is now reserved.

4. Pin 77 is now USER_PIN 3 instead of USER_PIN 2 and pin 78 is now USER_PIN 2 instead of USER_PIN 3.

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MC 9020 GENERAL DESCRIPTION

The MC 9020 is designed to provide the most compact, inexpensive and highest performance Micro Channel bus interface for Bus Master adapters that use the Intel 82596 Ethernet Controller Chip. Adapters which use the MC 9020 and the 82596 can achieve up to eight times the system bus transfer rate of a typical sixteen bit DMA slave LAN board and can be competitive in cost. LAN performance is also enhanced by the more efficient protocol processing capabilities of the 82596. Furthermore, a bus master frees the host processor from managing bus data transfer operations, which improves overall system performance.

MC 9020 FUNCTIONS

The MC 9020 is a 128 pin plastic QFP CMOS Micro Channel bus master interface chip. MC 9020 major functions include:

1. **Master Control Signal Protocol Converter.** The chip converts all the handshakes of the 82596 to Micro Channel bus master handshakes.
2. **Slave controller.** The MC 9020 includes a Micro Channel slave interface for control of adapter board slave functions.
3. **Arbitration with PREEMPT timer.** The MC 9020 contains a 16 level arbiter. The chip also has a timer which can be programmed to release the bus at a maximum of 4.0 or 6.8 microseconds after an external PREEMPT.
4. **Address decoder.** The MC 9020 decodes host address bits A16-A8, A4-A0 and contains an enable pin for an external A31-A17 or A24-A17 address decoder. The MC 9020 decodes these addresses to generate BIOS PROM, NODE ID PROM, CA and PORT selects and to configure and read POS registers.
5. **Interrupt generator.** The MC 9020 can generate one of four host interrupts from one local interrupt, programmable through POS registers.
6. **External Buffer Controller.** The MC 9020 generates all buffer enable, clocking and direction signals for external address and data transceivers or buffers.
7. **Clock.** The MC 9020 runs from a crystal or TTL oscillator and can generate a clock up to 40 MHz for external and internal use.
8. **User programmable configuration bits.** The MC 9020 provides up to four external bits which can be configured through POS registers.
9. **Bus drivers.** All Micro Channel control signals generated by the MC 9020 drive the bus directly, without requiring external drivers. Address and data signals do require buffers or transceivers.
10. **POS Registers.** The MC 9020 supports POS registers 100 through 105 (102 through 105 are internal).
11. **HOLD Release idle timer.** The MC 9020 will retain control of the bus for approximately 800 ns if the 82596 reasserts HOLD for a pre-fetch operation.
12. **Adapter ID number in Node ID PROM.** The adapter ID number is mapped into I/O address space to allow the option to implement the adapter ID number in the Node ID PROM, which reduces board component count.

POS Register Contents

Included in the POS registers are the board ID, interrupt request level, Data size, I/O address decode bits, PROM address decode bits, arbitration priority, Channel Check indicator and Data Streaming indicator. The MC 9020 also provides four external user bits for application specific configuration information.

The MC 9020 also contains an 8 bit register (Register 15) which is used to flag and control interrupt, reset and error conditions.

Data Transfer Modes

The MC 9020 supports both 16 and 32 bit Burst and Streaming Data Transfers. In addition, the MC 9020 supports Micro Channel slave bus cycles for initialization of CA and PORT accesses and access to other adapter board slave devices such as BIOS PROM, Node ID PROM or other memory and I/O functions.

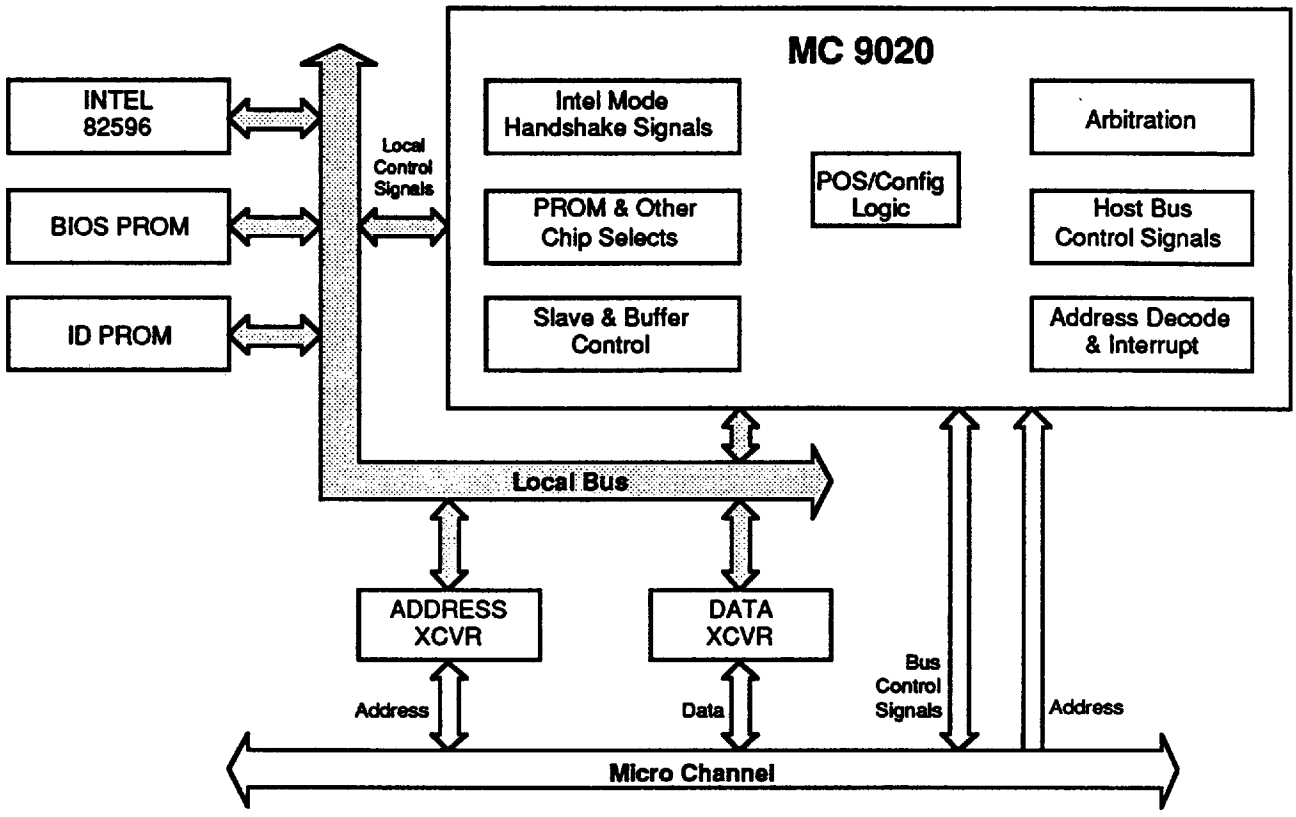

FIGURE 2. MC 9020 Functional Block Diagram

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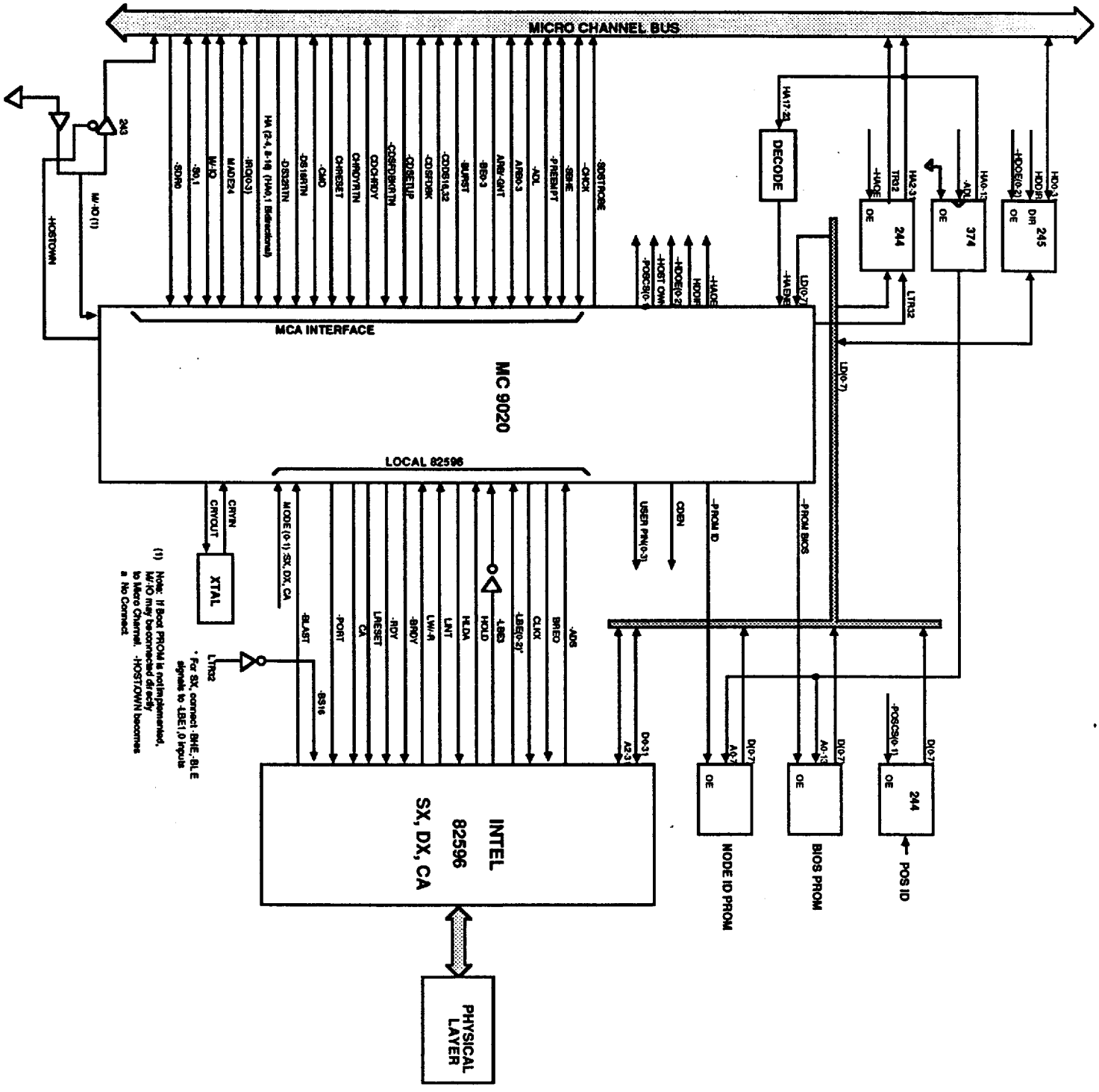

Figure 3. Low cost, Micro Channel Direct Bus Master Adapter Board

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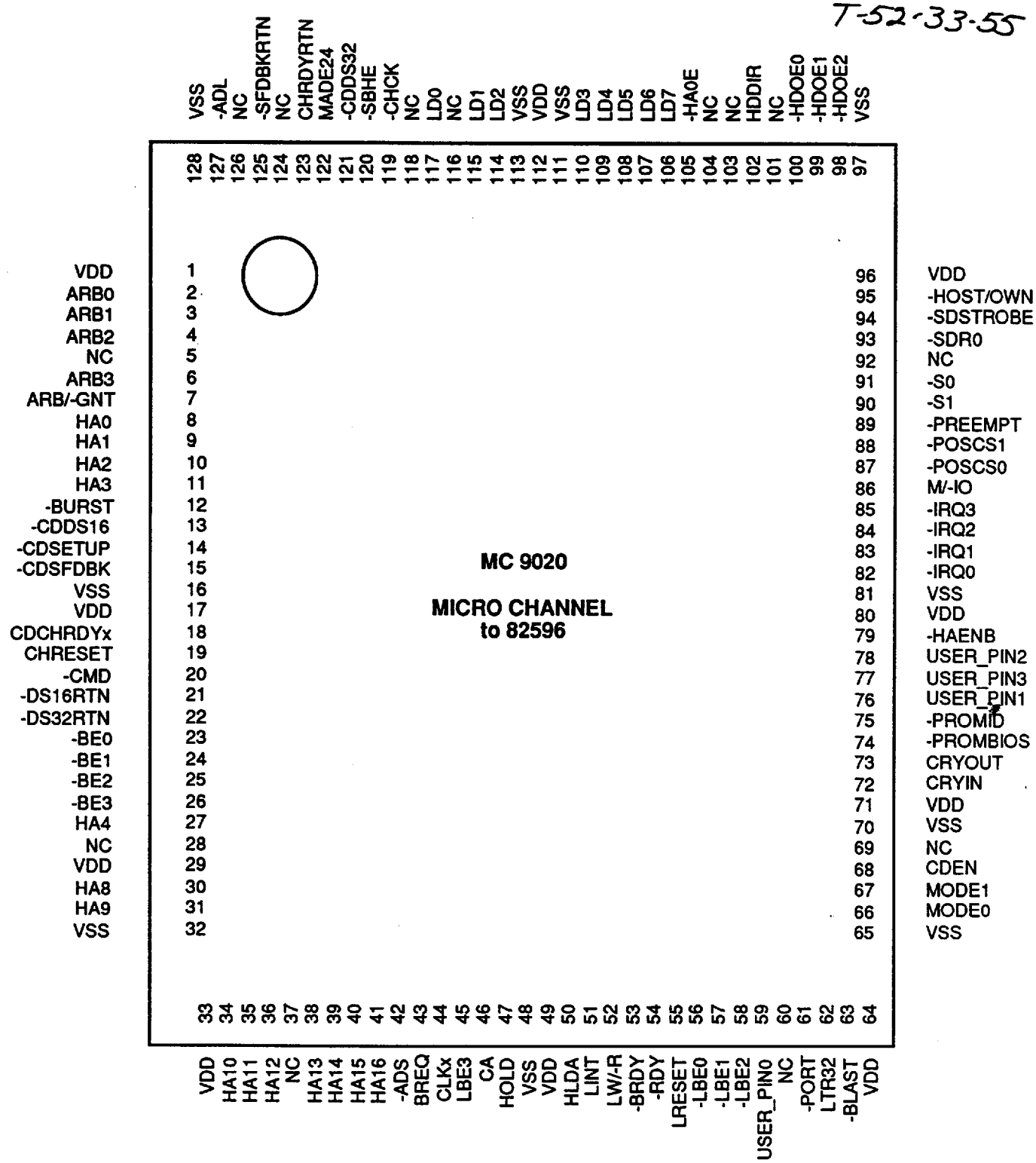

FIGURE 4. Pin Out

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SECTION 2 - REGISTER DESCRIPTION

Table 2.1 summarizes the POS register locations of the MC 9020. The "I" registers are internal to the chip. The "E" registers are external components which contain the adapter board ID.

Table 2.1 Register Summary

Register Number	Register Description
0	E - ID Byte 0 (POS 100)
1	E - ID Byte 1 (POS 101)
2	I - Config 0 (POS 102)
3	I - Config 1 (POS 103)
4	I - Config 2 (POS 104)
5	I - Config 3 (POS 105)
15	I - Config 15 (Transfer Status)

The four configuration (POS) registers may be accessed through a normal I/O decode as well as the Micro Channel Card Setup routine. Register 15, the transfer status register, is accessed through an I/O decode only.

The Adapter ID number is mapped into I/O space to allow the option to implement the adapter ID number in the ID PROM.

Address Decode Table

A15-A8	A7-A5	A4	A3-A0	
BASE (See POS 103)	XXX	0	0000-0001	- Adapter ID Number
BASE (See POS 103)	XXX	0	0010	- Config. 0 Register (POS 102)
BASE (See POS 103)	XXX	0	0011	- Config. 1 Register (POS 103)
BASE (See POS 103)	XXX	0	0100	- Config. 2 Register (POS 104)
BASE (See POS 103)	XXX	0	0101	- Config. 3 Register (POS 105)
BASE (See POS 103)	XXX	0	0110-0111	- Reserved
BASE (See POS 103)	XXX	0	1000-1110	- Node ID PROM
BASE (See POS 103)	XXX	0	1111	- Register 15 (Transfer Status)
BASE (See POS 103)	XXX	1	0000,1000, 0010,1010	- 82596 Port Select
BASE (See POS 103)	XXX	1	0100,1100	- 82596 CA Select
BASE (See POS 103)	XXX	All Others		- Reserved

Register Summary

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Register 0, 1 - ID Byte 0 and 1 (POS 100, 101)

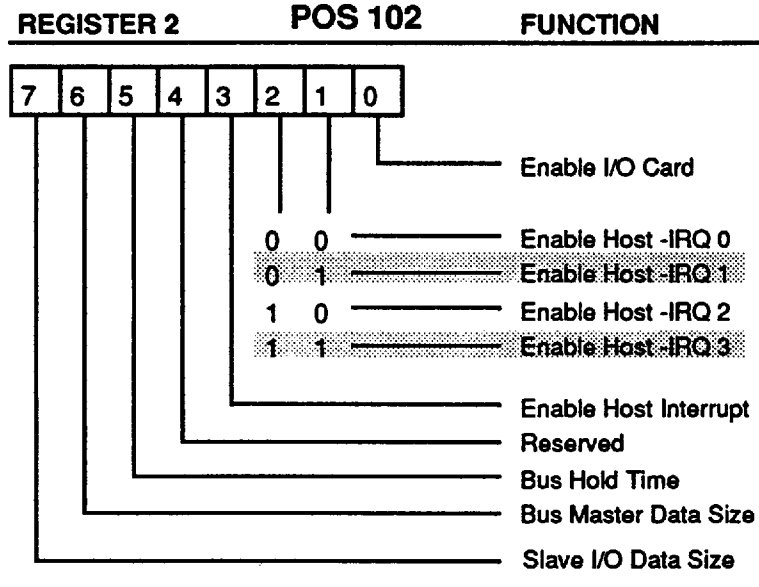
READ (host)

These external registers contain a unique card slot ID to support automatic I/O board set-up. During set-up the contents of these registers are gated to the host bus by the MC 9020 (enabled through pins -POSCS(0-1)). -POSCS(0-1) can enable the ID from -244s or the Node ID PROM.

Register 2 - Configuration 0 (POS 102)

This POS 102 register contains configuration data that is written by the host during I/O set-up.

WRITE / READ



Bit 0 - This bit is set to 0 whenever the MC 9020 is hard reset. The host processor writes this bit to a 1 thus enabling the card (and chip) for normal operation. When this bit is set to 0 the MC 9020 does not respond to any host bus access (except set-up).

Bits 1-2 - These bits select which Micro Channel interrupt signal to assert when the 82596 asserts its interrupt request line.

Bit 3 - When set to 1, this bit enables the -IRQ(0-3) signals

Bit 4 - Reserved

Bit 5 - When set to 0, the MC 9020 will hold the bus no longer than 4 microseconds after the MC 9020 detects a -PREEMPT condition. When this bit is set to 1, the MC 9020 holds the bus no longer than 6.8 microseconds after a -PREEMPT condition.

Bit 6 - This bit specifies the data width for bus master transfers. This bit selects between a 16 bit (when set to 1) or 32 bit (when set to 0) bus master interface.

Bit 7 - This bit specifies the data width for slave access to the 82596. Set to 0 is a 16 bit slave access (-CDDS16). Set to 1 is a 32 bit slave access (-CDDS32). Note that this configuration works with the CA, DX, SX mode setting. For CDDS32 to be enabled, the MC 9020 must be configured in the CA mode. SX and DX modes enable -CDDS16.

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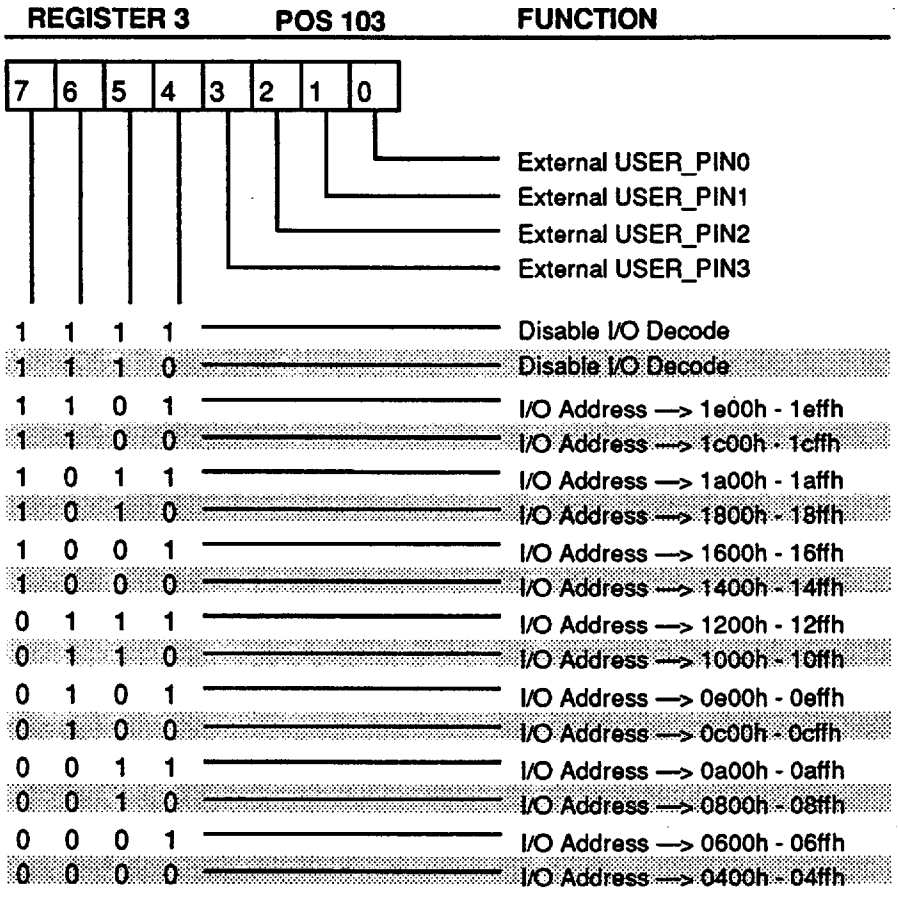
Register 3 - Configuration 1 (POS 103)

The Configuration 1 Register (POS 103) contains the I/O address decode range for the MC 9020's chip selects and registers. Bits 4-7 of this register are compared against host address bits A15-A8 to select the I/O address of the board as shown in the "Register 3" description below. This I/O address is a base address which selects a 256 byte I/O address range. The individual chip selects and the POS registers reside in 32 bytes of Micro Channel I/O space as shown at the beginning of this section, decoded from A0-4.

WRITE / READ



Bits 0-3 - These bits connect directly to the USER_PINs and allow POS control of external logic.

Bits 4-7 - The bits are compared against host address bits A15-A8 to select the I/O address of the board.

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Register 4 - Configuration 2 (POS 104)

This register (POS 104) contains the BIOS PROM address range, I/O board 32 bit bus master address enable, and the card select input enable bit.

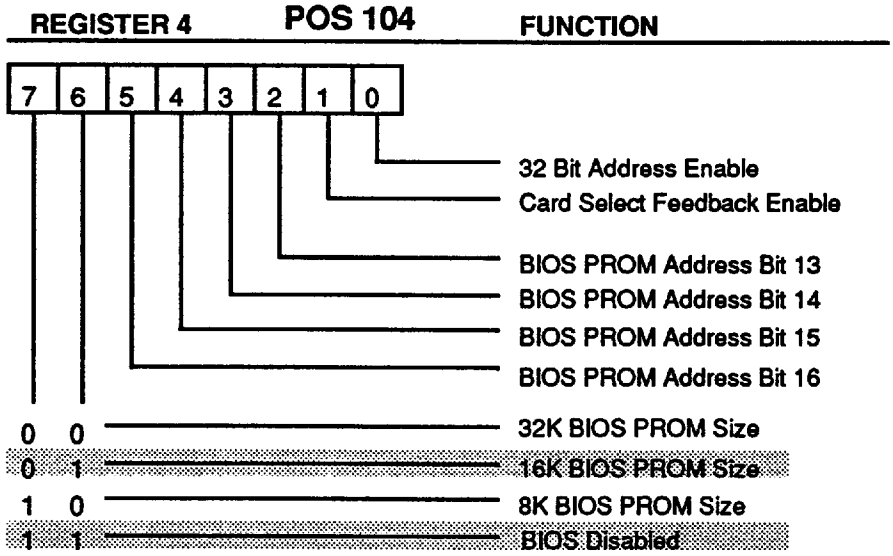
The BIOS PROM starting address and size information is placed in this register. The BIOS PROM normally resides in the 0C0000h to 0DFFFFh address range. The BIOS PROM address and range is written by the host processor during I/O card configuration. For BIOS PROM selection, address bits A23 - A13 are specified below:

A23	A22	A21	A20	A19	A18	A17	A16	A15	A14	A13
0	0	0	0	1	1	0	bit5	bit4	bit3	bit2

The adapter board must externally decode address bits A23 - A17 and connect the result of this decode to the -HAENB pin of the MC 9020. For 32 bit addresses the board must externally decode address bits A31-A17.

The reader should note that the BIOS PROM starting address must be on a memory boundary equal to the size of the BIOS PROM.

WRITE / READ



Bit 0 - When this bit is set to 0 the MC 9020 assumes 24 bit addressing when the MC 9020 is the Micro Channel bus master (MADE24 signal is high). When this bit is set to 1 the MC 9020 uses 32 bit addressing when it is the bus master.

Bit 1 - When this bit is set to 1 the MC 9020 must receive the -SFDBKRTN when it is the bus master on the Micro Channel. If this signal is not received, the current transfer is terminated and -CHCK signal is asserted on the Micro Channel.

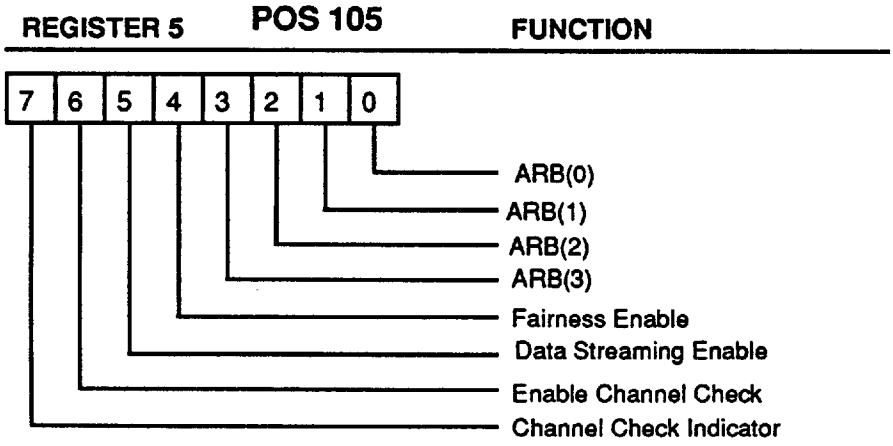
Bits 2-5 - These bits are compared against host address bits A13 -A16 for determining a BIOS PROM access.

Bits 6-7 - These bits specify the BIOS PROM size and BIOS Disable as indicated above.

Register 5 - Configuration 3 (POS 105)

This register (POS 105) provides arbitration, data streaming, and channel check configuration information to the MC 9020.

WRITE / READ



Bits 0-3 - These bits indicate the arbitration priority for the Micro Channel operation. A hexadecimal value of F (1111) has the lowest priority and a hexadecimal value of 0 (0000) has the highest priority.

Bit 4 - When this bit is set to 0 the MC 9020 implements the fairness algorithm for host bus arbitration. When this bit is set to 1 the the MC 9020 implements the linear priority arbitration algorithm.

Bit 5 - When this bit is set to 1 the MC 9020 is enabled for data streaming transfers on the Micro Channel.

Bit 6 - When this bit is set to 1, the -CHCK signal of the MC 9020 is enabled.

Bit 7 - This bit is set to 0 by the MC 9020 when the MC 9020 asserts -CHCK. The MC 9020 will assert -CHCK (providing POS 105 bit 6 is asserted) if either a -CDSFDBK error occurs or when the local adapter is forced off the bus prior to releasing the bus. This second condition may occur if the local adapter incorrectly holds the bus longer than the 7.8 seconds maximum after an external -PREEMPT and the system begins an arbitration cycle before the local adapter releases the bus. In most applications, the potential for this condition will exist only during adapter development and debug. A properly functioning hardware and software design will not allow this condition to occur. This bit is reset by the assertion of RESET. The host could also reset this bit to 1 by writing a 1 to it.

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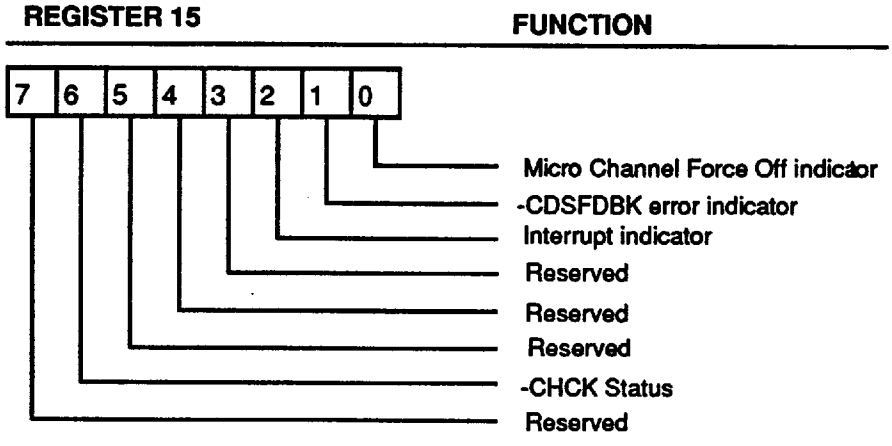
Register 15 - Configuration 15

This transfer status register (not a POS register) controls and flags interrupt, reset and error conditions.

WRITE / READ



Bit 0 - If the local adapter was forced off the bus, the MC 9020 sets this bit to a 1. This condition may occur if the local adapter incorrectly holds the bus longer than the maximum 7.8 microseconds after -PREEMPT and the system begins an arbitration cycle before the local adapter releases the bus. In most applications, the potential for this condition will exist only during adapter development and debug. A properly functioning hardware and software design will not allow this condition to occur. **To reset this bit to 0, the software must write a 1 to this location, which clears it and sets it to 0.**

Bit 1 - If a -CDSFDBK error occurs, the MC 9020 sets this bit to a 1. **To reset this bit to 0, the software must write a 1 to this location, which clears it and sets it to 0.**

Bit 2 - When the MC 9020 asserts an interrupt, it sets this bit to (1). **To reset this bit to 0, the software must write a 1 to this location, which clears it and sets it to 0.**

Bits 3-5 - Reserved

Bit 6 - If , while it is a bus master, the MC 9020 detects the assertion of -CHCK by another system component it sets this bit to 1. **To reset this bit to 0, the software must write a 1 to this location, which clears it and sets it to 0.**

Bit 7 - Reserved

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SECTION 3 PIN DESCRIPTION

The following abbreviations are used:

I/O - Input and Output Pin
I - Input Pin Only
O - Output Pin Only
TS - Three-State Pin
OC - Open Collector Pin
TP - Totem Pole Pin

Table 3.1 Micro Channel Pin Summary

Pin Names	Number of Signals	Input/ Output	Pin Type	Pin Drive (ma)
-ADL	1	I/O	TS	24
ARB(0-3)	4	I/O	OC	24
ARB/-GNT	1	I	-	-
-BE(0-3)	4	I/O	TS	24
-BURST	1	I/O	OC	24
-CDDS16	1	O	TP	6
-CDDS32	1	O	TP	6
-CDSETUP	1	I	-	-
-SFDBKRTN	1	I	-	-
-CDSFDBK	1	O	TP	6
CDCHRDYx	1	O	TP	6
-CHCK	1	I/O	OC	24
CHRDYRTN	1	I	-	-
CHRESET	1	I	-	-
-CMD	1	I/O	TS	24
-DS16RTN	1	I	-	-
-DS32RTN	1	I	-	-
-IRQ(0-3)	4	I/O	OC	24
MADE24	1	I/O	TS	24
M/-IO	1	I/O	TS	24
-PREEMPT	1	I/O	OC	24
-S1	1	I/O	TS	24
-S0	1	I/O	TS	24
-SBHE	1	I/O	TS	24
-SDR0	1	I	-	-
-SDSTROBE	1	O	TS	24
LTR32*	1	O	TP	4
TOTAL PINS	**36**			

*Must be buffered if used.

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Table 3.2. Local Bus Pins

Pin Names	Number of Signals	Input/ Output	Pin Type	Pin Drive (ma)
-ADS	1	I	-	-
-BLAST	1	I	-	-
-BRDY	1	O	TP	4
BREQ	1	O	TP	4
CA	1	O	TP	4
CDEN	1	O	TP	4
CLKx	1	O	TP	4
CRYIN	1	I	-	-
CRYOUT	1	O	-	-
HOLD	1	I	-	-
HLDA	1	O	TP	4
-LBE(0-3)	4	I	-	-
LINT	1	I	-	-
LRESET	1	O	TP	4
LW/-R	1	I	-	-
MODE(0-1)	2	I	-	-
-PORT	1	O	TP	4
-PROMBIOS	1	O	TP	4
-PROMID	1	O	TP	4
-RDY	1	O	TP	4
USER_PIN(0-3)	4	O	TP	4
TOTAL PINS	28			

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Table 3.3 Buffer Control, Address and Data Pins

Pin Names	Number of Signals	Input/ Output	Pin Type	Pin Drive (ma)
HA(0-1)	2	I/O	TS	24
HA(8-16),(2-4)	12	I	-	-
-HAENB	1	I	-	-
-HAOE	1	O	TP	6
HDDIR	1	O	TP	6
-HDOE(0-2)	3	O	TP	4
-HOST/OWN	1	O	TP	4
LD(0-7)	8	I/O	TS	4
-POSCS(0-1)	2	O	TP	4
TOTAL PINS	**31**			

Table 3.4 Power, Ground and No Connect Pins

Pin Names	Number of Signals	Input/ Output	Pin Type	Pin Drive (ma)
NC	13	I		
VDD	10			
VSS	10			
TOTAL PINS	**33**			

Table 3.5 Micro Channel Pin Description T-52-33-55

Symbol	Signal Name	I/O	Pin Number	Function
-ADL	Address Decode Latch	I/O	127	This active low, three-state signal is used to latch the contents of the address bus.The latch is open when this signal is low. Devices on the Micro Channel must latch the address since pipelining is possible. That is, the address may change for the next Micro Channel cycle before the -CMD strobe for the current cycle has been deasserted.
ARB(3) ARB(2) ARB(1) ARB(0)	Arbitration Bus Priority Out	I/O	6 4 3 2	These active high open collector signals are used to present arbitration bus participant priority levels.The highest value of (hex Fh) has the lowest priority and the lowest value (hex 0h) has the highest priority. The priority level of the MC 9020 is programmed into POS Configuration 3 (POS 105).
ARB/-GNT	Arbitrate/-Grant	I	7	This active high input signal indicates an arbitration cycle is in process. When this signal is low it is the grant to the winner to access the channel.
-BE(3) -BE(2) -BE(1) -BE(0)	Byte Enable	I/O	26 25 24 23	These active low three-state signals are used during 32 bit data transfers to indicate which data bytes to be placed on the Micro Channel.
-BURST	Burst	I/O	12	This active low open collector signal is driven low by arbitrating bus participants to indicate the extended use of the Micro Channel. The MC 9020 asserts this signal for all bus master transfers. It deasserts -BURST during the last transfer cycle.
-CDDS16	Card Select 16	O	13	This active low totem pole output indicates the MC 9020 is providing 16 bits of I/O information to the system. This pin is programmable in POS Configuration 0, bit (POS 102).
-CDDS32	Card Select 32	O	121	This active low totem pole output indicates the MC 9020 is providing 32 bits of I/O information to the system. This pin is programmable in POS Configuration 0, (POS 102).
-CDSETUP	Card Setup	I	14	This active low input signal is used to access POS registers. When it is active the host processor may read or write registers 0 - 7. Register selection is made via the address bits A0, A1, and A2.
-SFDBKRTN	Select Feedback Return	I	125	This active low input signal is used when the MC 9020 is the bus master to indicate a slave is present at the address requested. This pin can be disabled by POS Configuration 2, (POS 104).

-CDSFDBK	Card Select Feedback Out	O	15	This active low output signal indicates when the MC 9020 is being accessed by the Micro-Channel. It is generated from an address decode of the I/O registers, 82596, or PROM chip selects.
CDCHRDYx	Channel Ready Out	O	18	This active high totem pole output indicates that the MC 9020 chip needs additional time to complete the requested read or write operation.
-CHCK	Channel Check	I/O	119	This open collector indicates a check condition occurred on the host bus. This pin is asserted by the MC 9020 when a bus errors occurs and POS 105 Config 3, bit 6 is asserted.
CHRDYRTN	Channel Ready Return	I	123	This active high input indicates that the slave addressed by the MC 9020 needs additional time to complete the requested read or write operation. When the slave need more time it pulls this signal low. The MC 9020 inserts wait states until this signal is high.
CHRESET	Channel Reset	I	19	This active high input provides a hard reset to the MC 9020 chip. Internal logic is initialized by this signal and any transfer operations are aborted.
-CMD	Command	I/O	20	This active low three-state signal is used to define when data is valid on the data bus. During write operations, the data must be valid on the bus throughout the period -CMD is low. For read operations the data must be valid before the trailing edge of -CMD and held on the bus (hold time) until after -CMD is high.
-DS16RTN	Data Size 16 Return	I	21	This active low signal indicates that the slave device is providing(driving or receiving) 16 bits of data.
-DS32RTN	Data Size 32 Return	I	22	This active low input signal indicates that the slave device is providing (driving or receiving) 32 bits of data.
-IRQ(3) -IRQ(2) -IRQ(1) -IRQ(0)	Interrupt Request	O	85,84,83, 82	These active low open collector signals are used to inform the system processor of the completion of a task. The active interrupt line is programmable in POS Configuration 0.
MADE24	Memory Address Enable 24	I/O	122	This active high three-state signal indicates when an extended (address bits 24 -31) address is used on the Micro Channel. When this signal is low a 32 bit memory address is placed on the bus and when high a 24 bit address is on the bus. This signal is programmable in POS Config 2 (POS 104).
M/-IO	Memory or I/O	I/O	86	This three-state signal distinguishes a memory cycle from an I/O cycle. When this signal is high a memory cycle is in progress. When M/-IO is low an I/O cycle is in progress. If BIOS boot PROM is to be used, M/-IO needs to be driven low in slave mode.

-PREEMPT	PREEMPT	I/O	89	This active low open collector signal is driven low by arbitrating bus participants to request usage of the channel through arbitration. The requesting arbitration bus participant removes it PREEMPT upon being granted the channel. The MC 9020 asserts this signal when the use of the channel is needed and the fairness algorithm (if enabled through POS 105 Config 3) allows the access.
-S0 -S1	Status Bit 0 and 1	I/O	91 90	These active low three-state signals indicate the start of a Micro Channel cycle and also define the type of cycle when used with the M/-IO signal (see above).When the MC 9020 is a channel slave it latches these bits with the trailing edge of -ADL. M/-I/O -S0 -S1 Function 0 0 0 Reserved 0 0 1 I/O Write 0 1 0 I/O Read 0 1 1 Inactive 1 0 0 Reserved 1 0 1 Mem Write 1 1 0 Mem Read 1 1 1 Inactive
-SBHE	System Byte High Enable	I/O	120	This active low three-state signal enables the transfers of date on the high byte (bits 8-15) of the data bus. It is used with A0 to distinguish between byte 0 (bits 0-7) and byte 1 (bits 8-15) transfers.
-SDR0	Streaming Data Request	I	93	This active low input signal is driven by a slave device to indicate to the MC 9020 that the slave is capable of streaming data transfers. Data streaming is enabled when POS Configuration 3, bit 5 is asserted.
-SDSTROBE	Streaming Data Strobe	O	94	The MC 9020 asserts this active low output signal to clock data on and off the data bus during streaming transfers.
LTR32	Translate	O	62	This active high totem pole output is driven low when the MC 9020 is performing 32 bit data transfers. When this signal is low the MC 9020 drives Micro Channel signals -BE(0-3) to gate data between 32 bit slaves and the MC 9020.

Table 3.6 Local Bus Pin Description

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Symbol	Signal Name	I/O	Pin Number	Function
-ADS	Address Strobe	I	42	This active low input signal indicates the Intel 82596 has begun a valid bus master cycle and that the 82596 pins A31-A2, -BE(0-3) and W/-R are being driven valid.
-BLAST	Last Burst Cycle	I	63	This active low input signal indicates that the next -BRDY will be treated as a normal -RDY, thus ending a streaming data transfer. This input is only used for the 82596CA version. For the SX and DX versions this input should be tied high.
-BRDY	Burst Ready	O	53	This active low input signal performs the same function as -RDY during burst cycles. This output is not used for the Intel 82596 SX and DX versions.
BREQ	Bus Request	O	43	Bus Request to 82596. This signal is used to trigger the bus throttle timers.
CA	Channel Attention	O	46	This active high output is used to force the 82596 to begin executing memory resident commands. In other words, this signal wakes up the Intel 82596 and forces it to start executing command sequences from system memory. The I/O address of the signal is programmable in POS Configuration 1 (POS 103).
CDEN	Card Enable	O	68	This totem pole output is asserted when the I/O board has been enabled through POS.
CLKx	Clock X	O	44	This output signal provides the fundamental timing for the 82596. It is at the frequency or half the frequency of the crystal oscillator. The frequency depends on the setting of the MODE (0-1) pins. It provides all timing information. The MC 9020 synchronizes this signal with the Intel 82596 using the RESET pin. This ensures both the MC 9020 and the Intel 82596 are operating from the same CLKx edge.
CRYIN	Crystal Input	I	72	This input pin provides the timing for all synchronous operations in the MC 9020. It connects to either a TTL clock signal or directly to a crystal.
CRYOUT	Crystal Output	O	73	This output signal connects directly to crystal oscillator.It is a no connect pin when the the CRYIN pin connects to a TTL clock signal.
HOLD	Bus Hold Request	I	47	This active high input indicates the Intel 82596 needs to gain access to the host bus.
HLDA	Bus Hold Acknowledge	O	50	This active high totem pole output signal indicates the MC 9020 has successfully gained access to the host bus. When the Intel 82596 receives this signal it begins bus master operation.

-LBE(0-2) LBE3	Byte Enable	I	56,57, 58,45	These active low and active high input signals are used to indicate which bytes are involved with the current bus master memory access. LBE(3) specifies the high byte and -LBE(0) specifies the low byte. When operating in 16 bit mode, these pins are redefined to carry the -BHE and -BLE signals into -LBE1 and -LBE0.
LINT	82596 Local Interrupt	I	51	This active high input is asserted when the 82596 has an interrupt pending. The MC 9020 asserts one of four host interrupts when this signal is active. The host interrupt line that is asserted is programmable in POS 102 Configuration 0, bits 1 and 2. LINT is latched.
LRESET	Reset	O	55	This active high output signal provides a hard reset to the Intel 82596. It is also used to phase synchronize the clock for the MC 9020 and Intel 82596.
LW/-R	Write or Read	I	52	This input pin specifies whether the current bus master access is a read or write operation. When this pin is high a write cycle is requested and when low a read cycle.
MODE(1) MODE(0)	Mode	I	67 66	These pins are used to select the various types of 596 chips as outlined below: MODE1 MODE 0 596 Chip 0 0 Reserved 0 1 CA - 1x clk 1 0 DX - 2x clk 1 1 SX - 2x clk
-PORT	Port	O	61	This active low output signal causes the Intel 82596 to latch data from the system data bus into a 32 bit internal register. When operating is 16 bit mode, this signal must be activated twice for all CPU port access commands. This signal and the CA signal comprise the slave interface to the Intel 82596. The I/O address of the -PORT signal is programmable in POS Configuration 1 (POS 103).
-PROMBIOS	BIOS PROM Output Enable	O	74	This active low output pin connects to the output enable pin (-OE) of the BIOS Boot PROM. The MC 9020 gates the data from the PROM onto the system data bus. The system memory address of the BIOS PROM is programmable in POS Configuration 2 (POS 104).
-PROMID	ID PROM Output Enable	O	75	This active low output pin connects to the output enable pin (-OE) of the Node ID PROM. The MC 9020 gates the data from the Node ID PROM onto the system data bus. The system I/O address of the ID PROM is programmable in POS Configuration 1 (POS 103).

-RDY	Ready	O	54	The MC 9020 asserts this active low signal to inform the Intel 82596 that the current bus master access cycle maybe completed. When this signal is high, the Intel 82596 inserts wait cycles in the current bus access.
USER_PIN(3) USER_PIN(2) USER_PIN(1) USER_PIN(0)	User Defined Pin	O	77,78, 76, 59	These totem pole output pins are controlled from POS Config 1 for each host interface. They control logic on the I/O board.

Table 3.7 Buffer Control, Address and Data Pins

Symbol	Signal Name	I/O	Pin Number	Function
HA(0-1) HA(2-4) HA(8-16)	Host Address	I/O I I	8,9 10,11, 27 30,31,34, 35,36,38 39,40,41	These active high input signals are the host address lines needed for POS, I/O and BIOS PROM space decode. HA(0-2) are used for POS decode and HA(8-15) are used for the BIOS PROM and I/O address space decode. In addition, HA(16) is needed for the BIOS PROM decode. The address ranges are programmed in POS Configuration 1 and 2 (POS 103,104). HA(0-1) are outputs in 32 bit master mode and 16 bit master mode. If -LBE0 nad -LBE1 are high, then HA1 = 1. If -LBE0 or -LBE1 are low then HA1 = 0
-HAENB	Host Address Enable	I	79	This signal provides for an external decode of Host Address bits (17-23). This pin is used for BIOS PROM decode only.
-HAOE	Host Address Output Enable	O	105	This active low totem pole output signal connects to the -OE pin of the LS245s which gate the address bus between the adapter board and the Micro Channel, or AT bus.
HDDIR	Host Data Direction	O	102	This totem pole output signal connects to the -OE pin of the LS245s which gate the data bus between the adapter board and the Micro Channel. When this pin is low the host data bus is gated to the adapter board. When this pin is high the data bus from the adapter board is gated to the host data bus.
-HDOE(2) -HDOE(1) -HDOE(0)	Host Data Output	O	98 99 100	These active low totem pole output signals connect to the -OE pin of the LS245s which gate data between the adapter board and the host bus. These pins are connected as indicated below: Host byte -HDOE pin 0 -HDOE(0) 1 -HDOE(1) 2 -HDOE(2) 3 -HDOE(2)

-HOST/OWN	Host Own	O	95	When this active low totem pole signal is asserted, the MC 9020 is the owner of the host bus.
LD(0-7)	Host Data	I/O	117,115, 114,110, 109,108, 107,106	These three-state data signals program POS Configuration registers in the MC 9020.The host processor may also read back the POS registers through the 32 byte I/O port (see Configuration 1).
-POSCS(0-1)	POS Chip Select	O	87,88	These active low output pins are asserted when the host system accesses POS registers zero or one. The should be connected to the output enable pin of an LS244,S257 or PROM. The MC 9020 gates the POS data to the host bus.

Table 3.8 Power, Ground and No Connect Pin Description

NC	No Connect	-	5, 28, 37, 60, 69, 92, 101, 103, 104, 116, 118, 124, 126	No Connect
VDD	Power	I	1, 17, 29, 33, 49, 64, 71, 80, 96, 112	Five Volt Power Supply Pins
VSS	Ground	I	16, 32, 48, 65, 70, 81, 97, 111, 113, 128	Ground Pins

Section 4 - Bus Cycles

This section describes Micro Channel slave and master cycles. Timing relationships are described in more detail in Section 5. For more detailed information on the Micro Channel Bus, see the IBM PS/2 Technical Reference Manual. For detailed information on the 82596, see the Intel literature. Contact PLX Technology at 1-800- 759-3753 for assistance or other information.

Slave Cycles

POS Register Access

The MC 9020 responds to a setup routine when it detects the assertion of -CDSETUP by the system controller. When the card is selected, the MC 9020 decodes A0-A2 to determine the POS register to be read from or written to. M/-IO, -S0 and -S1 indicate whether the cycle is a read or write cycle. The MC 9020 has POS 102 through 105 on-chip.

In addition, the MC 9020 will drive the adapter ID number to the data bus (D0-7) when POS 100 or 101 are addressed. When POS 100 or 101 are selected, the MC 9020 will drive -POSCS0 or 1 respectively, which are chip select signals which enable two 244 buffers or the Node ID PROM to the D0-7 data lines.

The POS registers may also be accessed through an I/O read or write operation at the I/O address described at the beginning of Section 2.

82596 Register Access

The 82596 registers are accessed through a Micro Channel slave I/O cycle. The MC 9020 decodes the system address (as determined in POS registers, Section 2) and drives CA or -PORT to the 82596. The MC 9020 also drives the data direction signal (HDDIR) to the data buffers to indicate whether the cycle is read or write. If the slave is 32 bit, the MC 9020 drives the data buffer enable signals -HDOE(0,1,2). If the slave is 16 bit, the MC 9020 drives only -HDOE(0,1).

Node ID and BIOS PROM Access

The Ethernet Node ID PROM and BIOS PROM are accessed through a Micro Channel I/O slave cycle and Memory slave cycle respectively. The MC 9020 decodes the system address (as determined by POS 103 and 104, section 2) and drives the -PROMID and -PROMBIOS chip selects. HDDIR and -HDOE(0,1) are enabled for the BIOS PROM access. The MC 9020 automatically inserts a wait state by deasserting -CDCHRDY.

Master Cycles

Bus Request

The 82596 initiates a Micro Channel Bus Request by asserting HOLD to the MC 9020. When the MC 9020 detects HOLD, it drives -PREEMPT to the Micro Channel. The MC 9020 will assert -PREEMPT only when ARB/-GNT is low (in the grant state). This prevents arbitration errors. During the arbitration state, if -PREEMPT was asserted in the preceding grant state, it will remain asserted. Once -PREEMPT is asserted the local master will participate in the next arbitration cycle.

Arbitration Priority Levels

The MC 9020 can be configured to any of 16 arbitration priority levels through the POS registers (See Section 2). Although it can drive all sixteen levels, note that the IBM PS/2 Technical Reference Manual states that bus masters should have levels 8-15. Levels 0-7 are reserved for DMA slaves.

Arbitration Cycle

When ARB/-GNT enters the ARB state, the MC 9020 will participate in the arbitration cycle provided it has asserted -PREEMPT. The MC 9020 executes the arbitration cycle according to the Micro Channel specification.

When the MC 9020 wins arbitration, it will assert -BURST on the Micro Channel, HLDA to the 82596, -HAOE and -HOST/OWN. -HAOE enables the adapter board's 244 address buffers. HOST/OWN is always active when the MC 9020 owns the Micro Channel and is a useful signal during the debugging phase of board development.

After asserting HLDA, the MC 9020 releases -PREEMPT. The MC 9020 will continue to drive -BURST throughout the data transfer cycle.

If the FAIRNESS bit is enabled in POS 105 the MC 9020 will be prohibited from enabling -PREEMPT during subsequent arbitration cycles until all other system adapters have deasserted -PREEMPT, assuming that the local master wins and controls the bus in the current cycle.

BURST and Single Data Transfer Cycles

The data transfer cycle starts when the MC 9020 asserts HLDA, which is an indication to the 82596 that it may begin transferring data. After detecting HLDA, the 82596 asserts -ADS to the MC 9020 and LW/-R depending on whether the cycle is Read or Write. In turn, the MC 9020, on the next clock cycle, asserts -ADL and on the following cycle, -CMD. The MC 9020 also enables the address and data buffers in the proper sequence and drives the status lines to the Micro Channel.

When valid data has been transferred to the Micro Channel, the MC 9020 asserts -RDY, which indicates to the 82596 that it may reassert -ADS and start another cycle.

Data transfers will continue in this way until either the 82596 deasserts HOLD or the adapter is preempted off the bus by another adapter, or the adapter exceeds the maximum bus hold time limit programmed in POS. If one of the last three conditions occur, the MC 9020 will deassert HLDA. The adapter has the option to program the Bus Throttle timer, which is activated from BREQ. The MC 9020 asserts BREQ when the MC 9020 PREEMPT timer expires.

Provided that the adapter has not exceed the bus hold time limit programmed in POS and no other master has requested the bus, the MC 9020 will actually retain control of the bus for 0.8 microseconds after the deassertion of HOLD. If the 82596 does not reassert HOLD within this period, the MC 9020 will release the Micro Channel. This is to allow the 82596 to retain control of the bus for prefetch operations when the 82596 will immediately reassert HOLD.

The MC 9020 in conjunction with the 82596 can sustain Read and Write BURST data transfer cycles of 200 ns, provided of course that the responding slave does not slow the cycle through CHRDYRTN.

Streaming Data Transfers

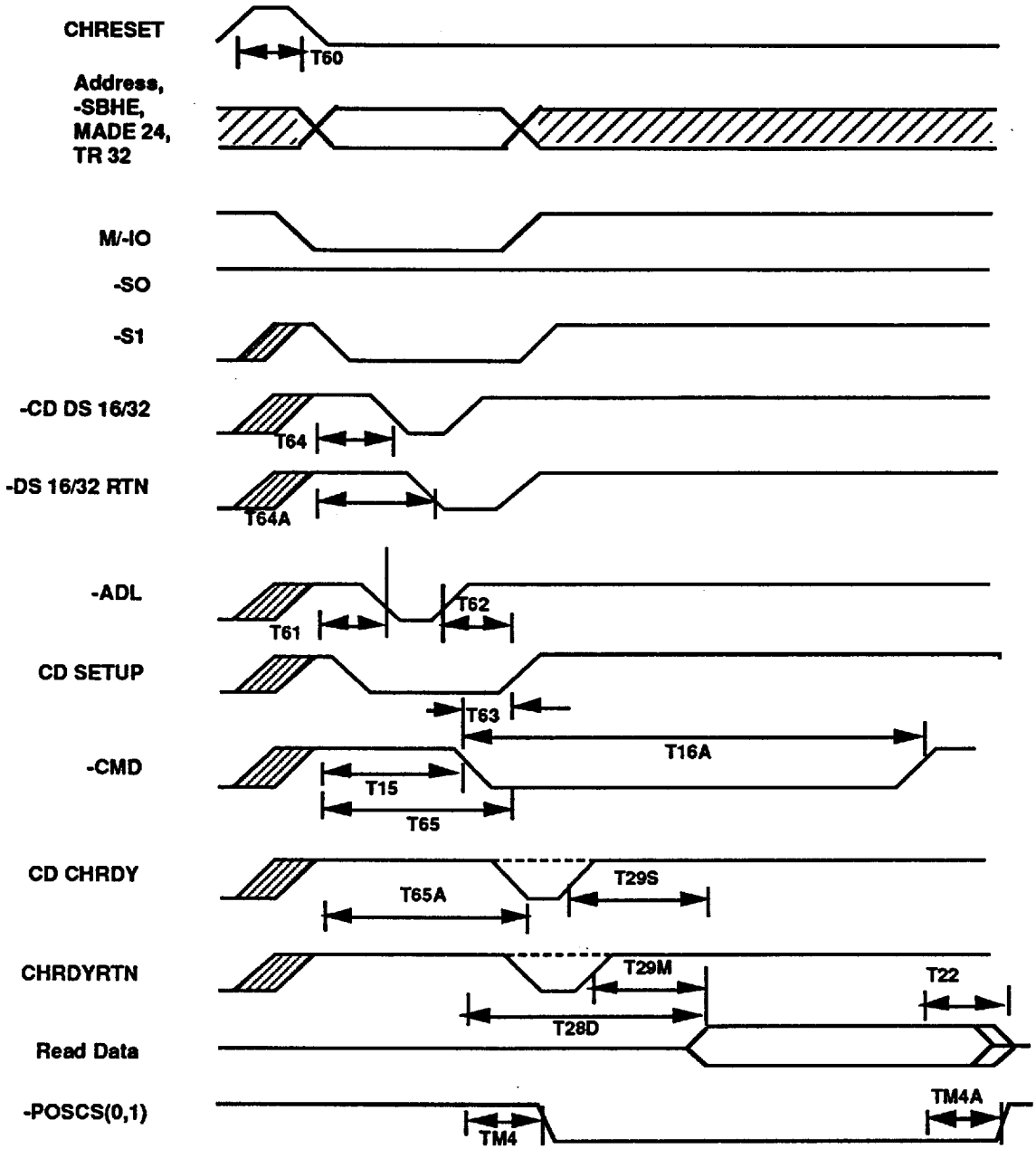
For CA versions of the 82596, the MC 9020 supports streaming data transfers. To enable streaming, the streaming enable POS 105 bit must be asserted and the slave must be able to support streaming transfers. The MC 9020 combined with the 82596CA will normally stream in 100 ns cycles unless "paced" by the slave to a slower rate through CHRDYRTN.

The streaming data cycle starts the same way as a BURST cycle. After the MC 9020 asserts -ADL it will also assert -SDSTROBE provided the slave has asserted -SDR0 (which indicates it supports streaming) and provided the MC 9020 has received CHRDYRTN. (The MC 9020 will conduct BURST cycles until it detects CHRDYRTN at which time it will transfer in streaming cycles). The MC 9020 cycles the flow of data in or out of the 82596 during streaming by toggling -BRDY.

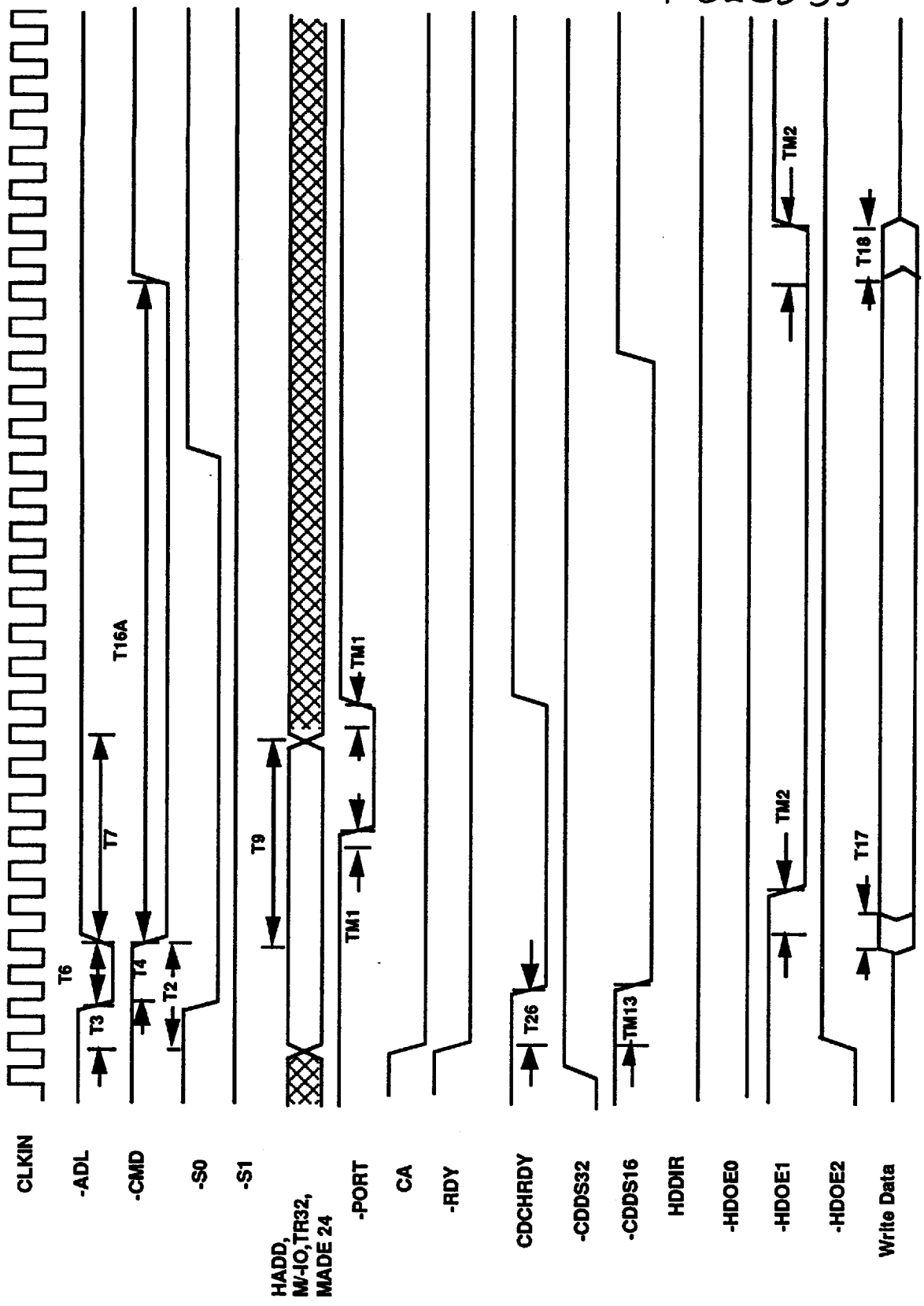
The slave may slow down the streaming cycle by deasserting CHRDYRTN. When the MC 9020 detects this condition it will not issue another -BRDY to the 82596CA until CHRDYRTN is reasserted, indicating that the slave is ready for another streaming transfer.

The streaming transfer is terminated by the slave if it deasserts -SDR0. The streaming data transfer is terminated by the 82596 if it deasserts -BLAST.

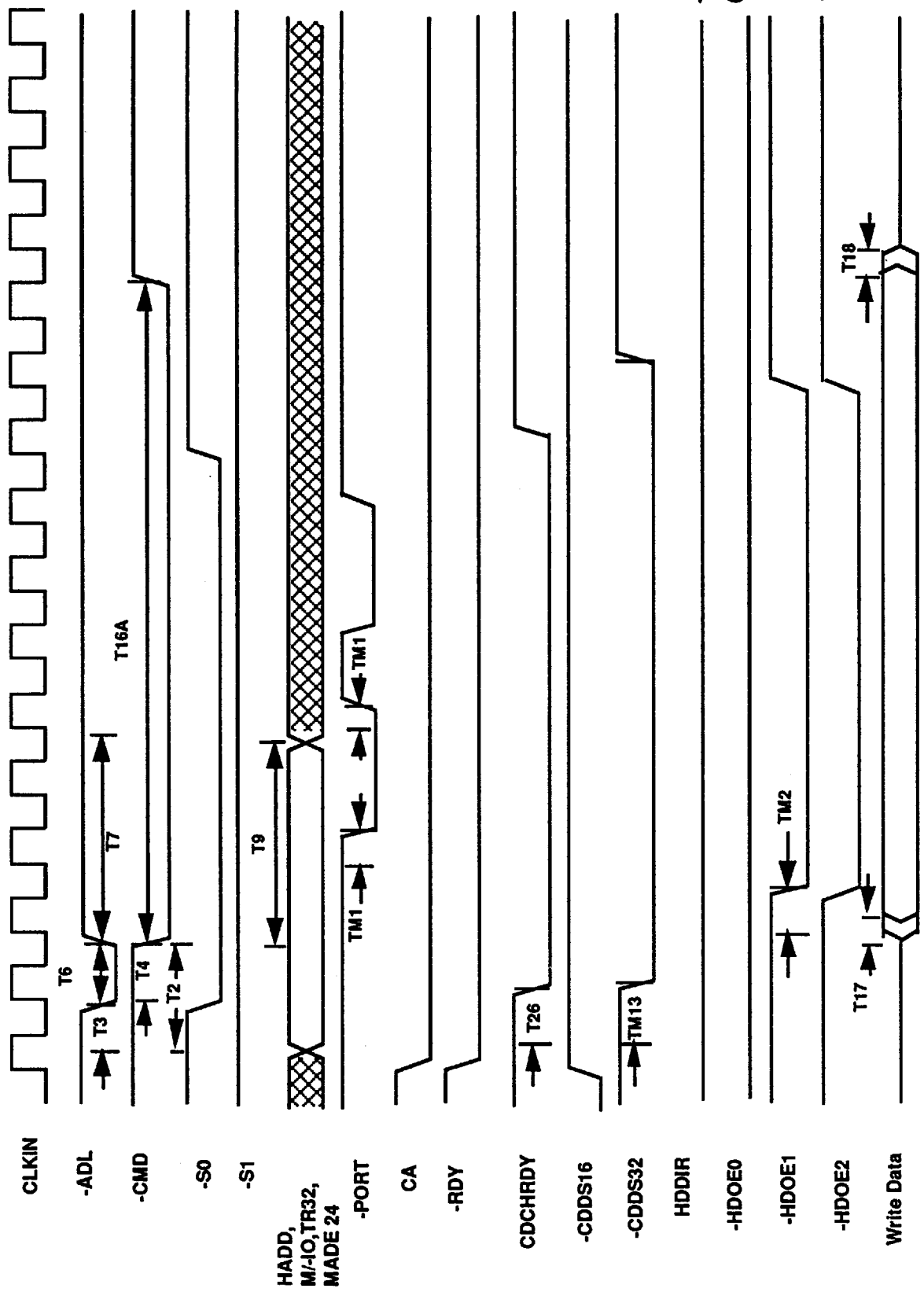
Section 5 - Timing



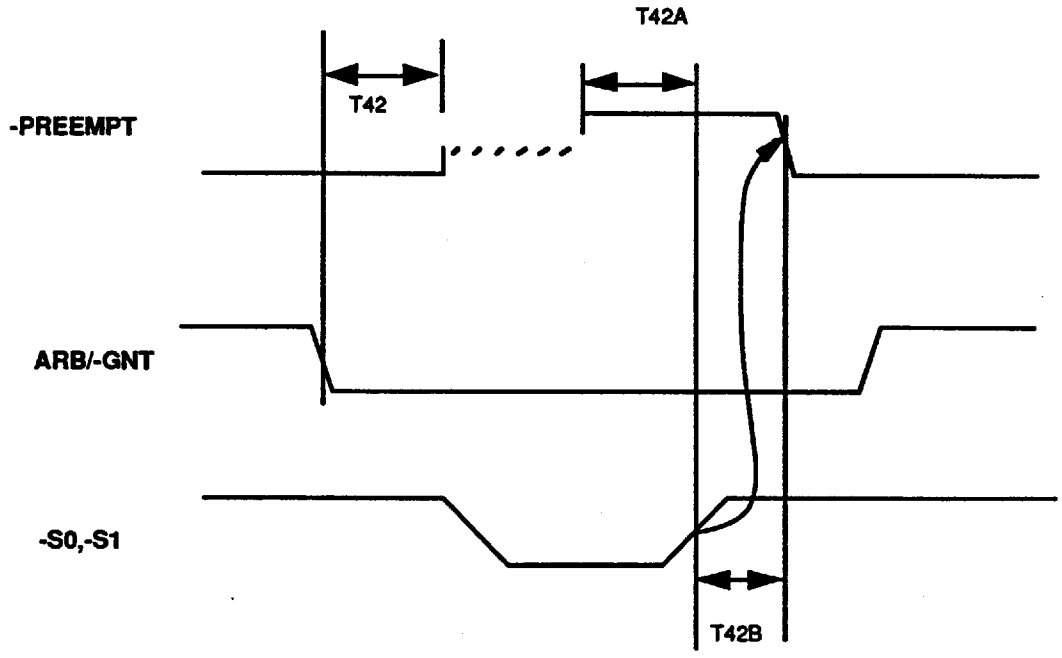
Micro Channel System Configuration Timing



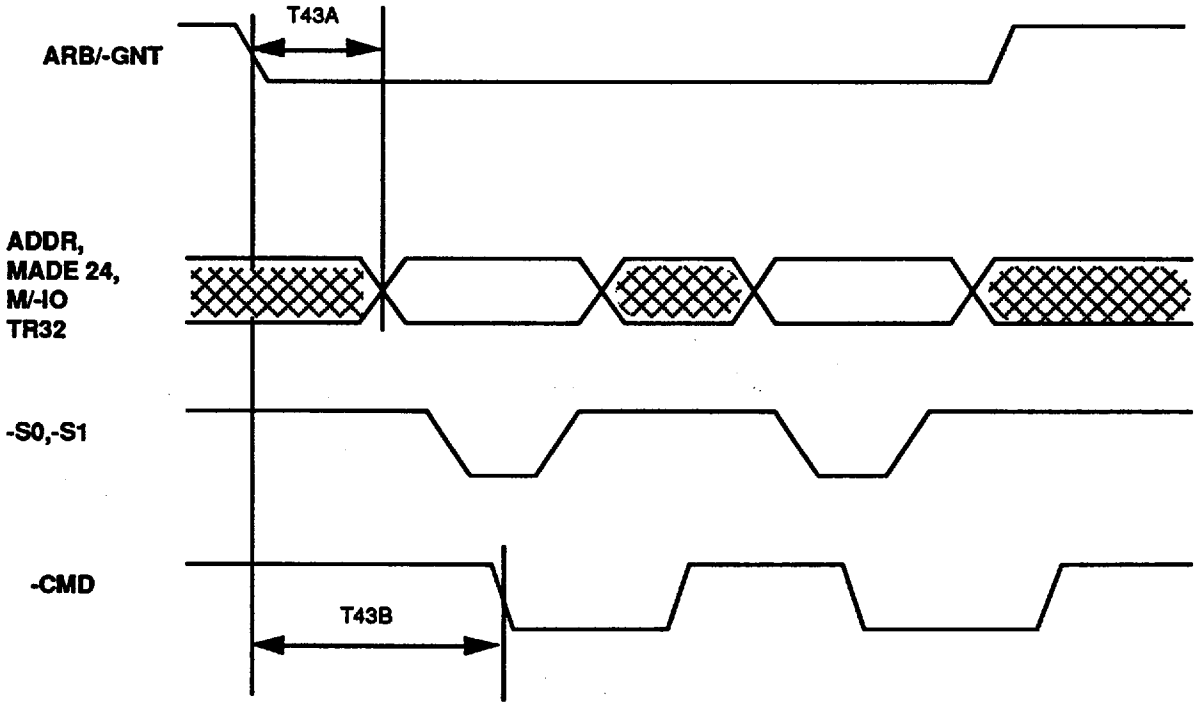
Micro Channel Slave I/O Write Cycle (82596SX)



Micro Channel, Slave I/O Write (Intel 82596 CA)



Exiting From the Inactive State



"First" DMA Cycle (after ARB/-GNT low)

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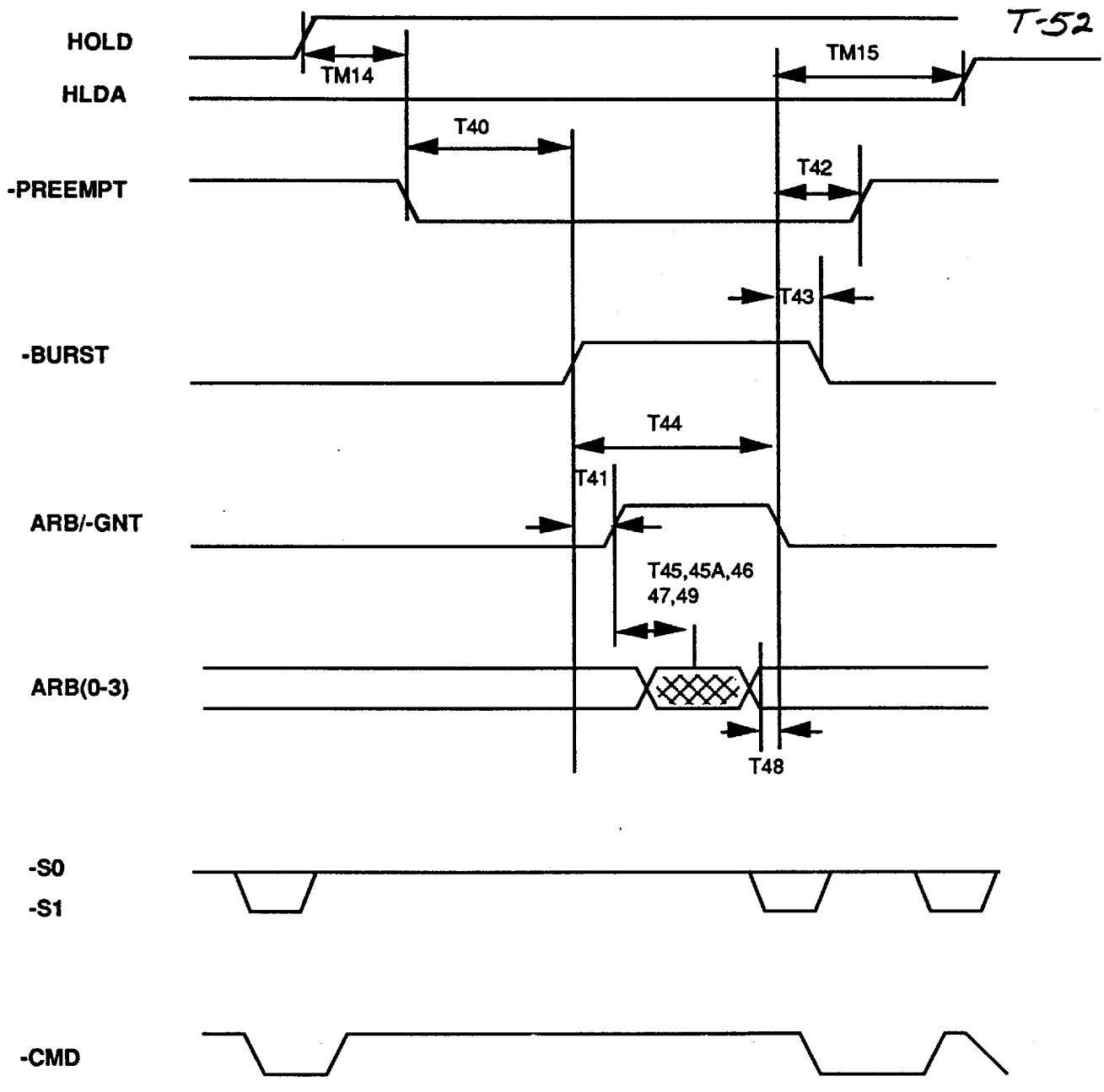

Arbitration Cycle

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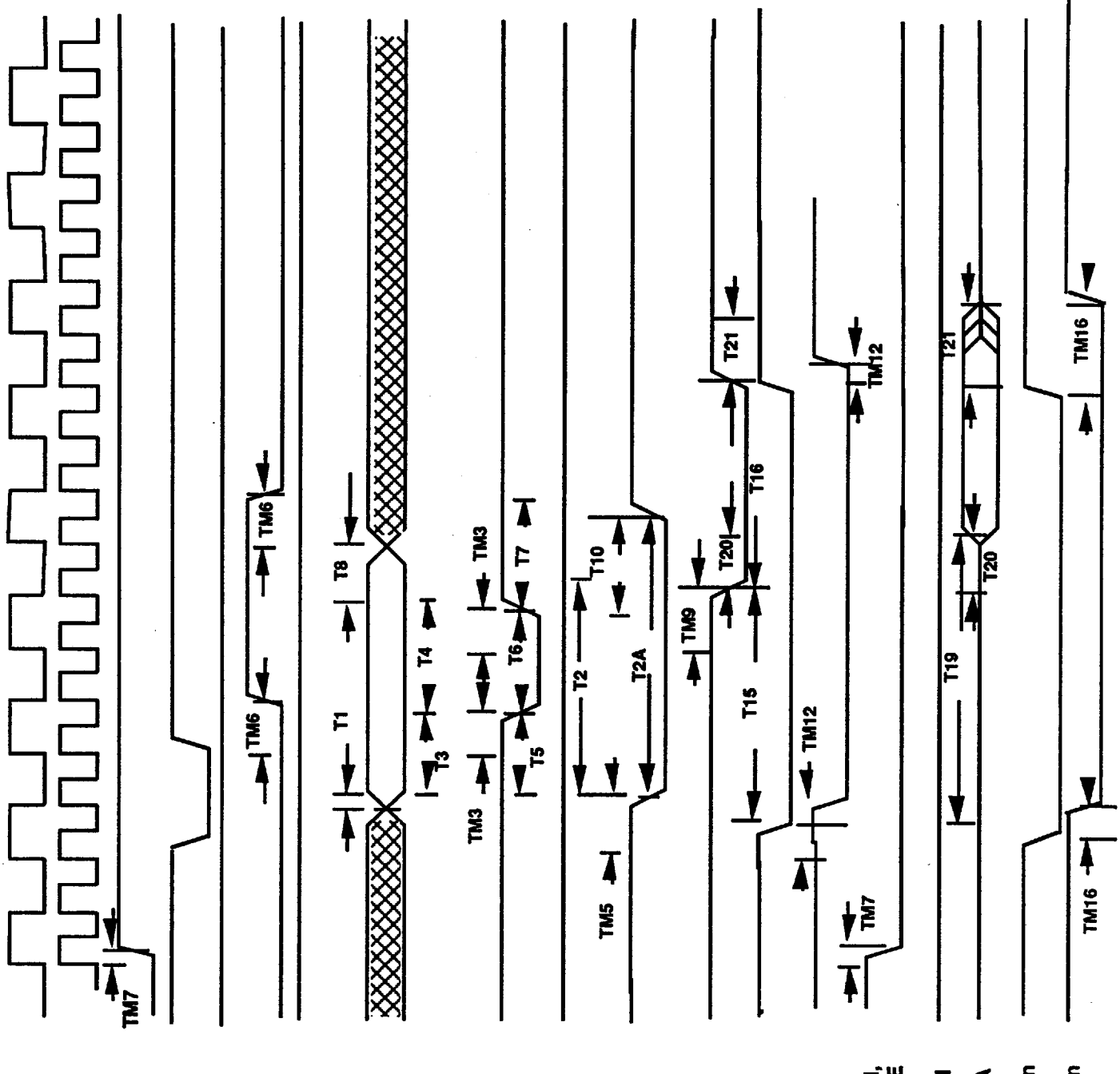
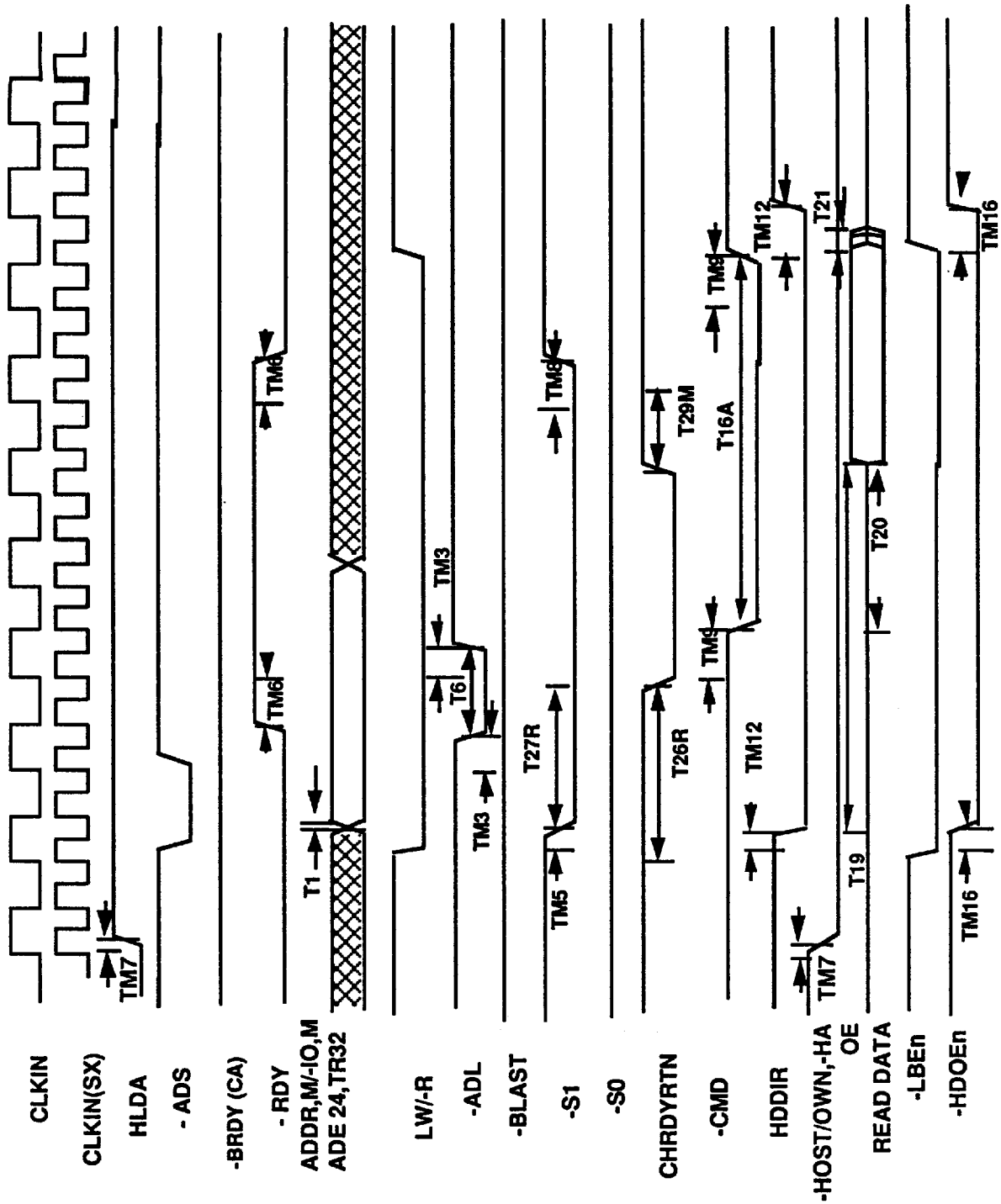
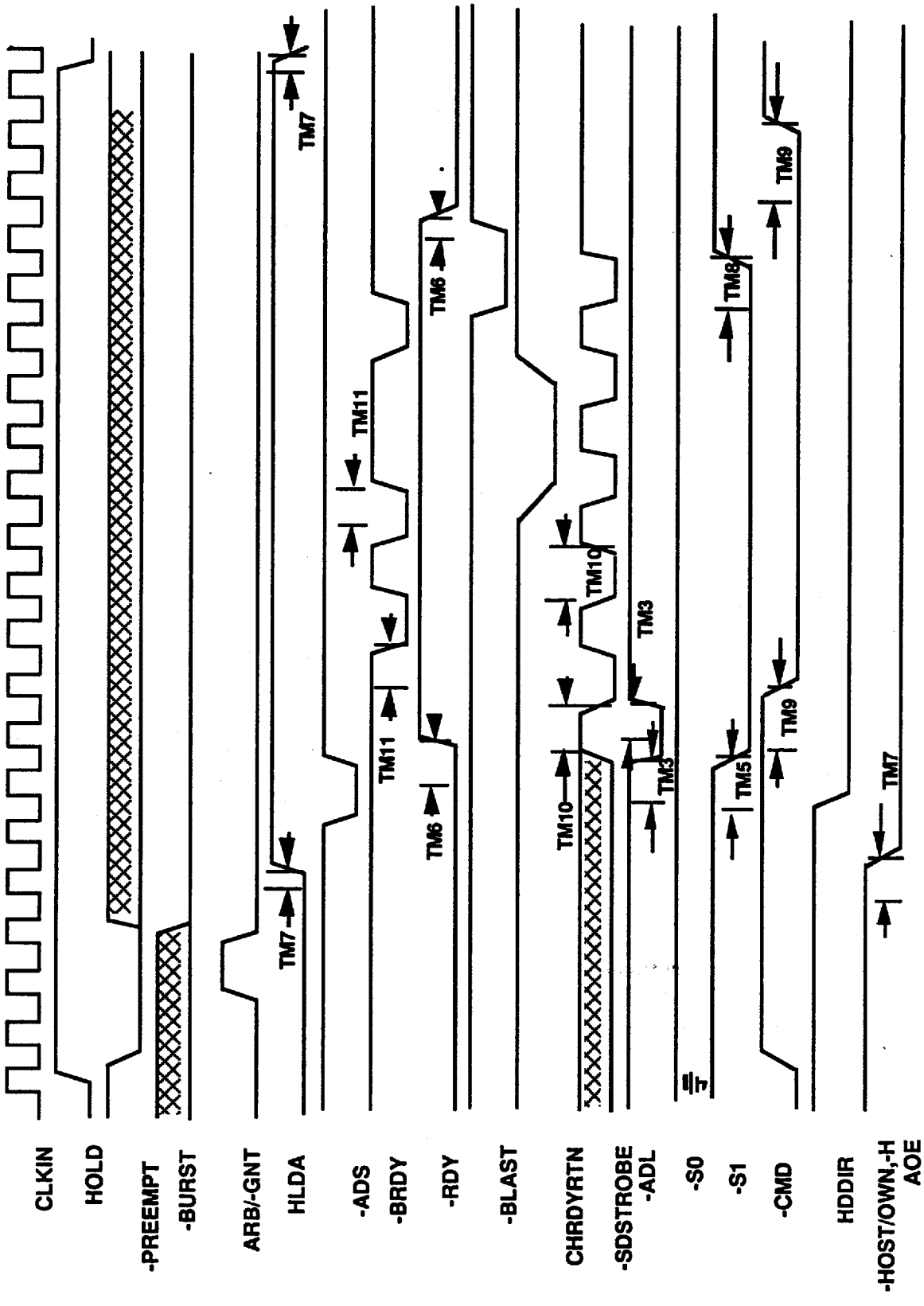


Micro Channel, Default Mode (Intel 82596) (Bus master Memory Read)



Micro Channel, Asynchronous Extended Cycles, Bus Master (Read Data)
(Intel 82596)

T-52-33-55



Streaming Data Read Cycle (Master Terminated by -BLAST)

In this example CHRDYRTN adds one wait states through data pacing

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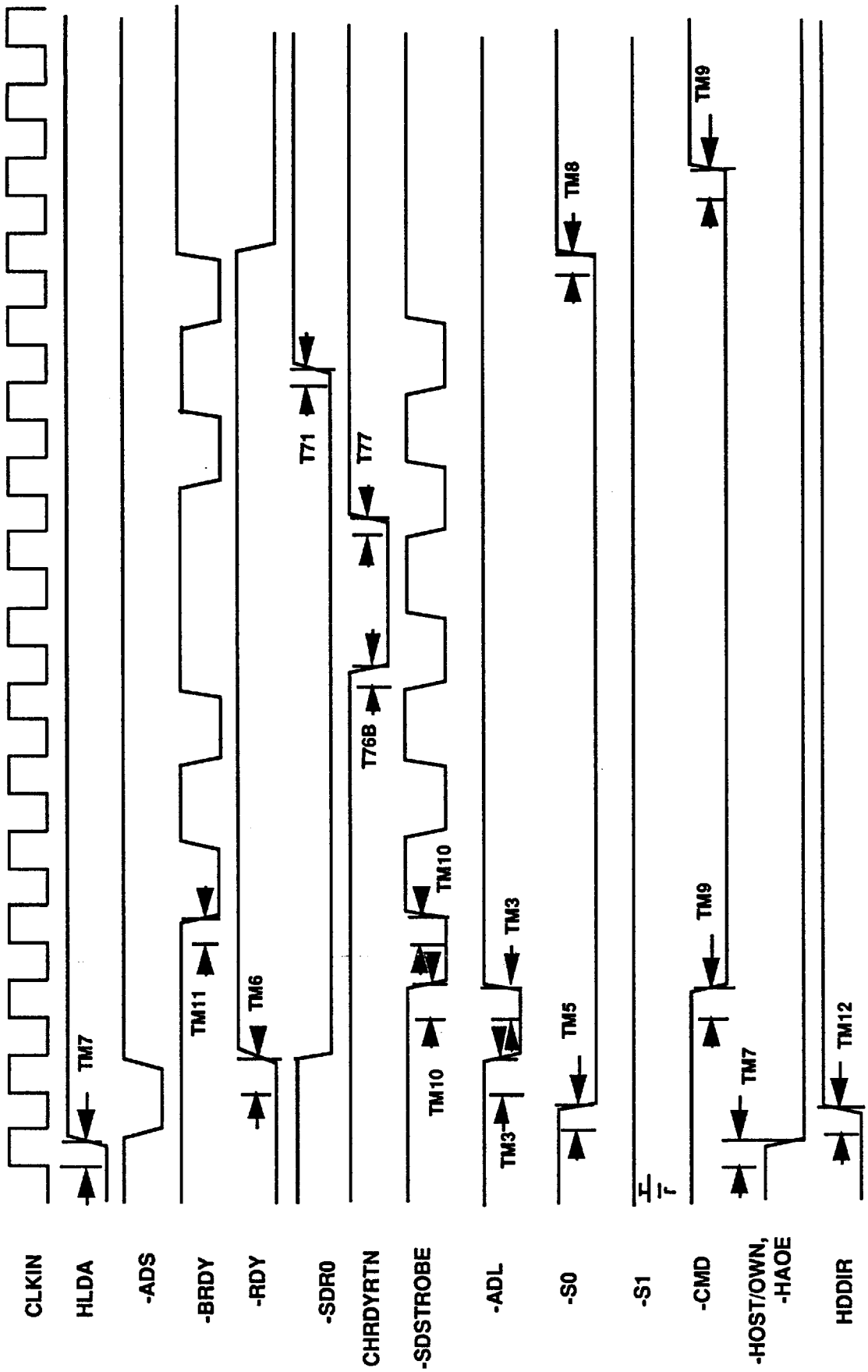

Micro Channel Master Streaming Data Write Cycle (Intel 82596CA)
(Terminated by Slave - SDR0)

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AC Timing Min/Max Specifications

Note: All timing values with a "TMn" label are specific to the MC 9020 device. All other values are from the IBM PS/2 Technical Reference Manual and have the same labels as the Technical Reference Manual.

MC 9020 specific timing

Time	Description	Min	Max	Unit
TM1	Clock high to -PORT valid delay		35	ns
TM2	-CMD low to -HDOE low delay		30	ns
TM3	Clock high to -ADL valid delay		35	ns
TM4	-CMD low to -POSCS(0,1) low delay		35	ns
TM4A	-CMD high to -POSCS(0,1) high delay		30	ns
TM5	-ADS low to -S(0,1) low delay		35	ns
TM6	Clock high to -RDY valid delay		35	ns
TM7	Clock high to -HAOE, -HOST/OWN, HLDA, valid delay		40	ns
TM8	Clock high to -S(0,1) high delay		35	ns
TM9	Clock high to -CMD valid delay		35	ns
TM10	Clock high to -SDSTROBE valid delay		35	ns
TM11	Clock high to -BRDY valid delay		35	ns
TM12	LW/-R to HDDIR valid delay		30	ns
TM13	Valid address to -CDDS16, -CDDS32 valid delay		40	ns
TM14	HOLD to -PREEMPT assertion		35	ns
TM15	ARB/-GNT asserted to HLDA asserted		35	ns
TM16	Local Byte enable to -HDOE		30	ns

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Micro Channel Timing from IBM PS/2 Technical Reference Manual

Time	Description	Min	Max	Unit
T1	Status active from Address, M/-IO, MADE24, TR32 valid	10		ns
T2	-CMD active from status active	55		ns
T2A	Status pulse width of an aborted cycle	85		ns
T3	-ADL active from Address, M/-IO, MADE24, TR32 valid	45		ns
T4	-ADL active to -CMD active	40		ns
T5	-ADL active from status active	12		ns
T6	-ADL pulse width	40		ns
T7	Status hold from -CMD active	25		ns
T8	Address, M/-IO, -SBHE, -BE(0-3), MADE24, TR32 from -ADL inactive	25		ns
T9	Address, M/-IO, -SBHE, -BE(0-3), MADE24, TR32 from -CMD active	30		ns
T10	Status hold from -CMD inactive	30		ns
T15	-CMD active from Address valid	85		ns
T16	-CMD pulse width	90		ns
T16A	-CMD pulse width (Asynchronous extended cycle)	190		ns
T17	Write Data setup to -CMD active	0		ns
T18	Write Data hold from -CMD inactive	30		ns
T19	Status active to Read Data valid (Access Time)		125	ns
T20	Read Data valid from -CMD active		60	ns
T21	Read Data hold from -CMD inactive	0		ns
T22	Read data bus tri-state from -CMD inactive		40	ns
T26	CD CHRDY inactive from Address Bus valid		60	ns
T26R	CHRDYRTN inactive from Address Bus valid		80	ns
T27R	CHRDYRTN inactive from status valid and previous -CMD inactive		50	ns

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Time	Description	Min	Max	Unit
T28D	Read valid data from -CMD active		160	ns
T29A	-CMD inactive from CHRDYRTN active	60		ns
T29M	Read Data valid to master from CHRDYRTN active		60	ns
T29S	Read data from salve valid from CD CHRDY active		60	ns
T35	CD CHRDY active from CD CHRDY inactive		3.5	us
T40	-PREEMPT active to EOT (channel release)		7.8	us
T41	ARB/-GNT in the ARB state from EOT (channel release)	30		ns
T42	-PREEMPT inactive from ARB/-GNT in -GNT state		50	ns
T42A	-PREEMPT inactive to status inactive	20		ns
T42B	-PREEMPT inactive from status inactive (Compete for the channel after the inactive state)	0		ns
T43	-BURST active from ARB/-GNT to -GNT state		50	ns
T43A	Address bus valid from ARB/-GNT in the -GNT state	0		ns
T43B	-CMD active from ARB/-GNT in the -GNT state	115		ns
T44	ARB/-GNT in ARB state	100		ns
T45	Driver turn-on delay from ARB/-GNT in ARB state	0	50	ns
T45A	Driver turn-on delay from lower priority line	0	50	ns
T46	Driver turn-off delay from ARB/-GNT in ARB state	0	50	ns
T47	Driver turn-off delay from higher priority line	0	50	ns
T48	Arbitration bus stable before ARB/-GNT in -GNT state	10		ns
T49	Tri-state drivers from ARB/-GNT in ARB state		50	ns
T60	CHRESET active pulse width	100		ms
T61	-CD SETUP active to -ADL active	15		ns
T62	-CD SETUP hold from -ADL active	15		ns
T63	-CD SETUP hold form -ADL inactive	30		ns
T64	-CD DS16/32 active from -CD SETUP active		25	ns
T64A	-DS 16/32 RTN active from -CD SETUP active		45	ns
T65	CD CHRDY inactive from -CD SETUP active and status active		100	ns
T65A	CHRDYRTN inactive from -CD SETUP active and status active		120	ns
T71	-SDR0 inactive from last -SDSTROBE fall (slave terminated cycle)	0	40	ns
T71B	-SDR0 inactive form -S0,-S1 inactive (master terminated, slave ready)	0	40	ns
T76B	CHRDYRTN valid from -SD STROBE fall	3	45	ns

Section 6 - Electrical Specifications & Max Ratings

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Absolute Maximum Ratings

Storage Temperature	-65°C to +150°C
Ambient Temperature with Power Applied	-55°C to +125°C
Supply Voltage to Ground	-0.5V to +7.0V
Input Voltage (VIN)	VSS - 0.5V VDD + 0.5V
Output Voltage (VOUT)	VSS - 0.5V VDD + 0.5V

Operating Ranges

Ambient Temperature	Supply Voltage (VDD)	Input Voltage (VIN)
0C to +70°C	5V +/- 5%	Min = VSS Max = VDD

Capacitance (sample tested only)

Parameter	Test Conditions	Pin Type	Typical Value	Units
CIN	VIN =2.0V f = 1 MHz	Input	5	pF
COUT	VOUT = 2.0V f = 1 MHz	Output	10	pF

Electrical Characteristics Tested Over Operating Range

Parameter	Description	Test Conditions		Min	Max	Units
VOH	Output High Voltage	VDD = Min, VIN=VIH or VIL	IOH = -4.0mA	2.4		V
VOL	Output Low Voltage		IOL per Tables 3.1-3.4		0.4	V
VIH	Input High Level			2.0		V
VIL	Input Low Level				0.8	V
ILI	Input Leakage Current	VSS <= VIN <=VDD VDD = Max		-10	+10	uA
IOZ	Tri-state Output Leakage Current	VDD= Max VSS <= VIN <=VDD		-10	+10	uA
ICC	Power Supply Current	VDD= Max		20	80	mA

Section 7 - Package Mechanical Dimensions

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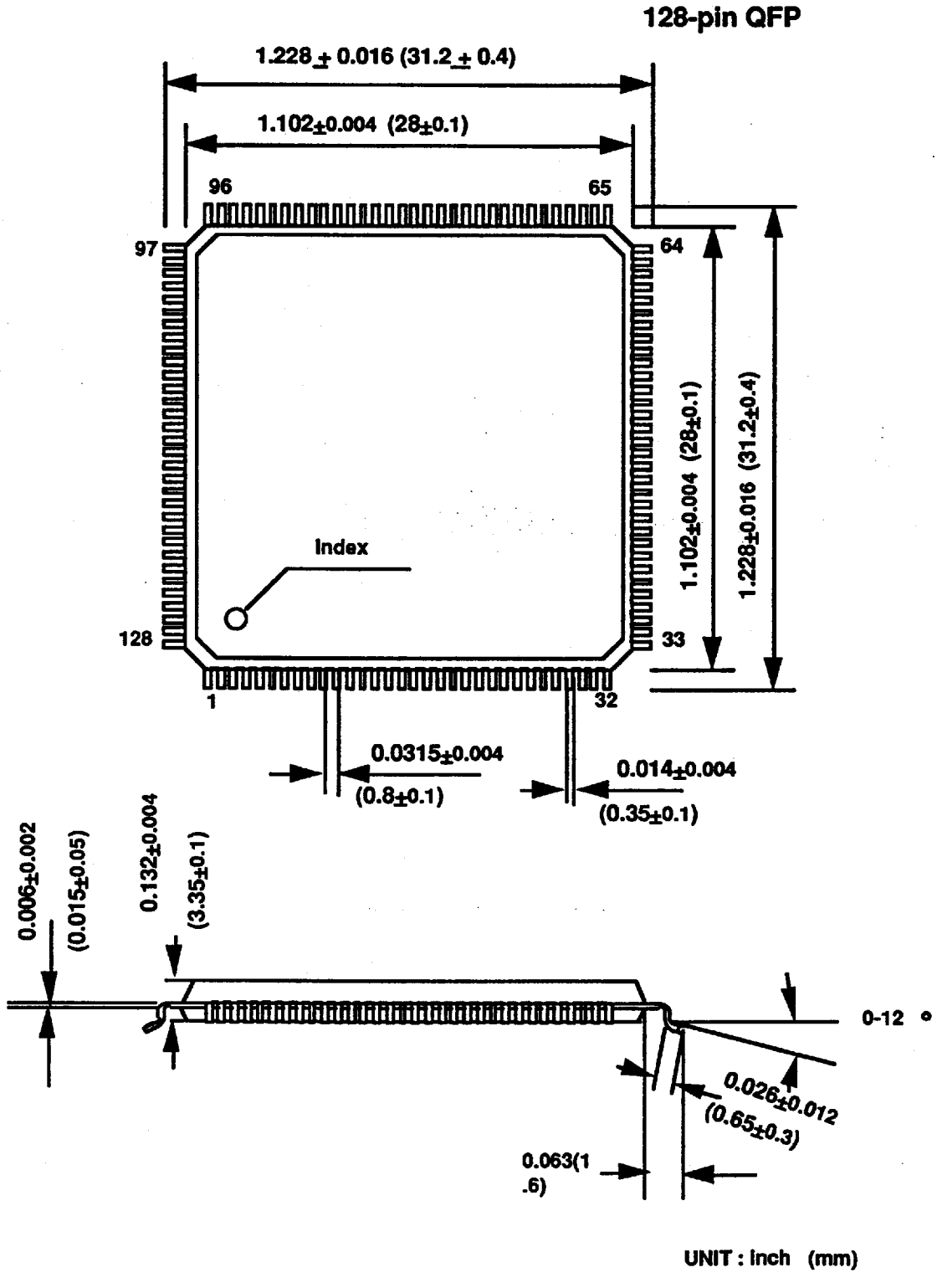

UNIT : Inch (mm)