OKI semiconductor

MSM3764A

65,536-WORD x 1-BIT DYNAMIC RAM

GENERAL DESCRIPTION

The Oki MSM3764A is a fully decoded, dynamic NMOS random access memory organized as 65,536 words x 1 bit. The design is optimized for high-speed, high-performance applications such as mainframe memory, buffer memory, peripheral storage, and environments where low power dissipation and compact layout are required.

Multiplexed row and column address inputs permit the MSM3764A to be housed in a standard 16 pin DIP or 18 pin PLCC. Pin-outs conform to the JEDEC approved pin out.

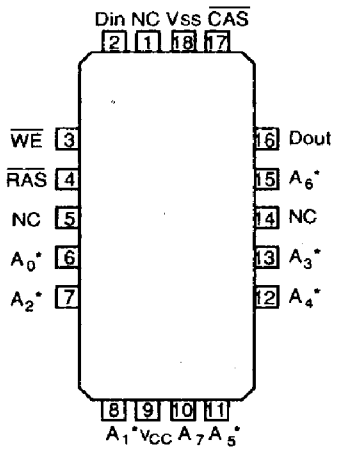
The MSM3764A is fabricated using silicon gate NMOS and Oki's advanced Double-Layer Polysilicon process. This process, coupled with single-transistor memory storage cells, permits maximum circuit density and minimum chip size. Dynamic circuitry, including the sense amplifiers, is employed in the design.

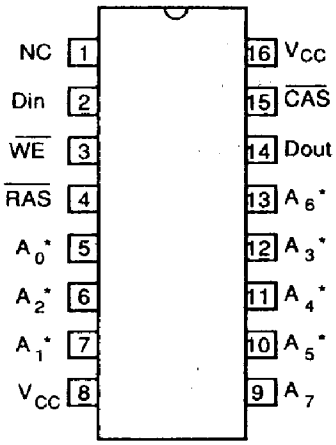
Clock timing requirements are noncritical, and power supply tolerance is very wide. All inputs and output are TTL compatible.

FEATURES

- 65,536 x 1 RAM, 16 or 18 pin package
- Silicon-gate, double-poly NMOS, single-transitor cell
- Row access time:
  120 ns max (MSM3764A-12)
  150 ns max (MSM3764A-15)
- Cycle time:
  220 ns min (MSM3764A-12)
  260 ns min (MSM3764A-15)
- Low power:
  330 mW active, 28 mW max standby
- Single +5V power supply, ±10% tolerance
- TTL compatible, low-capacitive load input
- Three-state TTL compatible output
- Gated $\overline{CAS}$
- 128 refresh cycles/2 ms
- Common I/O capability using Early Write operation
- Output unlatched at cycle end to allow extended page boundary and two-dimensional chip select
- Read-Modify-Write, $\overline{RAS}$-only refresh, and Page-Mode capability
- On-chip latches for addresses and data-in
- On-chip substrate bias generator for high performance

PIN CONFIGURATION (TOP VIEW)

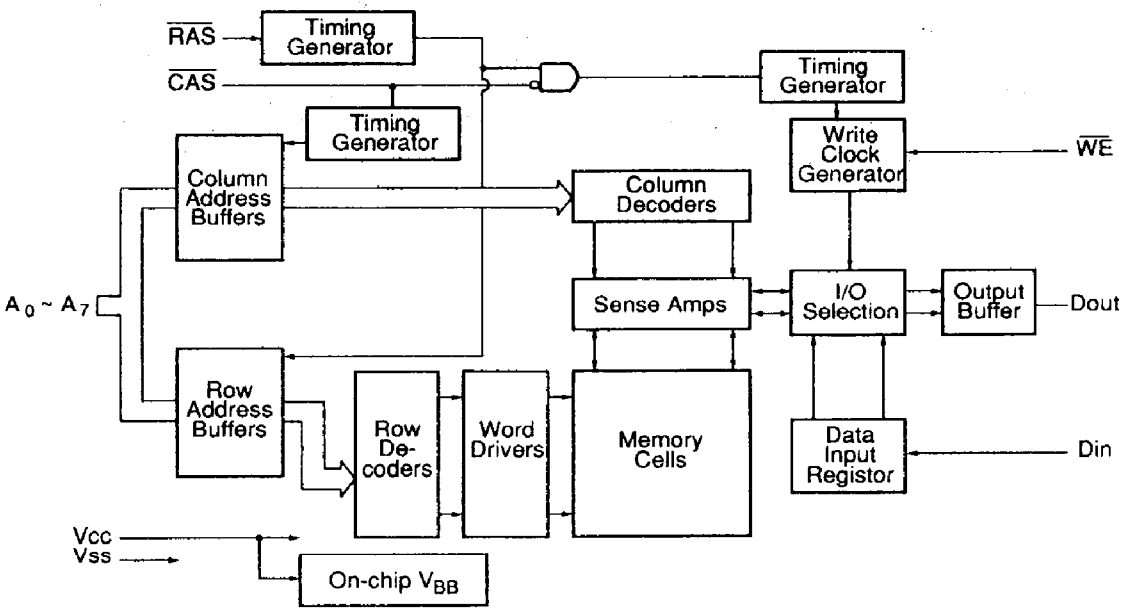




* Refresh Address

Pin Names	Function
$A_0 \sim A_7$	Address Inputs
$\overline{RAS}$	Row Address Strobe
$\overline{CAS}$	Column Address Strobe
$\overline{WE}$	Write Enable
Din	Data Input
Dout	Data Output
Vcc	Power Supply (+5V)
Vss	Ground (0V)
NC	No Connection

FUNCTIONAL BLOCK DIAGRAM



ELECTRICAL CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS (see Note)

Rating	Conditions	Symbol	Value	Unit
Voltage on any pin relative to V_{SS}	–	V_{IN}, V_{OUT}	−1 to +7	V
Voltage on V_{CC} supply relative to V_{SS}	–	V_{CC}	−1 to +7	V
Operating temperature	–	T_{opr}	0 to 70	°C
Storage temperature	–	T_{stg}	−55 to +150	°C
Power dissipation	–	P_D	1.0	W
Short circuit output current	–	–	50	mA

Note: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

4

RECOMMENDED OPERATING CONDITIONS

(Referenced to Vss)

Parameter	Symbol	Conditions	Value			Unit	Operating Temperature
			Min.	Typ.	Max.		
Supply voltage	V_{CC}	–	4.5	5.0	5.5	V	0°C to +70°C
	V_{SS}	–	0	0	0	V	
Input high voltage, all inputs	V_{IH}	–	2.4	–	6.5	V	
Input low voltage, all inputs	V_{IL}	–	−1.0	–	0.8	V	

DC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted.)

Parameter	Symbol	Conditions	MSM3764A			Unit	Notes
			Min.	Typ.	Max.		
Operating Current* Average power supply current ($\overline{RAS}$, $\overline{CAS}$ cycling; t_{RC}= min.)	I_{CC1}	–	–	–	60	mA	
Standby Current Power supply current ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH})	I_{CC2}	–	–	–	5.0	mA	
Refresh Current* Average power supply current ($\overline{RAS}$ cycling, $\overline{CAS}$ = V_{IH} ; t_{RC} = min.)	I_{CC3}	–	–	–	40	mA	
Page Mode Current* Average power supply current ($\overline{RAS}$ = V_{IL} , $\overline{CAS}$ cycling; t_{PC} = min.)	I_{CC4}	–	–	–	60	mA	
Input Leakage Current Input leakage current, any input (0V ≤ V_{IN} ≤ 5.5V, all other pins not under test =0V)	I_{LI}	–	–10	–	10	µA	
Output Leakage Current (Data out is disabled, 0V ≤ V_{OUT} ≤ 5.5V)	I_{LO}	–	–10	–	10	µA	
Output Levels Output high voltage (I_{OH} = –5 mA)	V_{OH}	–	2.4	–	–	V	
Output low voltage (I_{OL} = 4.2 mA)	V_{OL}		–		0.4	V	

* Icc depends on output loading and cycle rates. Specified values are obtained with the output open.

CAPACITANCE *

(Ta = 25°C, f = 1 MHz)

Parameter	Symbol	Conditions	Value		Unit
			Min.	Max.	
Input capacitance (A_0~ A_7, D_{IN})	C_{IN1}	–	–	5	pF
Input capacitance ($\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$)	C_{IN2}	–	–	8	pF
Output capacitance (D_{OUT})	C_{OUT}	–	–	7	pF

* Capacitance measured with Boonton Meter.

AC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted.) Notes 1,2,3

Parameter	Symbol	MSM3764A-12		MSM3764A-15		Unit	Notes
		Min.	Max.	Min.	Max.		
Refresh period	t_{REF}	–	2	–	2	ns	–
Random read or write cycle time	t_{RC}	220	–	260	–	ns	–
Read-write cycle time	t_{RWC}	245	–	280	–	ns	–
Page mode cycle time	t_{PC}	120	–	145	–	ns	–
Access time from $\overline{RAS}$	t_{RAC}	–	120	–	150	ns	4,6
Access time from $\overline{CAS}$	t_{CAC}	–	60	–	75	ns	4,6
Output buffer turn-off delay	t_{OFF}	0	35	0	40	ns	–
Transition time	t_T	3	35	3	35	ns	–
$\overline{RAS}$ precharge time	t_{RP}	90	–	100	–	ns	–
$\overline{RAS}$ pulse width	t_{RAS}	120	10,000	150	10,000	ns	–
$\overline{RAS}$ hold time	t_{RSH}	60	–	75	–	ns	–
$\overline{CAS}$ precharge time (Page cycle)	t_{CP}	50	–	60	–	ns	–
$\overline{CAS}$ pulse width	t_{CAS}	60	10,000	75	10,000	ns	–
$\overline{CAS}$ hold time	t_{CSH}	120	–	150	–	ns	–
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	25	60	25	75	ns	7
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	0	–	0	–	ns	–
Row address set-up time	t_{ASR}	0	–	0	–	ns	–
Row address hold time	t_{RAH}	15	–	15	–	ns	–
Column address set-up time	t_{ASC}	0	–	0	–	ns	–
Column address hold time	t_{CAH}	20	–	20	–	ns	–
Column address hold time referenced to $\overline{RAS}$	t_{AR}	80	–	95	–	ns	–
Read command set-up time	t_{RCS}	0	–	0	–	ns	–
Read command hold time	t_{RCH}	0	–	0	–	ns	–
Write command set-up time	t_{WCS}	–10	–	–10	–	ns	8
Write command hold time	t_{WCH}	40	–	45	–	ns	–
Write command hold time referenced to $\overline{RAS}$	t_{WRC}	100	–	120	–	ns	–
Write command pulse width	t_{WP}	40	–	45	–	ns	–
Write command to $\overline{RAS}$ lead time	t_{RWL}	40	–	45	–	ns	–
Write command to $\overline{CAS}$ lead time	t_{CWL}	40	–	45	–	ns	–
Data-in set-up time	t_{DS}	0	–	0	–	ns	–
Data-in hold time	t_{DH}	40	–	45	–	ns	–
Data-in hold time referenced to $\overline{RAS}$	t_{DHR}	100	–	120	–	ns	–
$\overline{CAS}$ to $\overline{WE}$ delay	t_{CWD}	40	–	45	–	ns	8
$\overline{RAS}$ to $\overline{WE}$ delay	t_{RWD}	100	–	120	–	ns	8
Read command hold time referenced to $\overline{RAS}$	t_{RRH}	0	–	0	–	ns	–
$\overline{CAS}$ precharge time	t_{CPN}	30	–	35	–	ns	–

4

Notes: 1. An initial pause of 100 µs is required after power-up followed by a minimum of any eight $\overline{RAS}$ cycles (example: $\overline{RAS}$ only Refresh) before proper device operation is achieved.

2. The AC measurements assume the transition time (t_T) = 5 ns.

3. V_{IH} (min.) and V_{IL} (max.) are reference levels for measuring the timing of the input signals. Transition times are measured between V_{IH} and V_{IL}.

4. Assumes that $t_{RCD} < t_{RCD}$ (max.) If t_{RCD} is greater than the maximum recommended value shown in this table, t_{RAC} will increase by the amount that t_{RCD} exceeds the value shown.

5. Assumes that $t_{RCD} < t_{RCD}$ (max.)

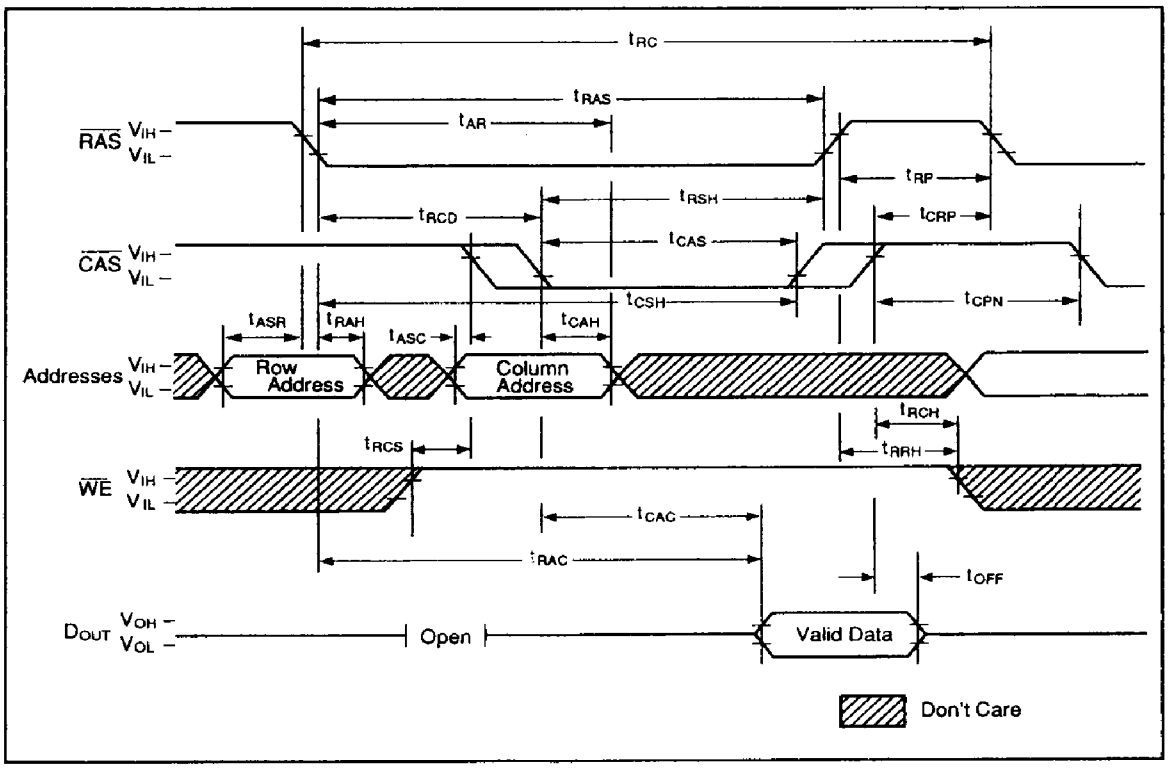
6. Measured using an equivalent load circuit of 2 TTL loads and 100 pF.

7. Operating within the t_{RCD} (max.) limit insures that t_{RAC} (max.) can be met. The spec. t_{RCD} (max.) is for reference only. If t_{RCD} is greater than the specified t_{RCD} (max.) limit, then access time will be controlled exclusively by t_{CAC}.

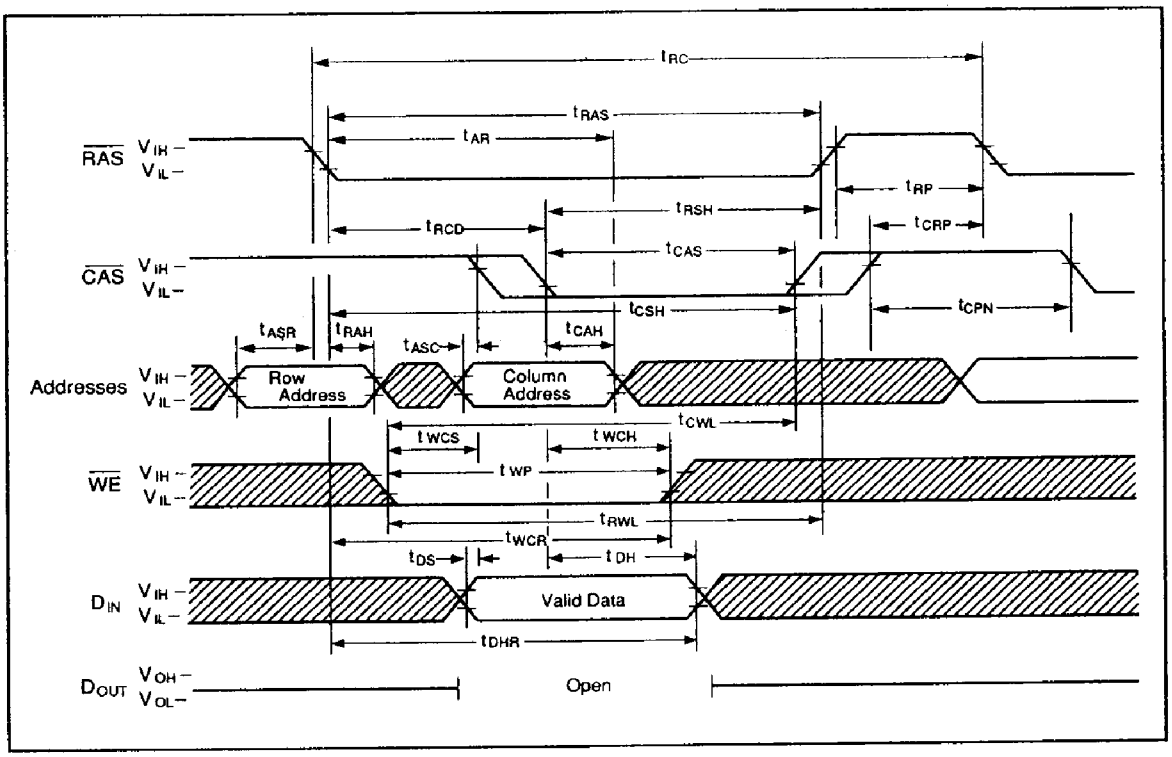
8. The specs t_{WCS}, t_{RWD}, and t_{CWD} are not restrictive operating parameters. They are included in the data sheet for reference only. If $t_{WCS} \geq t_{WCS}$ (min.) then the cycle is an "Early Write" cycle and the data out will remain in a high impedance state throughout the entire cycle. If $t_{CWD} \geq t_{CWD}$ (min.) and $t_{RWD} \geq t_{RWD}$ (min.) then the cycle is a "Read-Write" cycle and the data out will contain data read from the selected cell. If neither of the above sets of conditions are satisfied then the condition of data out will be indeterminate at access time.

9. Either the t_{RRH} or the t_{RCH} spec. must be satified for a proper read cycle.

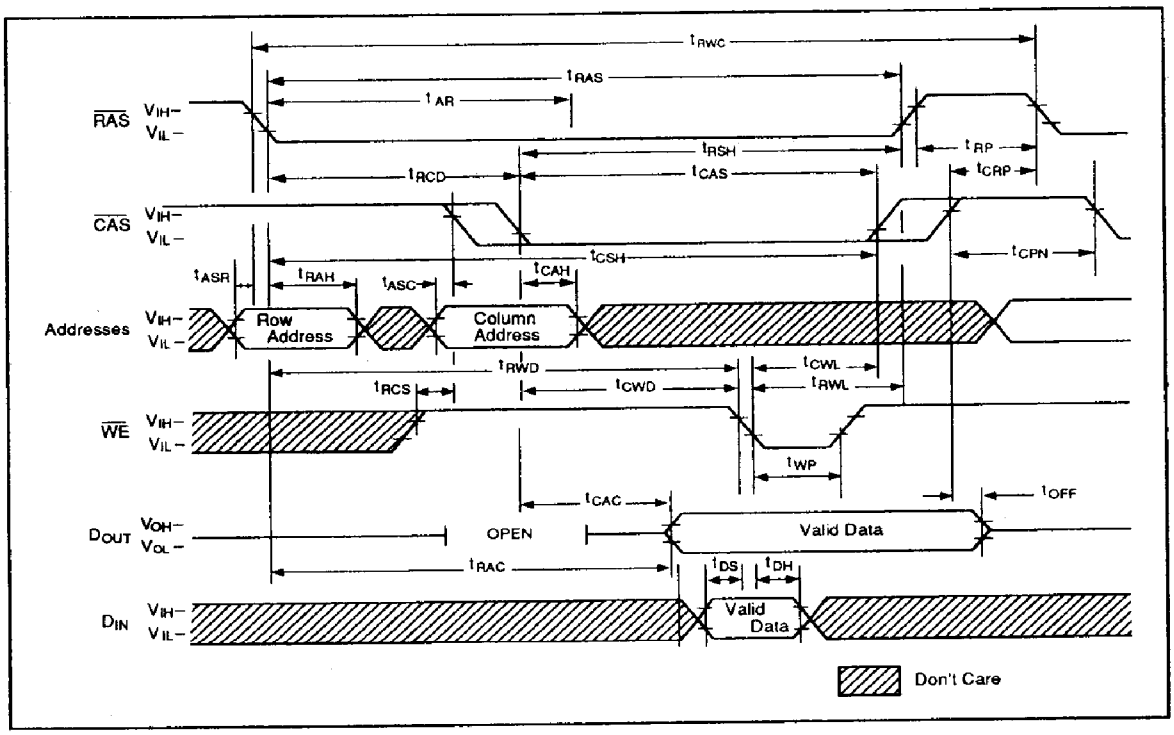
READ CYCLE TIMING



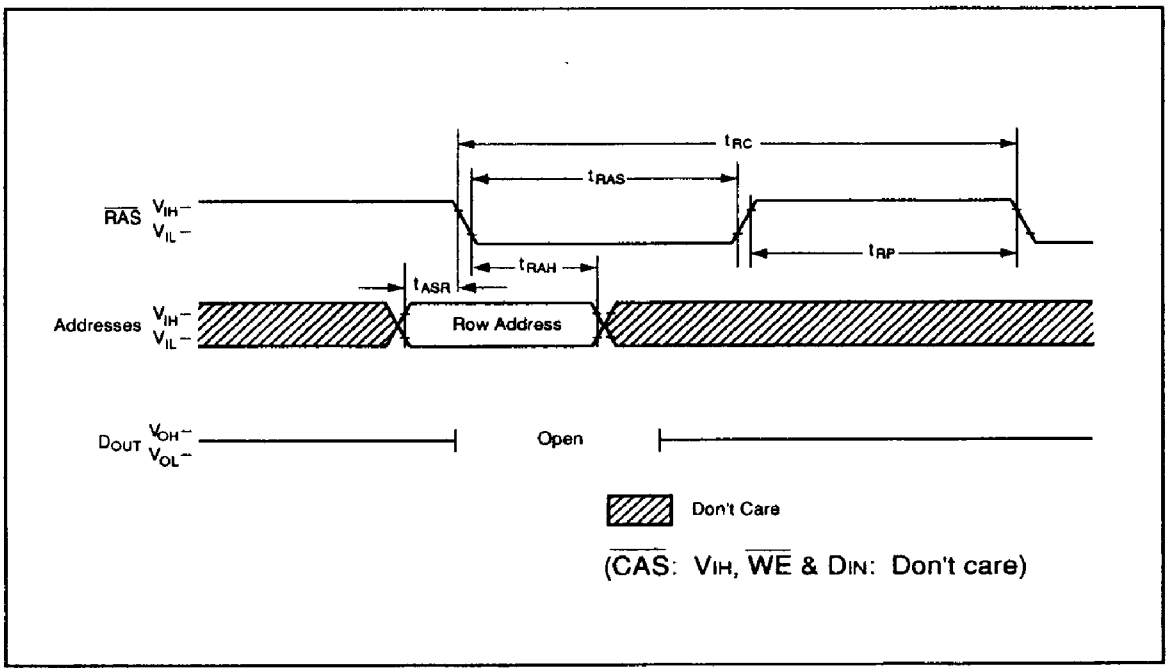
WRITE CYCLE TIMING (EARLY WRITE)



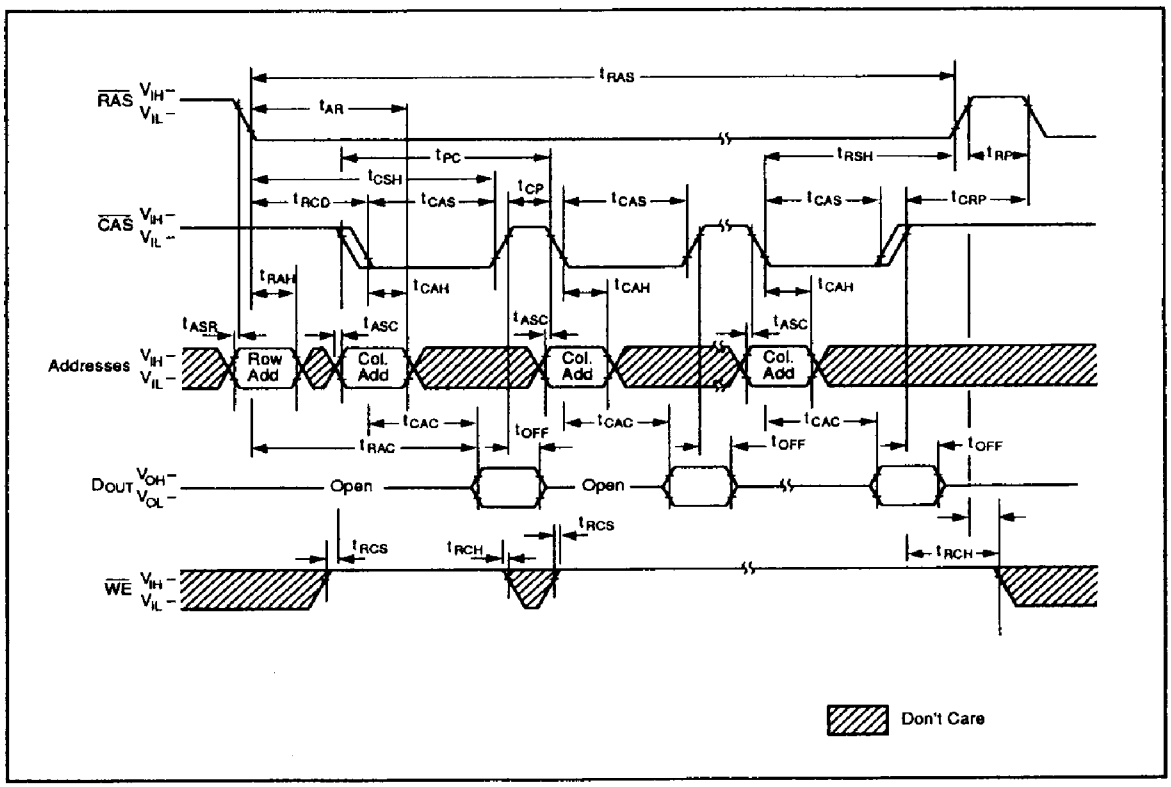
READ-WRITE READ-MODIFY-WRITE CYCLE



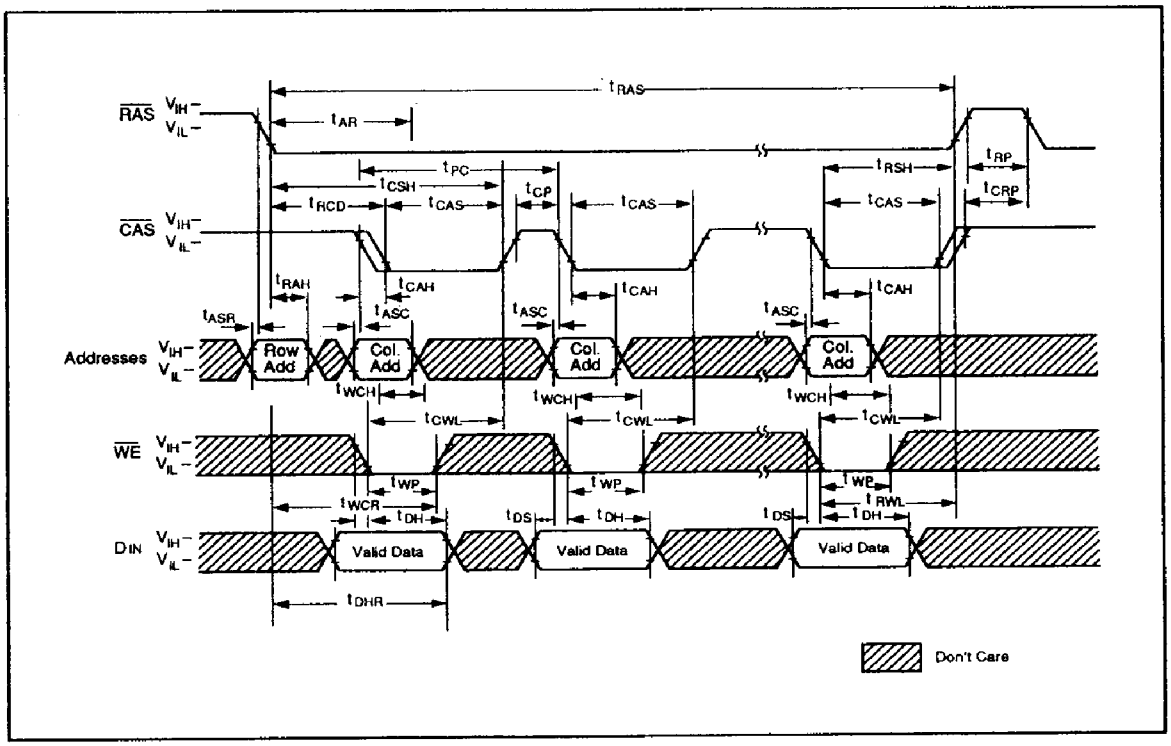
$\overline{\text{RAS}}$ ONLY REFRESH TIMING



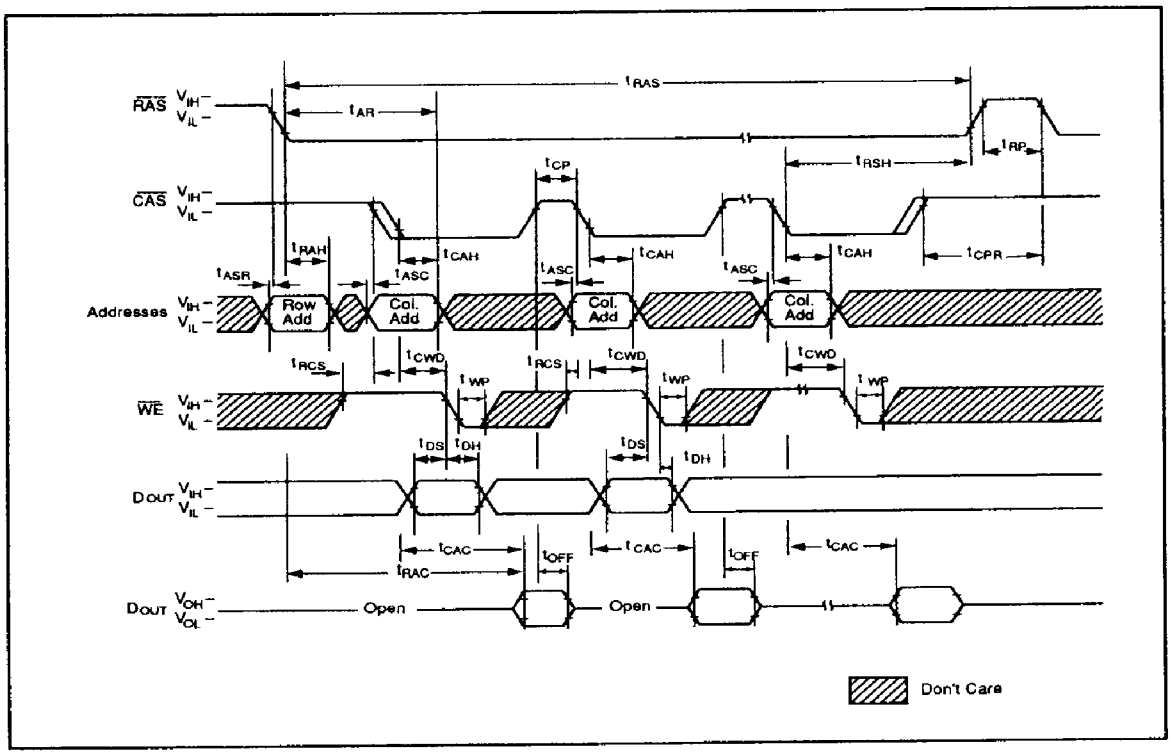
PAGE MODE READ CYCLE



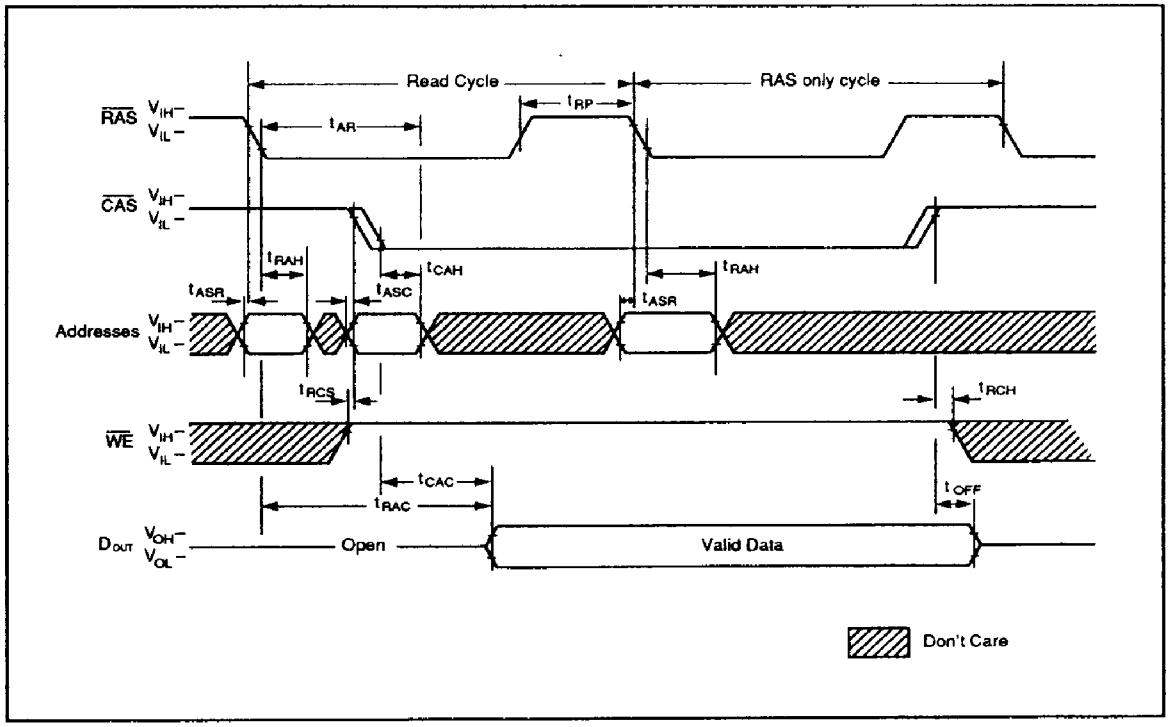
PAGE MODE WRITE CYCLE



PAGE MODE, READ-MODIFY-WRITE CYCLE

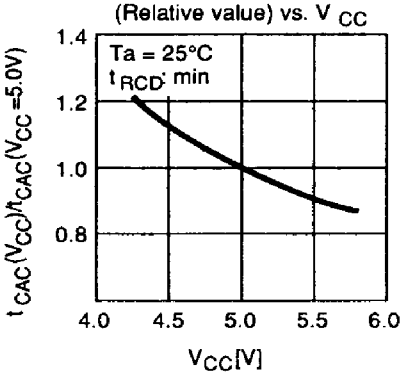


HIDDEN REFRESH

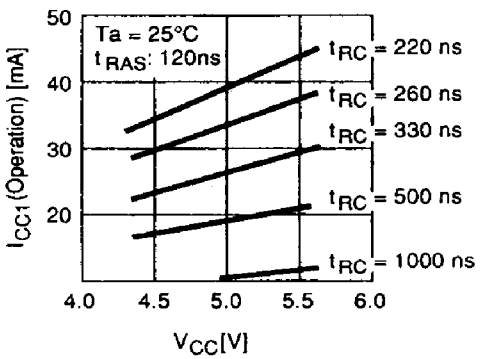


TYPICAL CHARACTERISTICS

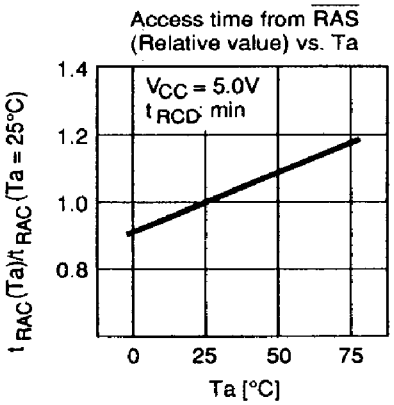
Access time from $\overline{RAS}$ (Relative value) vs. V_{CC}



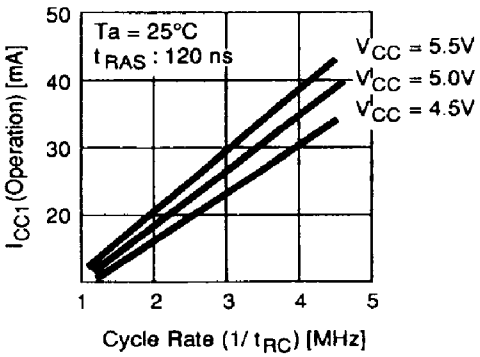
I_{CC1} (t_{RAS} : Constant) vs. V_{CC}



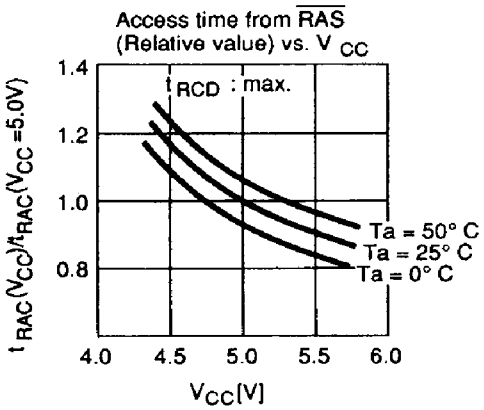
Access time from $\overline{RAS}$ (Relative value) vs. Ta



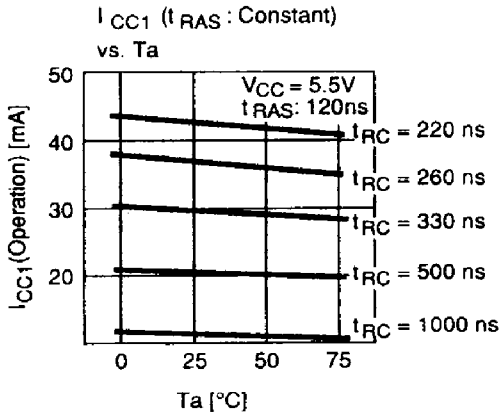
I_{CC1} (t_{RAS} : Constant) vs. Cycle rate



Access time from $\overline{RAS}$ (Relative value) vs. V_{CC}



I_{CC1} (t_{RAS} : Constant) vs. Ta



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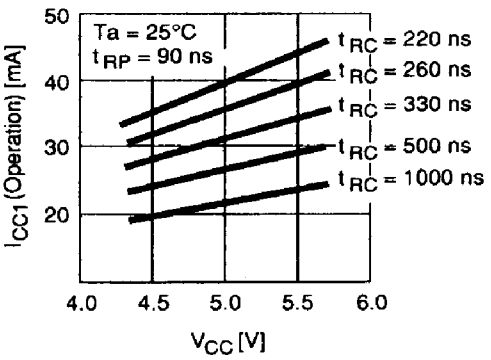
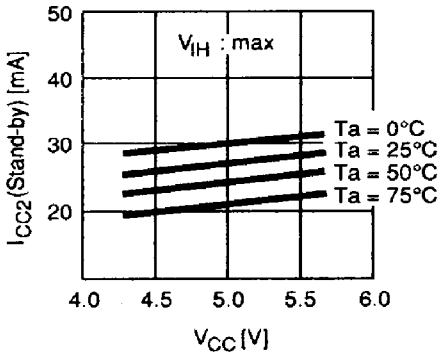
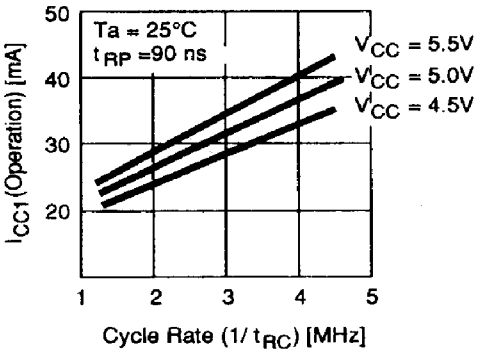
I_{CC1} (t_{RP} : Constant) vs. V_{CC}



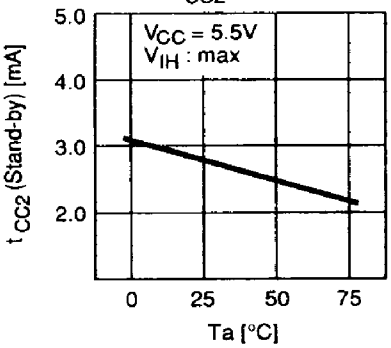
I_{CC2} vs. V_{CC}



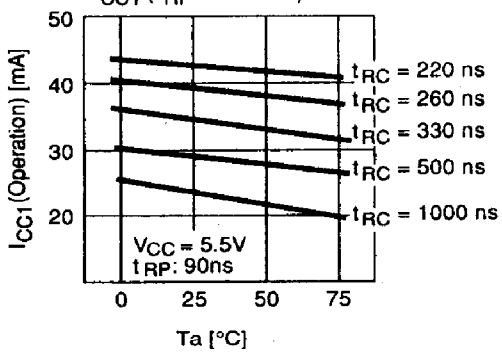
I_{CC1} (t_{RP} : Constant)
vs. Cycle rate



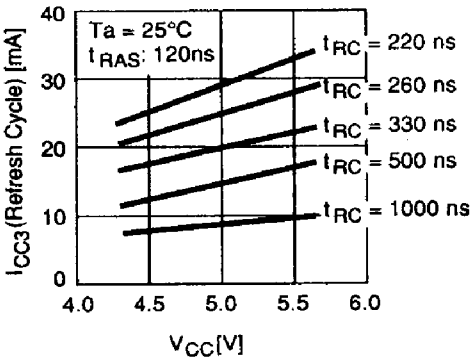
I_{CC2} vs. Ta



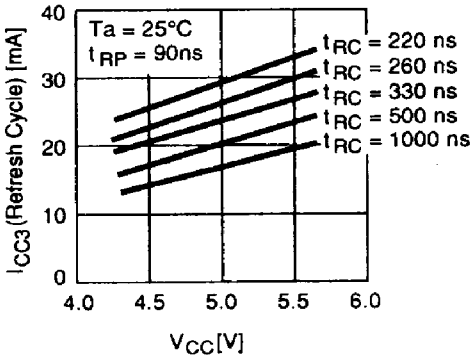
I_{CC1} (t_{RP}: Constant) vs. Ta



I_{CC3} (t_{RAS} : Constant) vs. V_{CC}



I_{CC3} (t_{RP}: Constant) vs. V_{CC}



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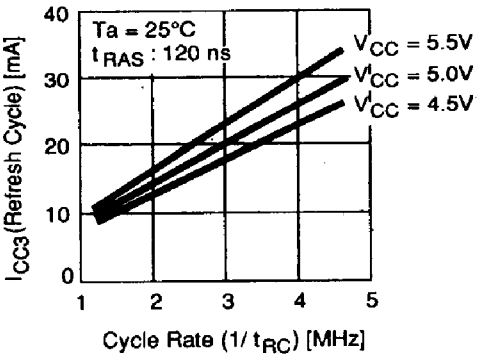
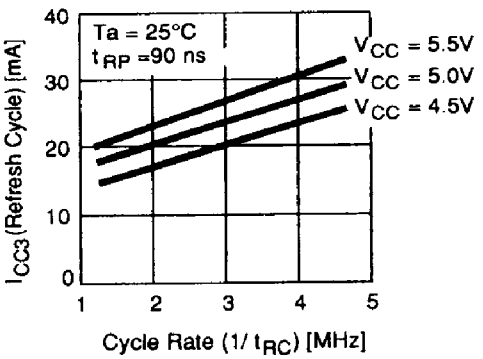
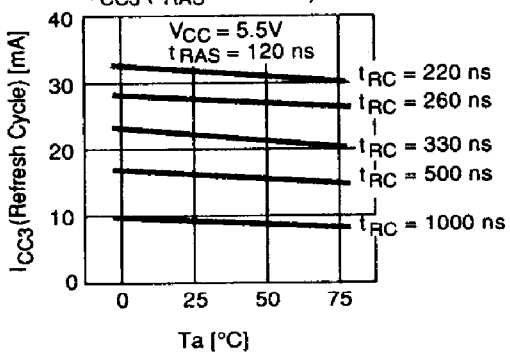
I_{CC3} (t_{RAS} : Constant) vs. Cycle rate



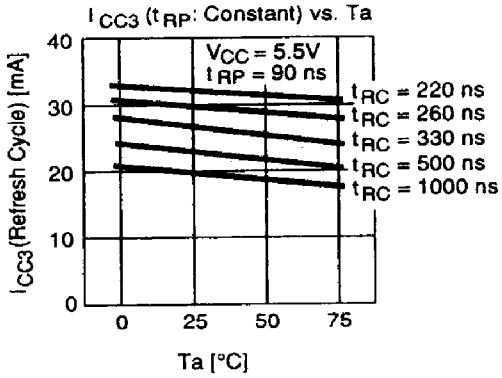
I_{CC3} (t_{RP} : Constant) vs. Cycle rate



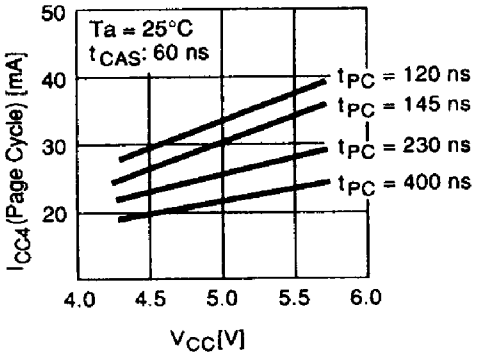
I_{CC3} (t_{RAS}: Constant) vs. Ta



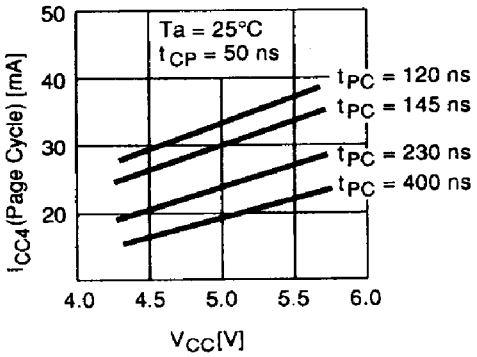
I_{CC3} (t_{RP}: Constant) vs. Ta



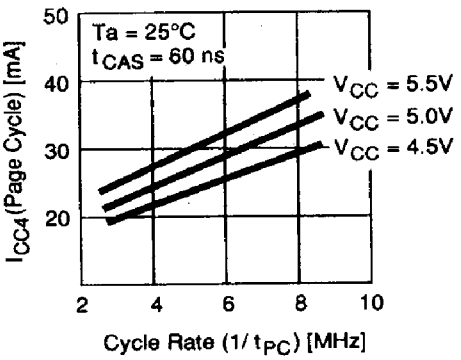
I_{CC4} (t_{CAS} : Constant)
vs. V_{CC}



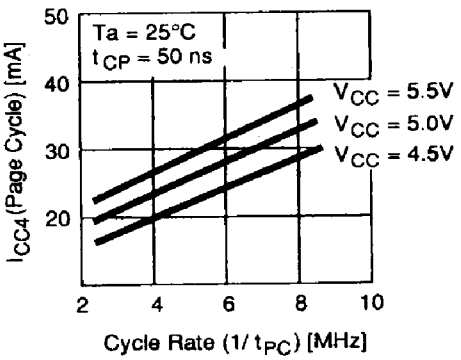
I_{CC4} (t_{CP} : Constant)
vs. V_{CC}



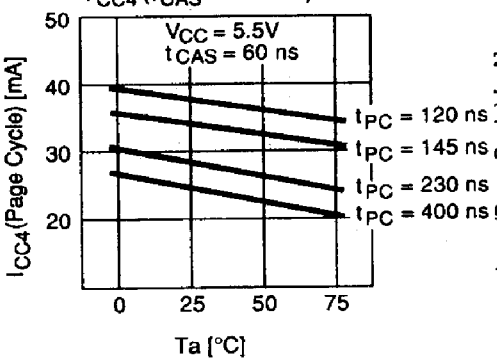
I_{CC4} (t_{CAS} : Constant)
vs. Cycle rate



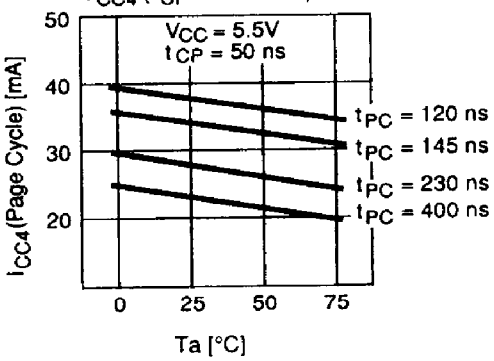
I_{CC4} (t_{CP}: Constant)
vs. Cycle rate



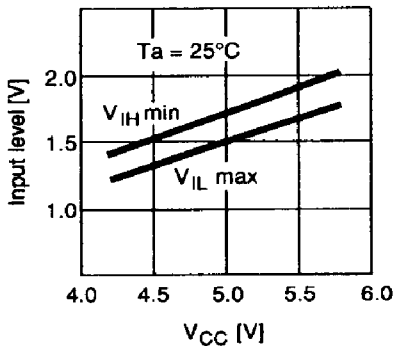
I_{CC4} (t_{CAS}: Constant) vs. Ta



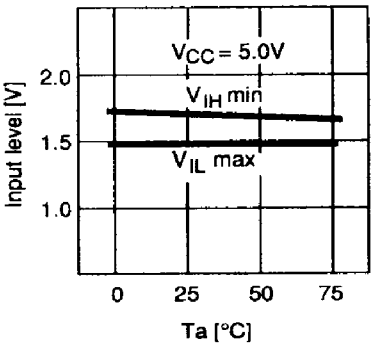
I_{CC4} (t_{CP} : Constant) vs. Ta



Address Input vs. V_{CC}

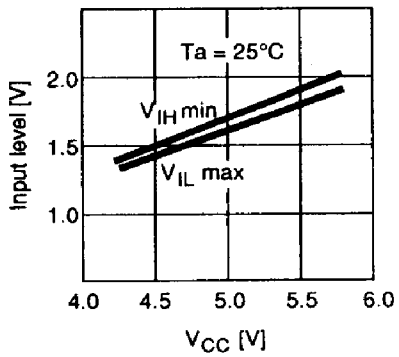


Address Input vs. Ta

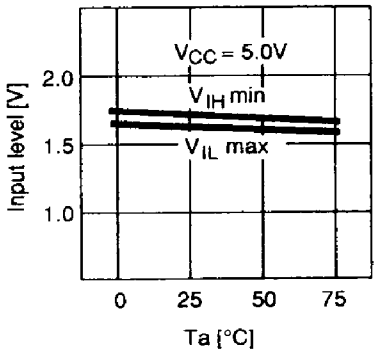


4

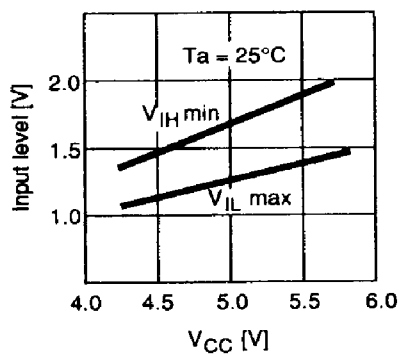
Data Input vs. V_{CC}



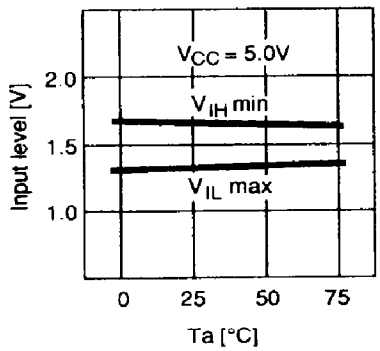
Data Input vs. Ta



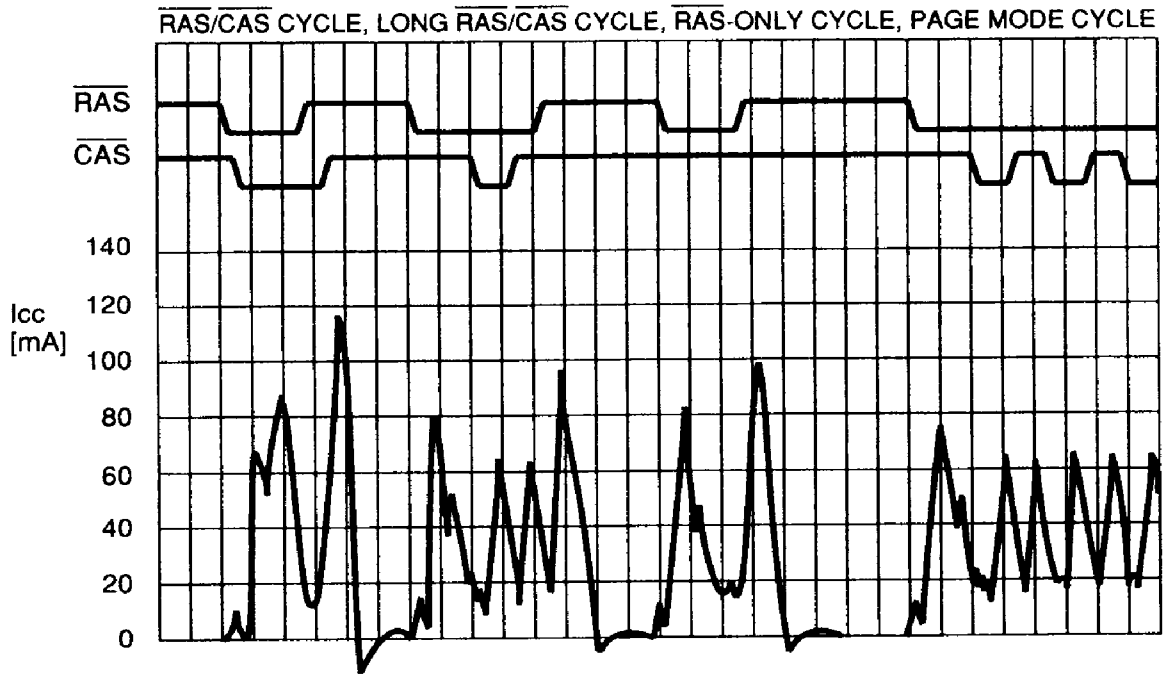
Clock Input vs. V_{CC}



Clock Input vs. Ta



(Vcc = 5.5V, Ta = 25°C, 50ns/div)



MSM3764A BIT MAP (PHYSICAL-DECIMAL)