CACHE DATA SRAM

DUAL 4K x 18 SRAM, SINGLE 8K x 18 SRAM

CONFIGURABLE CACHE DATA SRAM

FEATURES

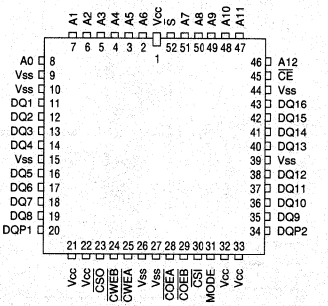
- Automatic WRITE cycle completion
- Operates as two 4K x 18 SRAMs with common addresses and data; also configurable as a single 8K x 18 SRAM
- Automatically controlled input address latches
- Built-in input data latches
- Separate upper and lower Byte Select
- Fast access times: 24 and 28ns allow operation with 33 MHz and 25 MHz microprocessor systems
- Fast Output Enable: 8ns
- Parity bits provided for large cache applications such as secondary cache for the Intel 80486 microprocessor
- Directly compatible with the Intel 82485 cache controller

OPTIONS

	MARKING
• Timing	
24ns access (33 MHz)	-24
28ns access (25 MHz)	-28
• Packages	
52-pin PLCC	EJ
52-pin PQFP	LG

PIN ASSIGNMENT (Top View)

52-Pin PLCC (D-3)
52-Pin PQFP (D-4)



GENERAL DESCRIPTION

The MT56C2818 is one of a family of fast SRAM cache memories. It employs a high-speed, low-power design using a four-transistor memory cell. It is fabricated using double-layer polysilicon, double-layer metal CMOS technology.

The MT56C2818 is a highly integrated cache data memory building block. A mode control pin (MODE) determines the configuration of the memory. When this pin is held LOW, the device functions as an 8K-word by 18-bit SRAM. When the mode pin is HIGH, the device is configured as a dual 4K-word by 18-bit SRAM.

Strobe ($\overline{S}$) controls the on-chip address and data latches. During READ and WRITE cycles the address latch is always transparent except for the time period ^{t}ALO following the rising edge of $\overline{S}$. The addresses are "locked out" during this time.

$\overline{S}$ has no effect on the data latch during a READ cycle. During a WRITE cycle, data is latched on the rising edge of $\overline{S}$. The rising edge of $\overline{S}$ also initiates the completion of the WRITE cycle.

The memory functions are controlled by the chip select ($\overline{CE}$, $\overline{CS0}$ and $\overline{CS1}$), output enable ($\overline{COEA}$ and $\overline{COEB}$) and write enable ($\overline{CWEA}$ and $\overline{CWEB}$) signals.

In either the DIRECT MAPPED (direct) or TWO-WAY SET ASSOCIATIVE (dual) operational modes, $\overline{CE}$ is a global chip enable, while $\overline{CS0}$ and $\overline{CS1}$ control lower and upper byte selection for READ and WRITE operations. Power consumption may be reduced by keeping either $\overline{CE}$ inactive (HIGH), or $\overline{CS0}$ and $\overline{CS1}$ inactive (HIGH) as much as possible.

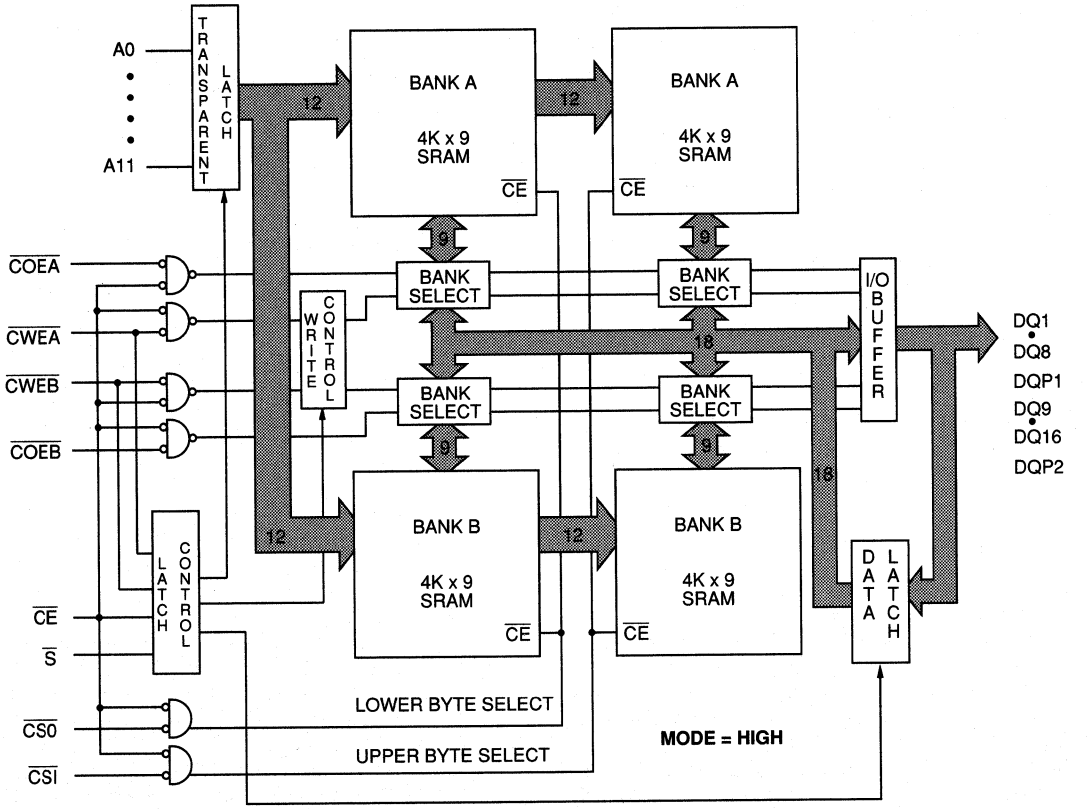
Outputs are enabled on a HIGH to LOW transition of $\overline{COEA}$ or $\overline{COEB}$. In the dual mode, bank "A" or bank "B" may be enabled. In the direct mode, $\overline{COEA}$ and $\overline{COEB}$ should be connected together externally and used as a single output enable. Alternately, $\overline{COEA}$ or $\overline{COEB}$ can be tied LOW externally, allowing the other signal to control the outputs.

Write enable is activated on a HIGH to LOW transition of $\overline{CWEA}$ or $\overline{CWEB}$. In the dual mode, data may be written to bank "A" or bank "B". In the direct mode, $\overline{CWEA}$ and $\overline{CWEB}$ should be connected together externally and used as a single write enable. Alternately, $\overline{CWEA}$ or $\overline{CWEB}$ can be tied LOW externally, allowing the other signal to control the write function.

The MT56C2818 operates from a +5V power supply and all inputs and outputs are fully TTL compatible.

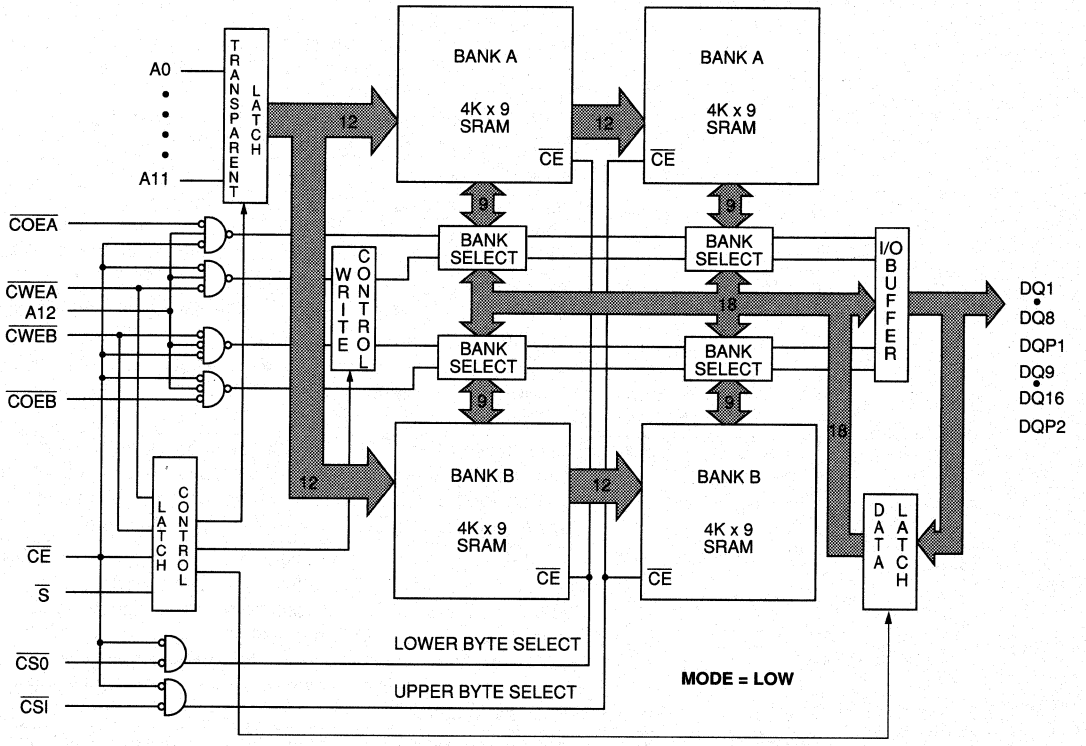
FUNCTIONAL BLOCK DIAGRAM

DUAL 4K x 18
(TWO-WAY SET ASSOCIATIVE)



FUNCTIONAL BLOCK DIAGRAM
($\overline{COEA}$ = $\overline{COEB}$; $\overline{CWEA}$ = $\overline{CWEB}$)

8K x 18
(DIRECT MAP)



CACHE DATA/LATCHED SRAM

PIN DESCRIPTIONS

PLCC PIN NUMBER(S)	SYMBOL	TYPE	DESCRIPTION
8, 7, 6, 5, 4, 3, 2, 51, 50, 49, 48, 47	A0-A11	Input	Address Inputs: A0-A11 are always sampled (transparent latch) except for the time ^{t}WAH and ^{t}ALO following the rising edge of $\overline{S}$.
46	A12	Input	Address Input: This input is the high order address bit in the direct 8K x 18 configuration. It is not used in the dual 4K x 18 configuration.
52	$\overline{S}$	Input	Strobe: This signal controls the internal data and address latches. The address latch is always transparent except for the time period ^{t}ALO following the rising edge of $\overline{S}$. The addresses are "locked out" during this time period. $\overline{S}$ does not affect the data latch during a READ cycle. During a WRITE cycle the rising edge of $\overline{S}$ latches the data. The rising edge also initiates the termination of the WRITE cycle.
31	MODE	Input	Mode Select: This controls the device configuration. When this pin is tied HIGH, the device is in the dual 4K x 18 configuration. When the pin is tied LOW, the device is configured as an 8K x 18 SRAM.
23, 30	$\overline{CS0}$, $\overline{CS1}$	Input	Chip Selects: These signals are used to select the upper and lower bytes for both READ and WRITE operations. When $\overline{CS0}$ is LOW, DQ1-DQ8 and DQP1 are enabled. When $\overline{CS1}$ is LOW, DQ9-DQ16 and DQP2 are enabled. Significant power savings can be achieved by keeping $\overline{CS0}$ and $\overline{CS1}$ inactive as much as possible.
45	$\overline{CE}$	Input	Chip Enable: When $\overline{CE}$ is LOW, the device is enabled. It is a global control signal that activates both bank "A" and bank "B" for READ or WRITE operations. Significant power savings can be achieved by keeping $\overline{CE}$ inactive as much as possible.
28, 29	$\overline{COEA}$, $\overline{COEB}$	Input	Output Enable: In the dual configuration, the signal that is LOW enables bank "A" or "B". Simultaneous LOW assertion will deselect both banks. In the direct mode, these signals should be externally connected and, when asserted LOW, allow A12 to determine which memory bank is enabled. Alternately, $\overline{COEA}$ or $\overline{COEB}$ can be tied LOW externally, allowing the other signal to control the outputs.
25, 24	$\overline{CWEA}$, $\overline{CWEB}$	Input	Write Enable: In the dual configuration, the signal that is LOW enables a data write to the addressed memory location. In the direct mode, these signals should be externally connected and, when asserted LOW, allow A12 to determine which memory bank is written. Alternately, $\overline{CWEA}$ or $\overline{CWEB}$ can be tied LOW externally, allowing the other signal to control the write function.
20, 34	DQP1, DQP2	Input/ Output	Parity Data I/O: DQP1 is the parity bit for the lower byte. DQP2 is the parity bit for the upper byte.
11, 12, 13, 14, 16 17, 18, 19, 35, 36, 37 38, 40, 41, 42, 43	DQ1-DQ16	Input/ Output	SRAM Data I/O: lower byte is DQ1-DQ8; upper byte is DQ9-DQ16.
1, 21, 22, 32, 33,	Vcc	Supply	Power Supply: +5V ±5%
9, 10, 15, 26, 27, 39, 44	Vss	Supply	Ground: GND

TRUTH TABLE
DUAL 4K x 18 (MODE PIN = HIGH)

OPERATION	$\overline{CE}$	$\overline{CS0}$	$\overline{CS1}$	$\overline{COEA}$	$\overline{COEB}$	$\overline{CWEA}$	$\overline{CWEB}$
Outputs High-Z, WRITE disabled	H	X	X	X	X	X	X
Outputs High-Z, WRITE disabled	X	H	H	X	X	X	X
Outputs High-Z	X	X	X	H	H	X	X
Outputs High-Z	X	X	X	L	L	X	X
READ DQ1-DQ8, DQP1 bank A	L	L	H	L	H	H	H
READ DQ1-DQ8, DQP1 bank B	L	L	H	H	L	H	H
READ DQ9-DQ16, DQP2 bank A	L	H	L	L	H	H	H
READ DQ9-DQ16, DQP2 bank B	L	H	L	H	L	H	H
READ DQ1-DQ16, DQP1, DQP2 bank A	L	L	L	L	H	H	H
READ DQ1-DQ16, DQP1, DQP2 bank B	L	L	L	H	L	H	H
WRITE DQ1-DQ8, DQP1 bank A	L	L	H	X	X	L	H
WRITE DQ1-DQ8, DQP1 bank B	L	L	H	X	X	H	L
WRITE DQ9-DQ16, DQP2 bank A	L	H	L	X	X	L	H
WRITE DQ9-DQ16, DQP2 bank B	L	H	L	X	X	H	L
WRITE DQ1-DQ16, DQP1, DQP2 bank A	L	L	L	X	X	L	H
WRITE DQ1-DQ16, DQP1, DQP2 bank B	L	L	L	X	X	H	L
WRITE DQ1-DQ8, DQP1 banks A & B	L	L	H	X	X	L	L
WRITE DQ9-DQ16, DQP2 banks A & B	L	H	L	X	X	L	L
WRITE DQ1-DQ16, DQP1, DQP2 banks A & B	L	L	L	X	X	L	L

TRUTH TABLE
8K x 18 (MODE PIN = LOW)

OPERATION	$\overline{CE}$	$\overline{CS0}$	$\overline{CS1}$	$\overline{COEA}$	$\overline{COEB}$	$\overline{CWEA}$	$\overline{CWEB}$
Outputs High-Z, WRITE disabled	H	X	X	X	X	X	X
Outputs High-Z, WRITE disabled	X	H	H	X	X	X	X
Outputs High-Z	X	X	X	H	H	X	X
READ DQ1-DQ8, DQP1	L	L	H	L	L	H	H
READ DQ9-DQ16, DQP2	L	H	L	L	L	H	H
READ DQ1-DQ16, DQP1, DQP2	L	L	L	L	L	H	H
WRITE DQ1-DQ8, DQP1	L	L	H	X	X	L	L
WRITE DQ9-DQ16, DQP2	L	H	L	X	X	L	L
WRITE DQ1-DQ16, DQP1, DQP2	L	L	L	X	X	L	L

NOTE: When mode pin is LOW, $\overline{COEA}$ and $\overline{COEB}$ must both be LOW to enable outputs. However, one signal can be tied LOW externally, allowing the other signal to control the outputs. Similarly $\overline{CWEA}$ and $\overline{CWEB}$ must both be LOW to enable a WRITE cycle. Either $\overline{CWEA}$ or $\overline{CWEB}$ can be tied LOW externally, allowing the other signal to control the WRITE function.

ABSOLUTE MAXIMUM RATINGS*

Voltage on Vcc Supply Relative to Vss ..... -1.0V to +7.0V
Storage Temperature (Plastic) ..... -55°C to +150°C
Power Dissipation (PLCC) 1.2W
Power Dissipation (PQFP) 1.2W
Short Circuit Output Current 50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

($0°C \le T_A \le 70°C$; Vcc = 5V ±5%)

DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS	NOTES
Power Supply Voltage		Vcc	4.75	5.25	V	
Input High Voltage		V_{IH}	2.2	Vcc +0.3	V	1
Input Low Voltage		V_{IL}	-0.3	0.8	V	1, 2
Input Leakage Current	V_{IN} = GND to Vcc	I_{LI}	-5	5	µA	
Output Leakage Current	$V_{I/O}$ = GND to Vcc Output(s) Disabled	I_{LO}	-5	5	µA	
Output Low Voltage	I_{OL} = 4.0mA	V_{OL}		0.4	V	1
Output High Voltage	I_{OH} = -1.0mA	V_{OH}	2.4		V	1

DESCRIPTION	CONDITIONS		SYMBOL	TYP	MAX	UNITS	NOTES
Power Supply Current: Average Operating Current	100% Duty Cycle V_{IN} = GND to Vcc		I_{CC1}	145	220	mA	
Power Supply Current: Average Operating Current	50% Duty Cycle V_{IN} = GND to Vcc		I_{CC2}	70	120	mA	
Power Supply Current: CMOS Standby	$\overline{CS1} \ge$ Vcc -0.2V and $\overline{CS0} \ge$ Vcc -0.2V or Vcc = MAX, f = 0 $V_{IL} \le$ Vss +0.2V $V_{IH} \ge$ Vcc -0.2V	CE ≤ Vss +0.2V	I_{SB1}	20	20	mA	

CAPACITANCE

DESCRIPTION	CONDITIONS	SYMBOL	MAX	UNITS	NOTES
Input Capacitance	T_A = 25°C, f = 1 MHz Vcc = 5V	C_I	6	pF	3
Input/Output Capacitance		$C_{I/O}$	6	pF	3

PQFP THERMAL CONSIDERATIONS

DESCRIPTION	CONDITIONS	SYMBOL	MAX	UNITS	NOTES
Thermal resistance – Junction to Ambient	Still Air	θ_{JA}	100	°C/W	
Thermal resistance – Junction to Case		θ_{JC}	45	°C/W	
Maximum Case Temperature		TC	110	°C	

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Note 8) ($0°C \le T_A \le +70°C$, V_{CC} = 5V ±5%)

DESCRIPTION		-24		-28			
	SYM	MIN	MAX	MIN	MAX	UNITS	NOTES
READ Cycle							
READ cycle time	^tRC	24		28		ns	4, 5
Address access time (A0-A11)	^tAA		24		28	ns	4, 5
A12 address access time	^tA12A		17		19	ns	
Chip Enable access time	^tACE		23		26	ns	
Chip Select access time	^tACS		23		26	ns	
Output Enable access time	^tAOE		8		10	ns	
Output hold from address change	^tOH	3		3		ns	
Chip Select/Chip Enable to output Low-Z	^tLZCS	3		3		ns	
Output Enable to output Low-Z	^tLZOE	2		2		ns	
Chip deselect/chip disable to output High-Z	^tHZCS		15		15	ns	6
Output disable to output High-Z	^tHZOE	2	10	2	10	ns	6
WRITE Cycle							
WRITE cycle time	^tWC	24		28		ns	
$\overline{S}$ strobe HIGH level width	^tSWH	11		14		ns	7
$\overline{S}$ strobe LOW level width	^tSWL	11		14		ns	7
WRITE, Chip Enable/Write Enable to $\overline{S}$ strobe setup	^tWSS	10		12		ns	7
WRITE, Chip Enable/Write Enable to $\overline{S}$ strobe hold	^tWSH	2		2		ns	7
WRITE, address setup to $\overline{S}$ strobe	^tWAS	13		16		ns	7
WRITE, address hold to $\overline{S}$ strobe	^tWAH	2		2		ns	7
Address latch closed	^tALO		8		8	ns	7
Chip Select to $\overline{S}$ strobe setup	^tCSS	13		16		ns	7
Chip Select to $\overline{S}$ strobe hold	^tCSH	2		2		ns	7
Data to $\overline{S}$ strobe setup	^tDSS	5		5		ns	7
Data to $\overline{S}$ strobe hold	^tDSH	3		3		ns	7
Write Enable to output in High-Z	^tHZWE		15		15	ns	6
Write Enable to output in Low-Z	^tLZWE	8		8		ns	

AC TEST CONDITIONS

Input pulse levels	Vss to 3.0V
Input rise and fall times	3ns
Input timing reference levels	1.5V
Output reference levels	1.5V
Output load (see notes 6 and 8).	Reference Figure 1

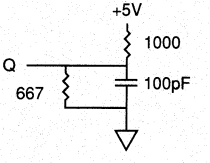


Fig. 1 OUTPUT LOAD EQUIVALENT

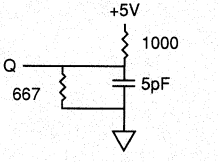
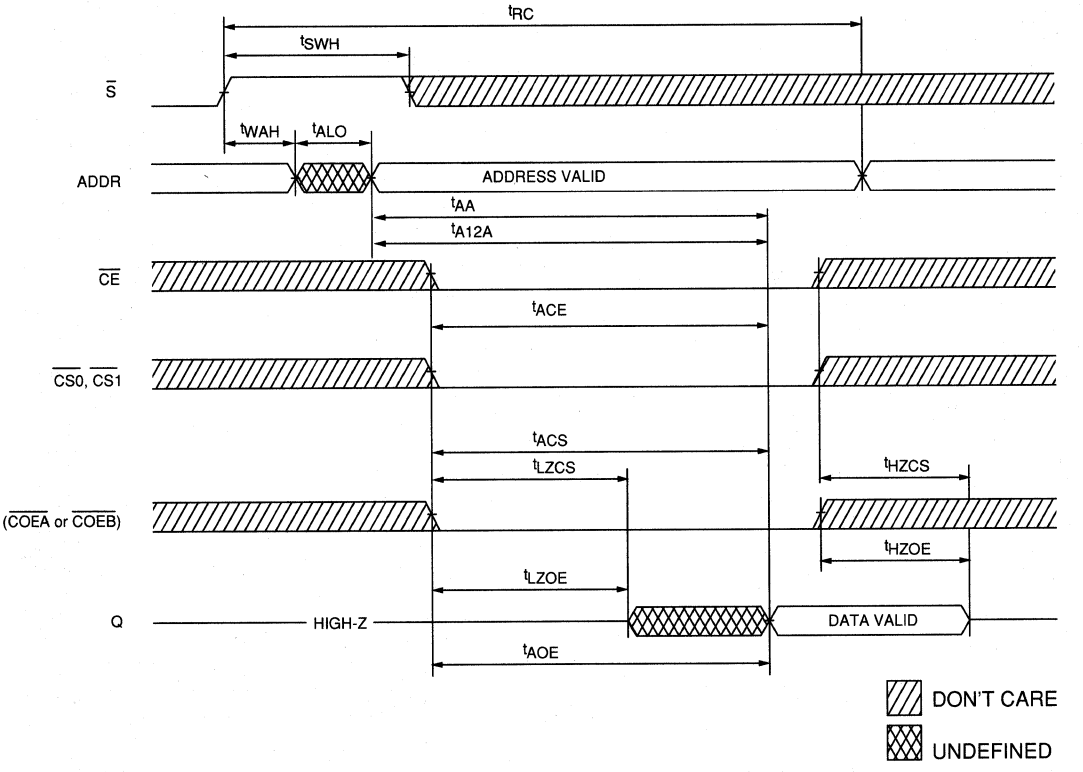


Fig. 2 OUTPUT LOAD EQUIVALENT

NOTES

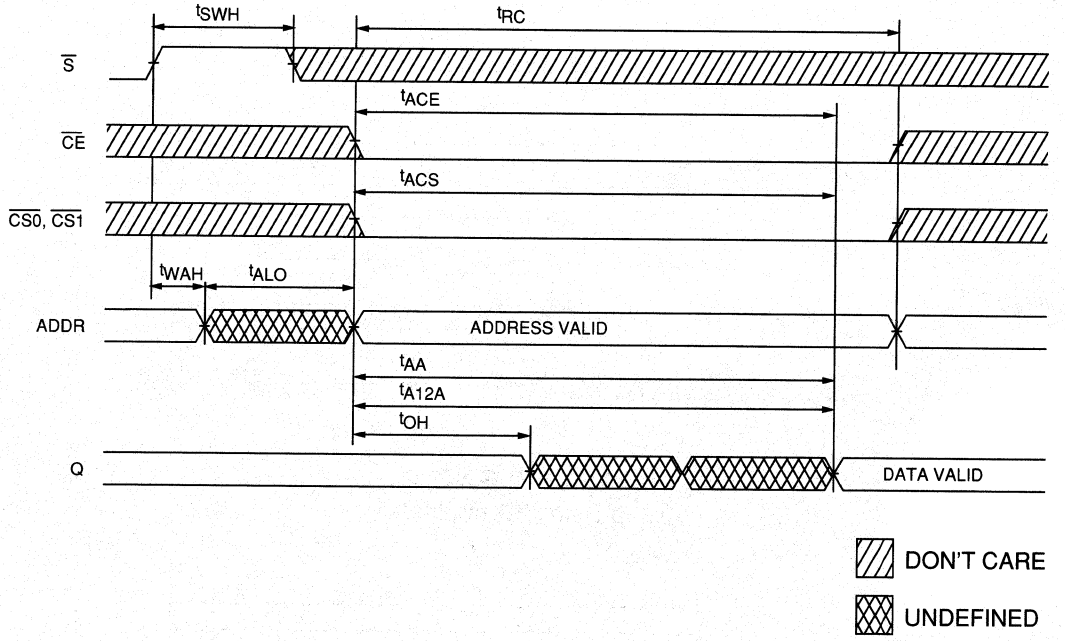
1. All voltages referenced to Vss (GND).
2. -3V for pulse width < 20ns.
3. This parameter is sampled.
4. $\overline{CWE}$ is HIGH for a READ cycle.
5. All READ cycle timings are referenced from the last valid address to the first transitioning address.
6. ^tHZCS, ^tHZOE, and ^tHZWE are specified with CL = 5pF as in Fig. 2. Transition is measured ±500mV from steady state voltage.
7. Self-timed WRITE parameter.
8. Output timing should be derated by 1ns for each additional 30pf of capacitive loading.

READ CYCLE NO. 1
($\overline{CWEA}$ = $\overline{CWEB}$ = V_{IH})

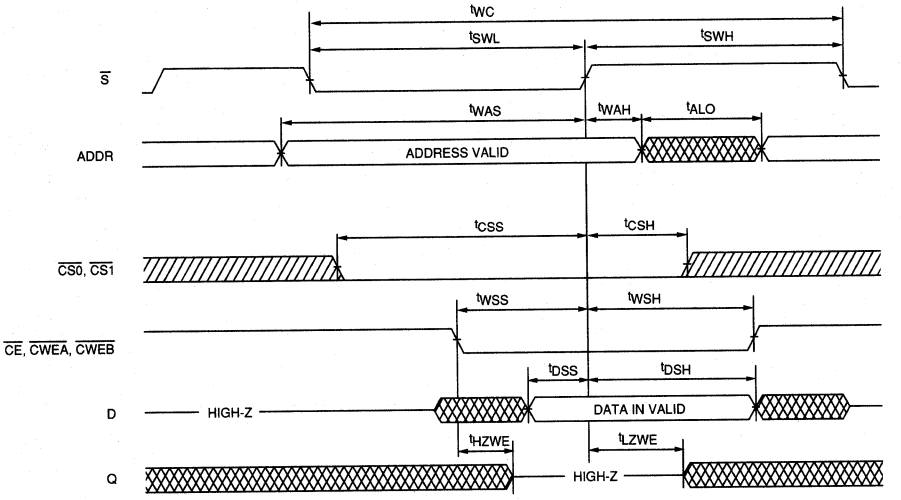


READ CYCLE NO. 2

($\overline{COEA}$ and/or $\overline{COEB}$ = V_{IL})
($\overline{CWEA}$ = $\overline{CWEB}$ = V_{IH})



WRITE CYCLE NO. 1
(Write Enable/Chip Enable Controlled)



WRITE CYCLE NO. 2
(Chip Select Controlled)