VRAM

256K x 4 DRAM WITH 512 x 4 SAM

FEATURES

- Industry-standard pinout, timing and functions
- High-performance, CMOS silicon-gate process
- Single +5V ±10% power supply
- Inputs and outputs are fully TTL compatible
- Refresh modes: RAS-ONLY, CAS-BEFORE-RAS (CBR) and HIDDEN
- 512-cycle refresh within 16.7ms
- Optional FAST-PAGE-MODE access cycles
- Dual-port organization: 256K x 4 DRAM port
  512 x 4 SAM port
- No refresh required for serial access memory
- Low power: 15mW standby; 275mW active, typical
- Fast access times: 70ns random, 22ns serial
  60ns random, 18ns serial*

SPECIAL FUNCTIONS

- JEDEC Standard Function set
- PERSISTENT MASKED WRITE
- SPLIT READ TRANSFER
- WRITE TRANSFER/SERIAL INPUT
- ALTERNATE WRITE TRANSFER
- BLOCK WRITE

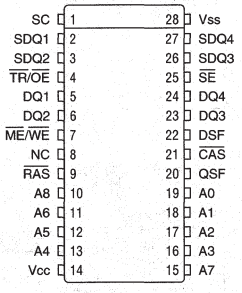
OPTIONS — MARKING

- Timing (DRAM, SAM [cycle/access])
  - 60ns, 18ns/18ns — -6*
  - 70ns, 22ns/22ns — -7
  - 80ns, 25ns/25ns — -8
- Packages
  - Plastic SOJ (400 mil) — DJ
  - Plastic ZIP (375 mil) — Z
- Part Number Example: MT42C4256DJ-7

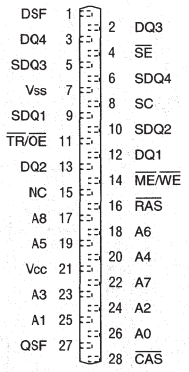
*60ns (-6) specifications are preliminary; consult factory for availability.

PIN ASSIGNMENT (Top View)

28-Pin SOJ (SDB-1)



28-Pin ZIP (SDA-1)



GENERAL DESCRIPTION

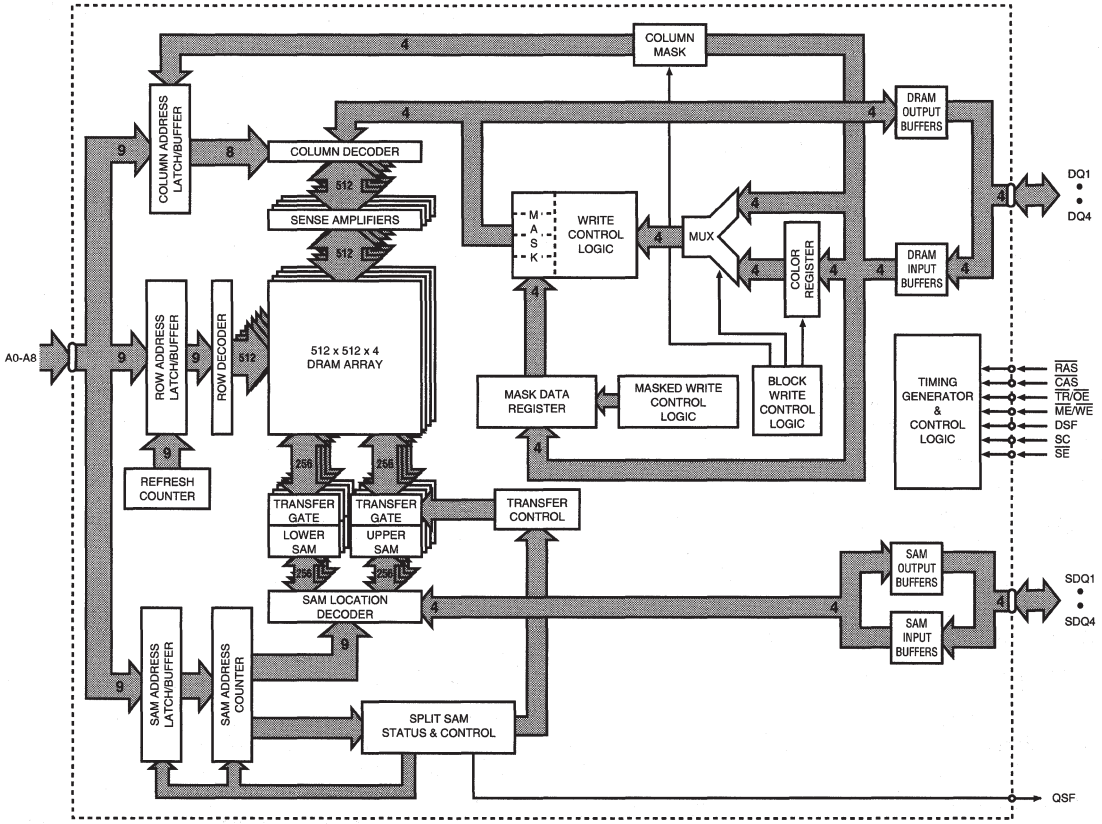
The MT42C4256 is a high-speed, dual-port CMOS dynamic random access memory or video RAM (VRAM) containing 1,048,576 bits. These bits may be accessed by a 4-bit-wide DRAM port or by a 512 x 4-bit serial access memory (SAM) port. Data may be transferred bidirectionally between the DRAM and the SAM.

The DRAM portion of the VRAM is similar to the MT4C4256 (256K x 4 DRAM). Four 512-bit data registers make up the SAM portion of the VRAM. Data I/O and internal data transfer are accomplished using three separate bidirectional data paths; the 4-bit random access I/O port, the four internal 512-bit-wide paths between the DRAM and the SAM, and the 4-bit serial I/O port for the SAM. The rest of the circuitry consists of the control, timing and address decoding logic.

Each port may be operated asynchronously and independently of the other except when data is being transferred internally. As with all DRAMs, the VRAM must be refreshed to maintain data. Refresh cycles must be timed so that all 512 combinations of RAS addresses are executed at least every 16.7ms (regardless of sequence). Micron recommends evenly spaced refresh cycles for maximum data integrity. An internal transfer between the DRAM and the SAM counts as a refresh cycle. The SAM portion of the VRAM is fully static and does not require any refresh.

The operation and control of the MT42C4256 are optimized for high-performance graphics and communication designs. The dual-port architecture is well suited to buffering the sequential data used in raster graphics display, serial and parallel networking and data communications. Special features, such as SPLIT READ TRANSFER and BLOCK WRITE allow further enhancements to system performance.

FUNCTIONAL BLOCK DIAGRAM



PIN DESCRIPTIONS

SOJ PIN NUMBERS	ZIP PIN NUMBERS	SYMBOL	TYPE	DESCRIPTION
1	8	SC	Input	Serial Clock: Clock input to the serial address counter for the SAM registers.
4	11	$\overline{TR/OE}$	Input	Transfer Enable: Enables an internal TRANSFER operation at $\overline{RAS}$ (H → L), or Output Enable: Enables the DRAM output buffers when taken LOW after $\overline{RAS}$ goes LOW ($\overline{CAS}$ must also be LOW); otherwise, the output buffers are in a High-Z state.
7	14	$\overline{ME/WE}$	Input	Mask Enable: If $\overline{ME/WE}$ is LOW at the falling edge of $\overline{RAS}$ a MASKED WRITE cycle is performed, or Write Enable: $\overline{ME/WE}$ is also used to select a READ ($\overline{ME/WE}$ = H) or WRITE ($\overline{ME/WE}$ = L) cycle when accessing the DRAM. This includes a READ TRANSFER ($\overline{ME/WE}$ = H) or WRITE TRANSFER ($\overline{ME/WE}$ = L).
25	4	$\overline{SE}$	Input	Serial Port Enable: $\overline{SE}$ enables the serial I/O buffers and allows a serial READ or WRITE operation to occur; otherwise, the output buffers are in a High-Z state. $\overline{SE}$ is also used during a WRITE TRANSFER operation to indicate whether a WRITE TRANSFER or a SERIAL INPUT MODE ENABLE cycle is performed.
22	1	DSF	Input	Special Function Select: DSF is used to indicate which special functions (BLOCK WRITE, MASKED WRITE vs. PERSISTENT MASKED WRITE, etc.) are used on a particular access cycle.
9	16	$\overline{RAS}$	Input	Row Address Strobe: $\overline{RAS}$ is used to clock-in the 9 row-address bits and strobe the $\overline{ME/WE}$, $\overline{TR/OE}$, DSF, $\overline{SE}$, $\overline{CAS}$ and DQ inputs. It also acts as the master chip enable and must fall for initiation of any DRAM or TRANSFER cycle.
21	28	$\overline{CAS}$	Input	Column Address Strobe: $\overline{CAS}$ is used to clock-in the 9 column-address bits, enable the DRAM output buffers (along with $\overline{TR/OE}$), and strobe the DSF input.
19, 18, 17, 16, 13, 12, 11, 15, 10	26, 25, 24, 23, 20, 19, 18, 22, 17	A0-A8	Input	Address Inputs: For the DRAM operation, these inputs are multiplexed and clocked by $\overline{RAS}$ and $\overline{CAS}$ to select one 4-bit word out of the 256K available. During TRANSFER operations, A0 to A8 indicate the DRAM row being accessed (when $\overline{RAS}$ goes LOW) and the SAM start address (when $\overline{CAS}$ goes LOW).
5, 6, 23, 24	12, 13, 2, 3	DQ1-DQ4	Input/ Output	DRAM Data I/O: Data input/output for DRAM cycles; inputs for Mask Data Register and Color Register load cycles, and DQ and Column Mask inputs for BLOCK WRITE.
2, 3, 26, 27	9, 10, 5, 6	SDQ1-SDQ4	Input/ Output	Serial Data I/O: Input, output, or High-Z.
20	27	QSF	Output	Split SAM Status: QSF indicates which half of the SAM is being accessed: LOW if address is 0-255, HIGH if address is 256-511.
8	15	NC	–	No Connect: This pin should be left either unconnected or tied to ground.
14	21	V_{CC}	Supply	Power Supply: +5V ±10%
28	7	V_{SS}	Supply	Ground

FUNCTIONAL DESCRIPTION

The MT42C4256 may be divided into three functional blocks (see Functional Block Diagram): the DRAM, the transfer circuitry, and the SAM. All of the operations described below are shown in the AC Timing Diagrams section of this data sheet and summarized in the Truth Table.

Note: *For dual-function pins, the function not being discussed will be surrounded by parentheses. For example, the TR/(OE) pin will be shown as TR/(OE) in references to transfer operations.*

DRAM OPERATION

DRAM REFRESH

Like any DRAM-based memory, the MT42C4256 VRAM must be refreshed to retain data. All 512 row-address combinations must be accessed within 16.7ms. The MT42C4256 supports CBR, RAS-ONLY and HIDDEN types of refresh cycles.

For the CBR REFRESH cycle, the row addresses are generated and stored in an internal address counter. The user need not supply any address data, but must simply perform 512 CBR cycles within the 16.7ms time period.

The refresh address must be generated externally and applied to A0-A8 inputs for RAS-ONLY refresh cycles. The DQ pins remain in a High-Z state for both the RAS-ONLY and CBR refresh cycles.

HIDDEN REFRESH cycles are performed by toggling RAS (and keeping CAS LOW) after a READ or WRITE cycle. This performs CBR cycles but does not disturb the DQ lines.

Any DRAM READ, WRITE, or TRANSFER cycle also refreshes the DRAM row being accessed. The SAM portion of the MT42C4256 is fully static and does not require any refreshing.

DRAM READ AND WRITE CYCLES

The DRAM portion of the VRAM is similar to standard 256K x 4 DRAMs. However, because several of the DRAM control pins are used for additional functions on this part, several conditions that were undefined or in "don't care" states for the DRAM are specified for the VRAM. These conditions are highlighted in the following discussion. In addition, the VRAM has several special functions that can be used when writing to the DRAM.

The 18 address bits that are used to select a 4-bit word from the 262,144 available are latched into the chip using the A0-A8, RAS and CAS inputs. First, the 9 row-address bits are set up on the address inputs and clocked into the part when RAS transitions from HIGH-to-LOW. Next, the 9 column address bits are set up on the address inputs and clocked-in when CAS goes from HIGH-to-LOW.

Note: *RAS also acts as a "master" chip enable for the VRAM. If RAS is inactive, HIGH, all other DRAM control pins (CAS, TR/OE, ME/WE, etc.) are "don't care" and may change state without effect. No DRAM or TRANSFER cycles will be initiated without RAS falling.*

For standard single-port DRAMs, the OE pin is a "don't care" when RAS goes LOW. However, for the VRAM, when RAS goes LOW, TR/(OE) selects between DRAM access or TRANSFER cycles. TR/(OE) must be HIGH at the RAS HIGH-to-LOW transition for all DRAM operations (except CBR, where it is "don't care").

If (ME)/WE is HIGH when CAS goes LOW, a DRAM READ operation is performed and the data from the memory cells selected will appear at the DQ1-DQ4 port. The (TR)/OE input must transition from HIGH-to-LOW some time after RAS falls to enable the DRAM output port.

For standard single-port DRAMs, WE is a "don't care" when RAS goes LOW. For the VRAM, ME/(WE) is used, when RAS goes LOW, to select between a MASKED WRITE cycle and a normal WRITE cycle. If ME/(WE) is LOW at the RAS HIGH-to-LOW transition, a MASKED WRITE operation is selected. For any DRAM access cycle (READ or WRITE), ME/(WE) must be HIGH at the RAS HIGH-to-LOW transition. If (ME)/WE is LOW before CAS goes LOW, a DRAM EARLY-WRITE operation is performed. If (ME)/WE goes LOW after CAS goes LOW, a DRAM LATE-WRITE operation is performed. Refer to the AC timing diagrams.

The VRAM can perform all the normal DRAM cycles including READ, EARLY-WRITE, LATE-WRITE, READ-MODIFY-WRITE, FAST-PAGE-MODE READ, FAST-PAGE-MODE WRITE (Late or Early), and FAST-PAGE-MODE READ-MODIFY-WRITE. Refer to the AC timing parameters and diagrams in the data sheet for more details on these operations.

NONPERSISTENT MASKED WRITE

The MASKED WRITE feature eliminates the need for a READ-MODIFY-WRITE cycle when changing only specific bits within a 4-bit word. The MT42C4256 supports two types of MASKED WRITE cycles, NONPERSISTENT MASKED WRITE and PERSISTENT MASKED WRITE.

If $\overline{ME}/(\overline{WE})$ and DSF are LOW at the $\overline{RAS}$ HIGH-to-LOW transition, a NONPERSISTENT MASKED WRITE is performed and the data (mask data) present on the DQ1-DQ4 inputs will be written into the mask data register. The mask data acts as an individual write enable for each of the four DQ1-DQ4 pins. If a LOW (logic "0") is written to a mask data register bit, the input port for that bit is disabled during the subsequent WRITE operation and no new data will be written to that DRAM cell location. A HIGH (logic "1") on a mask data register bit enables the input port and allows normal WRITE operation to proceed. Note that $\overline{CAS}$ is still HIGH. When $\overline{CAS}$ goes LOW, the bits present on the DQ1-DQ4 inputs will be either written to the DRAM (if the mask data bit is HIGH) or ignored (if the mask data bit is LOW). The DRAM contents that correspond to masked input bits will not be changed during the WRITE cycle. The MASKED WRITE is nonpersistent (must be re-entered at every $\overline{RAS}$ cycle) if DSF is LOW when $\overline{RAS}$ goes LOW. The mask data register is cleared at the end of every NONPERSISTENT MASKED WRITE. FAST PAGE MODE can be used with NONPERSISTENT MASKED WRITE to write several column locations in an addressed row. The same mask is used during the entire FAST-PAGE-MODE $\overline{RAS}$ cycle. An example NONPERSISTENT MASKED WRITE cycle is shown in Figure 1.

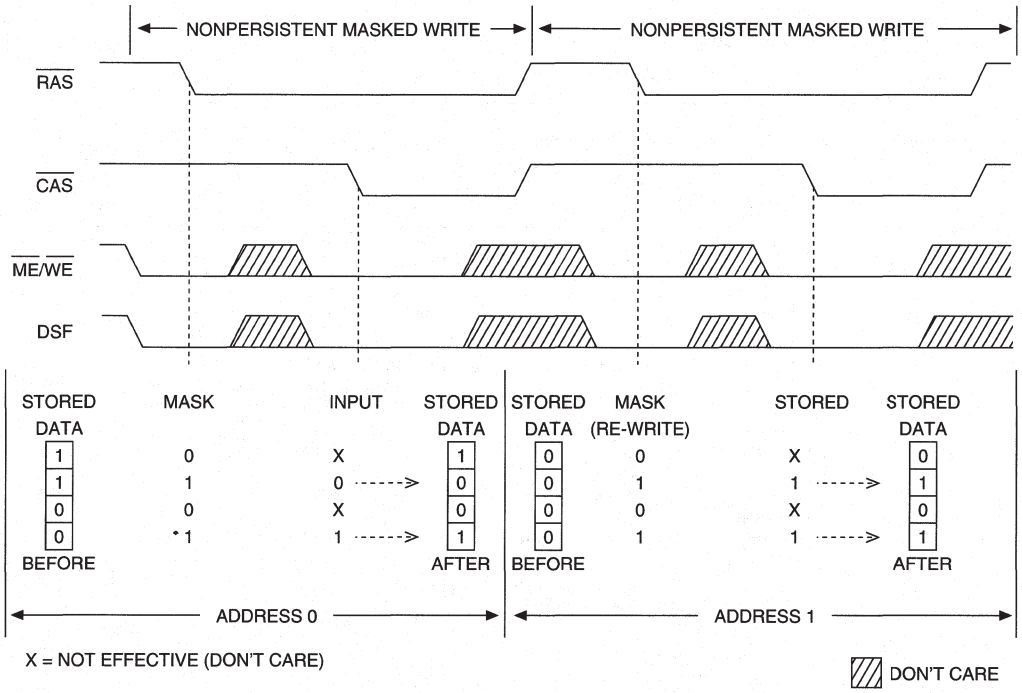


Figure 1
NONPERSISTENT MASKED WRITE EXAMPLE

PERSISTENT MASKED WRITE

The PERSISTENT MASKED WRITE feature eliminates the need to rewrite the mask data before each MASKED WRITE cycle if the same mask data is being used repeatedly. To initiate a PERSISTENT MASKED WRITE, a LOAD MASK REGISTER cycle is performed by taking $\overline{ME}/(\overline{WE})$ and DSF HIGH when $\overline{RAS}$ goes LOW. The mask data is loaded into the internal register when $\overline{CAS}$ goes LOW.

PERSISTENT MASKED WRITE cycles may then be performed by taking $\overline{ME}/(\overline{WE})$ LOW and DSF HIGH when $\overline{RAS}$ goes LOW. The contents of the mask data register will then be used as the mask data for the DRAM inputs. Unlike the NONPERSISTENT MASKED WRITE cycle, the data present on the DQ inputs is not loaded into the mask register when $\overline{RAS}$ falls, and the mask data register will not be cleared at the end of the cycle. Any number of PERSISTENT MASKED WRITE cycles, to any address, may be performed without having to reload the mask data register. Figure 2 shows the LOAD MASK REGISTER and two PERSISTENT MASKED WRITE cycles in operation. The LOAD MASK REGISTER and PERSISTENT MASKED WRITE cycles allow controllers that cannot provide mask data to the DQ pins at $\overline{RAS}$ time to perform MASKED WRITE operations. PERSISTENT MASKED WRITE operations may be performed during FAST PAGE MODE cycles and the same mask will apply to all addressed columns in the addressed row.

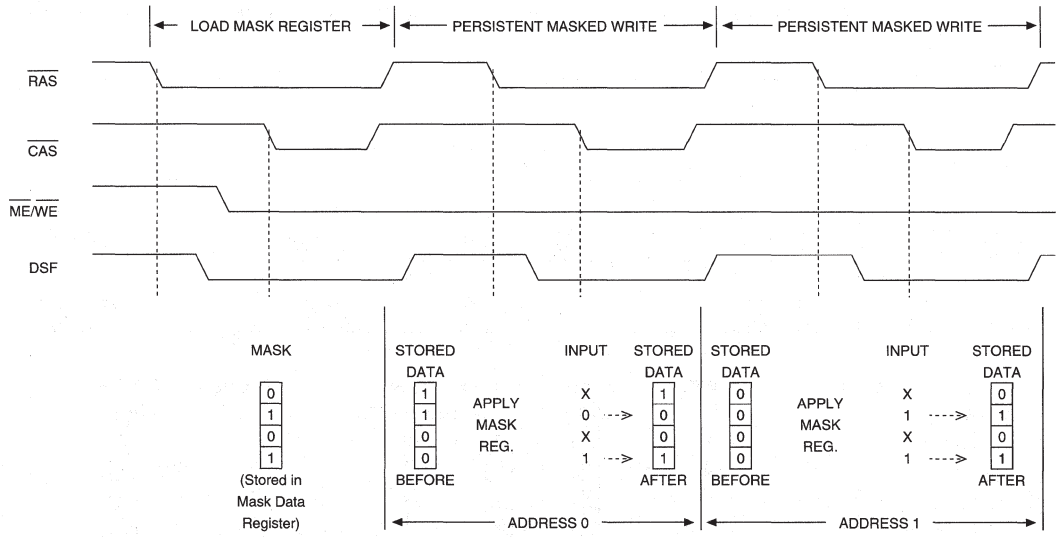


Figure 2
PERSISTENT MASKED WRITE EXAMPLE

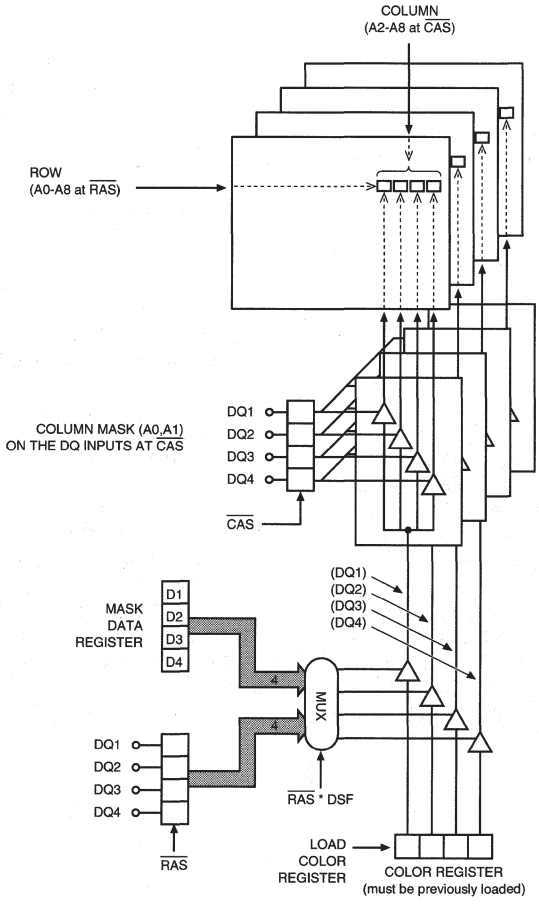


Figure 3
BLOCK WRITE EXAMPLE

BLOCK WRITE

If DSF is HIGH when $\overline{CAS}$ goes LOW, the MT42C4256 will perform a BLOCK WRITE cycle instead of a normal WRITE cycle. In BLOCK WRITE cycles, the contents of the color register are directly written to four adjacent column locations (see Figure 3). The color register must be loaded prior to beginning BLOCK WRITE cycles (see LOAD COLOR REGISTER). Each DQ location of the color register is written to the four column locations (or any of the four that are enabled) in the corresponding DQ bit plane.

The row is addressed as in a normal DRAM WRITE cycle. However, when $\overline{CAS}$ goes LOW, only the A2-A8 inputs are used. A2-A8 specify the "block" of four adjacent column locations that will be accessed. The DQ inputs are then used to determine what combination of the four column locations will be changed. DQ1 acts as a write enable for column location A0 = 0, A1 = 0; DQ2 controls column location A0 = 1, A1 = 0; DQ3 controls A0 = 0, A1 = 1; and DQ4 controls A0 = 1, A1 = 1. The write enable controls are active HIGH; the WRITE function is enabled by a logic 1 and disabled by a logic 0.

NONPERSISTENT MASKED BLOCK WRITE

The MASKED WRITE functions may be used during BLOCK WRITE cycles also. NONPERSISTENT MASKED BLOCK WRITE operates exactly like the normal NONPERSISTENT MASKED WRITE, except that the mask is now applied to four column locations instead of just one.

Like NONPERSISTENT MASKED WRITE, the combination of $\overline{ME}$/($\overline{WE}$) LOW and DSF LOW when $\overline{RAS}$ goes LOW initiates a NONPERSISTENT MASKED cycle. The DSF pin must be driven HIGH when $\overline{CAS}$ goes LOW, to perform the NONPERSISTENT MASKED BLOCK WRITE. By using both the column mask input and the MASKED WRITE function, any combination of the four bit planes or column locations may be masked.

PERSISTENT MASKED BLOCK WRITE

This cycle is also performed exactly like the normal PERSISTENT MASKED WRITE except that DSF is HIGH when $\overline{CAS}$ goes LOW to indicate the BLOCK WRITE function. Both the mask data register and the color register must be loaded with the appropriate data prior to starting a PERSISTENT MASKED BLOCK WRITE.

LOAD MASK DATA REGISTER

The LOAD MASK REGISTER operation and timing are identical to a normal WRITE cycle except that DSF is HIGH when $\overline{RAS}$ goes LOW. As shown in the Truth Table, the combination of $\overline{TR}$/($\overline{OE}$), $\overline{ME}$/($\overline{WE}$), and DSF being HIGH when $\overline{RAS}$ goes LOW indicates the cycle is a LOAD REGISTER cycle. DSF is used when $\overline{CAS}$ goes LOW to select the register to be loaded and must be LOW for a LOAD MASK REGISTER cycle. The data present on the DQ lines will then be written to the mask data register.

Note: *For a normal DRAM WRITE cycle, the mask data register is disabled but not modified. The contents of mask data register will not be changed unless NONPERSISTENT MASKED WRITE or LOAD MASK REGISTER cycles are performed.*

The row address supplied will be refreshed, but it is not necessary to provide any particular row address. The column address inputs are ignored during a LOAD MASK REGISTER cycle.

The mask data register contents are used during PERSISTENT MASKED WRITE and PERSISTENT MASKED BLOCK WRITE cycles to selectively enable writes to the four DQ planes.

LOAD COLOR REGISTER

A LOAD COLOR REGISTER cycle is identical to the LOAD MASK REGISTER cycle except DSF is HIGH when $\overline{CAS}$ goes LOW. The contents of the color register are retained until changed by another LOAD COLOR REGISTER cycle (or the part loses power) and are used as data inputs during BLOCK WRITE cycles.

TRANSFER OPERATIONS

TRANSFER operations are initiated when $\overline{TR}/(\overline{OE})$ is LOW then $\overline{RAS}$ goes LOW. The state of $(\overline{ME})/\overline{WE}$ when $\overline{RAS}$ goes LOW indicates the direction of the TRANSFER (to or from the DRAM), and DSF is used to select between NORMAL TRANSFER, SPLIT READ TRANSFER, and ALTERNATE WRITE TRANSFER cycles. Each of the TRANSFER cycles available is described below.

READ TRANSFER (DRAM-TO-SAM TRANSFER)

If $(\overline{ME})/\overline{WE}$ is HIGH and DSF is LOW when $\overline{RAS}$ goes LOW, a READ TRANSFER cycle is selected. The row address bits indicate the four 512-bit DRAM row planes to be transferred to the four SAM data register planes. The column address bits indicate the start address (or Tap address) of the serial output cycle from the SAM data registers. $\overline{CAS}$ must fall for every TRANSFER in order to load a valid Tap address. A read transfer may be accomplished in two ways. If the transfer is to be synchronized with SC (REAL-TIME READ TRANSFER), $\overline{TR}/(\overline{OE})$ is taken HIGH after $\overline{CAS}$ goes LOW. If the transfer does not have to be synchronized with SC (READ TRANSFER), $\overline{TR}/(\overline{OE})$ may go HIGH before $\overline{CAS}$ goes LOW (refer to the AC Timing Diagrams). The 2,048 bits of DRAM data are written into the SAM data registers and the serial shift start address is stored in an internal 9-bit register. QSF will be LOW if access is from the lower half (addresses 0 through 255), and HIGH if access is from the upper half (256 through 511). If $\overline{SE}$ is LOW, the first bits of the new row data will appear at the serial outputs with the first SC clock pulse. $\overline{SE}$ enables the serial outputs and may be either HIGH or LOW during this operation. The SAM address pointer will increment with the SC LOW-to-HIGH transition, regardless of the state of $\overline{SE}$. Performing a READ TRANSFER cycle sets the direction of the SAM I/O buffers to the output mode.

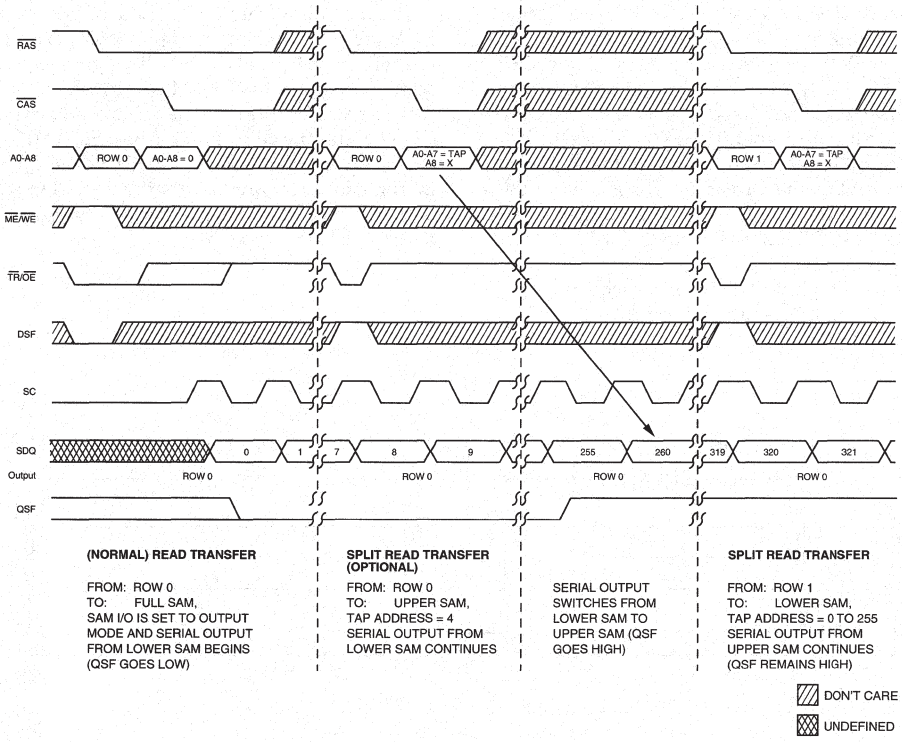


Figure 4
TYPICAL SPLIT-READ-TRANSFER INITIATION SEQUENCE

SPLIT READ TRANSFER (SPLIT DRAM-TO-SAM TRANSFER)

The SPLIT READ TRANSFER (SRT) cycle eliminates the critical transfer timing required to maintain a continuous serial output data stream. When using normal TRANSFER cycles, the REAL-TIME READ TRANSFER cycle has to occur immediately after the last bit of "old data" was clocked out of the SAM port.

When using the SPLIT TRANSFER mode, the SAM is divided into an upper half and a lower half. While data is being serially read from one half of the SAM, new DRAM data may be transferred to the other half. The transfer may occur at any time while the other half is sending data and need not be synchronized with the SC clock.

The $\overline{TR}/(\overline{OE})$ timing is also relaxed for SPLIT TRANSFER cycles. The rising edge of $\overline{TR}/(\overline{OE})$ is not used to complete the TRANSFER cycle and therefore is independent of the rising edges of $\overline{RAS}$ or $\overline{CAS}$. The transfer timing is generated internally for SPLIT TRANSFER cycles. An SRT does not change the direction of the SAM port.

A normal, non-split READ TRANSFER cycle must precede any sequence of SRT cycles to set SAM I/O direction and provide a reference to which half of the SAM the access will begin. Then SRTs may be initiated by taking DSF HIGH when $\overline{RAS}$ goes LOW during the TRANSFER cycle. As in nonsplit transfers, the row address is used to specify the DRAM row to be transferred. The column address, A0-A7, is used to input the SAM Tap address. Address pin A8 is a "don't care" when the Tap address is loaded at the HIGH-to-LOW transition of $\overline{CAS}$. It is internally generated so that the SPLIT TRANSFER will be to the SAM half not currently being accessed.

Figure 4 shows a typical SRT initiation sequence. The normal READ TRANSFER is first performed, followed by an SRT of the same row to the upper half of the SAM. The SRT to the upper half is optional and need be done only if the Tap for the upper half is ≠ 0. Serial access continues, and when the SAM address counter reaches 255 ("A8" = 0, A0-A7 = 1), the new Tap address is loaded for the next half ("A8" = 1, A0-A7 = Tap) and the QSF output goes HIGH. Once the serial access has switched to the upper SAM, new data may be transferred to the lower SAM. The controller must wait for the state of QSF to change and then the new data may be transferred to the SAM half not being accessed. For example, the next step in Figure 4 would be to wait until QSF went LOW (indicating that row-1 data is shifting out of the lower SAM) and then transfer the upper half of row 1 to the upper SAM. If the half boundary is reached before an SRT is done for the next half a Tap address of "0" will be used. Access will start at 0 if going to the lower half, or 256 if going to the upper half. See Figure 5.

WRITE TRANSFER (SAM-TO-DRAM TRANSFER)

The operation of the WRITE TRANSFER is identical to the READ TRANSFER described previously except $(\overline{ME})/\overline{WE}$ and $\overline{SE}$ must be LOW when $\overline{RAS}$ goes LOW. The row address indicates the DRAM row to which the SAM data registers will be written. The column address (Tap) indicates the starting address of the next SERIAL INPUT cycle for the SAM data registers. A WRITE TRANSFER changes the direction of the SAM I/O buffers to the input mode. QFS is LOW if access is to the lower half of the SAM, and HIGH if access is to the upper half.

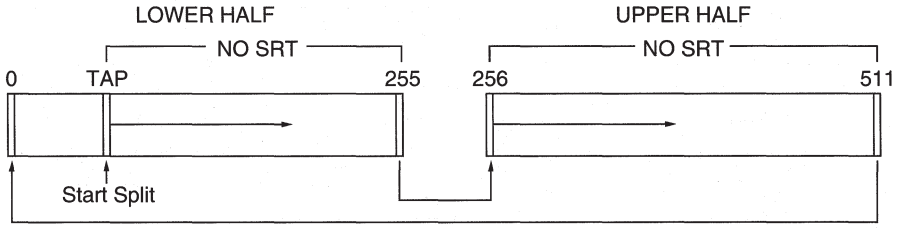


Figure 5
SPLIT SAM TRANSFER

PSEUDO WRITE TRANSFER (SERIAL-INPUT-MODE ENABLE)

The PSEUDO WRITE TRANSFER cycle is used to change the direction of the SAM port from output to input without performing a WRITE TRANSFER cycle. A PSEUDO WRITE TRANSFER cycle is a WRITE TRANSFER cycle with $\overline{SE}$ held HIGH instead of LOW. The DRAM data will not be disturbed and the SAM will be ready to accept input data.

ALTERNATE WRITE TRANSFER (SAM-TO-DRAM TRANSFER)

The operation of the ALTERNATE WRITE TRANSFER is identical to the WRITE TRANSFER except that the DSF pin is HIGH and $(\overline{ME})/\overline{WE}$ is LOW when $\overline{RAS}$ goes LOW, allowing $\overline{SE}$ to be a "don't care." This allows the outputs to be disabled using $\overline{SE}$ during a WRITE TRANSFER cycle. ALTERNATE WRITE TRANSFER will change the SAM I/O direction to an input condition.

SERIAL INPUT AND SERIAL OUTPUT

The control inputs for SERIAL INPUT and SERIAL OUTPUT are SC and $\overline{SE}$. The rising edge of SC increments the serial address counter and provides access to the next SAM location. $\overline{SE}$ enables or disables the serial input/output buffers.

Serial output of the SAM contents will start at the serial start address that was loaded in the SAM address counter during a READ or SPLIT READ TRANSFER cycle. The SC input increments the address counter and presents the contents of the next SAM location to the 4-bit port. $\overline{SE}$ is used as an output enable during the SAM output operation. The serial address is automatically incremented with every SC LOW-to-HIGH transition, regardless of whether $\overline{SE}$ is HIGH or LOW. The address progresses through the SAM and will wrap around (after count 255 or 511) to the Tap address of the next half for split modes. If an SRT was not performed before the half boundary is reached, the count will progress as illustrated in Figure 5. Address count will wrap around (after count 511) to Tap address 0 if in the "full" SAM modes.

SC is also used to clock-in data when the device is in the serial input mode. As in the serial output operation, the contents of the SAM address counter (loaded when the serial input mode was enabled) will determine the serial address of the first 4-bit word written. $\overline{SE}$ acts as a write enable for serial input data and must be LOW for valid serial input. If $\overline{SE}$ = HIGH, the data inputs are disabled and the SAM contents will not be modified. The serial address counter is incremented with every LOW-to-HIGH transition of SC, regardless of the logic level on the $\overline{SE}$ input.

POWER-UP AND INITIALIZATION

After Vcc is at specified operating conditions, for 100µs minimum, eight $\overline{RAS}$ cycles must be executed to initialize the dynamic memory array. Micron recommends that $\overline{RAS} = (\overline{TR})/\overline{OE} \geq V_{IH}$ during power up to ensure that the DRAM I/O pins (DQs) are in a High-Z state. The DRAM array will contain random data.

The SAM portion of the MT42C4256 is completely static in operation and does not require refresh or initialization. The SAM port will power-up in the serial input mode (WRITE TRANSFER) and the I/O pins (SDQs) will be High-Z, regardless of the state of $\overline{SE}$. The mask and color register will contain random data after power-up. QSF initializes in the LOW state.

TRUTH TABLE

CODE	FUNCTION	RAS FALLING EDGE					CAS FALL	A0-A8[1]		DQ1-DQ4[2]		REGISTERS	
		CAS	TR/OE	ME/WE	DSF	SE	DSF	RAS	CAS	RAS	CAS,WE[3]	MASK	COLOR
	DRAM OPERATIONS												
CBR	CBR REFRESH	0	X	X	X	X	X	—	X	—	X	X	X
ROR	RAS-ONLY REFRESH	1	1	X	X	X	—	ROW	—	X	—	X	X
RW	NORMAL DRAM READ OR WRITE	1	1	1	0	X	0	ROW	COLUMN	X	VALID	X	X
RWNM	NONPERSISTENT (LOAD AND USE) MASKED WRITE TO DRAM	1	1	0	0	X	0	ROW	COLUMN	WRITE MASK	VALID DATA	LOAD & USE	X
RWOM	PERSISTENT (USE REGISTER) MASKED WRITE TO DRAM	1	1	0	1	X	0	ROW	COLUMN	X	VALID DATA	USE	X
BW	BLOCK WRITE TO DRAM (NO DATA MASK)	1	1	1	0	X	1	ROW	COLUMN (A2-A8)	X	COLUMN MASK	X	USE
BWNM	NONPERSISTENT (LOAD & USE) MASKED BLOCK WRITE TO DRAM	1	1	0	0	X	1	ROW	COLUMN	WRITE MASK	COLUMN MASK	LOAD & USE	USE
BWOM	PERSISTENT (USE MASK REGISTER) MASKED BLOCK WRITE TO DRAM	1	1	0	1	X	1	ROW	COLUMN (A2-A8)	X	COLUMN MASK	USE	USE
	REGISTER OPERATIONS												
LMR	LOAD MASK REGISTER	1	1	1	1	X	0	ROW[4]	X	X	WRITE MASK	LOAD	X
LCR	LOAD COLOR REGISTER	1	1	1	1	X	1	ROW[4]	X	X	COLOR DATA	X	LOAD
	TRANSFER OPERATIONS												
RT	READ TRANSFER (DRAM-TO-SAM TRANSFER)	1	0	1	0	X	X	ROW	TAP[5]	X	X	X	X
SRT	SPLIT READ TRANSFER (SPLIT DRAM-TO-SAM TRANSFER)	1	0	1	1	X	X	ROW	TAP[5]	X	X	X	X
WT	WRITE TRANSFER (SAM-TO-DRAM TRANSFER)	1	0	0	0	0	X	ROW	TAP[5]	X	X	X	X
PWT	PSEUDO WRITE TRANSFER (SERIAL-INPUT-MODE ENABLE)	1	0	0	0	1	X	ROW[4]	TAP[5]	X	X	X	X
AWT	ALTERNATE WRITE TRANSFER (SAM-TO-DRAM TRANSFER)	1	0	0	1	X	X	ROW	TAP[5]	X	X	X	X

NOTE:
1. These columns show what must be present on the A0-A8 inputs when RAS falls and when CAS falls.
2. These columns show what must be present on the DQ1-DQ4 inputs when RAS falls and when CAS falls.
3. On WRITE cycles (except BLOCK WRITE and LOAD COLOR REGISTER), the input data is latched at the falling edge of CAS or ME/WE, whichever is later. Similarly, with READ cycles, the output data is activated at the falling edge of CAS or TR/OE, whichever is later.
4. The ROW that is addressed will be refreshed, but no particular ROW address is required.
5. This is the SAM location that the first SC cycle will access. For split SAM transfers, the Tap will be the first address location accessed of the "new" SAM half after the boundary of the current half is reached (255 for the lower half, 511 for the upper half).

ABSOLUTE MAXIMUM RATINGS*

Voltage on Vcc Supply Relative to Vss ..... -1V to +7V
Operating Temperature, T_A (ambient) ..... 0°C to +70°C
Storage Temperature (plastic) ..... -55°C to +150°C
Power Dissipation 1W
Short Circuit Output Current 50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

(0°C ≤ T_A ≤ 70°C)

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS	NOTES
Supply Voltage	V_{CC}	4.5	5.5	V	1
Input High (Logic 1) Voltage, all inputs	V_{IH}	2.4	V_{CC}+1	V	1
Input Low (Logic 0) Voltage, all inputs	V_{IL}	-1.0	0.8	V	1

DC ELECTRICAL CHARACTERISTICS

(0°C ≤ T_A ≤ 70°C; V_{CC} = 5V ±10%)

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS	NOTES
INPUT LEAKAGE CURRENT Any input (0V ≤ V_{IN} ≤ V_{CC}); all other pins not under test = 0V	I_L	-10	10	µA	
OUTPUT LEAKAGE CURRENT (DQ, SDQ disabled, 0V ≤ V_{OUT} ≤ V_{CC})	I_{OZ}	-10	10	µA	
OUTPUT LEVELS Output High Voltage (I_{OUT} = -2.5mA)	V_{OH}	2.4		V	1
Output Low Voltage (I_{OUT} = 2.5mA)	V_{OL}		0.4	V	

CAPACITANCE

PARAMETER	SYMBOL	MIN	MAX	UNITS	NOTES
Input Capacitance: A0-A8	C_{I1}		5	pF	2
Input Capacitance: $\overline{RAS}$, $\overline{CAS}$, $\overline{ME}$/$\overline{WE}$, $\overline{TR}$/$\overline{OE}$, SC, $\overline{SE}$, DSF	C_{I2}		7	pF	2
Input/Output Capacitance: DQ, SDQ	$C_{I/O}$		9	pF	2
Output Capacitance: QSF	C_O		9	pF	2

CURRENT DRAIN, SAM IN STANDBY

(0°C ≤ T_A ≤ 70°C; V_{CC} = 5V ±10%)

		MAX				
PARAMETER/CONDITION	SYMBOL	-6*	-7	-8	UNITS	NOTES
OPERATING CURRENT ($\overline{RAS}$ and $\overline{CAS}$ = Cycling: ^tRC = ^tRC [MIN])	I_{CC1}	105	95	85	mA	3, 4 26
OPERATING CURRENT: FAST-PAGE-MODE ($\overline{RAS}$ = V_{IL}; $\overline{CAS}$ = Cycling: ^tPC = ^tPC [MIN])	I_{CC2}	95	85	75	mA	3, 4 27
STANDBY CURRENT: TTL INPUT LEVELS Power supply standby current ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH} after 8 $\overline{RAS}$ cycles [MIN]; other inputs ≥ V_{IH} or ≤ V_{IL})	I_{CC3}	8	8	8	mA	4
REFRESH CURRENT: $\overline{RAS}$-ONLY ($\overline{RAS}$ = Cycling; $\overline{CAS}$ = V_{IH})	I_{CC5}	105	95	85	mA	3, 26
REFRESH CURRENT: CBR ($\overline{RAS}$ and $\overline{CAS}$ = Cycling)	I_{CC6}	105	95	85	mA	3, 5
SAM/DRAM DATA TRANSFER	I_{CC8}	115	105	95	mA	3

CURRENT DRAIN, SAM ACTIVE (^tSC = MIN)

(0°C ≤ T_A ≤ 70°C; V_{CC} = 5V ±10%)

		MAX				
PARAMETER/CONDITION	SYMBOL	-6*	-7	-8	UNITS	NOTES
OPERATING CURRENT ($\overline{RAS}$ and $\overline{CAS}$ = Cycling: ^tRC = ^tRC [MIN])	I_{CC9}	170	150	130	mA	3, 4, 26
OPERATING CURRENT: FAST-PAGE-MODE ($\overline{RAS}$ = V_{IL}; $\overline{CAS}$ = Cycling: ^tPC = ^tPC [MIN])	I_{CC10}	160	140	120	mA	3, 4, 27
STANDBY CURRENT: TTL INPUT LEVELS Power supply standby current ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH} after 8 $\overline{RAS}$ cycles [MIN]; other inputs ≥ V_{IH} or ≤ V_{IL})	I_{CC11}	65	55	45	mA	3, 4
REFRESH CURRENT: $\overline{RAS}$-ONLY ($\overline{RAS}$ = Cycling; $\overline{CAS}$ = V_{IH})	I_{CC12}	170	150	130	mA	3, 4, 26
REFRESH CURRENT: CBR ($\overline{RAS}$ and $\overline{CAS}$ = Cycling)	I_{CC13}	170	150	130	mA	3, 4, 5
SAM/DRAM DATA TRANSFER	I_{CC14}	190	160	130	mA	3, 4

*60ns (-6) specifications are preliminary; consult factory for availability.

DRAM TIMING PARAMETERS

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 6, 7, 8, 9, 10, 11, 12, 13) (0°C ≤ T_A ≤ +70°C; Vcc = 5V ±10%)

AC CHARACTERISTICS		-6*		-7		-8			
PARAMETER	**SYM**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**UNITS**	**NOTES**
Random READ or WRITE cycle time	tRC	110		130		150		ns	
READ-MODIFY-WRITE cycle time	tRWC	148		170		190		ns	
FAST-PAGE-MODE READ or WRITE cycle time	tPC	35		40		45		ns	
FAST-PAGE-MODE READ-MODIFY-WRITE cycle time	tPRWC	83		90		95		ns	
Access time from $\overline{RAS}$	tRAC		60		70		80	ns	14
Access time from $\overline{CAS}$	tCAC		18		20		25	ns	15
Access time from $\overline{(TR)}/\overline{OE}$	tOE		15		20		20	ns	
Access time from column-address	tAA		30		35		40	ns	
Access time from $\overline{CAS}$ precharge	tCPA		35		40		45	ns	
$\overline{RAS}$ pulse width	tRAS	60	100,000	70	100,000	80	100,000	ns	
$\overline{RAS}$ pulse width (FAST-PAGE-MODE)	tRASP	60	100,000	70	100,000	80	100,000	ns	
$\overline{RAS}$ hold time	tRSH	18		20		25		ns	
$\overline{RAS}$ precharge time	tRP	40		50		60		ns	
$\overline{CAS}$ pulse width	tCAS	18	100,000	20	100,000	25	100,000	ns	
$\overline{CAS}$ hold time	tCSH	60		70		80		ns	
$\overline{CAS}$ precharge time	tCP	10		10		10		ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	tRCD	20	42	20	50	20	55	ns	17
$\overline{CAS}$ to $\overline{RAS}$ precharge time	tCRP	10		10		10		ns	
Row-address setup time	tASR	0		0		0		ns	
Row-address hold time	tRAH	10		10		10		ns	
$\overline{RAS}$ to column-address delay time	tRAD	15	30	15	35	15	40	ns	18
Column-address setup time	tASC	0		0		0		ns	
Column-address hold time	tCAH	12		15		15		ns	
Column-address hold time (referenced to $\overline{RAS}$)	tAR	40		45		55		ns	
Column-address to $\overline{RAS}$ lead time	tRAL	30		35		40		ns	
Read command setup time	tRCS	0		0		0		ns	
Read command hold time (referenced to $\overline{CAS}$)	tRCH	0		0		0		ns	19
Read command hold time (referenced to $\overline{RAS}$)	tRRH	0		0		0		ns	19
$\overline{CAS}$ to output in Low-Z	tCLZ	3		3		3		ns	
Output buffer turn-off delay	tOFF	3	12	3	12	3	15	ns	20, 23
Output disable	tOD	3	10	3	10	3	10	ns	20, 23
Output disable hold time from start of WRITE	tOEH	10		10		10		ns	25
$\overline{OE}$ LOW to $\overline{RAS}$ HIGH delay time	tROH	0		0		0		ns	

*60ns (-6) specifications are preliminary; consult factory for availability.

DRAM TIMING PARAMETERS (continued)

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 6, 7, 8, 9, 10, 11, 12, 13) (0°C ≤ T_A ≤ +70°C; Vcc = 5V ±10%)

AC CHARACTERISTICS		-6*		-7		-8			
PARAMETER	SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
Write command setup time	^tWCS	0		0		0		ns	21
Write command hold time	^tWCH	12		15		15		ns	
Write command hold time (referenced to $\overline{RAS}$)	^tWCR	40		45		55		ns	
Write command pulse width	^tWP	10		15		15		ns	
Write command to $\overline{RAS}$ lead time	^tRWL	18		20		20		ns	
Write command to $\overline{CAS}$ lead time	^tCWL	18		20		20		ns	
Data-in setup time	^tDS	0		0		0		ns	22
Data-in hold time	^tDH	12		15		15		ns	22
Data-in hold time (referenced to $\overline{RAS}$)	^tDHR	40		45		55		ns	
$\overline{RAS}$ to $\overline{WE}$ delay time	^tRWD	80		90		100		ns	21
Column-address to $\overline{WE}$ delay time	^tAWD	50		55		60		ns	21
$\overline{CAS}$ to $\overline{WE}$ delay time	^tCWD	38		40		45		ns	21
Transition time (rise or fall)	^tT		35		35		35	ns	9, 10
Refresh period (512 cycles)	^tREF		16.7		16.7		16.7	ms	
$\overline{RAS}$ to $\overline{CAS}$ precharge time	^tRPC	0		0		0		ns	
$\overline{CAS}$ setup time (CBR REFRESH)	^tCSR	10		10		10		ns	5
$\overline{CAS}$ hold time (CBR REFRESH)	^tCHR	10		10		10		ns	5
$\overline{ME}$/$\overline{WE}$ to $\overline{RAS}$ setup time	^tWSR	0		0		0		ns	
$\overline{ME}$/$\overline{WE}$ to $\overline{RAS}$ hold time	^tRWH	12		15		15		ns	
Mask Data to $\overline{RAS}$ setup time	^tMS	0		0		0		ns	
Mask Data to $\overline{RAS}$ hold time	^tMH	12		15		15		ns	

*60ns (-6) specifications are preliminary; consult factory for availability.

TRANSFER AND MODE CONTROL TIMING PARAMETERS

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes 6, 7, 8, 9, 10) (0° C ≤ T_A ≤ + 70°C; Vcc = 5V ±10%)

AC CHARACTERISTICS		-6*		-7		-8			
PARAMETER	**SYM**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**UNITS**	**NOTES**
$\overline{TR}/(\overline{OE})$ LOW to $\overline{RAS}$ setup time	^tTLS	0		0		0		ns	
$\overline{TR}/(\overline{OE})$ LOW to $\overline{RAS}$ hold time	^tTLH	15	10,000	15	10,000	15	10,000	ns	
$\overline{TR}/(\overline{OE})$ LOW to $\overline{RAS}$ hold time (REAL-TIME READ TRANSFER only)	^tRTH	65	10,000	65	10,000	70	10,000	ns	
$\overline{TR}/(\overline{OE})$ LOW to $\overline{CAS}$ hold time (REAL-TIME READ TRANSFER only)	^tCTH	25		25		25		ns	
$\overline{TR}/(\overline{OE})$ HIGH to SC lead time	^tTSL	5		5		5		ns	
$\overline{TR}/(\overline{OE})$ to $\overline{RAS}$ HIGH hold time	^tTRD	15		15		15		ns	
$\overline{TR}/(\overline{OE})$ HIGH to $\overline{RAS}$ precharge time	^tTRP	40		50		60		ns	
$\overline{TR}/(\overline{OE})$ precharge time	^tTRW	15		20		20		ns	
First SC edge to $\overline{TR}/(\overline{OE})$ HIGH delay time	^tTSD	15		15		15		ns	
Serial output buffer turn-off delay from $\overline{RAS}$	^tSDZ	7	40	7	40	7	40	ns	
SC to $\overline{RAS}$ setup time	^tSRS	20		25		30		ns	
Serial data input to $\overline{SE}$ delay time	^tSZE	0		0		0		ns	
Serial data input delay from $\overline{RAS}$	^tSDD	50		50		50		ns	
Serial data input to $\overline{RAS}$ delay time	^tSZS	0		0		0		ns	
Serial-input-mode enable ($\overline{SE}$) to $\overline{RAS}$ setup time	^tESR	0		0		0		ns	
Serial-input-mode enable ($\overline{SE}$) to $\overline{RAS}$ hold time	^tREH	15		15		15		ns	
$\overline{TR}/(\overline{OE})$ HIGH to $\overline{RAS}$ setup time	^tYS	0		0		0		ns	
$\overline{TR}/(\overline{OE})$ HIGH to $\overline{RAS}$ hold time	^tYH	12		15		15		ns	
DSF to $\overline{RAS}$ setup time	^tFSR	0		0		0		ns	
DSF to $\overline{RAS}$ hold time	^tRFH	12		15		15		ns	
SC to QSF delay time	^tSQD		30		30		30	ns	
SPLIT TRANSFER setup time	^tSTS	20		25		30		ns	
SPLIT TRANSFER hold time	^tSTH	0		0		0		ns	
$\overline{RAS}$ to QSF delay time	^tRQD		70		75		75	ns	
DSF to $\overline{RAS}$ hold time	^tFHR	40		45		55		ns	
DSF to $\overline{CAS}$ setup time	^tFSC	0		0		0		ns	
DSF to $\overline{CAS}$ hold time	^tCFH	12		15		15		ns	
$\overline{TR}/\overline{OE}$ to QSF delay time	^tTQD		25		25		25	ns	
$\overline{CAS}$ to QSF delay time	^tCQD		30		35		35	ns	
$\overline{RAS}$ to first SC delay	^tRSD	70		80		80		ns	
$\overline{CAS}$ to first SC delay	^tCSD	25		30		30		ns	

*60ns (-6) specifications are preliminary; consult factory for availability.

SAM TIMING PARAMETERS

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes 6, 7, 8, 9, 10) (0° C ≤ T_A ≤ + 70°C; Vcc = 5V ±10%)

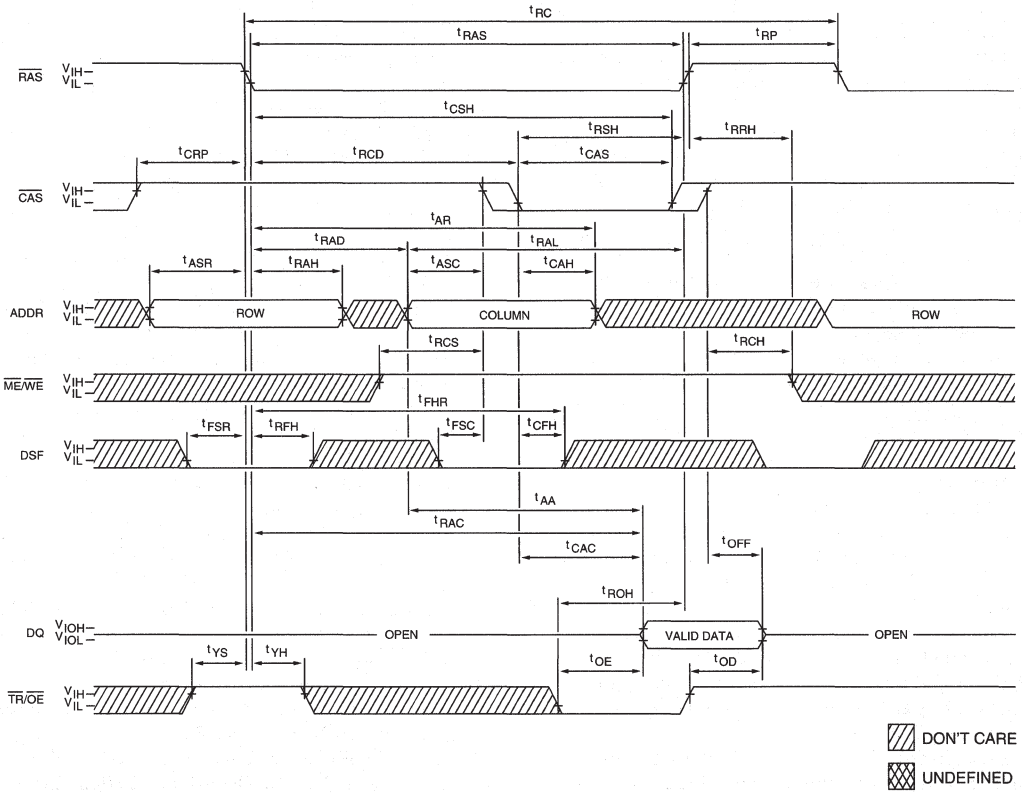
AC CHARACTERISTICS		-6*		-7		-8			
PARAMETER	**SYM**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**UNITS**	**NOTES**
Serial clock-cycle time	^tSC	18		22		25		ns	
Access time from SC	^tSAC		18		22		25	ns	24, 28
SC precharge time (SC LOW time)	^tSP	7		8		10		ns	
SC pulse width (SC HIGH time)	^tSAS	7		8		10		ns	
Access time from $\overline{SE}$	^tSEA		12		15		15	ns	24
$\overline{SE}$ precharge time	^tSEP	7		8		10		ns	
$\overline{SE}$ pulse width	^tSE	7		8		10		ns	
Serial data-out hold time after SC high	^tSOH	5		5		5		ns	24, 28
Serial output buffer turn-off delay from $\overline{SE}$	^tSEZ	3	10	3	12	3	12	ns	20, 24
Serial data-in setup time	^tSDS	0		0		0		ns	
Serial data-in hold time	^tSDH	9		10		10		ns	
Serial input (Write) Enable setup time	^tSWS	0		0		0		ns	
Serial input (Write) Enable hold time	^tSWH	15		15		15		ns	
Serial input (Write) disable setup time	^tSWIS	0		0		0		ns	
Serial input (Write) disable hold time	^tSWIH	15		15		15		ns	

*60ns (-6) specifications are preliminary; consult factory for availability.

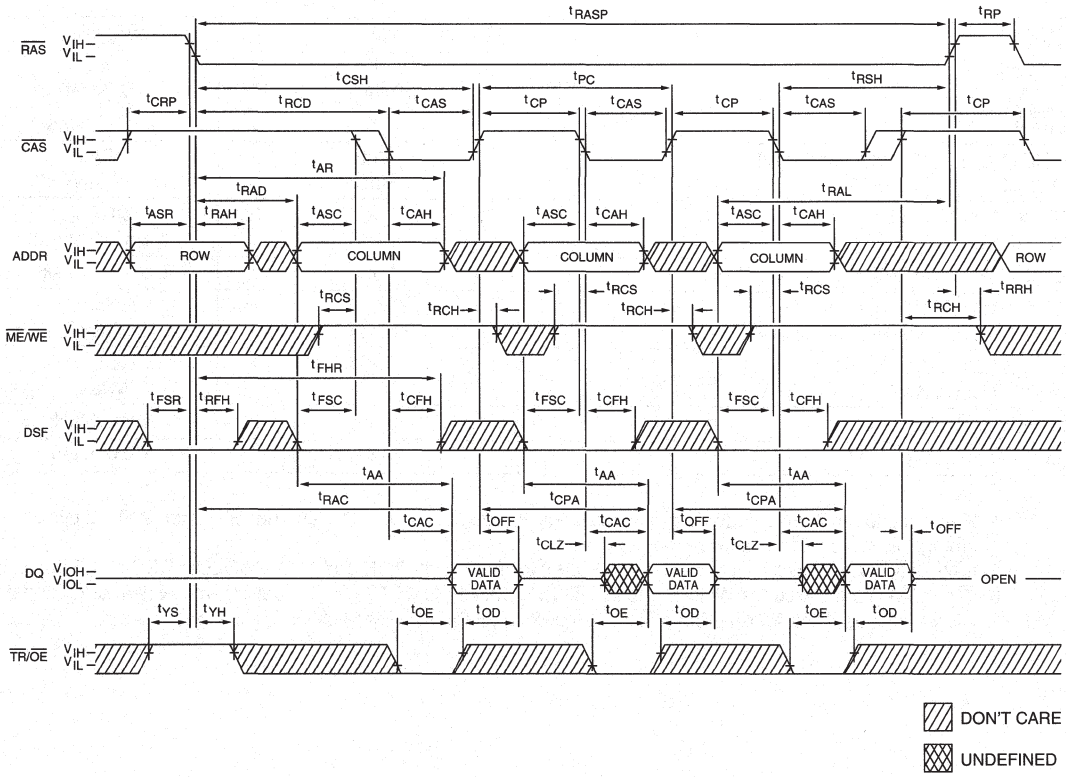
NOTES

1. All voltages referenced to V_{SS}.
2. This parameter is sampled. V_{CC} = 5V ±10%, f = 1 MHz.
3. I_{CC} is dependent on cycle rates.
4. I_{CC} is dependent on I/O loading. Specified values are obtained with minimum cycle time and the I/Os open.
5. Enables on-chip refresh and address counters.
6. The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range ($0°C \le T_A \le 70°C$) is assured.
7. An initial pause of 100µs is required after power-up followed by any eight $\overline{RAS}$ cycles before proper device operation is assured. The eight $\overline{RAS}$ cycle wake-up should be repeated any time the ^tREF refresh requirement is exceeded.
8. AC characteristics assume ^tT = 5ns.
9. V_{IH} (MIN) and V_{IL} (MAX) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}). Input signals transition between 0V and 3V for AC testing.
10. In addition to meeting the transition rate specification, all input signals must transit between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner.
11. If $\overline{CAS}$ = V_{IH}, DRAM data output (DQ1-DQ4) is High-Z.
12. If $\overline{CAS}$ = V_{IL}, DRAM data output (DQ1-DQ4) may contain data from the last valid READ cycle.
13. DRAM output timing measured with a load equivalent to 2 TTL gates and 100pF. Output reference levels: V_{OH} = 2.0V; V_{OL} = 0.8V.
14. Assumes that $^tRCD < ^tRCD$ (MAX). If ^tRCD is greater than the maximum recommended value shown in this table, ^tRAC will increase by the amount that ^tRCD exceeds the value shown.
15. Assumes that $^tRCD \ge ^tRCD$ (MAX).
16. If $\overline{CAS}$ is LOW at the falling edge of $\overline{RAS}$, DQ will be maintained from the previous cycle. To initiate a new cycle and clear the data out buffer, $\overline{CAS}$ must be pulsed HIGH for ^tCPN.
17. Operation within the ^tRCD (MAX) limit ensures that ^tRAC (MAX) can be met. ^tRCD (MAX) is specified as a reference point only; if ^tRCD is greater than the specified ^tRCD (MAX) limit, then access time is controlled exclusively by ^tCAC.
18. Operation within the ^tRAD (MAX) limit ensures that ^tRCD (MAX) can be met. ^tRAD (MAX) is specified as a reference point only; if ^tRAD is greater than the specified ^tRAD (MAX) limit, then access time is controlled exclusively by ^tAA.
19. Either ^tRCH or ^tRRH must be satisfied for a READ cycle.
20. ^tOD, ^tOFF and ^tSEZ define the time when the output achieves open circuit (V_{OH} -200mV, V_{OL} +200mV). This parameter is sampled and not 100 percent tested.
21. ^tWCS, ^tRWD, ^tAWD and ^tCWD are restrictive operating parameters in LATE-WRITE, READ-WRITE and READ-MODIFY-WRITE cycles only. If $^tWCS \ge ^tWCS$ (MIN), the cycle is an EARLY-WRITE cycle and the data output will remain an open circuit throughout the entire cycle, regardless of $\overline{TR}/\overline{OE}$. If $^tWCS \le ^tWCS$ (MIN), the cycle is a LATE-WRITE and $\overline{TR}/\overline{OE}$ must control the output buffers during the WRITE to avoid data contention. If $^tRWD \ge ^tRWD$ (MIN), $^tAWD \ge ^tAWD$ (MIN) and $^tCWD \ge ^tCWD$ (MIN), the cycle is a READ-WRITE and the data output will contain data read from the selected cell. If neither of the above conditions is met, the state of the output buffers (at access time and until $\overline{CAS}$ goes back to V_{IH}) is indeterminate but the WRITE will be valid, if ^tOD and ^tOEH are met. See the LATE-WRITE AC Timing diagram.
22. These parameters are referenced to $\overline{CAS}$ leading edge in EARLY-WRITE cycles and $\overline{ME}/\overline{WE}$ leading edge in LATE-WRITE or READ-WRITE cycles.
23. During a READ cycle, if $\overline{TR}/\overline{OE}$ is LOW then taken HIGH, DQ goes open. The DQs will go open with $\overline{OE}$ or $\overline{CAS}$, whichever goes HIGH first.
24. SAM output timing is measured with a load equivalent to 1 TTL gate and 30pF. Output reference levels: V_{OH} = 2.0V; V_{OL} = 0.8V.
25. ^tOD and ^tOEH must be met in LATE-WRITE and READ-MODIFY-WRITE cycles ($\overline{OE}$ HIGH during WRITE cycle) in order to ensure that the output buffers will be open during the WRITE cycle. The DQs will provide previously read data if $\overline{CAS}$ remains LOW and $\overline{OE}$ is taken LOW after ^tOEH is met. If $\overline{CAS}$ goes HIGH prior to $\overline{OE}$ going back LOW, the DQs will remain open.
26. Address (A0-A8) may be changed two times or less while $\overline{RAS}$ = V_{IL}.
27. Address (A0-A8) may be changed once or less while $\overline{CAS}$ = V_{IH} and $\overline{RAS}$ = V_{IL}.
28. ^tSAC is MAX at 70° C and 4.5V Vcc; ^tSOH is MIN at 0°C and 5.5V Vcc. These limits will not occur simultaneously at any given voltage or temperature. ^tSOH = ^tSAC - output transition time; this is guaranteed by design.

DRAM READ CYCLE



DRAM FAST-PAGE-MODE READ CYCLE



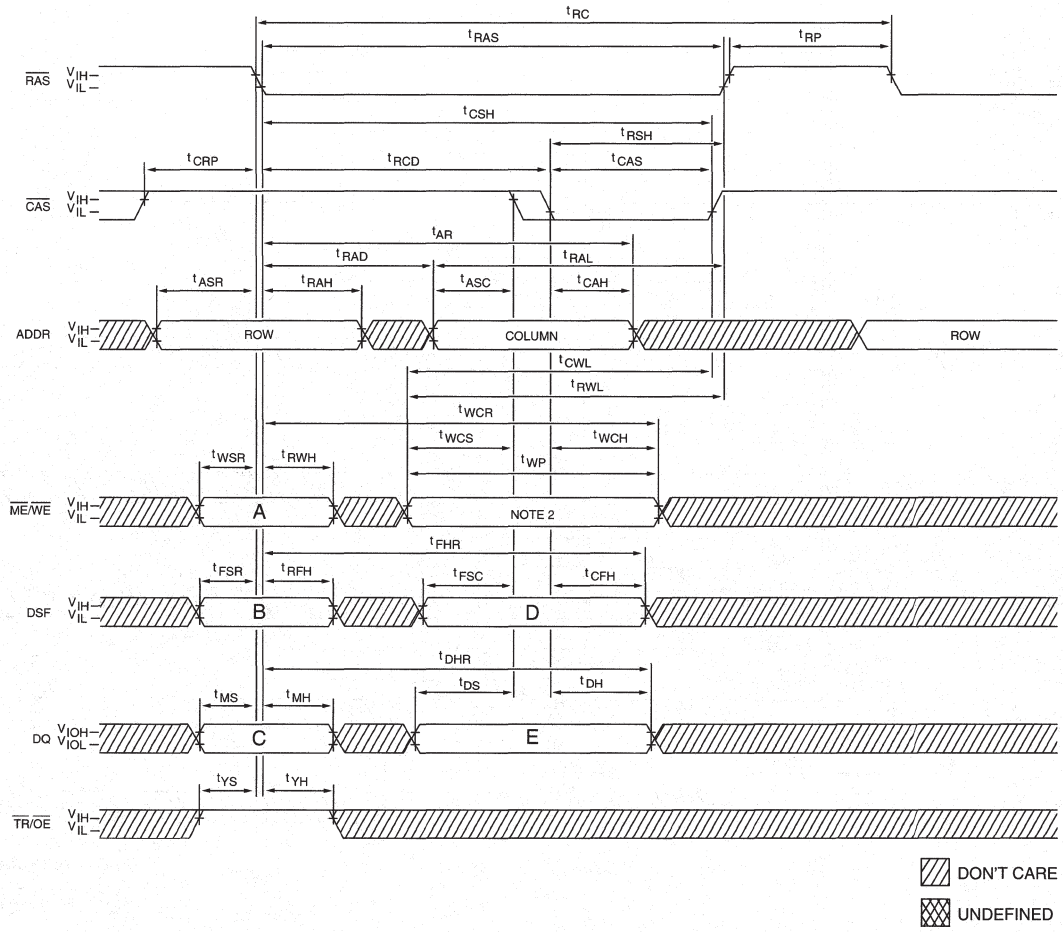
NOTE: WRITE cycles or READ-MODIFY-WRITE cycles may be mixed with READ cycles while in FAST-PAGE-MODE.

WRITE CYCLE FUNCTION TABLE [1]

FUNCTION	LOGIC STATES				
	$\overline{RAS}$ Falling Edge			$\overline{CAS}$ Falling Edge	
	A $\overline{ME}/\overline{WE}$	B DSF	C DQ (Input)	D DSF	E[2] DQ (Input)
Normal DRAM WRITE	1	0	X	0	DRAM Data
NONPERSISTENT (Load and Use) MASKED WRITE to DRAM	0	0	Write Mask	0	DRAM Data (Masked)
PERSISTENT (Use Register) MASKED WRITE to DRAM	0	1	X	0	DRAM Data (Masked)
BLOCK WRITE to DRAM (No Data Mask)	1	0	X	1	Column Mask[3]
NONPERSISTENT (Load and Use) MASKED BLOCK WRITE to DRAM	0	0	Write Mask	1	Column Mask[3]
PERSISTENT (Use Register) MASKED BLOCK WRITE to DRAM	0	1	X	1	Column Mask[3]
Load Mask Register	1	1	X	0	Write Mask
Load Color Register	1	1	X	1	Color Data

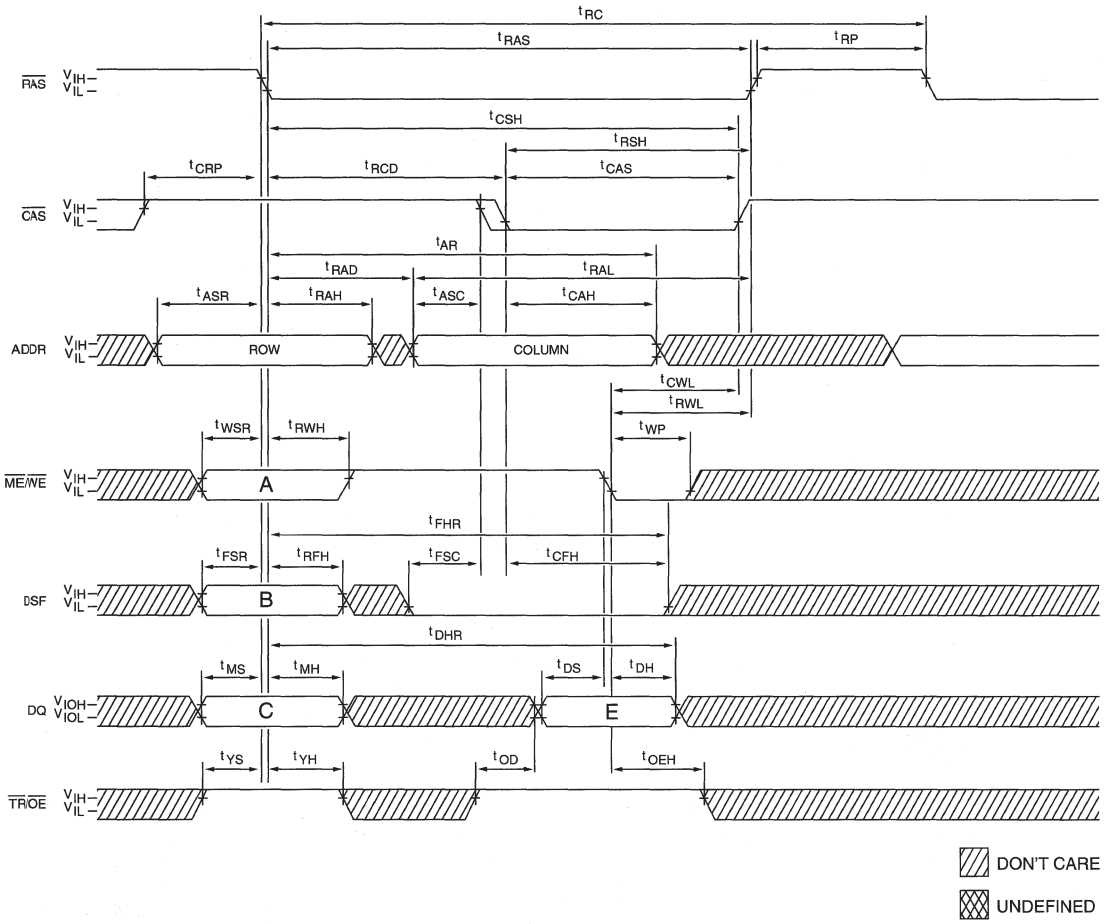
NOTE:
1. Refer to this function table to determine the logic states of "A", "B", "C", "D" and "E" for the WRITE cycle timing diagrams on the following pages.
2. $\overline{CAS}$ or $\overline{ME}/\overline{WE}$, whichever occurs later (Except for BLOCK WRITE and LOAD COLOR REGISTER).
3. $\overline{WE}$ = "don't care" BLOCK WRITE and LOAD COLOR REGISTER. The DQ column-mask data or color data will be latched at the falling edge of $\overline{CAS}$, regardless of the state of $\overline{ME}/\overline{WE}$.

DRAM EARLY-WRITE CYCLE [1]



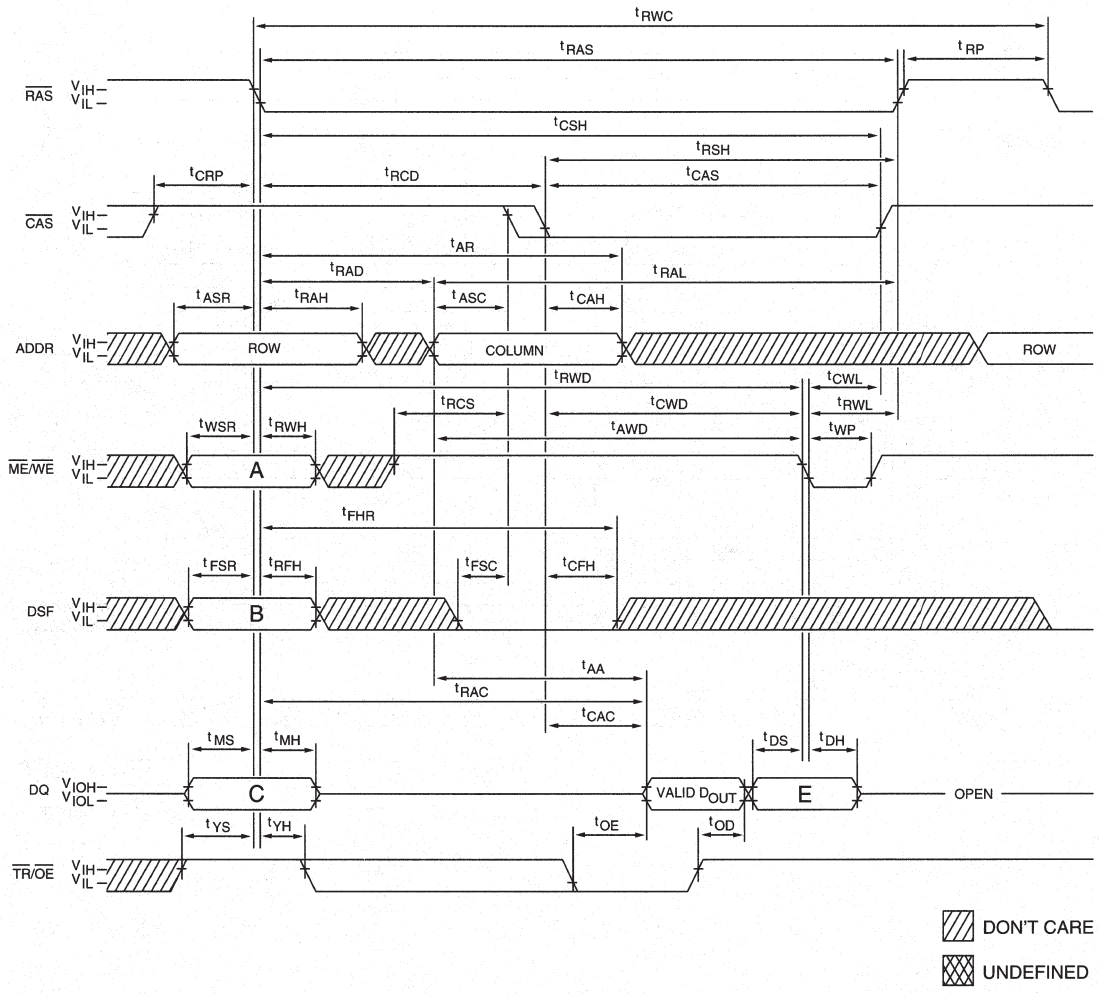
NOTE: 1. The logic states of "A", "B", "C", "D" and "E" determine the type of WRITE operation performed. See the Write Cycle Function Table for a detailed description.
2. For Block Write, $\overline{ME}/\overline{WE}$ = "don't care." For all other EARLY-WRITE cycles, $\overline{ME}/\overline{WE}$ = LOW.

DRAM LATE-WRITE CYCLE [1]



NOTE: 1. The logic states of "A", "B", "C" and "E" determine the type of WRITE operation performed. See the Write Cycle Function Table for a detailed description.

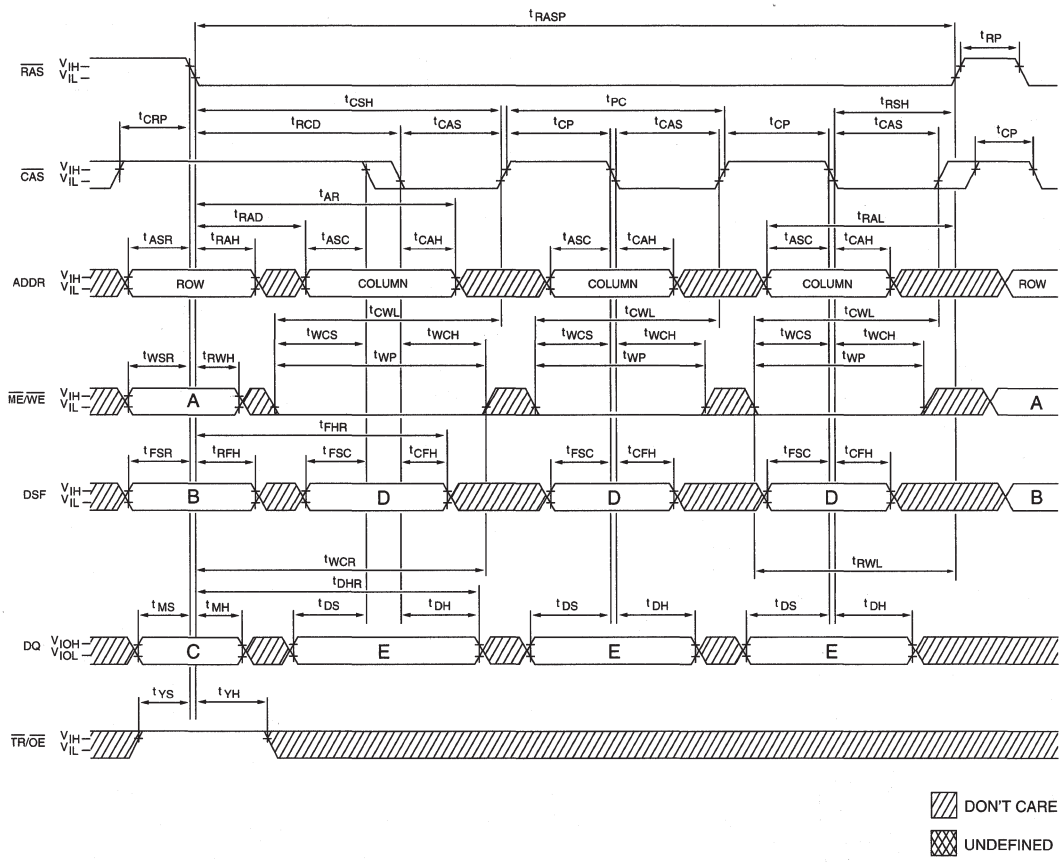
DRAM READ-WRITE CYCLE
(READ-MODIFY-WRITE CYCLE)



NOTE: The logic states of "A", "B", "C" and "E" determine the type of WRITE operation performed. See the Write Cycle Function Table for a detailed description.

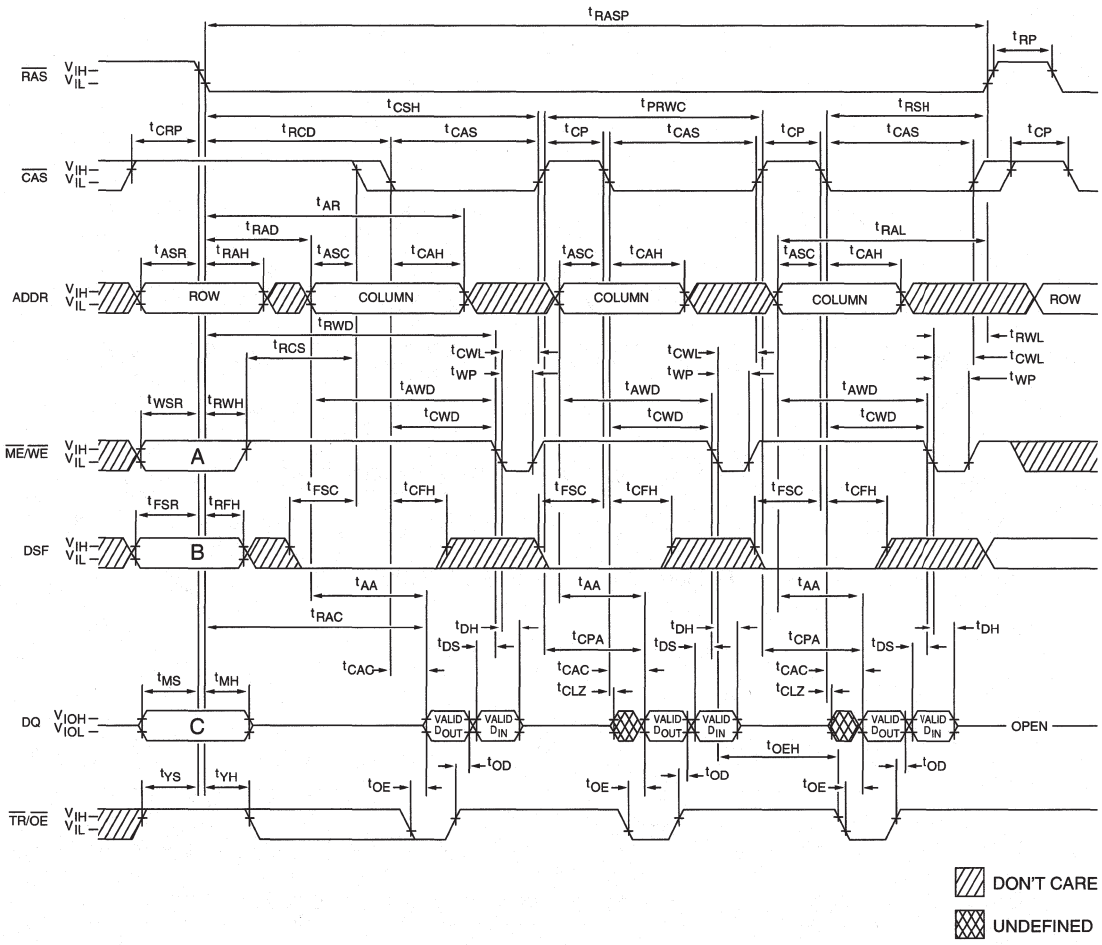
VRAM

DRAM FAST-PAGE-MODE EARLY-WRITE CYCLE



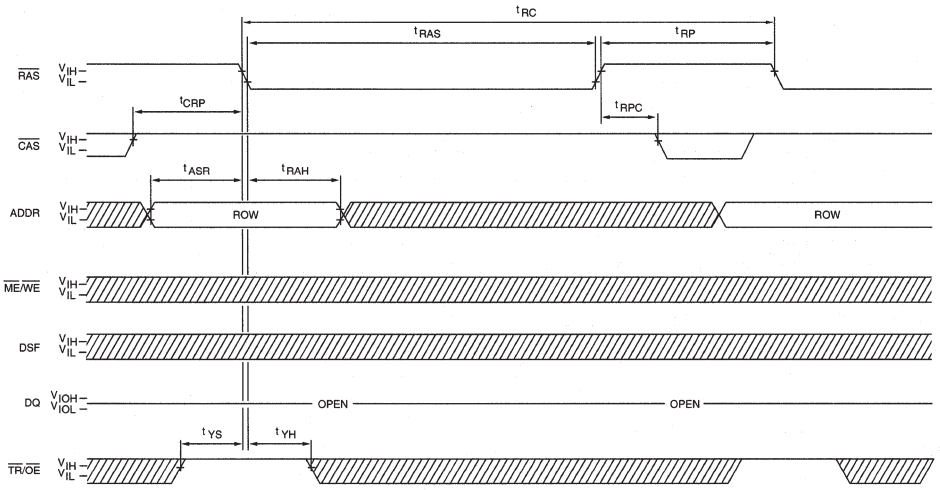
NOTE: 1. READ cycles or READ-MODIFY-WRITE cycles can be mixed with WRITE cycles while in FAST-PAGE-MODE.
2. The logic states of "A", "B", "C", "D" and "E" determine the type of WRITE operation performed. See the Write Cycle Function Table for a detailed description.

DRAM FAST-PAGE-MODE READ-WRITE CYCLE
(READ-MODIFY-WRITE OR LATE-WRITE CYCLES)

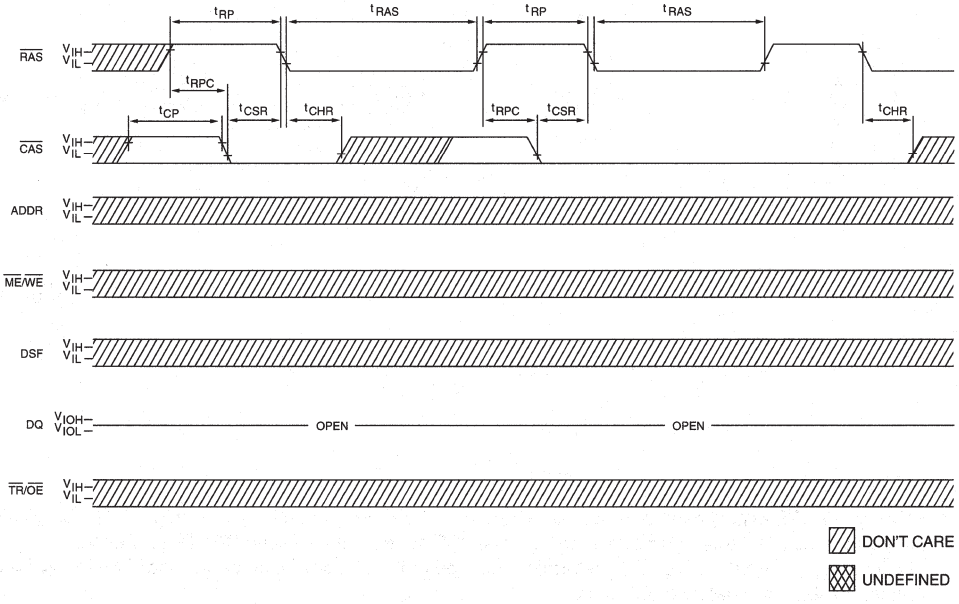


NOTE: 1. READ or WRITE cycles can be mixed with READ-MODIFY-WRITE cycles while in FAST-PAGE-MODE. Use the Write Function Table to determine the proper DSF state for the desired WRITE operation.
2. The logic states of "A", "B" and "C" determine the type of WRITE operation performed. See the Write Cycle Function Table for a detailed description.

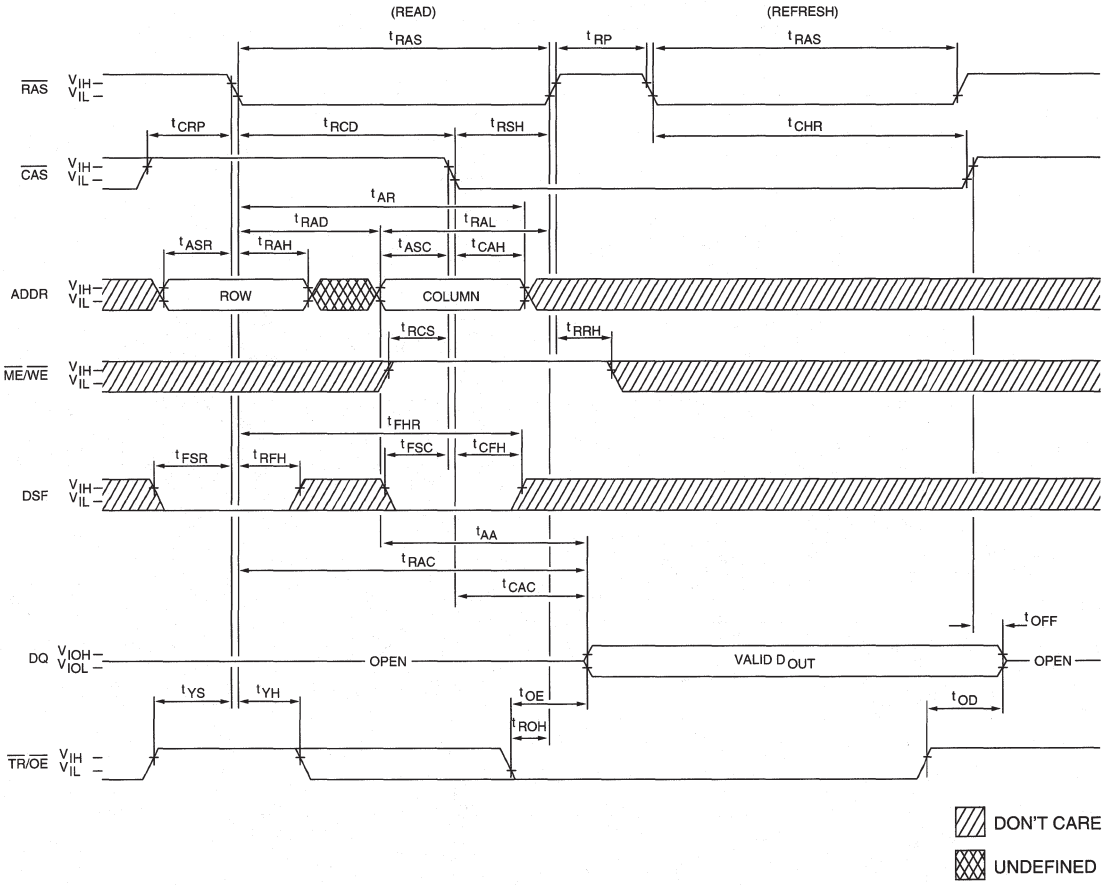
DRAM $\overline{RAS}$-ONLY REFRESH CYCLE
(ADDR = A0-A8)



DRAM CBR REFRESH CYCLE

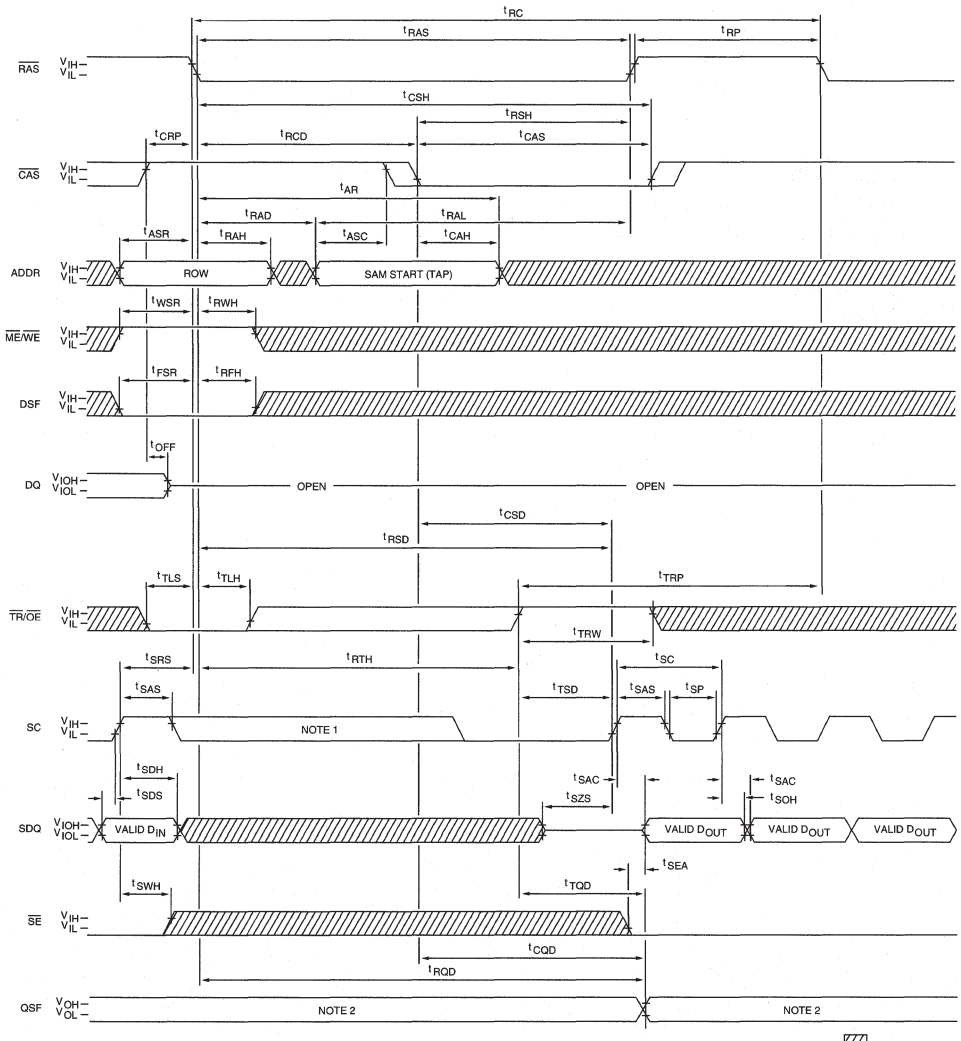


DRAM HIDDEN-REFRESH CYCLE



NOTE: A HIDDEN-REFRESH may also be performed after a WRITE or TRANSFER cycle. In the WRITE case, $\overline{ME}/\overline{WE}$ = LOW (when $\overline{CAS}$ goes LOW) and $\overline{TR}/\overline{OE}$ = HIGH and the DQ pins stay High-Z. In the TRANSFER case, $\overline{TR}/\overline{OE}$ = LOW (when $\overline{RAS}$ goes LOW) and the DQ pins stay High-Z during the refresh period, regardless of $\overline{TR}/\overline{OE}$.

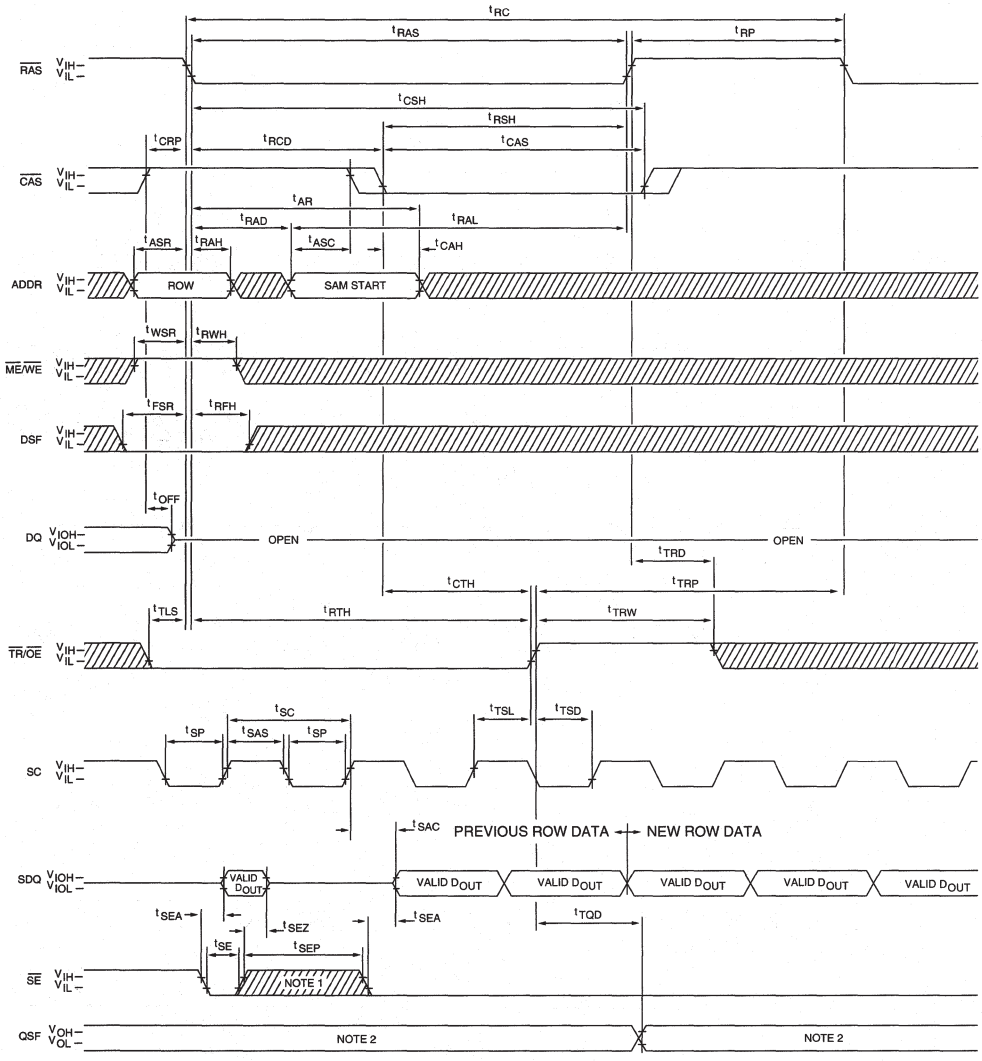
READ TRANSFER [3]
(DRAM-TO-SAM TRANSFER)
(When part was previously in the SERIAL INPUT mode or SC idle)



NOTE:
1. There must be no rising edges on the SC input during this time period.
2. QSF = 0 when the Lower SAM (bits 0–255) is being accessed.
   QSF = 1 when the Upper SAM (bits 256–511) is being accessed.
3. If tTLH is timing for the $\overline{TR}/(\overline{OE})$ rising edge, the transfer is self-timed and the tCSD and tRSD times must be met. If tRTH is timing for the $\overline{TR}/(\overline{OE})$ rising edge, the transfer is done off of the $\overline{TR}/(\overline{OE})$ rising edge and tTSD must be met.

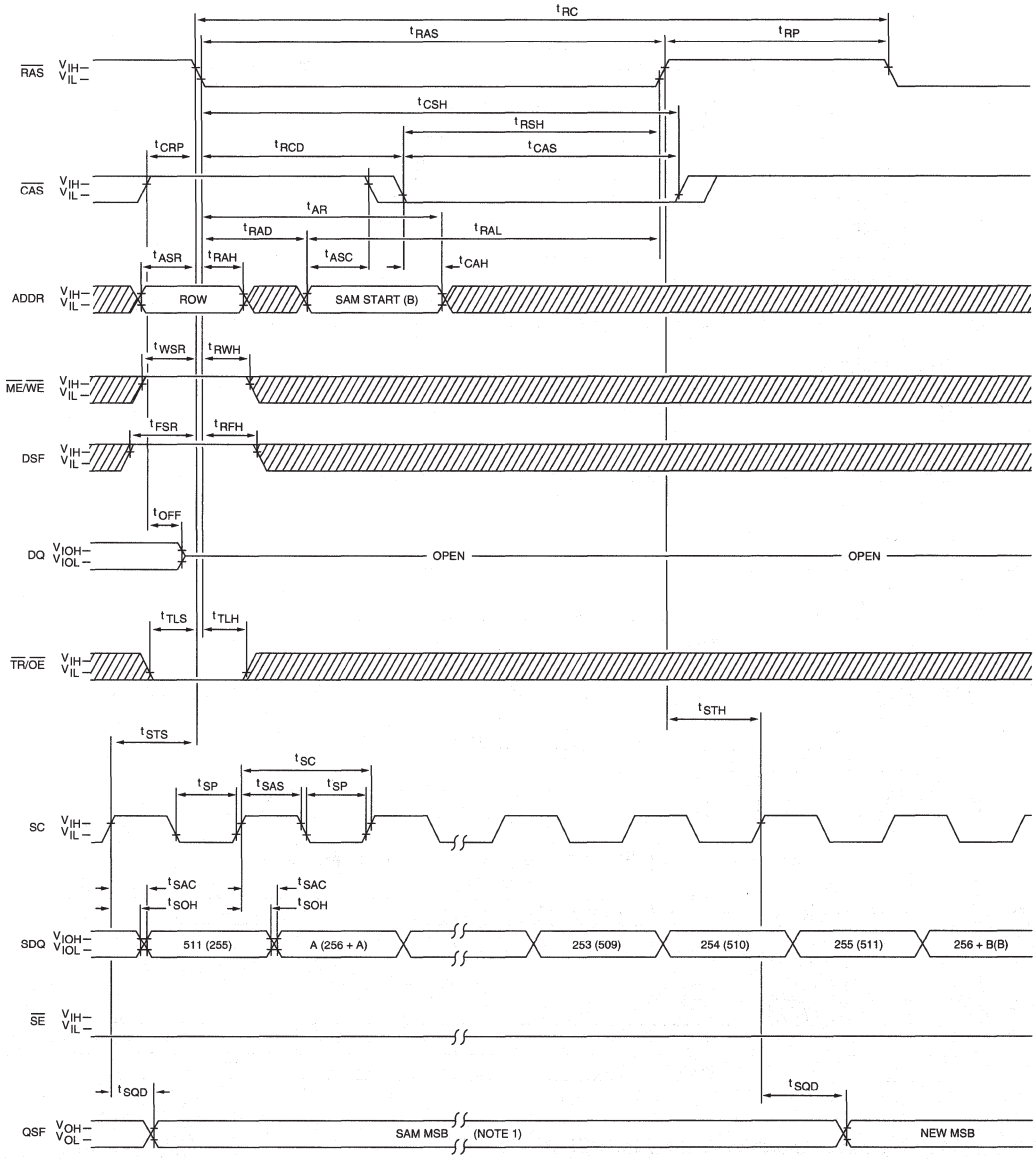
REAL-TIME READ-TRANSFER (DRAM-TO-SAM TRANSFER)

(When part was previously in the SERIAL OUTPUT mode)



NOTE: 1. The $\overline{SE}$ pulse is shown to illustrate the SERIAL OUTPUT ENABLE and DISABLE timing. It is not required.
2. QSF = 0 when the Lower SAM (bits 0–255) is being accessed.
QSF = 1 when the Upper SAM (bits 256–511) is being accessed.

SPLIT READ TRANSFER
(SPLIT DRAM-TO-SAM TRANSFER)

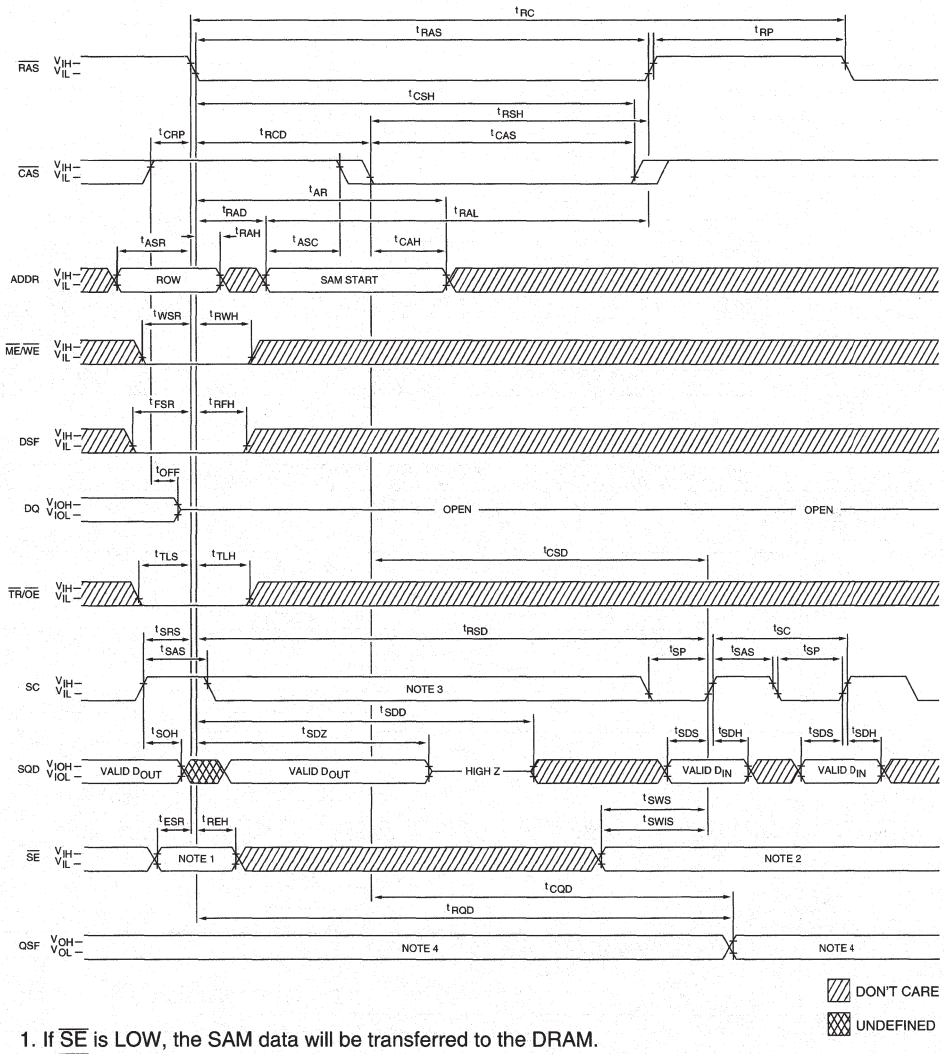


NOTE: 1. QSF = 0 when the Lower SAM (bits 0–255) is being accessed.
QSF = 1 when the Upper SAM (bits 256–511) is being accessed.

DON'T CARE
UNDEFINED

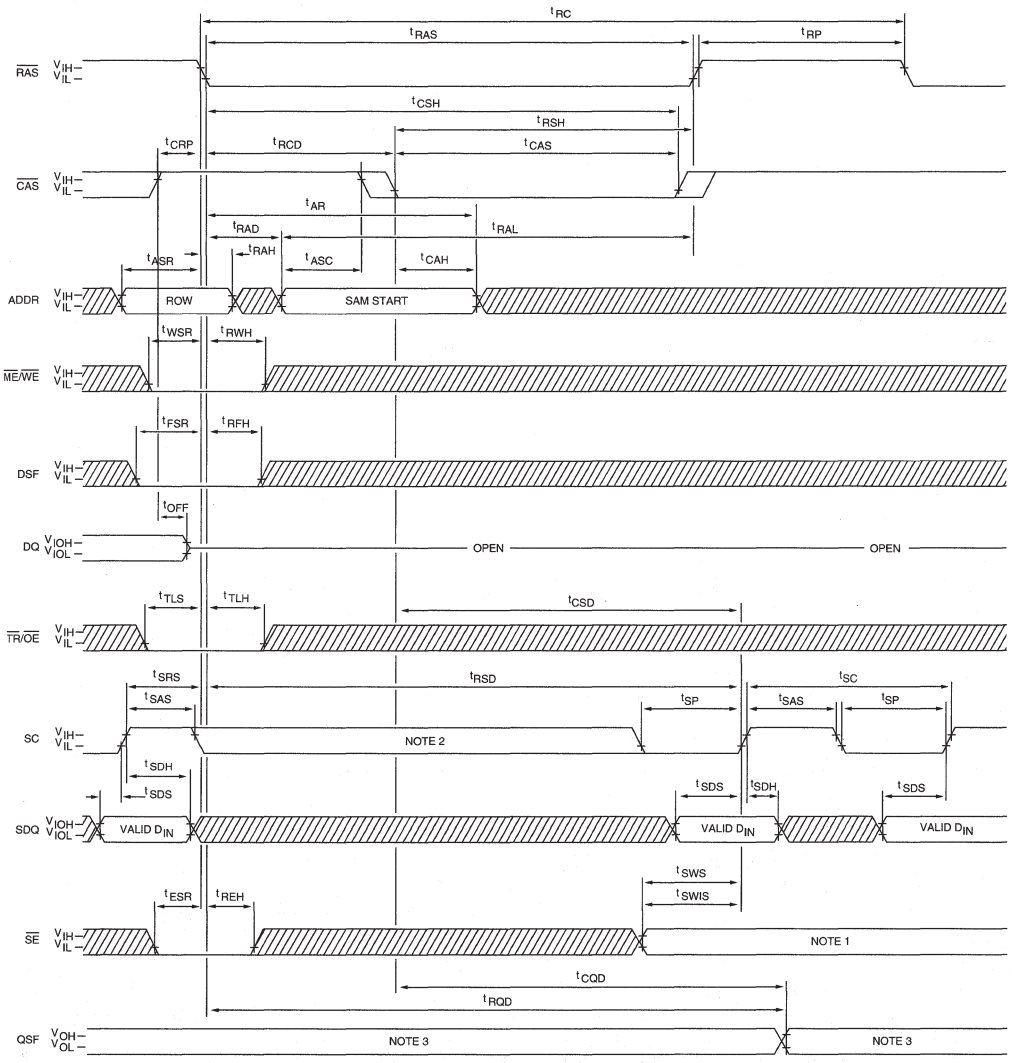
WRITE TRANSFER and PSEUDO WRITE TRANSFER (SAM-TO-DRAM TRANSFER)

(When part was previously in the SERIAL OUTPUT mode)



NOTE:
1. If $\overline{SE}$ is LOW, the SAM data will be transferred to the DRAM.
   If $\overline{SE}$ is HIGH, the SAM data will not be transferred to the DRAM (SERIAL-INPUT-MODE ENABLE cycle).
2. $\overline{SE}$ must be LOW to input new serial data, but the serial address register is incremented by SC regardless of $\overline{SE}$.
3. There must be no rising edges on the SC input during this time period.
4. QSF = 0 when the Lower SAM (bits 0–255) is being accessed.
   QSF = 1 when the Upper SAM (bits 256–511) is being accessed.

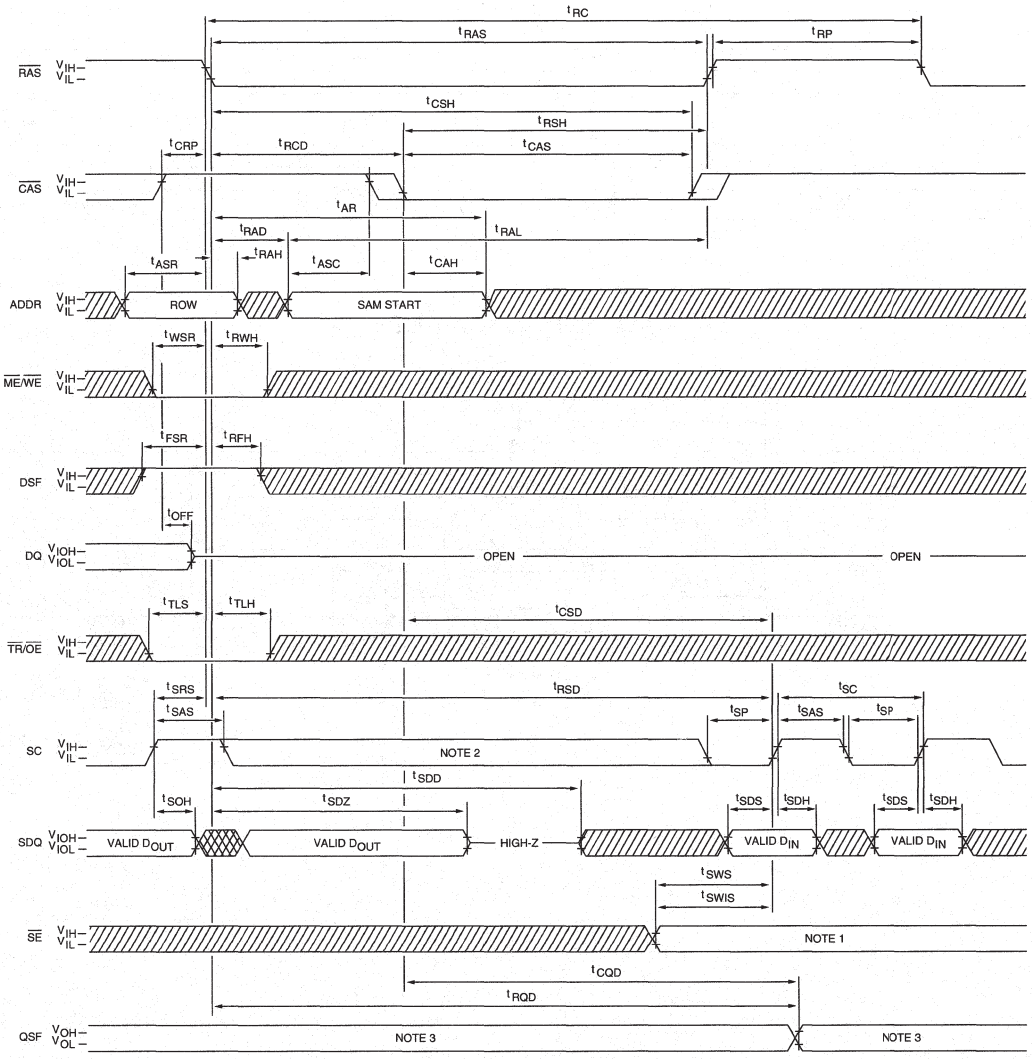
WRITE TRANSFER
(SAM-TO-DRAM TRANSFER)
(When part was previously in the SERIAL INPUT mode)



NOTE:
1. $\overline{SE}$ must be LOW to input new serial data, but the serial address register is incremented by SC regardless of $\overline{SE}$.
2. There must be no rising edges on the SC input during this time period.
3. QSF = 0 when the Lower SAM (bits 0–255) is being accessed.
   QSF = 1 when the Upper SAM (bits 256–511) is being accessed.

DON'T CARE
UNDEFINED

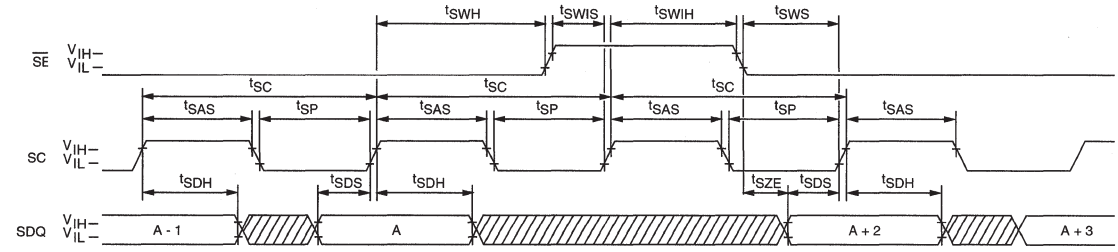
ALTERNATE WRITE TRANSFER (SAM-TO-DRAM TRANSFER)



NOTE:
1. $\overline{SE}$ must be LOW to input new serial data, but the serial address register is incremented by SC regardless of $\overline{SE}$.
2. There must be no rising edges on the SC input during this time period.
3. QSF = 0 when the Lower SAM (bits 0–255) is being accessed.
   QSF = 1 when the Upper SAM (bits 256–511) is being accessed.

VRAM

SAM SERIAL INPUT



SAM SERIAL OUTPUT