INTERNATIONAL CMOS
TECHNOLOGY, INC.

93C46
1,024-Bit Serial (5V only) CMOS Electrically Erasable Programmable Read Only Memory (EEPROM)

Features

- **Advanced CMOS EEPROM Technology**
- **Read/Write Non-volatile Memory**
  - — Single 5V supply operation
  - — 1,024 bits, 64 x 16 organization
  - — Versatile, easy to use serial data interface
- **Low Power Consumption**
  - — 3mA max Active
  - — 1mA max Standby, TTL interface
  - — 100µA max Standby, CMOS interface
- **Special Features**
  - — Automatic write cycle time-out
  - — Ready/Busy status signal
  - — Software controlled write protection
- **Ideal For Low-Density Data Storage**
  - — Low cost, space saving, 8-pin package
  - — Commercial, industrial, & military versions
  - — Interfaces with popular microcomputers (ie., COP4XX, 8048, 8049, 8051, 8096, 6805, 6801, TMS1000, Z8)
- **Application Versatility**
  - — Alarms, Electronic Locks, Appliances, Terminals, Smart Cards, Robotics, Meters, Telephones, Tuners, etc.
- **Reliability**
  - — 10,000 or 100,000 erase/write cycles
  - — Over 40 year data retention[1]

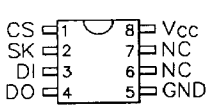
General Description

The ICT 93C46 is a 1,024-bit, 5V-only, serial read/write, non-volatile memory device fabricated using an advanced CMOS EEPROM technology. Its 1,024 bits of memory are organized into 64 registers each. Each register is individually addressable for serial read or write operations. A versatile serial interface consisting of chip select, clock, data-in and data-out, can easily be controlled by popular microcomputers (ie., COP4XX, 8048, 8049, 8051, 6805, 6801, TMS1000,Z8) or standard microprocessors.

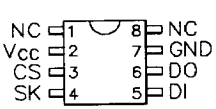
Low power consumption, low cost, and space efficiency make the ICT 93C46 an ideal candidate for high volume, low density data storage applications. Special features of the 93C46 include: automatic write time-out, ready/busy status signal, software controlled write protection, and ultra-low standby power mode when deselected (CS low). Additionally, the 93C46 offers functional compatibility with existing NMOS serial EEPROMs. The 93C46 is designed for applications requiring 10,000 or 100,000 erase/write cycles per register.

Connection Diagrams

DIP Package

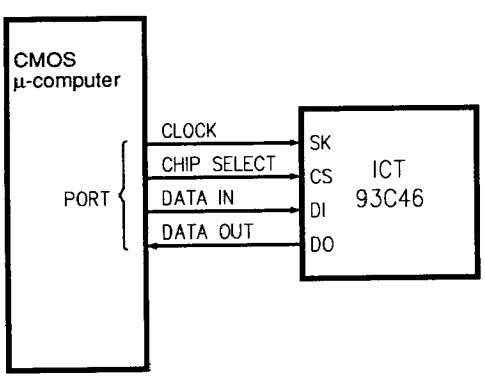


SO8 Package



Pin Names

CS	= Chip Select
SK	= Serial Data Clock
DI	= Serial Data Input
DO	= Serial Data Output
GND	= Ground
Vcc	= Power Supply
NC	= Not Connected



Interfacing the 93C46

Function Description

Device Operation

The ICT 93C46 is a serial 1,024-bit non-volatile memory device organized as 64 registers by 16 bits. Each register is independently addressable for read, write, or erase operations. Seven, 9-bit instructions control the operation of the device. These instructions are clocked into the data input (DI) pin in a serial fashion as controlled by the chip select (CS) and serial data clock (SK) inputs. The instructions include: read; write; erase; erase/write enable; erase/write disable; write all; and erase all registers.

The format of each 9-bit instruction-starting with the most significant bit-is as follows: start bit (logical "1"); a two-bit op code; and an eight-bit address. The DO pin is normally in a high-impedance state, except when reading data from the device, or when checking the BUSY/READY status after a programming operation. The BUSY/READY status can be determined after a programming operation by selecting the device (CS high) and polling the DO pin. DO low indicates that the programming operation is not completed, while DO high indicates that the device is ready for the next operation. DO will return to the high-impedance state when the next instruction is initiated.

The 93C46 operates on a single supply voltage, which may range from 4.5 Volts to 5.5 Volts, and will generate, on chip, the high voltage required for any programming operation.

Read (READ)

The read (READ) instruction outputs serial data on the DO pin. After a read instruction is received, the instruction and the address are decoded. Then data is transferred from the selected memory register to a 16-bit shift register and DO comes out of the high-impedance state. After sending a dummy bit (logical "0"), the 16-bit data string is shifted out of the device. The DO transitions occur on the rising edge of the clock and the data is stable after the specified delay t_{PO} or t_{PD1}.

Erase/Write Enable and Disable (EWEN and EWDS)

The 93C46 powers up in the programming-disable state. Any programming after power-up, or following a write disable (WDS) instruction, must first be preceded by a write enable (WEN) instruction. Once enabled, programming remains enabled until a write disable (WDS) instruction is executed or power is removed from the device. The write disable instruction disables all programming functions of the 93C46 and can be used to prevent accidentally disturbing data in the device. Data can be read from the 93C46 regardless of the programming enable/disable status.

Erase (ERASE)

It is necessary to erase each register (all bits set to logical "1") before writing to it (certain bits set to logical "0"). After receiving the erase instruction, CS (chip select) must be held low for a minimum period specified by t_{CS}. After inputting an erase instruction, the falling edge of CS initiates the self-timed write cycle. After observing t_{CS}, the READY/BUSY status of the device can be determined by selecting the device and polling the DO pin.

Write (WRITE)

The write instruction (opcode plus address to be written to) is followed by 16 bits of data to be written into the specified address. After the last bit of data (D_0) has been clocked into the DI pin, the CS (chip select) must be brought low before the next rising edge of the SK clock and held low for the minimum period specified by t_{CS}. The falling edge of CS initiates the self-timed programming cycle. It is not necessary to clock the SK pin after initiating the self-timed write mode. The READY/BUSY status of the device can be determined by selecting the device and polling the DO pin.

Write All (WRAL)

The write-all (WRAL) instruction simultaneously programs all registers with the data pattern specified in the instruction. After receiving the write-all instruction and 16 bits of data, CS (chip select) must be held low for a minimum period specified by t_{CS}. The falling edge of CS initiates the self-timed write cycle. It is not necessary to clock the SK pin after initiating the self-timed write-all mode. The BUSY/READY status of the device can be determined by selecting the device and polling the DO pin.

Erase All (ERAL)

Entire chip erasing is provided for ease of programming. The erase-all (ERAL) instruction simultaneously programs every bit on the chip to a logical "1". After receiving the erase-all instruction, CS (chip select) must be held low for a minimum period specified by t_{CS}. The falling edge of CS initiates the self-timed write cycle. It is not necessary to clock the SK pin after initiating the self-timed erase-all mode. The BUSY/READY status of the device can be determined by selecting the device and polling the DO pin.

Absolute Maximum Ratings

Exposure to absolute maximum ratings over extended periods of time may affect device reliability. Exceeding absolute maximum ratings may cause permanent damage

Symbol	Parameter	Conditions	Rating	Unit
V_{CC}	Supply Voltage	Relative to GND	− 0.6 to +7.0	V
V_{IO}	Voltage Applied to Any Pin	Relative to GND	− 0.6 to V_{CC} + 0.6	V
T_{ST}	Storage Temperature		− 65 to + 150	°C
T_{LT}	Lead Temperature	Soldering 10 seconds	+ 300	°C

Operating Ranges

Symbol	Parameter	Commercial 93C46		Industrial 93C46 I		Military 93C46 M		Unit
		Min	Max	Min	Max	Min	Max	
V_{CC}	Supply Voltage	4.5	5.5	4.5	5.5	4.5	5.5	V
T_A	Ambient Temperature[1]	0	+ 70	− 40	+ 85	− 55	+ 125	°C

DC and AC Electrical Characteristics

Over the operating range

Symbol	Parameter	Conditions	93C46		93C46 I		93C46 M		Unit
			Min	Max	Min	Max	Min	Max	
I_{CC}	Power Supply Current, Active, TTL/CMOS Interface	V_{CC} = 5.5V, CS=SK=V_{IH} DO = Open, f = 250 KHz		3		6		7	mA
I_{CCSB1}	Supply Current, Standby, TTL/CMOS Interface	V_{CC} = 5.5V, CS = V_{IL} DO = Open		1		3		3	mA
I_{CCSB2}	Supply Current, Standby, CMOS Interface			100		100		100	µA
V_{IH}	Input HIGH Level		2.0	V_{CC}+1	2.0	V_{CC}+1	2.0	V_{CC}+1	V
V_{IL}	Input LOW Level		− 0.1	0.8	− 0.1	0.8	− 0.1	0.8	V
V_{OH}	Output HIGH Voltage	I_{OH} = − 0.4mA	2.2		2.2		2.2		V
V_{OL}	Output LOW Voltage	I_{OL} = 2.1mA		0.4		0.4		0.4	V
I_{LI}	Input Leakage Current	V_{IN} = 5.5V		10		10		10	µA
I_{LO}	Output Leakage Current	V_O=5.5V, CS=0, $V_{CC} \leq$ 5.5V		10		10		10	µA
t_{SKP}	SK Period		4	0	4	0	4	0	µs
t_{SKW}	SK Pulse Width	High or Low	1		1		1		µs
t_{CSS}	CS High to SK High Delay		200		200		200		ns
t_{CSH}	SK Low to CS Low Delay		0		0		0		ns
t_{DIS}	Data Setup Time (Write)		400		400		400		ns
t_{DIH}	Data Hold Time (Write)		400		400		400		ns
t_{PD1} t_{PD0}	Serial Clock to Output Delay	C_L = 100pF, V_{OL} = 0.8V, V_{OH} = 2.0V, V_{IL} = 0.45V, VIH = 2.4V		2		2		2	µs
$t_{E/W}$	Self-timed Program Cycle [2]			10		10		10	ms
t_{CS}	Min CS Low Time		1		1		1		µs
t_{SV}	CS to Status Valid	CL = 100pF		1		1		1	µs
t_{OH}, t_{IH}	Falling Edge of CS to DO High Impedence			400		400		400	ns

Notes

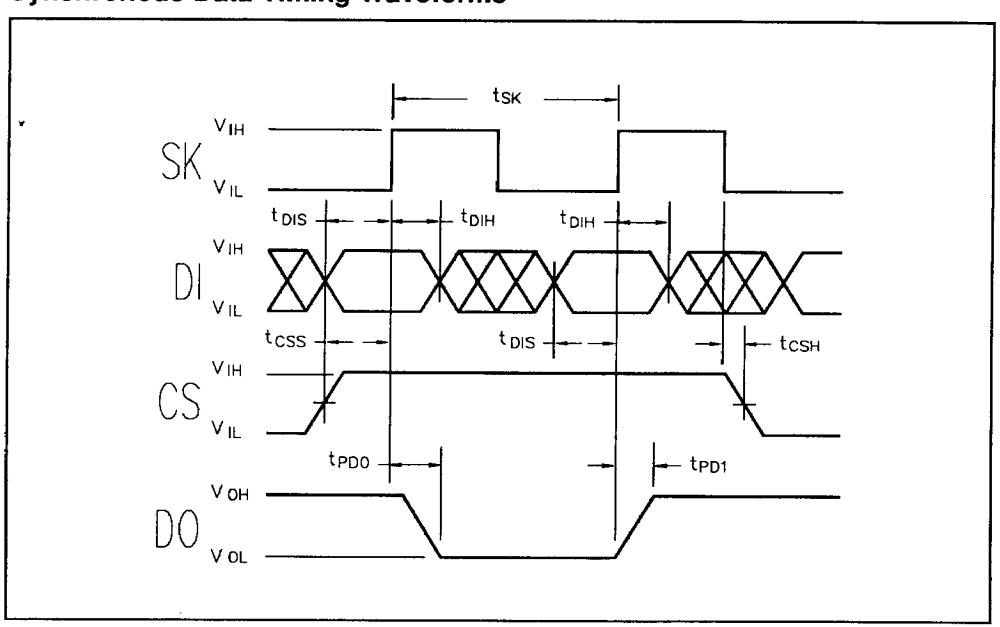
1. ICT's E^2 devices are designed to endure 10,000 or 100,000 (93C46E) Erase/Write cycles and to retain data for at least forty years while operating at 55°C. ICT's standard test flow verifies at least ten years of data retention for Commercial and Industrial temperature devices and at least two years data retention for Military temperature devices. Data retention verification is performed on 100% of the units being shipped. Cycling endurance is verified by lot sample testing.

2. Although the 93C46 self-timed program cycle allows software delay loops to be used to achieve the necessary Erase/Write delay, using the Ready/Busy feature is recommended instead. Using the Ready/Busy feature allows faster response time since TE/W will typically be less than the maximum specification.

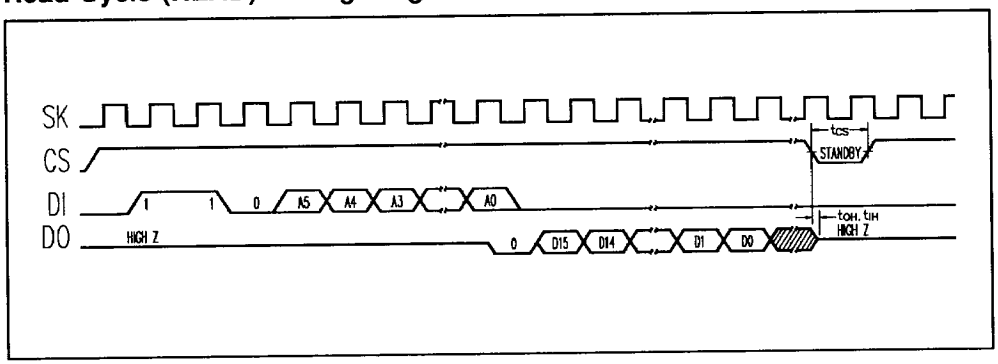
Instruction set for the 93C46

Instruction	Start Bit	Opcode	Address	Data	Comments
READ	1	10	$A_5A_4A_3A_2A_1A_0$		Read address
WRITE	1	01	$A_5A_4A_3A_2A_1A_0$	D_{15} - D_0	Write to address
ERASE	1	11	$A_5A_4A_3A_2A_1A_0$		Erase address
EWEN	1	00	1 1 X X X X		ERASE/WRITE enable
EWDS	1	00	0 0 X X X X		ERASE/WRITE disable
ERAL	1	00	1 0 X X X X		Erase all addresses
WRAL	1	00	0 1 X X X X	D_{15} - Do	Write all addresses

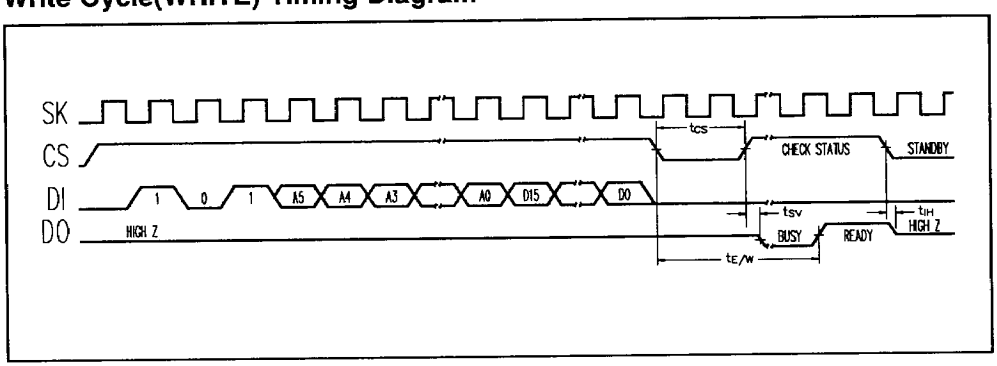
Synchronous Data Timing Waveforms



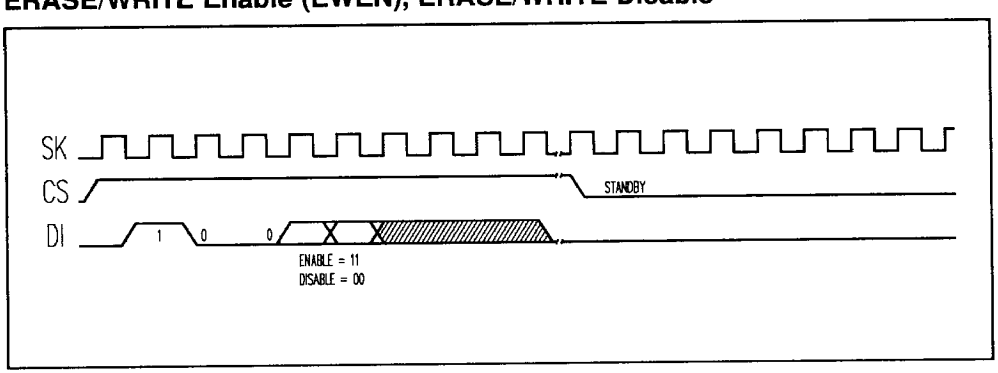
Read Cycle (READ) Timing Diagram



Write Cycle(WRITE) Timing Diagram



ERASE/WRITE Enable (EWEN), ERASE/WRITE Disable



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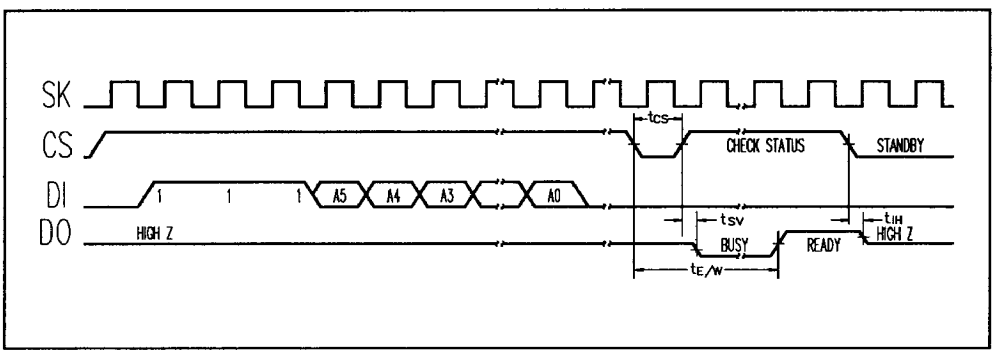
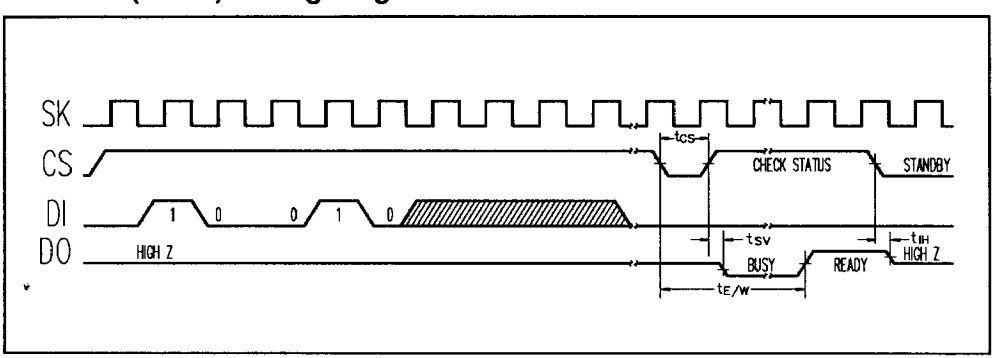
Erase (ERASE)Timing Diagram



Erase All (ERAL) Timing Diagram



Write All (WRAL) Timing Diagram