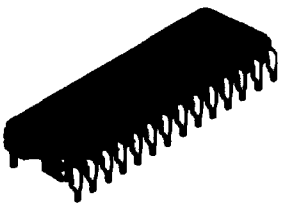
HN58C65 Series

8192-word x 8-bit Electrically Erasable and Programmable CMOS ROM

■ FEATURES

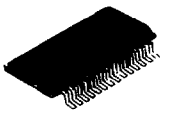
- Single 5V Supply
- On Chip Latches; Address, Data, $\overline{CE}$, $\overline{OE}$, $\overline{WE}$
- Automatic Byte Write . . . . . 10ms typ.
- Automatic Page Write
  (32byte) . . . . . 10ms typ.
- Fast Access Time . . . . . 250ns max.
- Low Power Dissipation . . . 20mW/MHz typ. (Active)
  . . . 2mW typ. (Standby)
- $\overline{Data}$ Polling and Ready/$\overline{Busy}$
- Data Protection Circuity on Power On/Power Off
- Conforms to JEDEC Byte-Wide Standard
- Reliable CMOS with MNOS Cell Technology
- 10000 Erase/Write Cycles and 10 year Data Retention

HN58C65P Series



(DP-28)

HN58C65FP Series

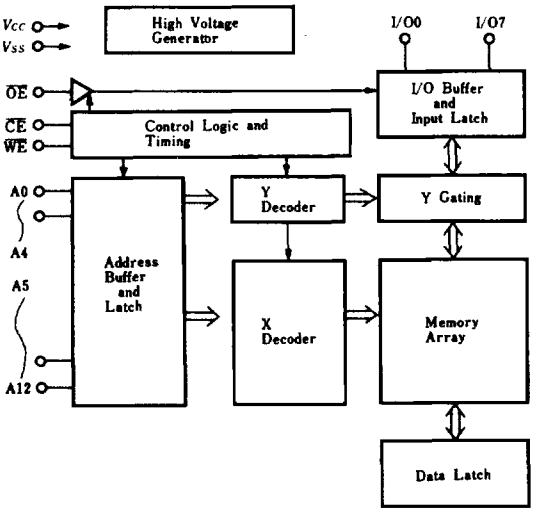


(FP-28DA)

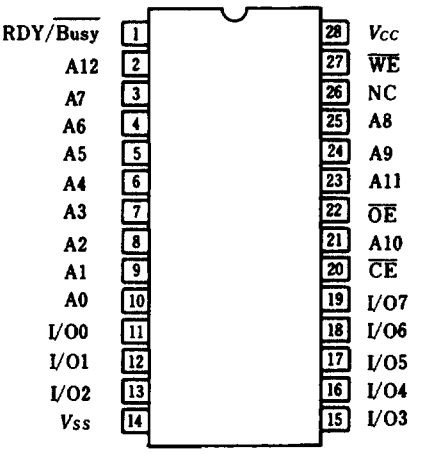
■ ORDERING INFORMATION

Type No.	Access Time	Package
HN58C65P-25	250ns	600 mil 28 pin Plastic DIP
HN58C65FP-25T	250ns	28 pin Plastic SOP

■ BLOCK DIAGRAM



■ PIN ARRANGEMENT



(Top View)

■ PIN DESCRIPTION

A0 – A12	Address Input
I/O1 – I/O7	Data In/Data Out
$\overline{OE}$	Output Enable
$\overline{CE}$	Chip Enable
$\overline{WE}$	Write Enable
RDY/$\overline{Busy}$	Ready/$\overline{Busy}$
V_{CC}	Power (+5V)
V_{SS}	GND
NC	No Connect

■ MODE SELECTION

MODE \ PINS	$\overline{CE}$ (20)	$\overline{OE}$ (22)	$\overline{WE}$ (27)	RDY/$\overline{Busy}$ (1)	I/O (11 – 13, 15 – 19)
Read	V_{IL}	V_{IL}	V_{IH}	High Z	Dout
Standby	V_{IH}	×	×	High Z	High Z
Write	V_{IL}	V_{IH}	V_{IL}	High Z→ V_{OL}	Din
Deselect	V_{IL}	V_{IH}	V_{IH}	High Z	High Z
Write Inhibit	×	×	V_{IH}	High Z	–
Write Inhibit	×	V_{IL}	×	High Z	–
Data Polling	V_{IL}	V_{IL}	V_{IH}	V_{OL}	Data Out (I/O7)

Note) X: V_{IL} or V_{IH}

■ ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Value	Unit
Supply Voltage*1	V_{CC}	–0.6 to +7.0	V
Input Voltage*1	V_{in}	–0.5*2 to +7.0	V
Operating Temperature Range	T_{opr}	0 to +70	°C
Storage Temperature Range	T_{stg}	–55 to +125	°C

Notes) *1. With respect to V_{SS}.
*2. –3.0V for pulse width ≦ 50ns.

■ RECOMMENDED DC OPERATING CONDITIONS

Item	Symbol	min.	typ.	max.	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Input Voltage	V_{IL}	–0.3	–	0.8	V
	V_{IH}	2.2	–	V_{CC}+1	V
Operating Temperature	T_{opr}	0	–	70	°C

■ DC AND OPERATING CHARACTERISTICS (T_a=0 to +70°C, V_{CC}=5V±10%)

Parameter	Symbol	Test Condition	min.	typ.	max.	Unit
Input Leakage Current	I_{LI}	V_{CC} = 5.5V V_{in} = 5.5V	–	–	2	μA
Output Leakage Current	I_{LO}	V_{CC} = 5.5V V_{out} = 5.5/0.4V	–	–	2	μA
V_{CC} Current (Standby)	I_{CC1}	$\overline{CE}$ = V_{IH}	–	–	1	mA
V_{CC} Current (Active)	I_{CC2}	Iout=0mA, duty=100%, cycle 1μs	–	–	8	mA
		Iout=0mA, duty=100%, Min. Cycle	–	–	25	mA
Input Low Voltage	V_{IL}		–0.3*1	–	0.8	V
Input High Voltage	V_{IH}		2.2	–	V_{CC}+1	V
Output Low Voltage	V_{OL}	I_{OL} = 2.1mA	–	–	0.4	V
Output High Voltage	V_{OH}	I_{OH} = –400μA	2.4	–	–	V

Note) *1. –1.0V for pulse width ≦ 50ns

■ CAPACITANCE (T_a=25°C, f=1MHz)

Parameter	Symbol	Test Condition	min.	typ.	max.	Unit
Input Capacitance	C_{in}	V_{in} = 0V	–	–	6	pF
Output Capacitance	C_{out}	V_{out} = 0V	–	–	12	pF

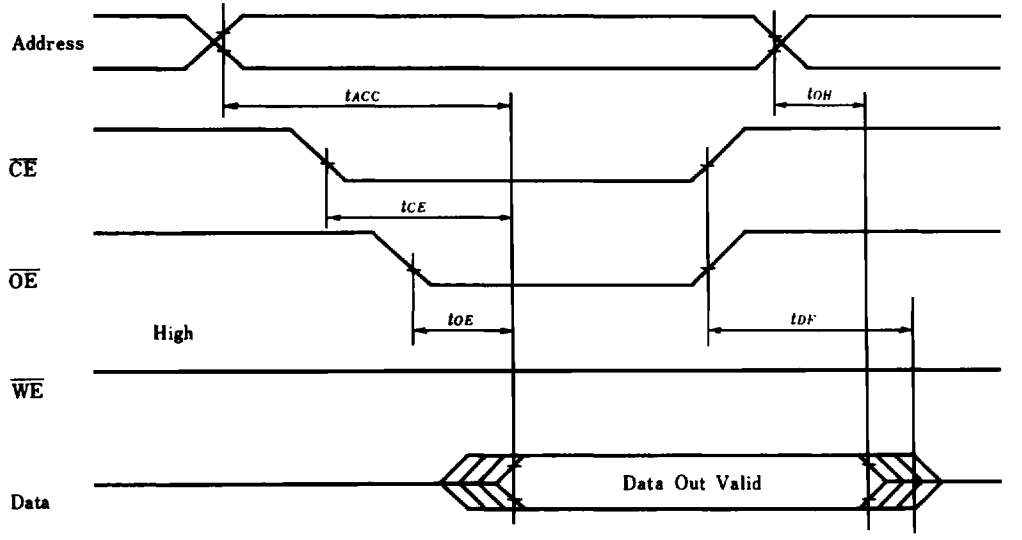
■ AC CHARACTERISTICS (T_a=0 to +70°C, V_{CC}=5V±10%)

• AC Test Conditions

Input Pulse Levels:	0.40V to 2.4V
Input Rise and Fall Time:	≤20ns
Output Load:	1TTL Gate + 100pF
Reference Levels for Measuring Timing Inputs Outputs:	0.8V and 2V

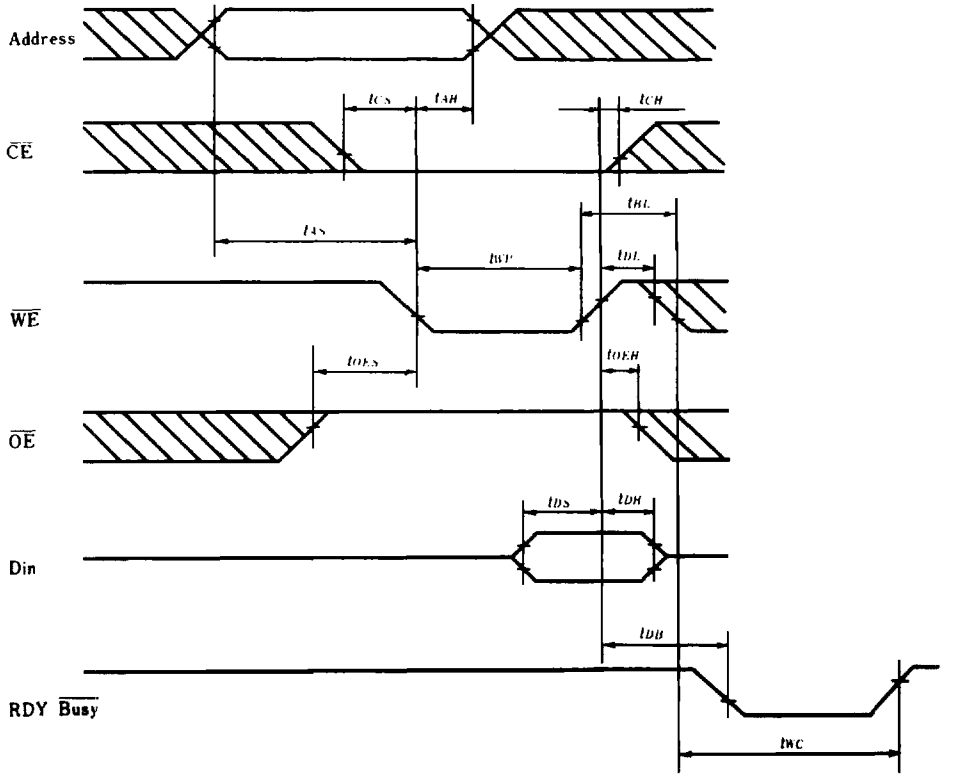
• Read Operation

Parameter	Symbol	Test Condition	HN58C65-25		Unit
			min.	max.	
Address to Output Delay	t_{ACC}	$\overline{CE}$ = $\overline{OE}$ = V_{IL} $\overline{WE}$ = V_{IH}	–	250	ns
$\overline{CE}$ to Output Delay	t_{CE}	$\overline{OE}$ = V_{IL} $\overline{WE}$ = V_{IH}	–	250	ns
$\overline{OE}$ to Output Delay	t_{OE}	$\overline{CE}$ = V_{IL} $\overline{WE}$ = V_{IH}	10	100	ns
Address to Output Hold	t_{OH}	$\overline{CE}$ = $\overline{OE}$ = V_{IL} $\overline{WE}$ = V_{IH}	0	–	ns
$\overline{OE}$ High to Output Float	t_{DF}	$\overline{CE}$ = V_{IH} $\overline{WE}$ = V_{IH}	0	90	ns



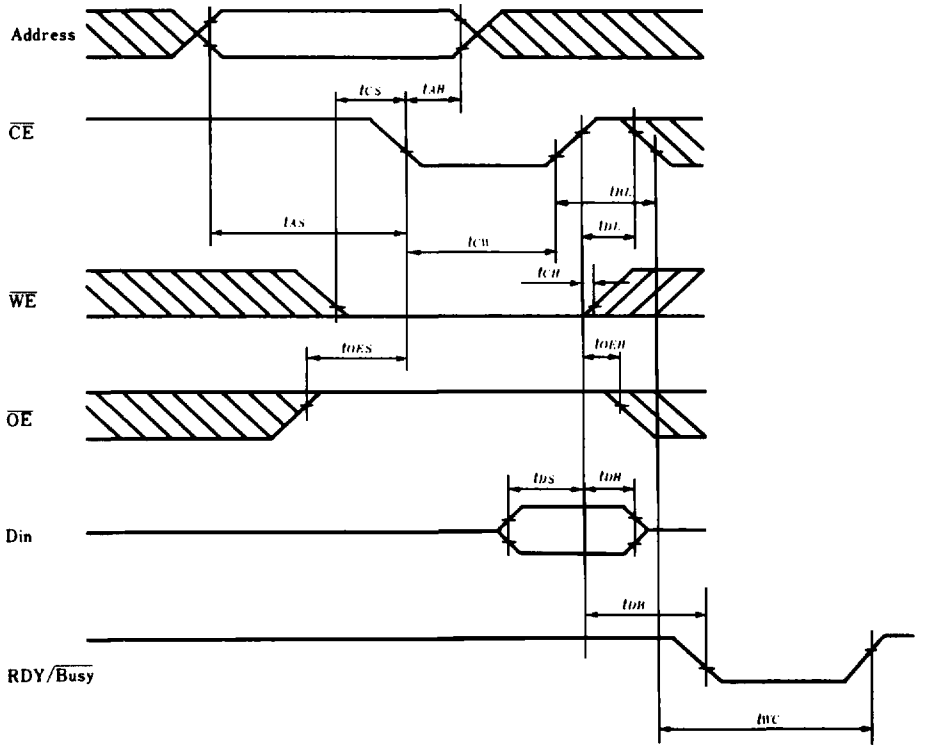
• Byte Erase and Byte Write Operation ($\overline{WE}$ Controlled Write Cycle)

Parameter	Symbol	min.	typ.	max.	Unit
Address Setup Time	t_{AS}	0	–	–	ns
$\overline{CE}$ to Write Setup Time	t_{CS}	0	–	–	ns
Write Pusle Width	t_{WP}	200	–	–	ns
Address Hold Time	t_{AH}	150	–	–	ns
Data Setup Time	t_{DS}	100	–	–	ns
Data Hold Time	t_{DH}	20	–	–	ns
$\overline{CE}$ Hold Time	t_{CH}	0	–	–	ns
$\overline{OE}$ to Write Setup Time	t_{OES}	0	–	–	ns
$\overline{OE}$ Hold Time	t_{OEH}	0	–	–	ns
Data Latch Time	t_{DL}	100	–	–	ns
Time to Device Busy	t_{DB}	120	–	–	ns
Write Cycle Time	t_{WC}	–	–	15	ms
Byte Load Window	t_{BL}	30	–	100	μs



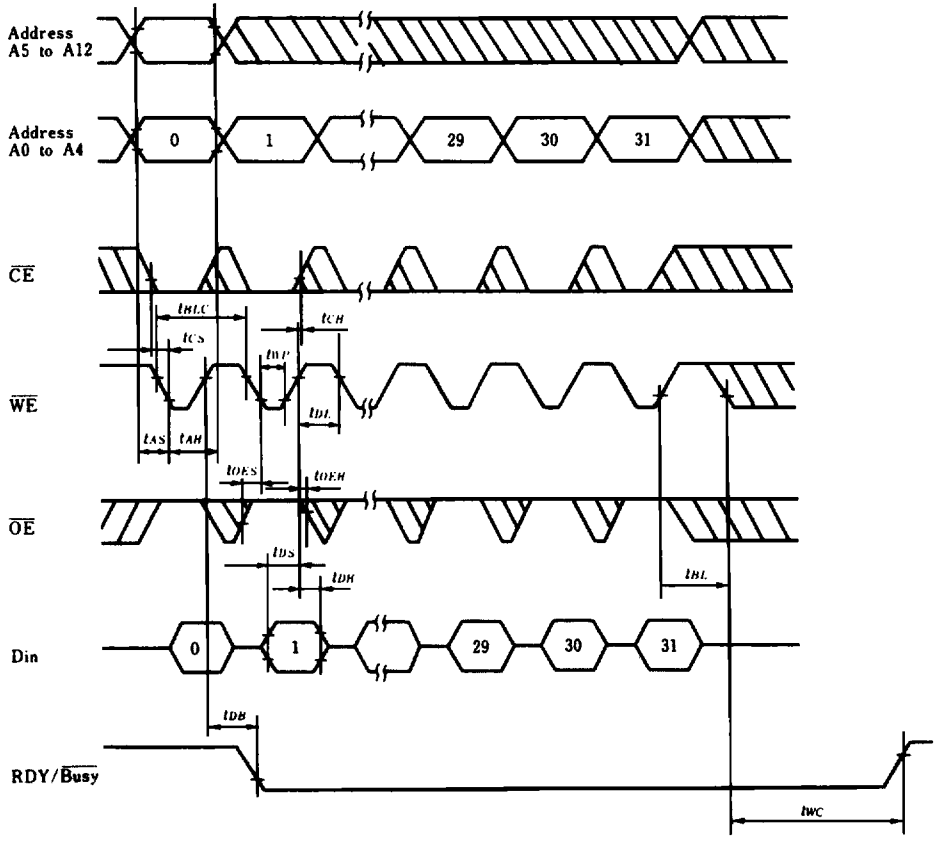
• Byte Erase and Byte Write Operation ($\overline{CE}$ Controlled Write Cycle)

Parameter	Symbol	min.	typ.	max.	Unit
Address Setup Time	t_{AS}	0	–	–	ns
$\overline{CE}$ to Write Setup Time	t_{CS}	0	–	–	ns
$\overline{CE}$ Pulse Width	t_{CW}	200	–	–	ns
Address Hold Time	t_{AH}	150	–	–	ns
Data Setup Time	t_{DS}	100	–	–	ns
Data Hold Time	t_{DH}	20	–	–	ns
$\overline{CE}$ Hold Time	t_{CH}	0	–	–	ns
$\overline{OE}$ to Write Setup Time	t_{OES}	0	–	–	ns
$\overline{OE}$ Hold Time	t_{OEH}	0	–	–	ns
Data Latch Time	t_{DL}	100	–	–	ns
Time to Device Busy	t_{DB}	120	–	–	ns
Write Cycle Time	t_{WC}	–	–	15	ms
Byte Load Window	t_{BL}	30	–	100	µs



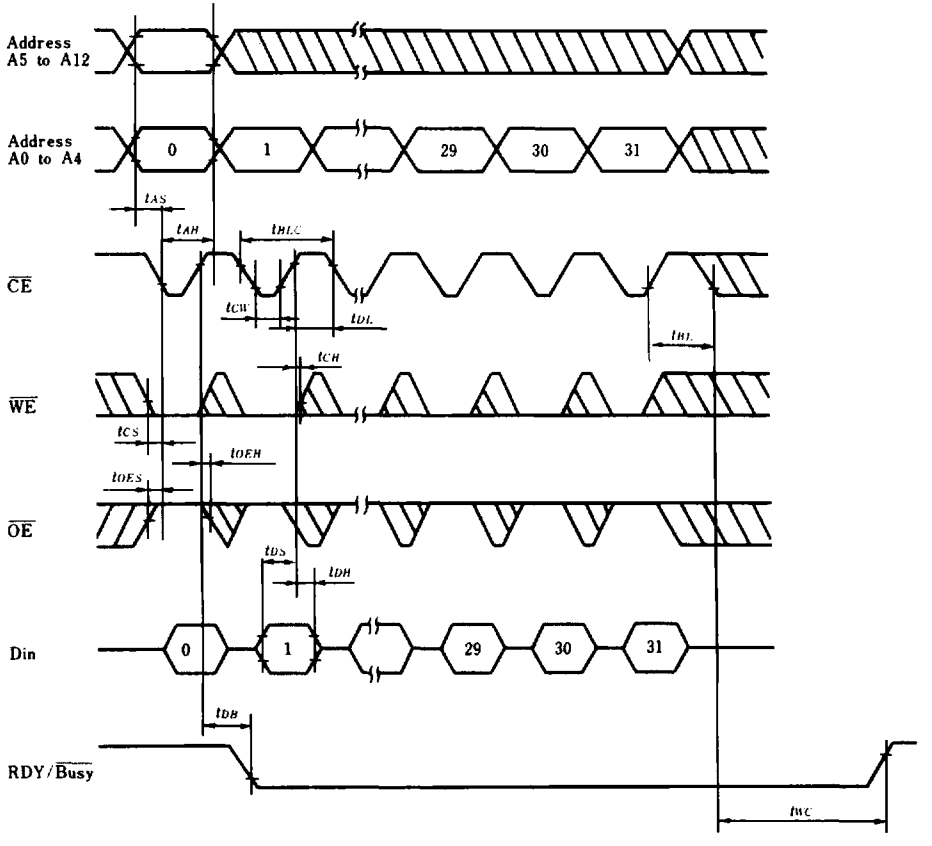
• Page Erase and Page Write Operation ($\overline{WE}$ Controlled Write Cycle)

Parameter	Symbol	min.	typ.	max.	Unit
Address Setup Time	t_{AS}	0	–	–	ns
$\overline{CE}$ to Write Setup Time	t_{CS}	0	–	–	ns
Write Pusle Width	t_{WP}	200	–	–	ns
Address Hold Time	t_{AH}	150	–	–	ns
Data Setup Time	t_{DS}	100	–	–	ns
Data Hold Time	t_{DH}	20	–	–	ns
$\overline{CE}$ Hold Time	t_{CH}	0	–	–	ns
$\overline{OE}$ to Write Setup Time	t_{OES}	0	–	–	ns
$\overline{OE}$ Hold Time	t_{OEH}	0	–	–	ns
Data Latch Time	t_{DL}	100	–	–	ns
Time to Device Busy	t_{DB}	120	–	–	ns
Write Cycle Time	t_{WC}	–	–	15	ms
Byte Load Window	t_{BL}	30	–	100	µs
Byte Load Cycle	t_{BLC}	0.3	–	30	µs



• Page Erase and Page Write Operation ($\overline{CE}$ Controlled Write Cycle)

Parameter	Symbol	min.	typ.	max.	Unit
Address Setup Time	t_{AS}	0	–	–	ns
$\overline{CE}$ to Write Setup Time	t_{CS}	0	–	–	ns
$\overline{CE}$ Pulse Width	t_{CW}	200	–	–	ns
Address Hold Time	t_{AH}	150	–	–	ns
Data Setup Time	t_{DS}	100	–	–	ns
Data Hold Time	t_{DH}	20	–	–	ns
$\overline{CE}$ Hold Time	t_{CH}	0	–	–	ns
$\overline{OE}$ to Write Setup Time	t_{OES}	0	–	–	ns
$\overline{OE}$ Hold Time	t_{OEH}	0	–	–	ns
Data Latch Time	t_{DL}	100	–	–	ns
Time to Device Busy	t_{DB}	120	–	–	ns
Write Cycle Time	t_{WC}	–	–	15	ms
Byte Load Window	t_{BL}	30	–	100	µs
Byte Load Cycle	t_{BLC}	0.3	–	30	µs



- **Automatic Page Write**

Page-mode write feature allows 1 to 32 bytes of data to be written into the EEPROM in a single write cycle. Following the initial byte cycle, an additional 1 to 31 bytes can be written in the same manner as the first byte was written. Each additional byte load cycle must be started within 30μs of the preceding rising edge of the $\overline{WE}$.

- **$\overline{Data}$ Polling**

$\overline{Data}$ polling allows comparison operation to determine the status of the EEPROM. During a write cycle, an attempted read of the last byte written in the EEPROM results in the complement data of that byte at I/O7.

- **Ready/$\overline{Busy}$ Signal**

RDY/$\overline{Busy}$ signal also allows to determine the status of the EEPROM, RDY/$\overline{Busy}$ signal has high impedance except in a write cycle and is lowered to V_{OL} after the first write signal. At the end of a write cycle, RDY/$\overline{Busy}$ signal changes its state to high impedance.

- **$\overline{WE}$, $\overline{CE}$ Pins Operation**

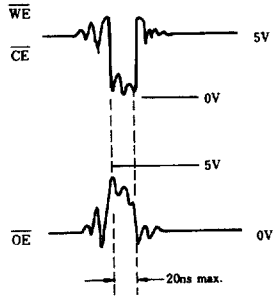
During a write cycle, addresses are latched on the falling edge of $\overline{WE}$ or $\overline{CE}$: data are latched on the rising edge of $\overline{WE}$ or $\overline{CE}$.

- **Data Protection**

To protect the data during operation and turning on/off, HN58C65 internally provides the following function.

1. Data Protection against the Noise on Control Pins ($\overline{CE}$, $\overline{OE}$, $\overline{WE}$) during Operation

During reading out or standby, the noise on control pins may become trigger and turn EEPROM to program mode by error.
To prevent this phenomenon, HN58C65 has the noise cancell function of cutting the noise if its width is 20ns or less in program mode.
Care should be taken not to exist the noise whose width is more than 20ns on control pins.



2. Data Protection on Turning On/Off the V_{CC}

2-1 Prevention of unintentional programming on turning on/off the V_{CC}

On turning on/off V_{CC}, the noise on control pins generated by outer circuits (CPU, etc) may become trigger and turn the EEPROM to program mode by error. To prevent this unintentional programming, the EEPROM should be kept in unprogrammable state while CPU is in unstable state.

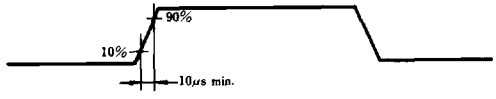
In addition, on turning on/off V_{CC}, the input level on control pins should be held as shown in the table below.

$\overline{CE}$	V_{CC}	X	X
$\overline{OE}$	X	V_{SS}	X
$\overline{WE}$	X	X	V_{CC}

X: Don't care.

2-2 Specifications of tr min. for V_{CC}

On turning on V_{CC}, if tr for VCC is shorter than 1μs, the EEPROM turns into program mode regardless of the input level on control pins and results in data destruction.



Since the actual minimum value of tr for proper operation is about 1μs, to take into account the timing margin, please keep tr longer than 10μs.