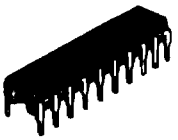
HM514256S Series
HM514256A Series

262144-Word × 4-Bit CMOS Dynamic RAM

The Hitachi HM514256S/A is a CMOS dynamic RAM organized 262144-word x 4-bit. HM514256S/A has realized higher density, higher performance and various functions by employing 1.3 µm CMOS technology and some new CMOS circuit design technologies. The HM514256S/A offers Fast Page Mode as a high speed access mode.

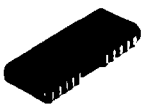
Multiplexed address input permits the HM514256S/A to be packaged in standard 20-pin plastic DIP, 20-pin plastic SOJ and 20-pin plastic ZIP.

HM514256SP Series
HM514256AP Series



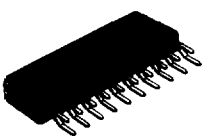
(DP-20NA)

HM514256SJP Series
HM514256AJP Series



(CP-20D)

HM514256SZP Series
HM514256AZP Series



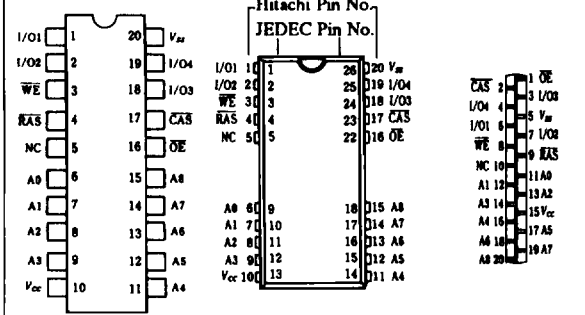
(ZP-20)

Features

- Single 5 V (±10%)
- High speed: Access Time 80 ns/100 ns/120 ns (max)
- Low power: Standby 11 mW (max)
  Active 363 mW/302.5 mW/258.5 mW (max)
- Fast page mode capability
- 512 refresh cycles: (8 ms)
- 2 variations of refresh: $\overline{RAS}$-only refresh
  $\overline{CAS}$-before-$\overline{RAS}$ refresh

Pin Arrangement

• HM514256SP Series • HM514256AP Series	• HM514256SJP Series • HM514256AJP Series	• HM514256SZP Series • HM514256AZP Series



(Top View) (Top View) (Bottom View)

Pin Description

Pin Name	Function
A0–A8	Address input
A0–A8	Refresh address input
I/O1–I/O4	Data input/Data output
$\overline{RAS}$	Row address strobe
$\overline{CAS}$	Column address strobe
$\overline{WE}$	Write enable
$\overline{OE}$	Output enable
Vcc	Power supply (+5 V)
Vss	Ground

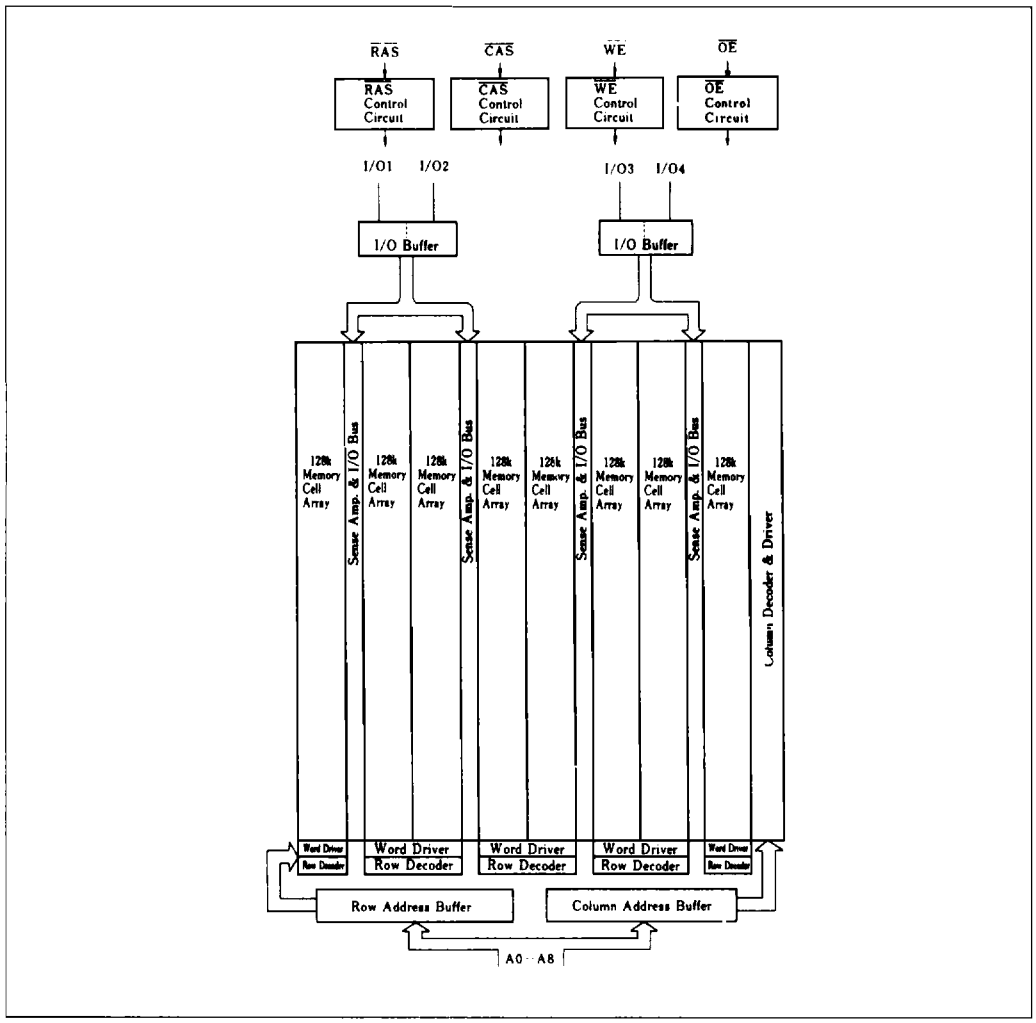
Ordering Information

Type No.	Access Time	Package
HM514256P-8S	80 ns	300-mil 20-pin
HM514256P-10S	100 ns	plastic DIP
HM514256P-12S	120 ns	(DP-20NA)
HM514256JP-8S	80 ns	300-mil 20-pin
HM514256JP-10S	100 ns	plastic SOJ
HM514256JP-12S	120 ns	(CP-20D)
HM514256ZP-8S	80 ns	400-mil 20-pin
HM514256ZP-10S	100 ns	plastic ZIP
HM514256ZP-12S	120 ns	(ZP-20)

Type No.	Access Time	Package
HM514256AP-8	80 ns	300-mil 20-pin
HM514256AP-10	100 ns	plastic DIP
HM514256AP-12	120 ns	(DP-20NA)
HM514256AJP-8	80 ns	300-mil 20-pin
HM514256AJP-10	100 ns	plastic SOJ
HM514256AJP-12	120 ns	(CP-20D)
HM514256AZP-8	80 ns	400-mil 20-pin
HM514256AZP-10	100 ns	plastic ZIP
HM514256AZP-12	120 ns	(ZP-20)

Block Diagram

HM514256S Series



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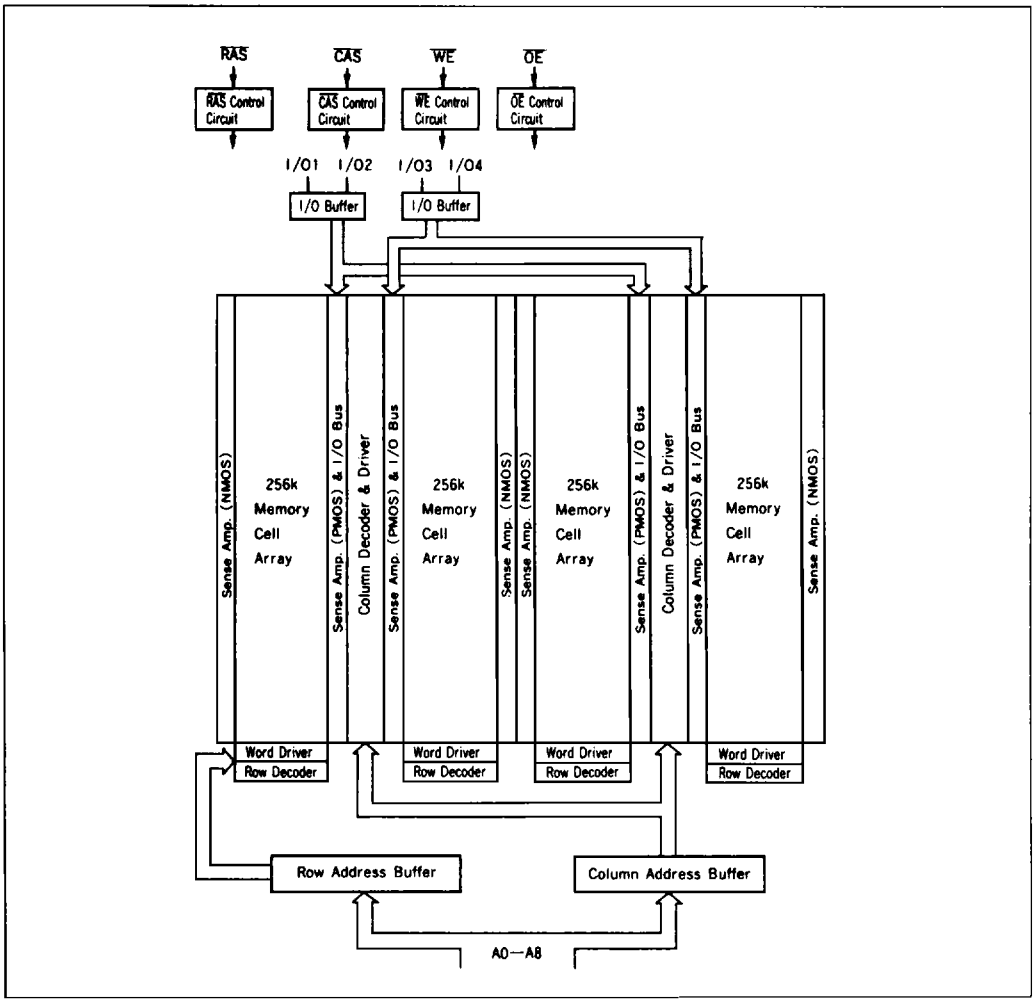
HM514256A Series



Absolute Maximum Ratings

Item	Symbol	Value	Unit
Voltage on any pin relative to Vss	V_T	−1.0 to +7.0	V
Supply voltage relative to Vss	Vcc	−1.0 to +7.0	V
Short circuit output current	Iout	50	mA
Power dissipation	P_T	1.0	W
Operating temperature	Topr	0 to +70	°C
Storage temperature	Tstg	−55 to +125	°C

Recommended DC Operating Conditions (Ta = 0 to +70°C)

Item		Symbol	Min	Typ	Max	Unit	Note
Supply voltage		V_{SS}	0	0	0	V	
		V_{CC}	4.5	5.0	5.5	V	*1
Input high voltage		V_{IH}	2.4	—	6.5	V	*1
Input low voltage	I/O pin	V_{IL}	−1.0	—	0.8	V	*1
	Others	V_{IL}	−2.0	—	0.8	V	*1

Note: *1. All voltage referenced to V_{SS}.

DC Characteristics (Ta = 0 to +70°C, V_{CC} = 5V ± 10%, V_{SS} = 0 V)

Item	Symbol	HM514256-8S HM514256A-8		HM514256-10S HM514256A-10		HM514256-12S HM514256A-12		Unit	Test Conditions	Note
		Min	Max	Min	Max	Min	Max			
Operating current	I_{CC1}	—	66	—	55	—	47	mA	$\overline{RAS}$, $\overline{CAS}$ cycling t_{RC} = Min	*1, *2
Standby current	I_{CC2}	—	2	—	2	—	2	mA	$\overline{RAS}$, $\overline{CAS}$ = V_{IH} Dout = High-Z TTL interface	
		—	1	—	1	—	1		$\overline{RAS}$, $\overline{CAS}$ ≥ Vcc − 0.2 V Dout = High-Z CMOS interface	
$\overline{RAS}$-only refresh current	I_{CC3}	—	66	—	55	—	47	mA	t_{RC} = Min	*2
Standby current	I_{CC5}	—	5	—	5	—	5	mA	$\overline{RAS}$ = V_{IH} $\overline{CAS}$ = V_{IL} Dout = enable	*1
$\overline{CAS}$-before-$\overline{RAS}$ refresh current	I_{CC6}	—	66	—	55	—	47	mA	t_{RC} = Min	
Fast page mode current	I_{CC7}	—	55	—	55	—	47	mA	t_{PC} = Min	*1, *3
Input leakage current	I_{LI}	−10	10	−10	10	−10	10	µA	0 V ≤ Vin ≤ 7 V	
Output leakage current	I_{LO}	−10	10	−10	10	−10	10	µA	0 V ≤ Vout ≤ 7 V Dout = disable	
Output high voltage	V_{OH}	2.4	Vcc	2.4	Vcc	2.4	Vcc	V	High Iout = −5 mA	
Output low voltage	V_{OL}	0	0.4	0	0.4	0	0.4	V	Low Iout = 4.2 mA	

Notes: *1. I_{CC} depends on output loading condition when the device is selected.
I_{CC} max is specified at the output open condition.
*2. Address can be changed less than three times while $\overline{RAS}$ = V_{IL}.
*3. Address can be changed once or less while $\overline{CAS}$ = V_{IH}.

Capacitance (Ta = 25°C, V_{CC} = 5 V ± 10%)

Item		Symbol	Typ	Max	Unit	Note
Input capacitance	Address	C_{I1}	—	5	pF	*1
	Clock	C_{I2}	—	7	pF	*1
Input/Output capacitance	Data input/Data output	$C_{I/O}$	—	10	pF	*1, *2

Notes: *1. Capacitance measured with Boonton Meter or effective capacitance measuring method.
*2. $\overline{CAS}$ = V_{IH} to disable Dout.

AC Characteristics (Ta = 0 to +70°C, V_{CC} = 5 V ± 10%, V_{SS} = 0 V)*14

Test Conditions

Input rise and fall times: 5 ns
Input timing reference levels: 0.8 V, 2.4 V
Output load: 2TTL Gate + C_L (100 pF) (Including scope and jig)

Read, Write, Read-Modify-Write and Refresh Cycles (Common Parameters)

Item	Symbol	HM514256-8S HM514256A-8		HM514256-10S HM514256A-10		HM514256-12S HM514256A-12		Unit	Note
		Min	Max	Min	Max	Min	Max		
Random read or write cycle time	t_{RC}	160	—	190	—	220	—	ns	
$\overline{RAS}$ precharge time	t_{RP}	70	—	80	—	90	—	ns	
$\overline{RAS}$ pulse width	t_{RAS}	80	10000	100	10000	120	10000	ns	
$\overline{CAS}$ pulse width	t_{CAS}	25	10000	25	10000	30	10000	ns	
Row address setup time	t_{ASR}	0	—	0	—	0	—	ns	
Row address hold time	t_{RAH}	12	—	15	—	15	—	ns	
Column address setup time	t_{ASC}	0	—	0	—	0	—	ns	
Column address hold time	t_{CAH}	20	—	20	—	25	—	ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	22	55	25	75	25	90	ns	*8
$\overline{RAS}$ to column address delay time	t_{RAD}	17	40	20	55	20	65	ns	*9
$\overline{RAS}$ hold time	t_{RSH}	25	—	25	—	30	—	ns	
$\overline{CAS}$ hold time	t_{CSH}	80	—	100	—	120	—	ns	
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	10	—	10	—	10	—	ns	
$\overline{OE}$ to Din delay time	t_{ODD}	20	—	25	—	30	—	ns	
$\overline{OE}$ delay time from Din	t_{DZO}	0	—	0	—	0	—	ns	
$\overline{CAS}$ delay time from Din	t_{DZC}	0	—	0	—	0	—	ns	
Transition time (rise and fall)	t_T	3	50	3	50	3	50	ns	*1, *7
Refresh period	t_{REF}	—	8	—	8	—	8	ms	

Read Cycle

Item	Symbol	HM514256-8S HM514256A-8		HM514256-10S HM514256A-10		HM514256-12S HM514256A-12		Unit	Note
		Min	Max	Min	Max	Min	Max		
Access time from $\overline{RAS}$	t_{RAC}	—	80	—	100	—	120	ns	*2, *3
Access time from $\overline{CAS}$	t_{CAC}	—	25	—	25	—	30	ns	*3, *4
Access time from Address	t_{AA}	—	40	—	45	—	55	ns	*3, *5
Access time from $\overline{OE}$	t_{OAC}	—	25	—	25	—	30	ns	
Read command setup time	t_{RCS}	0	—	0	—	0	—	ns	
Read command hold time to $\overline{CAS}$	t_{RCH}	0	—	0	—	0	—	ns	
Read command hold time to $\overline{RAS}$	t_{RRH}	10	—	10	—	10	—	ns	
Column address to RAS lead time	t_{RAL}	40	—	45	—	55	—	ns	
Output buffer turn-off time	t_{OFF1}	—	20	—	25	—	30	ns	*6
Output buffer turn-off to $\overline{OE}$	t_{OFF2}	—	20	—	25	—	30	ns	*6
$\overline{CAS}$ to Din delay time	t_{CDD}	20	—	25	—	30	—	ns	

Write Cycle

Item	Symbol	HM514256-8S HM514256A-8		HM514256-10S HM514256A-10		HM514256-12S HM514256A-12		Unit	Note
		Min	Max	Min	Max	Min	Max		
Write command setup time	t_{WCS}	0	—	0	—	0	—	ns	*10
Write command hold time	t_{WCH}	20	—	20	—	25	—	ns	
Write command pulse width	t_{WP}	15	—	15	—	20	—	ns	
Write command to $\overline{RAS}$ lead time	t_{RWL}	25	—	25	—	30	—	ns	
Write command to $\overline{CAS}$ lead time	t_{CWL}	25	—	25	—	30	—	ns	
Data-in setup time	t_{DS}	0	—	0	—	0	—	ns	*11
Data-in hold time	t_{DH}	20	—	20	—	25	—	ns	*11

Read-Modify-Write Cycle

Item	Symbol	HM514256-8S HM514256A-8		HM514256-10S HM514256A-10		HM514256-12S HM514256A-12		Unit	Note
		Min	Max	Min	Max	Min	Max		
Read-write cycle time	t_{RWC}	220	—	255	—	295	—	ns	
$\overline{RAS}$ to $\overline{WE}$ delay time	t_{RWD}	110	—	135	—	160	—	ns	*10
$\overline{CAS}$ to $\overline{WE}$ delay time	t_{CWD}	55	—	60	—	70	—	ns	*10
Column address to $\overline{WE}$ delay time	t_{AWD}	70	—	80	—	95	—	ns	*10
$\overline{OE}$ hold time from $\overline{WE}$	t_{OEH}	25	—	25	—	30	—	ns	

Refresh Cycle

Item	Symbol	HM514256-8S HM514256A-8		HM514256-10S HM514256A-10		HM514256-12S HM514256A-12		Unit	Note
		Min	Max	Min	Max	Min	Max		
$\overline{CAS}$ setup time ($\overline{CAS}$-before-$\overline{RAS}$ refresh cycle)	t_{CSR}	10	—	10	—	10	—	ns	
$\overline{CAS}$ hold time ($\overline{CAS}$-before-$\overline{RAS}$ refresh cycle)	t_{CHR}	20	—	20	—	25	—	ns	
$\overline{RAS}$ precharge to $\overline{CAS}$ hold time	t_{RPC}	10	—	10	—	10	—	ns	

Fast Page Mode Cycle

Item	Symbol	HM514256-8S HM514256A-8		HM514256-10S HM514256A-10		HM514256-12S HM514256A-12		Unit	Note
		Min	Max	Min	Max	Min	Max		
Fast page mode cycle time	t_{PC}	55	—	55	—	65	—	ns	
Fast page mode $\overline{CAS}$ precharge time	t_{CP}	10	—	10	—	15	—	ns	
Fast page mode $\overline{RAS}$ pulse width	t_{RASC}	—	100000	—	100000	—	100000	ns	*12
Access time from $\overline{CAS}$ precharge	t_{ACP}	—	50	—	50	—	60	ns	*13
$\overline{RAS}$ hold time from $\overline{CAS}$ precharge	t_{RHCP}	50	—	50	—	60	—	ns	
Fast page mode read-write cycle time	t_{PCM}	110	—	115	—	135	—	ns	

Notes: *1. AC measurements assume t_T = 5ns.

*2. Assumes that $t_{RCD} \leq t_{RCD}$ (max) and $t_{RAD} \leq t_{RAD}$ (max). If t_{RCD} or t_{RAD} is greater than the maximum recommended value shown in this table, t_{RAC} exceeds the value shown.

*3. Measured with a load circuit equivalent to 2TTL loads and 100pF.

*4. Assumes that $t_{RCD} \geq t_{RCD}$ (max) and $t_{RAD} \leq t_{RAD}$ (max).

*5. Assumes that $t_{RCD} \leq t_{RCD}$ (max) and $t_{RAD} \geq t_{RAD}$ (max).

*6. t_{OFF} (max) is defined as the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.

*7. Transition times are measured between V_{IH} and V_{IL}.

*8. Operation with the t_{RCD} (max) limit insures that t_{RAC} (max) can be met, t_{RCD} (max) is specified as a reference point only, if t_{RCD} is greater than the specified t_{RCD} (max) limit, then access time is controlled exclusively by t_{CAC}.

*9. Operation with the t_{RAD} (max) limit insures that t_{RAC} (max) can be met, t_{RAD} (max) is specified as a reference point only, if t_{RAD} is greater than the specified t_{RAD} (max) limit, then access time is controlled exclusively by t_{AA}.

*10. t_{WCS}, t_{RWD}, t_{CWD} and t_{AWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only: if $t_{WCS} \geq t_{WCS}$ (min), the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) throughout the entire cycle; if $t_{RWD} \geq t_{RWD}$ (min), $t_{CWD} \geq t_{CWD}$ (min) and $t_{AWD} \geq t_{AWD}$ (min), the cycle is a read-write and the data output will contain data read from the selected cell; if neither of the above sets of conditions is satisfied, the condition of the data out (at access time) is indeterminate.

*11. These parameters are referenced to $\overline{CAS}$ leading edge in early write cycles and to $\overline{WE}$ leading edge in delayed write or read-modify-write cycles.

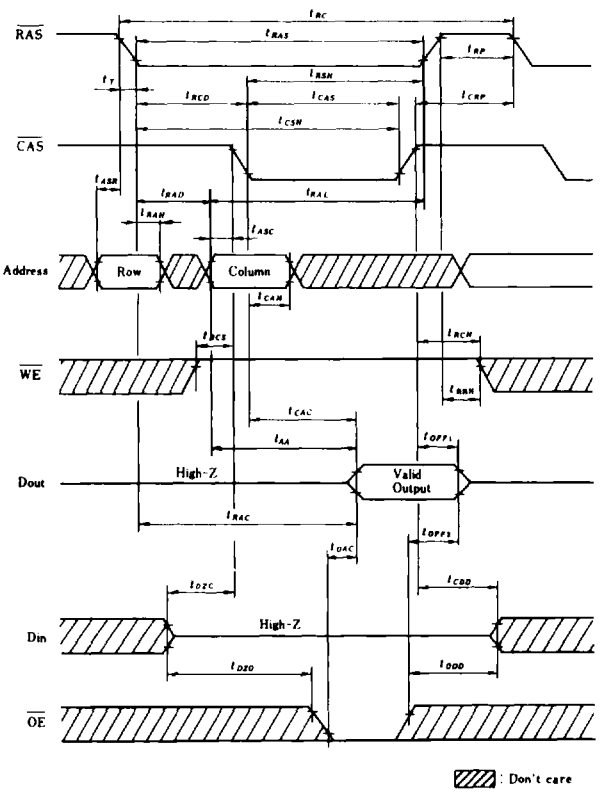
*12. t_{RASC} is determined by $\overline{RAS}$ pulse width in fast page mode cycles.

*13. Access time is determined by the longer of t_{AA}, t_{CAC} or t_{ACP}.

*14. An initial pause of 100 µs is required after power-up followed by eight or more initialization cycles (any combination of cycles containing $\overline{RAS}$ clock such as $\overline{RAS}$-only refresh). If the internal refresh counter is used, eight or more $\overline{CAS}$-before-$\overline{RAS}$ refresh cycles are required.

Timing Waveforms

Read Cycle



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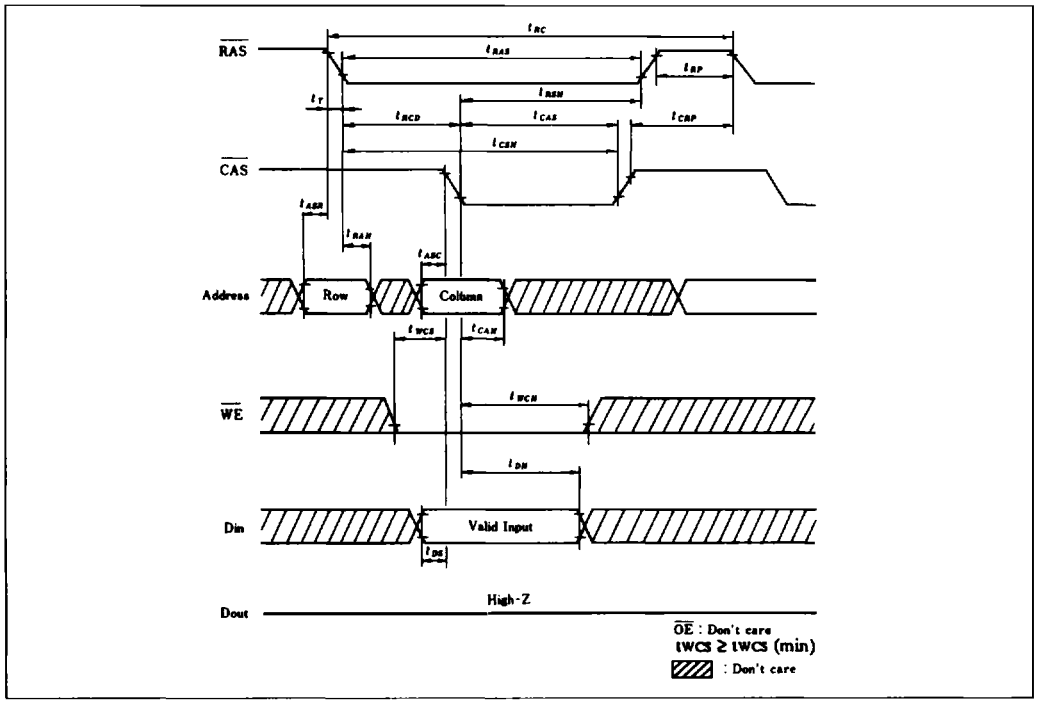
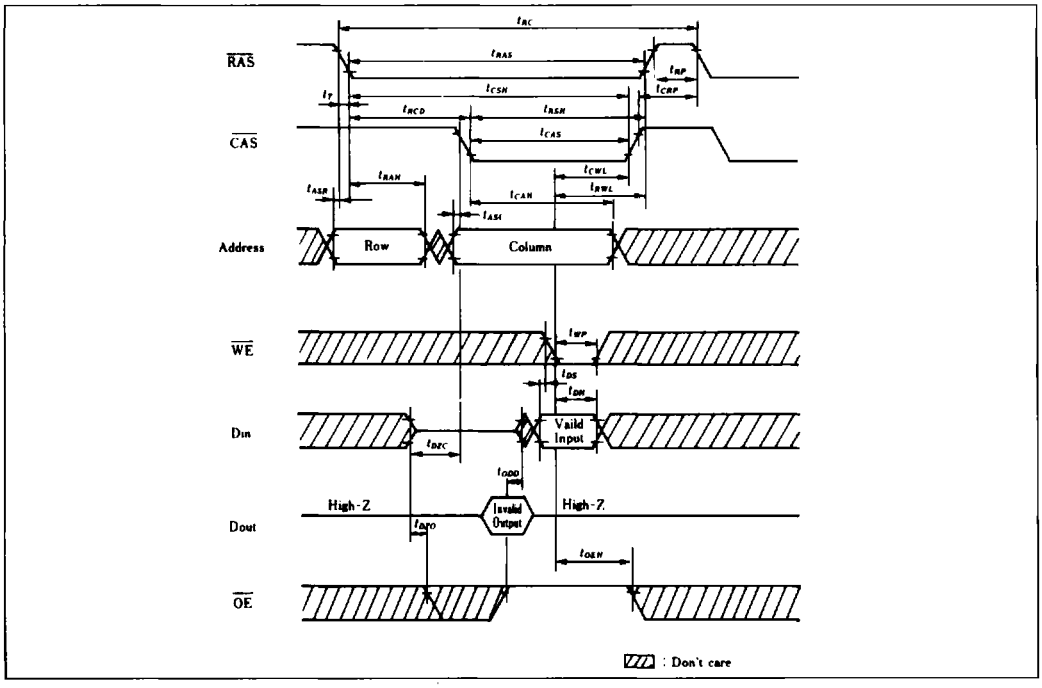
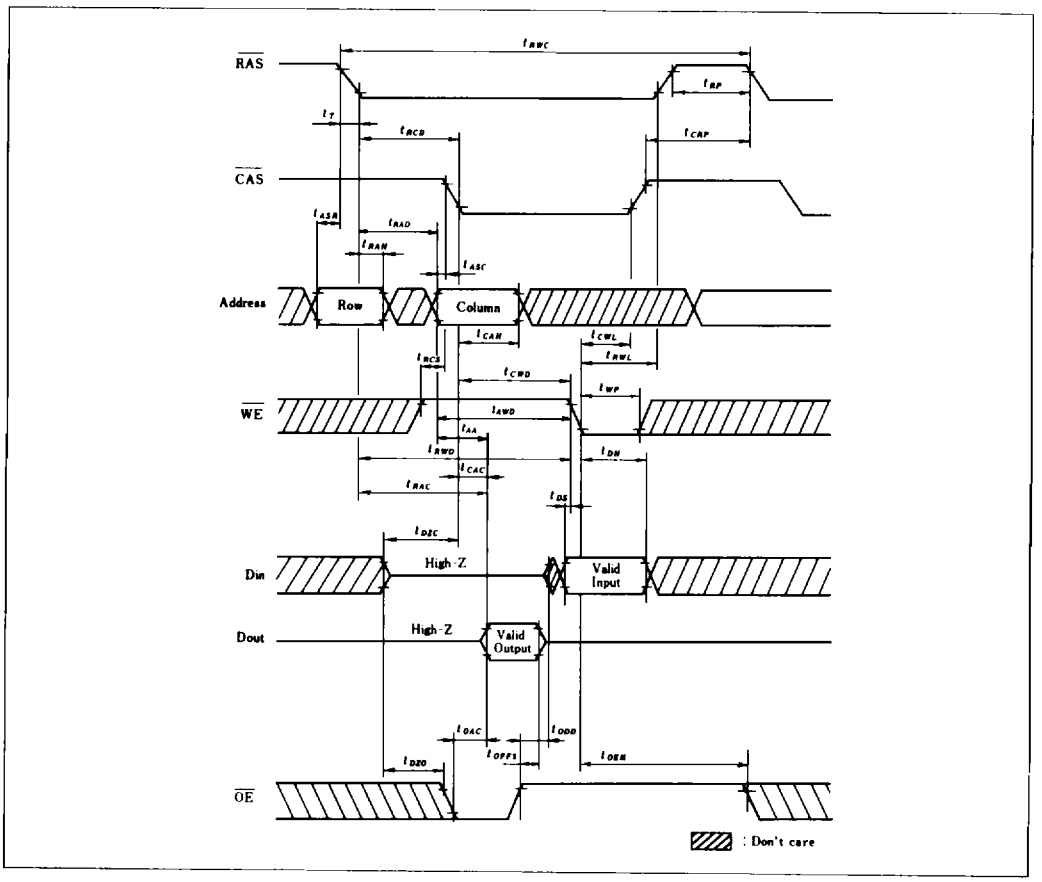
Early Write Cycle



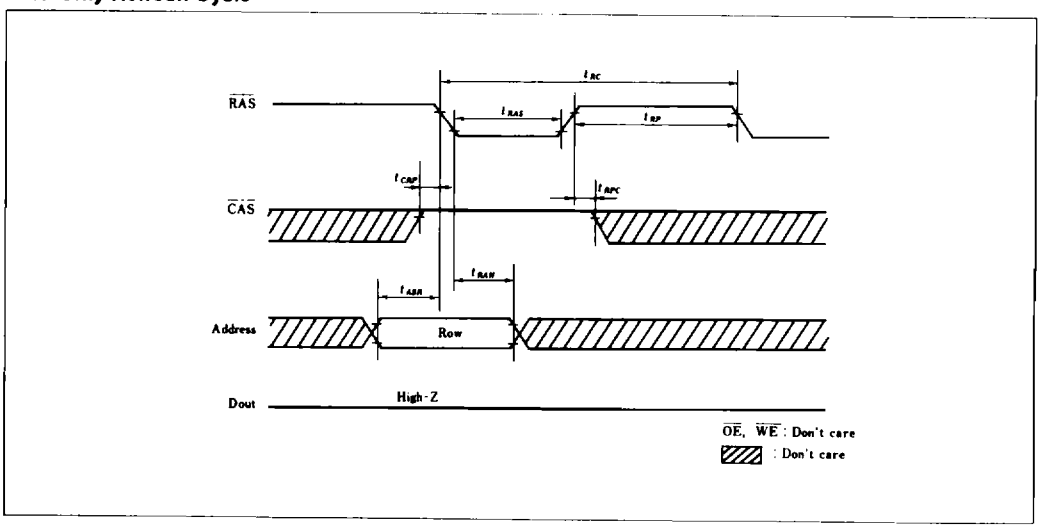
Delayed Write Cycle



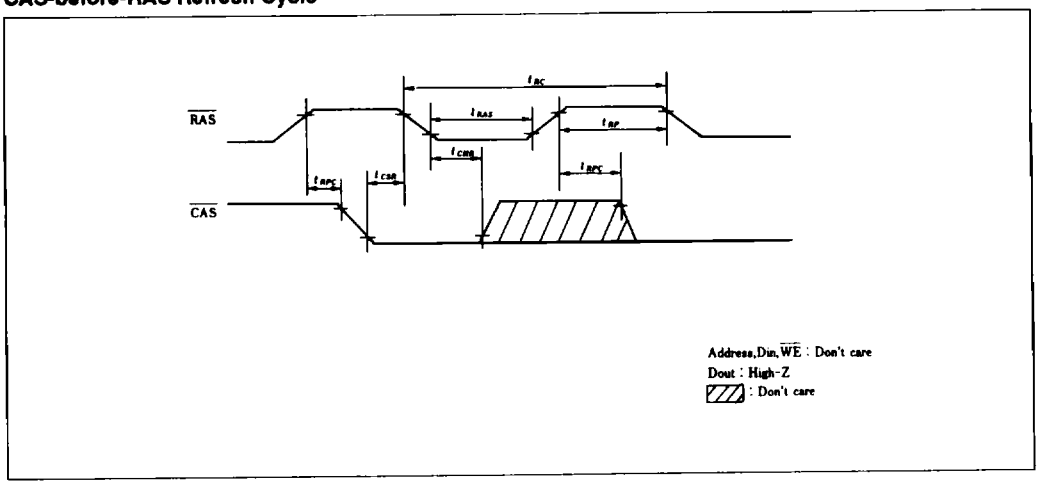
Read-Modify-Write Cycle



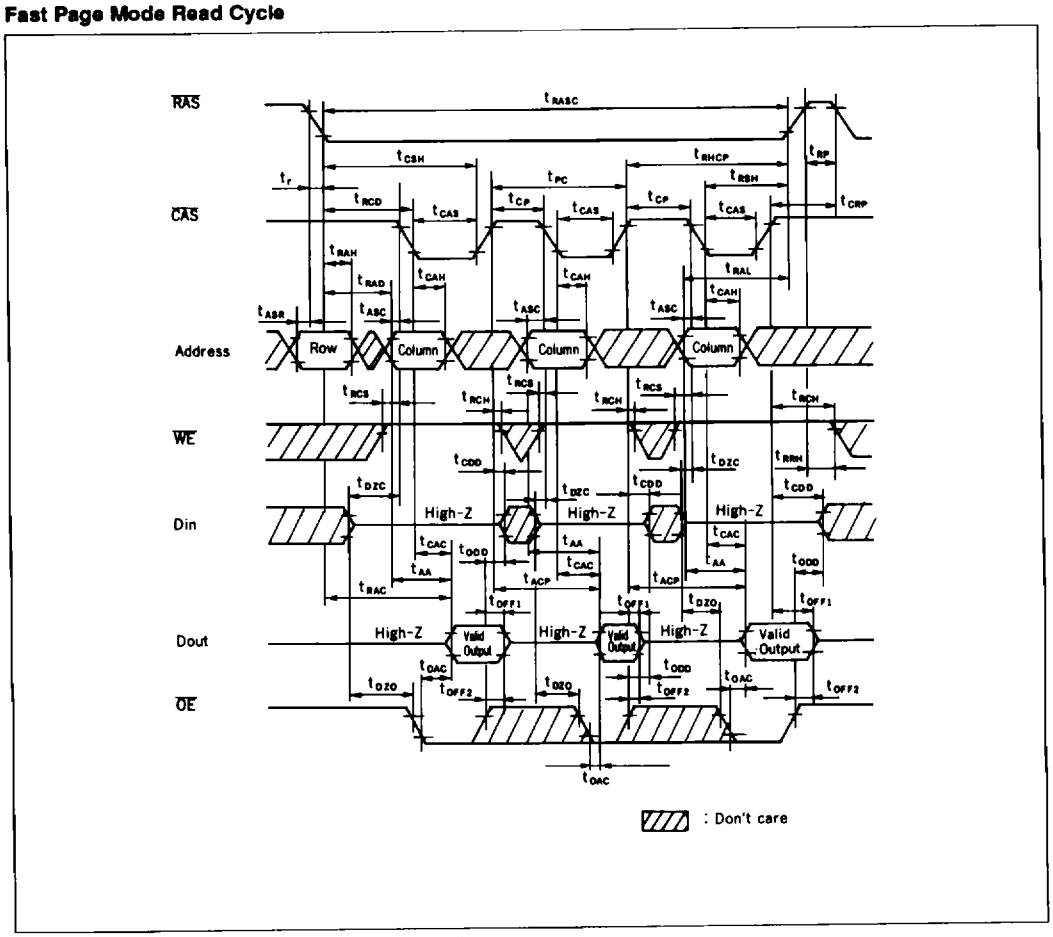
RAS-Only Refresh Cycle



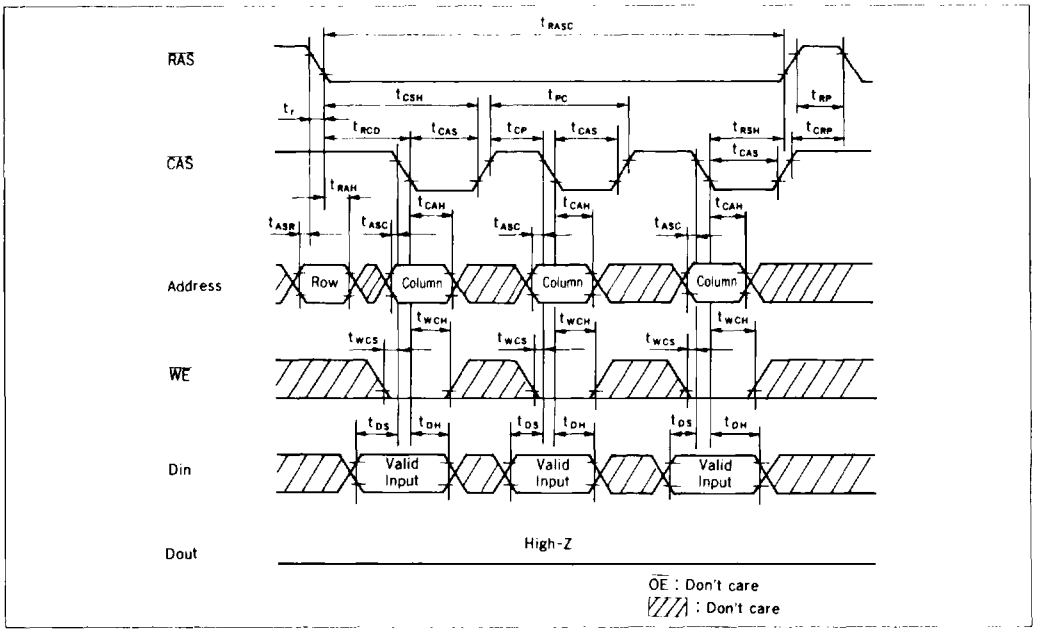
$\overline{CAS}$-before-$\overline{RAS}$ Refresh Cycle



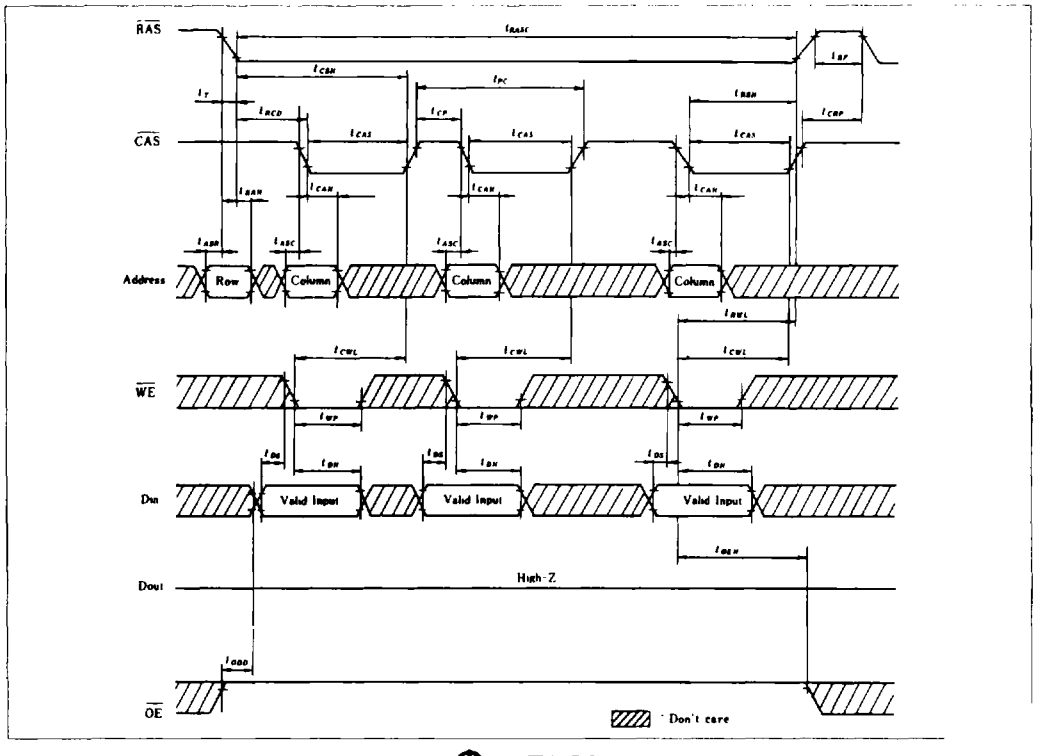
Fast Page Mode Read Cycle



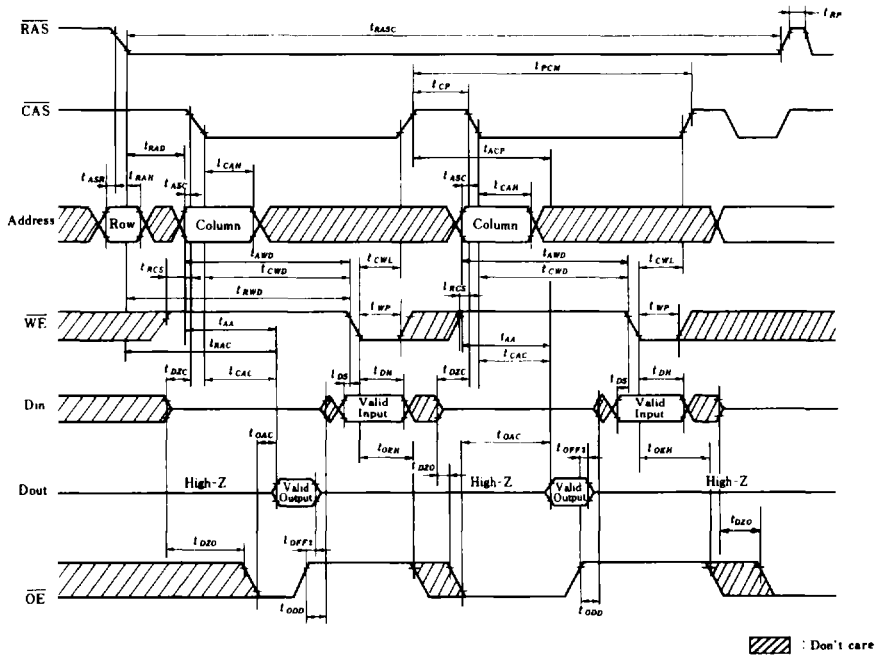
Fast Page Mode Early Write Cycle



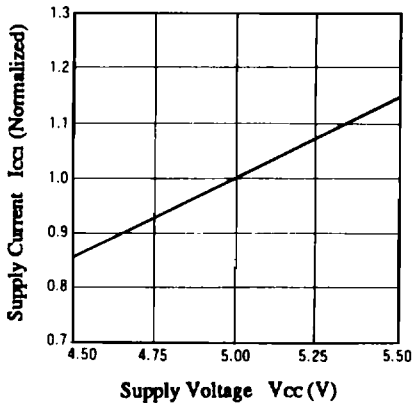
Fast Page Delayed Write Cycle



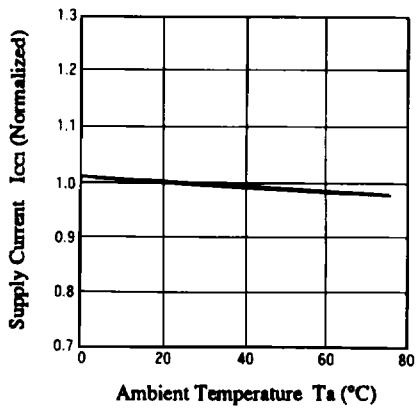
Fast Page Mode Read-Modify-Write Cycle



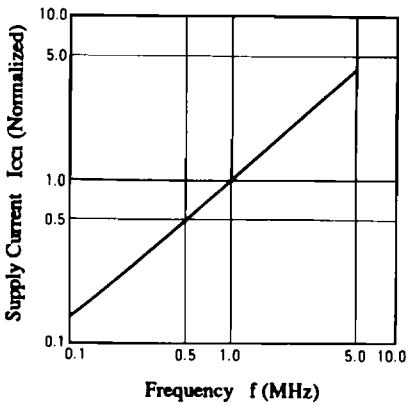
Supply Current (Active) vs. Supply Voltage



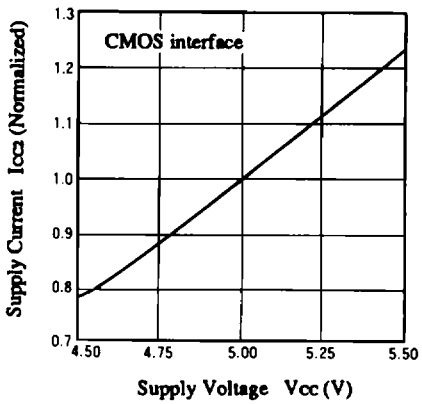
Supply Current (Active) vs. Ambient Temperature



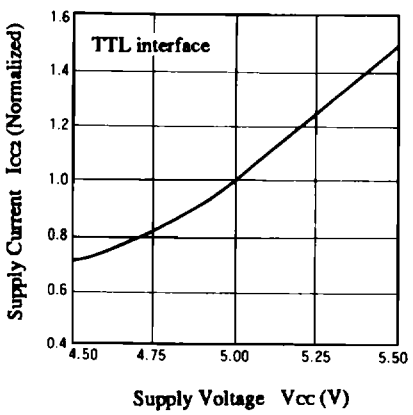
Supply Current (Active) vs. Frequency



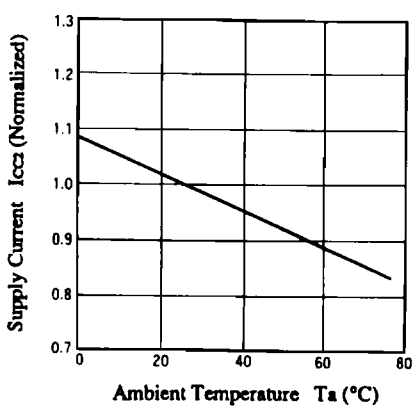
Supply Current (Standby) vs. Supply Voltage



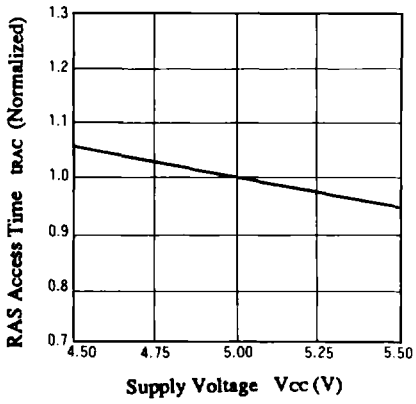
Supply Current (Standby) vs. Supply Voltage



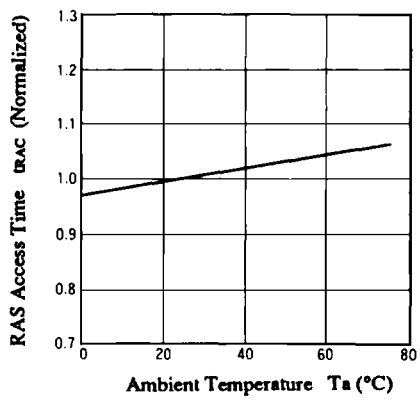
Supply Current (Standby) vs. Ambient Temperature



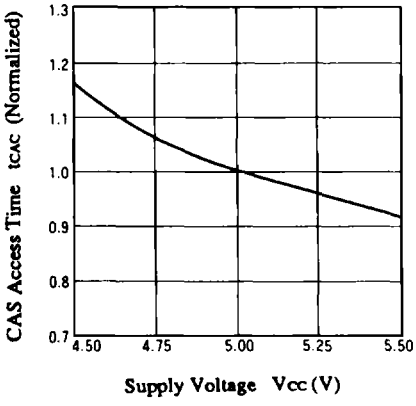
$\overline{RAS}$ Access Time vs. Supply Voltage



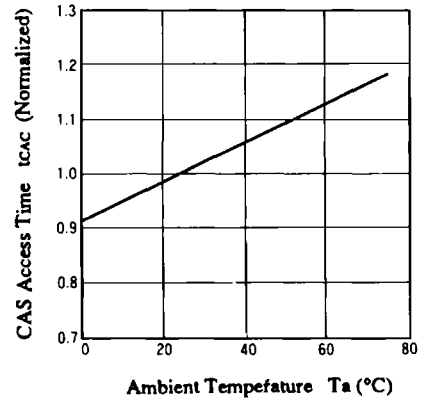
$\overline{RAS}$ Access Time vs. Ambient Temperature



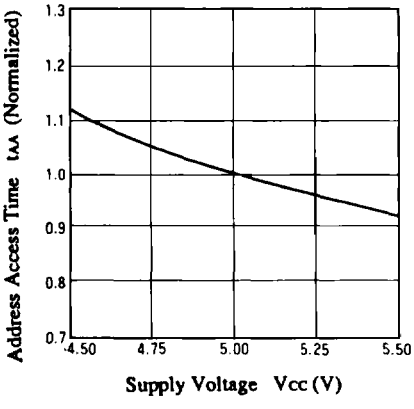
$\overline{CAS}$ Access Time vs. Supply Voltage



$\overline{CAS}$ Access Time vs. Ambient Temperature



Address Access Time vs. Supply Voltage



Address Access Time vs. Ambient Temperature