CRYSTAL
Semiconductor Corporation

CS4231A

# Parallel Interface, Multimedia Audio Codec

Features

- Windows Sound System™ Compatible Codec

- ADPCM Compression/Decompression

- Extensive Software Support

- MPC Level 2 Compatible Mixer

- Dual DMA Registers support Full Duplex Operation

- On-Chip FIFOs for higher performance

- Selectable Serial Audio Data Port

- Pin Compatible with CS4231/CS4248

General Description

The CS4231A includes stereo 16-bit audio converters and complete on-chip filtering for record and playback of 16-bit audio data. In addition, analog mixing and programmable gain and attenuation are included to provide a complete audio subsystem. A selectable serial port can pass audio data to and from DSPs or ASICs. Crystal-developed high-performance software drivers for various operating systems are available that support all the CS4231A features including full duplex transfers. The CS4231A is a pin compatible upgrade to the CS4231 and CS4248.

ORDERING INFORMATION:

CS4231A-KL	0 to 70°C	68-pin PLCC
CS4231A-KQ	0 to 70°C	100-pin TQFP
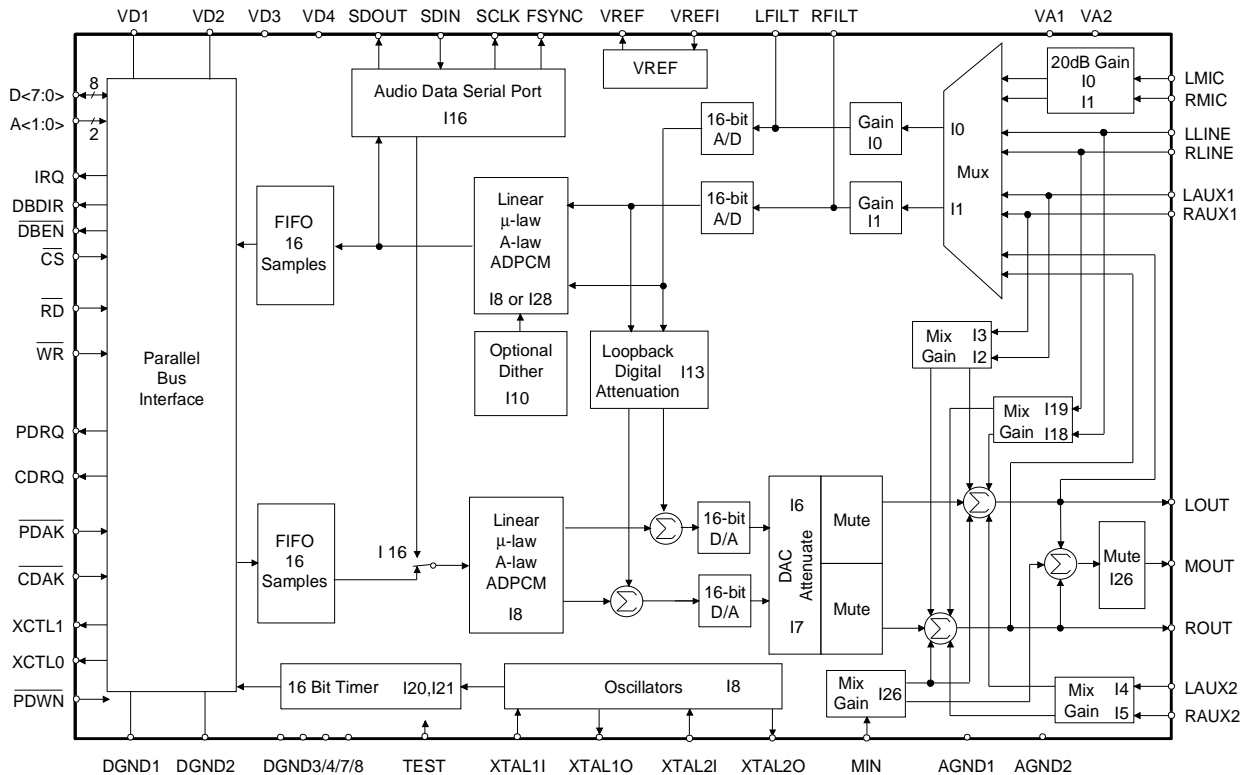
Preliminary Product Information | This document contains information for a new product. Crystal Semiconductor reserves the right to modify this product without notice.

TABLE OF CONTENTS:

ANALOG CHARACTERISTICS (T_A = 25 °C; VA1, VA2, VD1-VD4 = +5V;

Input Levels: Logic 0 = 0V, Logic 1 = VD1-VD4; 1 kHz Input Sine wave; Conversion Rate = 48 kHz;
Measurement Bandwidth is 10 Hz to 20 kHz, 16-bit linear coding.)

Parameter*	Symbol	Min	Typ	Max	Units
Analog Input Characteristics - Minimum Gain Setting (0dB); unless otherwise specified.					
ADC Resolution (Note 1)			16		Bits
ADC Differential Nonlinearity (Note 1)				±0.5	LSB
Instantaneous Dynamic Range Line Inputs	IDR	80	85		dB
(Note 2) Mic Inputs		72	77		dB
Total Harmonic Distortion Line Inputs	THD		0.006	0.02	%
Mic Inputs			0.01	0.025	%
Signal-to-Intermodulation Distortion			90		dB
Interchannel Isolation Line to Line Inputs			80		dB
Line to Mic Inputs			80		dB
Line-to-AUX1			90		dB
Line-to-AUX2			90		dB
Interchannel Gain Mismatch Line Inputs				0.5	dB
Mic Inputs				0.5	dB
Programmable Input Gain Span Line Inputs		21.5	22.5		dB
Gain Step Size		1.3	1.5	1.7	dB
ADC Offset Error 0 dB gain			10	100	LSB
Full Scale Input Voltage: (MGE=1) MIC Inputs		0.266	0.29	0.31	V_{pp}
(MGE=0) MIC Inputs		2.66	2.9	3.1	V_{pp}
LINE, AUX1, AUX2, MIN Inputs		2.66	2.9	3.1	V_{pp}
Gain Drift			100		ppm/°C
Input Resistance (Note 1)		20			kΩ
Input Capacitance (Note 1)				15	pF

Notes: 1. This specification is guaranteed by characterization, no production testing.
         2. MGE = 1 and a 10 μF capacitor on the VREF pin.

*Parameter definitions are given at the end of this data sheet.

Windows and Windows Sound System are registered trademarks of Microsoft Corporation.

Specifications are subject to change without notice.

ANALOG CHARACTERISTICS (Continued)

Parameter*			Symbol	Min	Typ	Max	Units
Analog Output Characteristics - Minimum Attenuation (0dB); unless otherwise specified.							
DAC Resolution					16		Bits
DAC Differential Nonlinearity		(Note 1)				±0.5	LSB
Dynamic Range	-Total	All Outputs	TDR		95		dB
	-Instantaneous		IDR	80	85		dB
Total Harmonic Distortion		(Note 3)	THD		0.01	0.02	%
Signal-to-Intermodulation Distortion					85		dB
Interchannel Isolation	Line Out	(Note 3)			95		dB
Interchannel Gain Mismatch		Line Out			0.1	0.5	dB
Voltage Reference Output				2.0	2.2	2.35	V
Voltage Reference Output Current		(Note 4)			100		µA
DAC Programmable Attenuation Span				93	94.5		dB
DAC Attenuation Step Size	0 dB to -81 dB			1.3	1.5	1.7	dB
	-82.5 dB to -94.5 dB			1.0	1.5	2	dB
DAC Offset Voltage					1	10	mV
Full Scale Output Voltage:	OLB = 0	(Notes 3, 5)		1.8	2.0	2.25	V_{pp}
	OLB = 1	OUT, MOUT		2.6	2.8	3.2	V_{pp}
Gain Drift					100		ppm/°C
Deviation from Linear Phase		(Note 1)				1	Degree
External Load Impedance				10			kΩ
Mute Attenuation (0 dB)				80			dB
Total Out-of-Band Energy	0.6xFs to 100 kHz	(Note 1)				-45	dB
Audible Out-of-Band Energy	0.6xFs to 22 kHz	(Fs=8kHz)				-60	dB
Power Supply							
Power Supply Current	Digital, Operating				55	65	mA
	Analog, Operating				43	60	mA
	Total				98	120	mA
	Digital, Power Down				0.1	1	mA
	Analog, Power Down				0.8	1	mA
Power Supply Rejection	1 kHz	(Note 1)		40			dB

Notes: 3. 10 kΩ, 100 pF load.
4. DC current only. If dynamic loading exists, then the voltage reference output must be buffered or the performance of ADCs and DACs will be degraded.
5. All mixer and output gain tables assume the output level bit, OLB, in indirect register 16 (I16) is set, wherein the input and output full scale values are equal. When OLB=0, the output value is 3 dB below the input value, given no gain or attenuation.

AUXILIARY INPUT MIXERS (TA = 25 °C; VA1, VA2, VD1-VD4 = +5V;
Input Levels: Logic 0 = 0V, Logic 1 = VD1-VD4; 1 kHz Input Sine wave)

Parameter	Symbol	Min	Typ	Max	Units
Mixer Gain Range Span LINE, AUX1, AUX2 (Note 6) MIN		45 42	46.5 45		dB dB
Step Size LINE, AUX1, AUX2 MIN		1.3 2.3	1.5 3.0	1.7 3.4	dB dB

Notes: 6. All mixer gain values assume OLB=1. If OLB=0, the analog output will be 3 dB below listed settings.

ABSOLUTE MAXIMUM RATINGS (AGND, DGND = 0V, all voltages with respect to 0V.)

Parameter	Symbol	Min	Max	Units
Power Supplies: Digital	VD1-VD4	-0.3	6.0	V
Analog	VA1,VA2	-0.3	6.0	V
Input Current per Pin (Except Supply Pins)		-10.0	+10.0	mA
Output Current per Pin (Except Supply Pins)		-50	+50	mA
Analog Input Voltage		-0.3	VA+0.3	V
Digital Input voltage		-0.3	VD+0.3	V
Ambient Temperature (Power Applied)		-55	+125	°C
Storage Temperature		-65	+150	°C

Warning: Operation beyond these limits may result in permanent damage to the device.
                   Normal operation is not guaranteed at these extremes.

RECOMMENDED OPERATING CONDITIONS (AGND, DGND = 0V, all voltages with repect to 0V.)

Parameter	Symbol	Min	Typ	Max	Units
Power Supplies: Digital	VD1-VD4	4.75	5.0	5.25	V
Analog	VA1,VA2	4.75	5.0	5.25	V
Operating Ambient Temperature	T$_A$	0	25	70	°C

DIGITAL FILTER CHARACTERISTICS

Parameter		Symbol	Min	Typ	Max	Units
Passband			0		0.40xFs	Hz
Frequency Response			-0.5		+0.2	dB
Passband Ripple	(0-0.4xFs)				±0.1	dB
Transition Band			0.40xFs		0.60xFs	Hz
Stop Band			0.60xFs			Hz
Stop Band Rejection			74			dB
Group Delay	16- and 8-bit formats				10/Fs	s
	ADPCM stereo format				14/Fs	s
	ADPCM mono format				18/Fs	s
Group Delay Variation vs. Frequency	ADCs				0.0	μs
	DACs				0.1/Fs	μs

DIGITAL CHARACTERISTICS (T_A = 25°C; VA1, VA2, VD1-VD4 = 5V;
AGND1, AGND2, DGND1-DGND4, DGND7, DGND8 = 0V.)

| Parameter			Symbol	Min	Max	Units
High-level Input Voltage	Digital Inputs		V_{IH}	2.0	VD+0.3	V
	XTAL1I, XTAL2I, PDWN			VD-1.0	VD+0.3	V
Low-level Input Voltage			V_{IL}	-0.3	0.8	V
High-level Output Voltage:	D<7:0>	I_0 = -16.0 mA	V_{OH}	2.4	VD	V
	All Others	I_0 = -1.0 mA		2.4	VD	V
Low-level Output Voltage:	D<7:0>	I_0 = 16.0 mA	V_{OL}		0.4	V
	All Others	I_0 = 4.0 mA			0.4	V
Input Leakage Current	(Digital Inputs)			-10	10	μA
Output Leakage Current	(High-Z Digital Outputs)			-10	10	μA

TIMING PARAMETERS (T$_A$ = 25 °C; VA1, VA2, VD1-VD4 = +5V, outputs loaded with 30 pF; Input Levels: Logic 0 = 0V, Logic 1 = VD1-VD4)

Parameter	Symbol	Min	Max	Units
WR or RD strobe width	t$_{STW}$	90		ns
Data valid to WR rising edge (write cycle)	t$_{WDSU}$	22		ns
RD falling edge to data valid (read cycle)	t$_{RDDV}$		60	ns
CS setup to WR of RD falling edge	t$_{CSSU}$	10		ns
CS hold from WR or RD rising edge	t$_{CSHD}$	0		ns
ADDR <> setup to RD or WR falling edge	t$_{ADSU}$	22		ns
ADDR <> hold from WR or RD rising edge	t$_{ADHD}$	10		ns
DAK inactive to WR or RD falling edge (DMA cycle completion immediately followed by a non-DMA cycle)	t$_{SUDK1}$	60		ns
DAK active from WR or RD rising edge (non-DMA cycle completion immediately followed by DMA cycle)	t$_{SUDK2}$	0		ns
DAK setup to RD falling edge (DMA cycles) DAK setup to WR falling edge	t$_{DKSUa}$ t$_{DKSUb}$	25 25		ns ns
Data hold from WR rising edge	t$_{DHD2}$	15		ns
DRQ hold from WR or RD falling edge (assumes no more DMA cycles needed)	t$_{DRHD}$	0	25	ns
Time between rising edge of WR or RD to next falling edge of WR or RD	t$_{BWND}$	80		ns
Data hold from RD rising edge	t$_{DHD1}$	0	20	ns
DAK hold from WR rising edge DAK hold from RD rising edge	t$_{DKHDa}$ t$_{DKHDb}$	25 25		ns ns
DBEN or DBDIR active from WR or RD falling edge	t$_{DBDL}$		40	ns
PDWN pulse width low	t$_{PDWN}$	200		ns
Crystals, XTAL1I, XTAL2I frequency (Notes 1,7,8)			25.6	MHz
XTAL1I, XTAL2I high time (Notes 1,8)		18		ns
XTAL1I, XTAL2I low time (Notes 1,8)		18		ns
Sample frequency (Note 1)	Fs	5.5	50	kHz
Serial Port Timing				
SCLK frequency (Note 9)	t$_{SCLKW}$		Fsx64	Hz
SCLK rising to SDOUT valid	t$_{PD1}$		30	ns
SCLK rising to FSYNC transition	t$_{PD2}$	-20	20	ns
SDIN valid to SCLK falling	t$_{S1}$	30		ns
SDIN hold after SCLK falling	t$_{H1}$	30		ns

Notes: 7. When only one crystal is used, it must be XTAL1. When using two crystals, the high frequency crystal should be on XTAL1 which is designed for higher loop gains.
   8. Sample frequency specifications must not be exceeded.
   9. When SF1, 0 = 10, 32-bit mode, SCLK is active for the first 32 bit periods of the frame, and remains low during the last 32 bit periods of the frame.
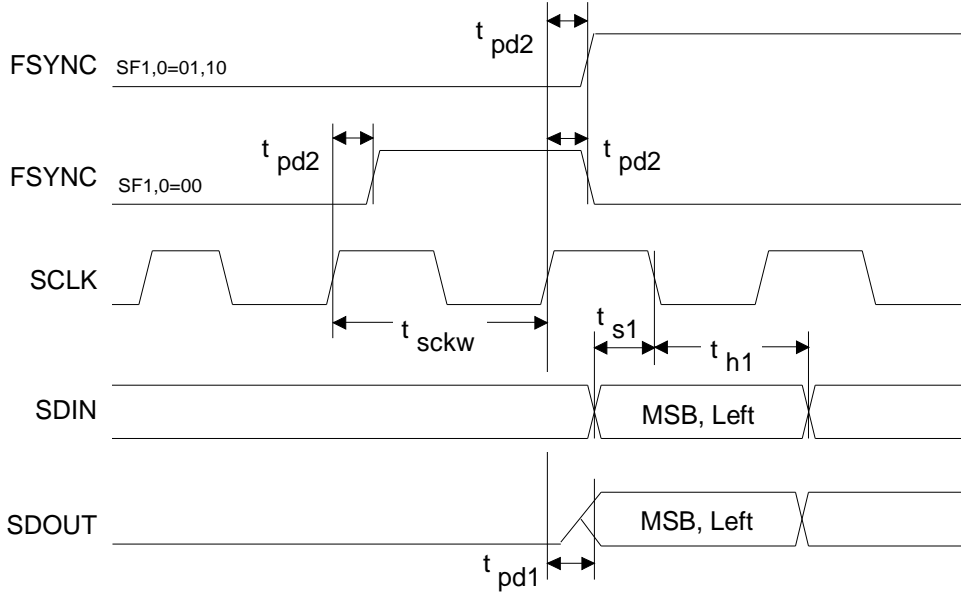
Serial Port Timing
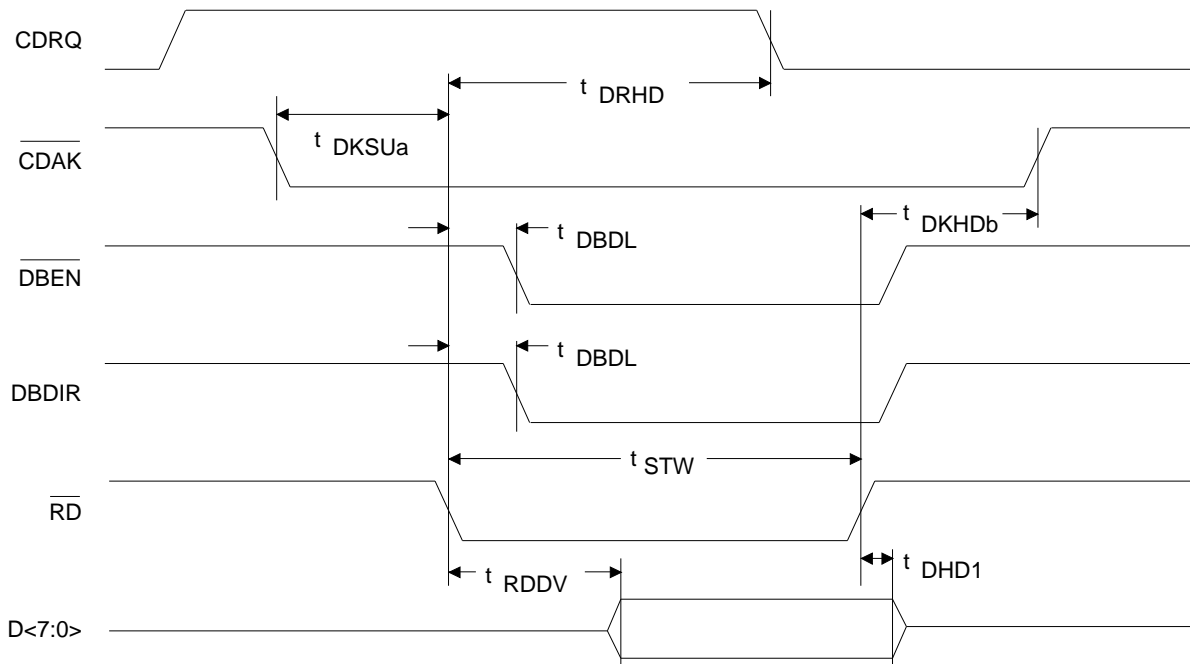
8-Bit Mono DMA Read/Capture Cycle
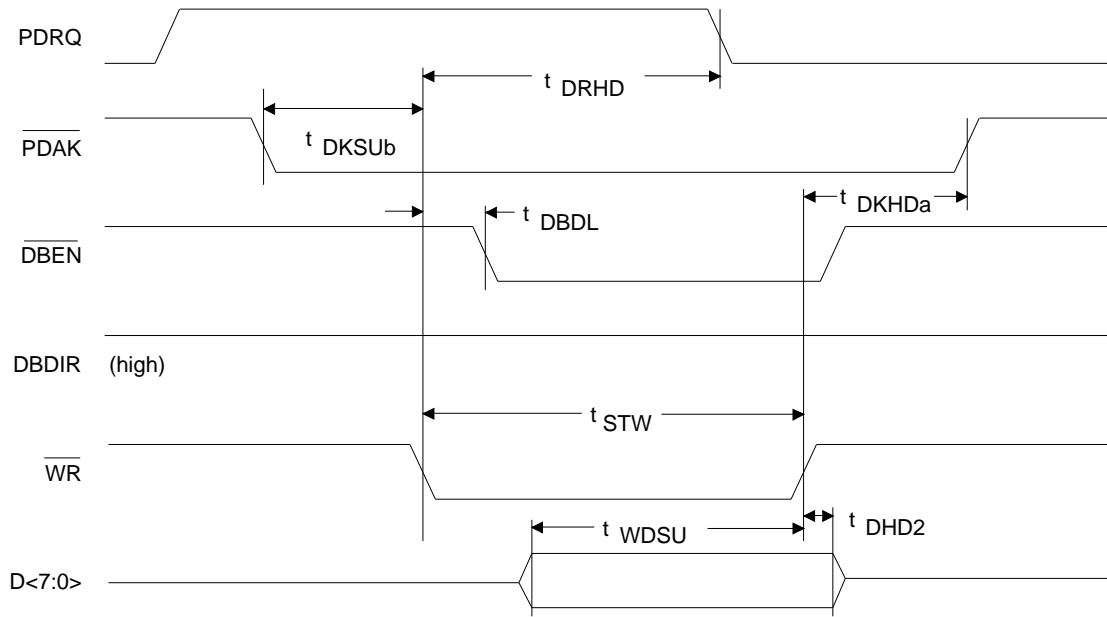
8-Bit Mono DMA Write/Playback Cycle
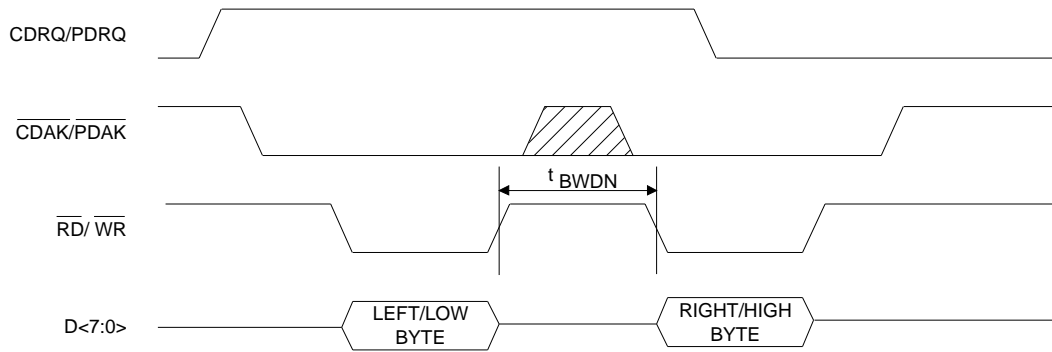
8-Bit Stereo or 16-Bit Mono DMA Cycle
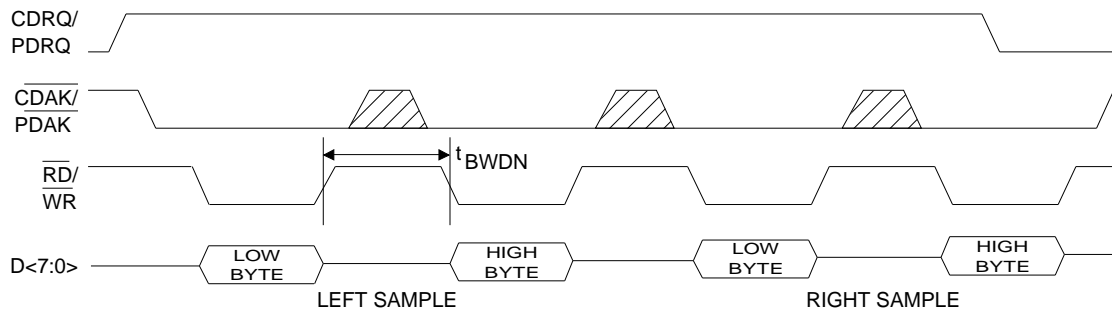
16-Bit Stereo or ADPCM DMA Cycle
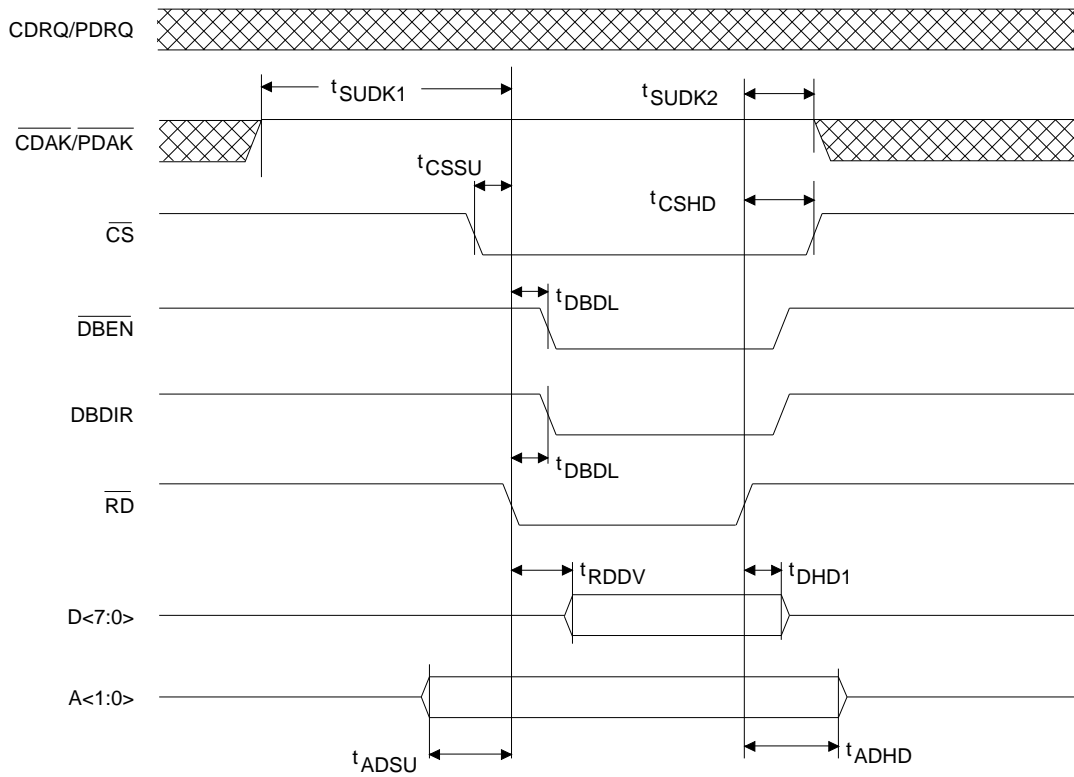
I/O Read Cycle
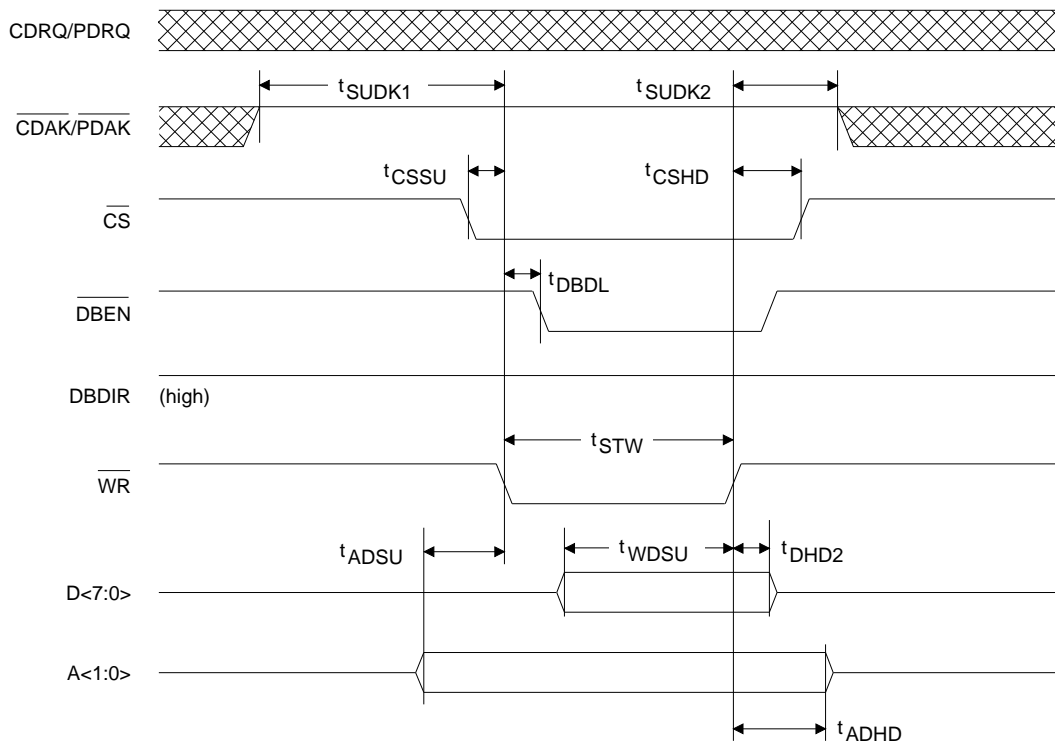
I/O Write Cycle
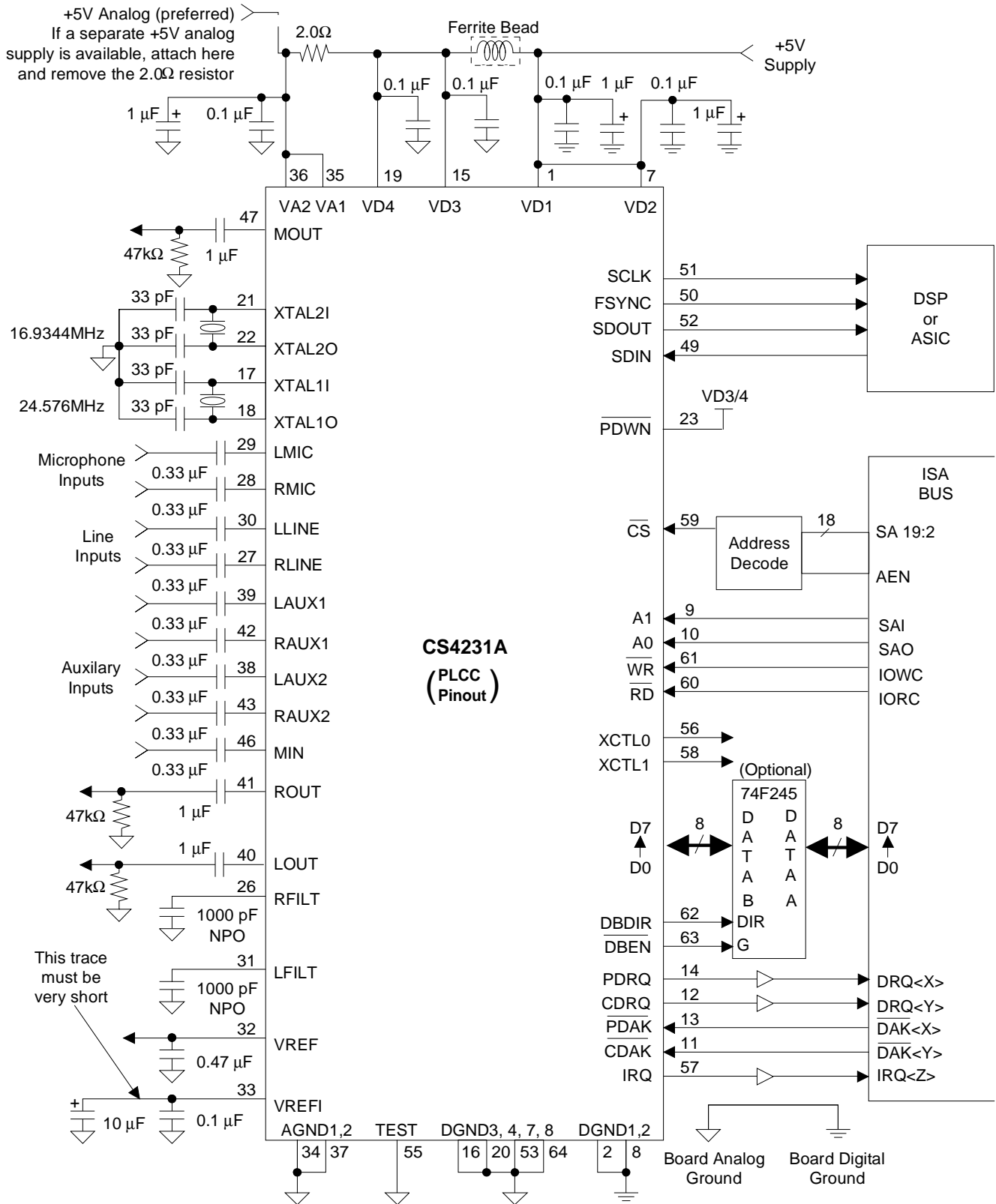
Figure 1. Recommended Connection Diagram
(See Figures 16 & 17 for Layout Recommendations)

GENERAL DESCRIPTION

The CS4231A is a monolithic integrated circuit that provides audio in personal computers or other parallel interface environments. The functions include stereo Analog-to-Digital and Digital-to-Analog converters (ADCs and DACs), analog mixing, anti-aliasing and reconstruction filters, line and microphone level inputs, optional A-Law / μ-Law coding, simultaneous capture and playback and a parallel bus interface. Five analog inputs are provided and three can be multiplexed to the ADC. The line input, two auxiliary inputs and a mono input can be mixed with the output of the DAC with full volume control. Several data modes are supported including 8- and 16-bit linear as well as 8-bit companded, 4-bit ADPCM compressed, and 16-bit Big Endian. The CS4231A is packaged in a 68-pin PLCC or a 100-pin TQFP.

Enhanced Functions (MODE 2)

The CS4231A's initial state is labeled MODE 1 and forces the CS4231A to appear as a CS4248. Enhanced functionality is provided by a second mode on the CS4231A. To switch from MODE 1 to MODE 2, the MODE2 bit should be set to one in the MODE and ID register (I12). When MODE 2 is selected, the bit IA4 in the Index Address register (R0) will be decoded as a valid index pointer, providing 16 additional registers and increased functionality over the CS4248.

To reverse the procedure, clear the MODE2 bit and the CS4231A will resume operation in MODE 1. Since previous code writes a zero to bit IA4 of the Index Address register (R0), the CS4231A is backwards compatible with the CS4248 and the AD1848.

Mixer Attenuation Control on Line Input

The CS4231A adds mixer attenuation control for the LINE inputs which are then summed into the output mixer. This fourth input to the mixer completes the recommended mixer configuration for MPC Level-2 compliance. The LINE mix register provides 32 volume adjustments in 1.5 dB steps. In addition, there is a one bit mute control.

The additional MODE 2 functions are:

1. Full-Duplex DMA support
2. A programmable timer
3. Mono output with mute control
4. Mono input with mixer volume control
5. ADPCM and Big Endian audio data formats
6. Independent selection of capture and playback audio data formats
7. Selectable serial audio data port.

ANALOG HARDWARE DESCRIPTION

The analog hardware consists of an MPC Level 2-compatible mixer (four stereo mix sources), three line-level stereo inputs, a stereo microphone input, a mono input, a mono output, and a stereo line output. This section describes the analog hardware needed to interface with these pins.

Analog Inputs

The analog inputs consist of four stereo analog inputs, and one mono input. As shown on this data sheet cover, the input to the ADCs comes from a multiplexer that selects between two analog line-level inputs (LINE, AUX1), a microphone level input (MIC), and the output from the MPC-compatible mixer. The LINE and AUX1 lines also feed the MPC mixer and include individual volume controls. Unused analog inputs should be connected together and then connected through a capacitor to analog ground.

Line-Level Inputs plus MPC Mixer

The analog input interface is designed to accommodate four stereo inputs and one mono input. Three of these sources are multiplexed to the ADC. These inputs are: a stereo line-level input (LINE), a stereo microphone input (MIC), and a stereo auxiliary line-level input (AUX1). The LINE and AUX1 inputs have a separate path, with volume control, to the output analog mixer which has the additional inputs of a stereo AUX2 channel, a mono input channel, and the output of the DACs. All audio inputs should be capacitively coupled to the CS4231A.

Since some analog inputs can be as large as 2 V_{RMS}, the circuit shown in Figure 2 can be used to attenuate the analog input to 1 V_{RMS} which is the maximum voltage allowed for the line-level inputs on the CS4231A.
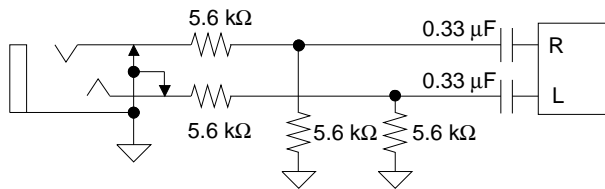
Figure 2. Line Inputs

Microphone Level Inputs

The microphone level inputs, LMIC and RMIC, include a selectable + 20dB gain stage for interfacing to an external microphone. The 20 dB gain block can be turned off to provide another stereo line-level input. Figure 3 illustrates a single-ended microphone input buffer with +18 dB of gain that will support lower gain mics, and should be placed as close to the input jack as possible to minimize noise coupling.

Mono Input with Attenuation and Mute

The mono input, MIN, is useful for mixing the output of the "beeper" (timer chip), provided in
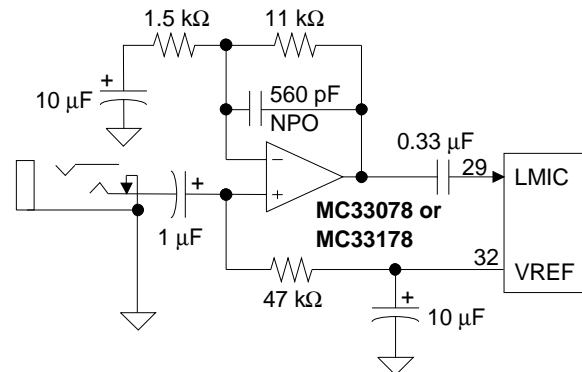
Figure 3. Left or Mono Microphone Input

all PCs, with the rest of the audio signals. The attenuation control allows 16 levels in -3dB steps. In addition, a mute control is provided. The attenuator is a single channel block with the resulting signal sent to the output mixer where it is mixed with the left and right outputs. Figure 4 illustrates a typical input circuit for the Mono In. Although this input is described for a low-quality beeper, the input is of the same high-quality as all other analog inputs and may be used for other purposes. At power-up, the MIN line is unmuted (as is the mono out line) allowing the initial beeps heard, when the computer is initializing, to pass through.
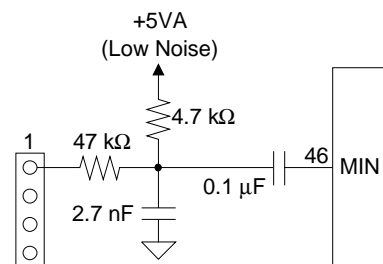
Figure 4. Mono Input

Analog Outputs

The analog output section of the CS4231A provides a stereo line-level output. The other output types (headphone and speaker) can be implemented with external circuitry. LOUT and ROUT outputs should be capacitively coupled to external circuitry.

Mono Output with Mute Control

The mono output, MOUT, is a sum of the left and right output channels, attenuated by 6dB to prevent clipping at full scale. The mono out channel can be used to drive the PC-internal mono speaker using an appropriate drive circuit. This approach allows the traditional PC-sounds to be integrated with the rest of the audio system. Figure 5 illustrates a typical speaker driver circuit. The mute control is independent of the line outputs allowing the mono channel to mute the speaker without muting the line outputs. The power-up default has MIN and MOUT enabled to provide a pass-through for the beeps heard at power-up.
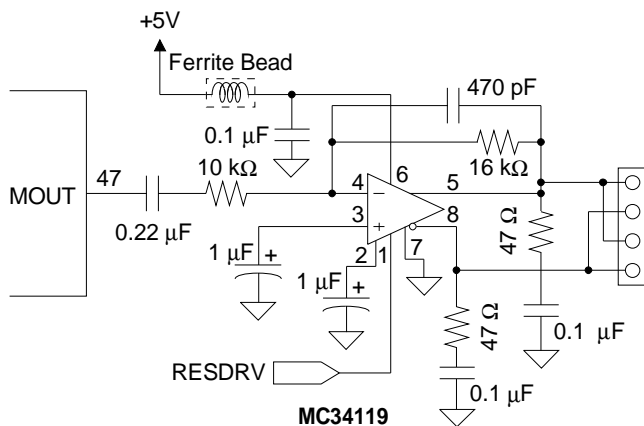
Figure 5. Mono Output

Miscellaneous Analog Signals

The LFILT and RFILT pins must have a 1000 pF NPO capacitor to analog ground. These capacitors, along with an internal resistor, provide a single-pole low-pass filter used at the inputs to the ADCs. By placing these filters at the ADC inputs, low-pass filters at each analog input pin are avoided.

The VREFI pin is used to lower the noise of the internal voltage reference. A 10µF and 0.1µF capacitor to analog ground should be connected with a short wide trace to this pin. No other connection should be made, since noise coupling onto this pin can degrade the analog performance of the codec. Likewise, digital signals should be kept away from VREFI for similar reasons.

The VREF pin is typically 2.1 V and provides a common mode signal for single-supply external circuits. VREF only supports DC loads and should be buffered if AC loading is needed. For typical use, a 0.47 µF capacitor should be connected to VREF. The signal-to-noise ratio of the microphone inputs can be improved by increasing the capacitance on VREF to 10 µF.

DIGITAL HARDWARE DESCRIPTION

The digital hardware consist of the data bus, address bus, and control signals needed for the parallel bus, as well as an interrupt and DMA signals.

Parallel Data Interface

The 8-bit parallel port of the CS4231A provides an interface which is compatible with most computer peripheral busses. This parallel interface is designed to operate on the Industry Standard Architecture (ISA) bus, but the CS4231A will easily interface with other buses such as EISA and Microchannel. Two types of accesses can occur via the parallel interface: Programmed I/O (PIO) access, and DMA access.

There is no provision for the CS4231A to "hold off" or extend a cycle occurring on the parallel interface. Therefore, the internal architecture of the CS4231A accepts asynchronous parallel bus cycles without interfering with the flow of data to or from the ADC and DAC sections.

FIFOs

The CS4231A contains 16-sample FIFOs in both the playback and capture paths. The FIFOs are

transparent and have no programming associated with them.

When playback is enabled, the playback FIFO continually requests data until the FIFO is full, and then makes requests as positions inside the FIFO are emptied, thereby keeping the playback FIFO as full as possible. Thus when the system cannot respond within a sample period, the FIFO is emptied, avoiding a momentary loss of audio data. If the FIFO runs out of data, the last valid sample can be continuously output to the DACs (if DACZ in I16 is set) which will eliminate pops from occurring.

When capture is enabled, the capture FIFO tries to continually stay empty by making requests every sample period. Thus when the system cannot respond within a sample period, the capture FIFO starts filling thereby avoiding a loss of data in the audio data stream.

High Current Data Bus Drivers

The CS4231A provides 16 mA drivers eliminating the need for off chip drivers in many cases. If a full 24 mA drive is required, the appropriate direction and driver select lines are provided. The current drivers are provided for the data bus, DMA request line, and the interrupt request line.

PIO Registers Interface

The first type of parallel bus access is programmed I/O (PIO) to the four control registers. The control registers allow access to status, audio data, and all indirect registers via the index registers. The $\overline{RD}$ and $\overline{WR}$ signals are used to define the read and write cycles respectively. The PIO register cycle is defined by the assertion of the CS4231A $\overline{CS}$ signal while the DMA acknowledge signals, $\overline{CDAK}$ and $\overline{PDAK}$, are inactive. For read cycles, the CS4231A will drive data on the DATA lines while the host asserts the $\overline{RD}$ strobe. Write cycles require the host to assert data on the DATA lines and strobe the $\overline{WR}$ sig-

nal. The CS4231A will latch data into the PIO register on the rising edge of the $\overline{WR}$ strobe. The CS4231A $\overline{CS}$ signal should remain active until after completion of the read or write cycle. I/O cycles are the only type of cycle which can access the internal control and status registers.

When reading or writing audio data via PIO, the Status register (R2) indicates which byte of the audio sample is ready. The Status register does not have to be read after every byte; however, once all bytes of a sample are transferred, the Status register must be read before the next sample can be transferred.

The audio data interface typically uses DMA request/grant pins to transfer the digital audio data between the CS4231A and the bus. The CS4231A is responsible for asserting a request signal whenever the CS4231A's internal buffers need updating. The logic interfaced with the CS4231A responds with an acknowledge signal and strobes data to and from the CS4231A, 8 bits at a time. The CS4231A keeps the request pin active until the appropriate number of 8-bit cycles have occurred to transfer one audio sample. Notice that different audio data types will require a different number of 8-bit transfers.

DMA Interface

The second type of parallel bus cycle on the CS4231A is a DMA transfer. DMA cycles are distinguished from PIO register cycles by the assertion by the CS4231A of a CDRQ (or PDRQ) followed by an acknowledgment by the host by the assertion of $\overline{CDAK}$ (or $\overline{PDAK}$). While the acknowledgment is received from the host, the CS4231A assumes that any cycles occurring are DMA cycles and ignores the addresses on the address lines and the $\overline{CS}$ line.

The CS4231A may assert the DMA request signal at any time. Once asserted, the DMA request will remain asserted until a DMA cycle occurs to the CS4231A. Once the falling edge of the final

$\overline{WR}$ or $\overline{RD}$ strobe of a full sample of a DMA cycle occurs, the DMA request signal is negated immediately. DMA transfers may be terminated by resetting the PEN and/or CEN bits in the Interface Configuration register (I9), depending on the DMA that is in progress (playback, capture, or both). Termination of DMA transfers may only happen between sample transfers on the bus. If PDRQ and/or CDRQ goes active while resetting PEN and/or CEN, the request must be acknowledged ($\overline{PDAK}$ and/or $\overline{CDAK}$) and a final sample transfer completed. The CS4231A supports up to two DMA channels.

Dual DMA Channel Mode

In dual DMA channel mode, playback and capture DMA requests and acknowledges occur on independent DMA channels. In this mode, capture and playback are enabled and set for DMA transfers. In addition, the dual DMA mode must be set (SDC = 0). The Playback- and Capture-Enables (PEN, CEN, I9) can be changed without a Mode Change Enable (MCE, R0). This allows for proper full duplex control where applications are independently using playback and capture.

Single DMA Channel (SDC) Mode

When two DMA channels are not available, the SDC mode forces all DMA transfers (capture or playback) to occur on a single DMA channel (playback channel). The trade-off is that the CS4231A will no longer be able to perform simultaneous DMA capture and playback.

To enable the SDC mode, set the SDC bit in the Interface Configuration register (I9). With the SDC bit asserted, the internal workings of the CS4231A remain exactly the same as dual mode, except for the manner in which DMA request and acknowledges are handled.

The playback of audio data will occur on the playback channel exactly as dual channel operation. However, the capture audio channel is now

diverted to the playback channel. This means that the capture DMA request occurs on the PDRQ pin and the $\overline{PDAK}$ pin is used to acknowledge the capture request. (In MODE 2, the capture data format is always set in register I28.) Note, simultaneous capture and playback cannot occur in SDC mode. If both playback and capture are enabled, the default will be playback.

In SDC mode, the CDRQ pin is logic low (inactive). The $\overline{CDAK}$ pin is ignored by the CS4231A. SDC does not have any affect when using PIO accesses.

Serial Audio Data Port

The bits controlling the serial port can only be changed when the Mode Change Enable bit, MCE, in R0 is high. The audio serial port is software selectable via the SPE bit in I16. Once enabled, the data from the ADCs is sent to the SDOUT pin and the audio data input on the SDIN pin is routed to the DACs. The parallel bus on the CS4231A is still used for control information such as volume and audio data formats. While the serial port is enabled, audio data can still be read from the codec ADCs (capture) on the parallel port, but the DACs (playback) only accept data from the serial port in pin. When the serial port is disabled (SPE = 0); FSYNC, SCLK, and SDOUT are held low.

FSYNC and SCLK are always output from the CS4231A. The serial port can be configured in one of three serial port formats, shown in Figures 6-8. SF1 and SF0 in I16 select the particular format. Both left and right audio words are always 16 bits wide with the actual audio data left justified in the word (i.e. ADPCM occupies the first four bits). Unused bits are output as zeros after the LSB. The justification is illustrated in Figure 9. When the mono audio format is selected, the right channel output is set to zero and the left channel input is sent to both DAC channels. When changing sample frequencies the

output clocks will stretch, but will not have any glitches. This allows the serial port to operate through a sample frequency change.

The first format - SPF0, shown in Figure 6, is called 64-bit enhanced. This format has 64 SCLKs per frame with a one bit period wide FSYNC that precedes the frame. The first 16 bits
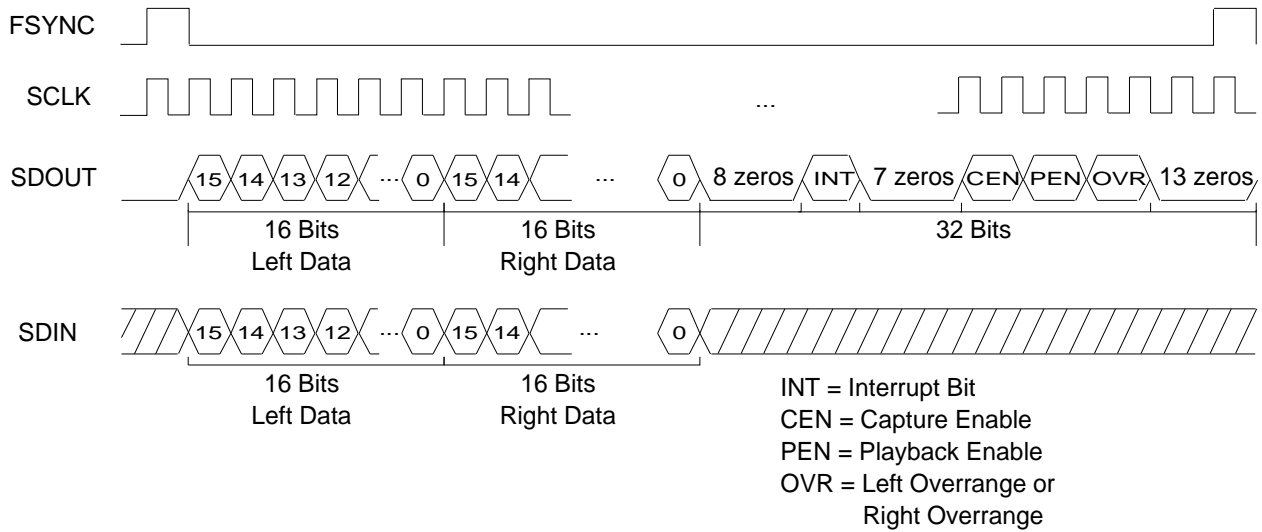
Figure 6. 64-bit enhanced mode (SF1,0 = 00)
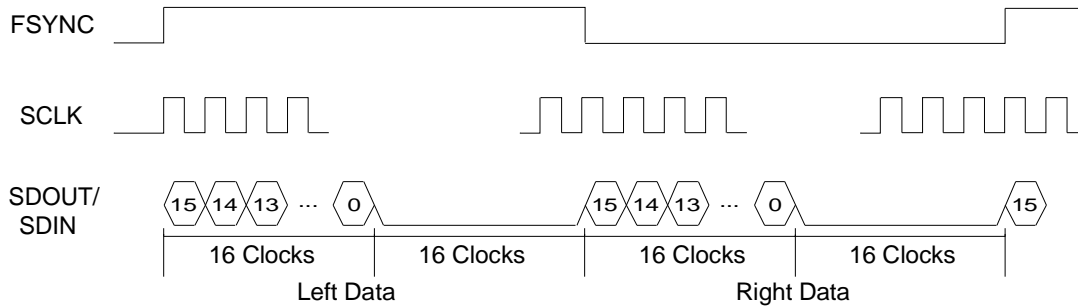
Figure 7. 64-bit mode (SF1,0 = 01)
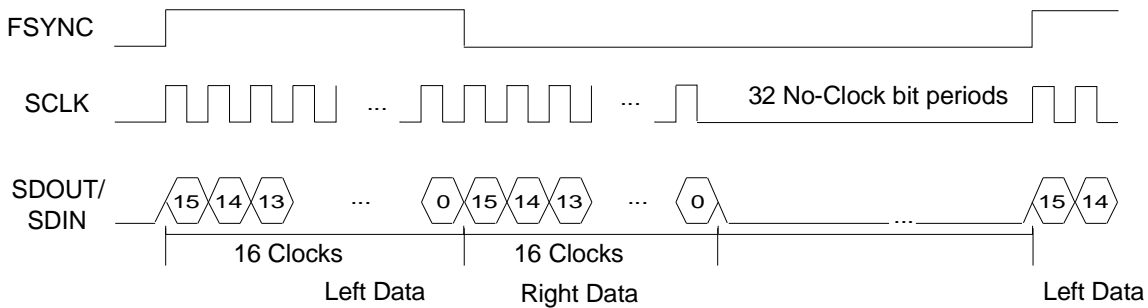
Figure 8. 32-bit mode (SF1,0 = 10)

is the left word and the second 16 bits is the right word. The last 32 bits contains four status bits and 28 zeros. This is the only mode that contains status information.

The second serial format - SPF1, shown in Figure 7, is called 64-bit mode. This format also has 64 SCLKs per frame, but has FSYNC transitioning high at the start of the left data word and transitioning low at the start of the right data word. Both the left and the right data word are followed by 16 zeros.

The third serial format - SPF2, shown in Figure 7, is called 32-bit mode. This format contains 32 SCLKs per frame wherein FSYNC is high for the left channel and low for the right channel. The absolute time is similar to the other two modes but SCLK is stopped after the right channel is finished until the start of the next frame (stopped for 32 bit period times). This mode is useful for DSPs that do not want the interrupt overhead of the 32 unused bit periods. As an example, if a DSP serial word length is 16 bits, then four interrupts will occur in SPF0 and SPF1; whereas in SPF2 the DSP will only get two interrupts.

Miscellaneous Signals

The power supply providing analog power should be as clean as possible to minimize noise coupling into the analog section and degrading analog performance. The VD1 and VD2 pins are isolated from the rest of the digital power pins and provide digital power for the asynchronous parallel bus. These two pins can be connected directly to the digital power supply. VD3 and VD4 digital power supply pins provide power to the internal digital section of the codec and should be optimally quieter than VD1 and VD2. This can be achieved by using a ferrite bead as shown in the typical connection diagram in Figure 1. Grounding is covered in the *Grounding and Layout* section.

An interrupt pin, IRQ, is provided to allow for host notification by the CS4231A. Since the interrupt is mainly a software function, it is described in more detail under the software section.

Crystals / Clocks

Four pins have been allocated to allow the interfacing of two crystal oscillators to the CS4231A: XTAL1I, XTAL1O, XTAL2I, XTAL2O. The crystals should be designed as fundamental mode, parallel resonant, with a load capacitor of between 10 and 20 pF. The capacitors shown in Figure 1, connected to each of the crystal pins, should be twice the load capacitance specified to the crystal manufacturer. The XTAL1 oscillator is designed with slightly more gain to handle

Audio Word

Bits	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

| 16 | MSB | | | | | | | | | | | | | | | LSB |

| 8 | MSB | | | | | | | LSB | X | X | X | X | X | X | X | X |

| 4 | MSB | | LSB | X | X | X | X | X | X | X | X | X | X | X |

X: SDIN - Don't care, SDOUT - 0
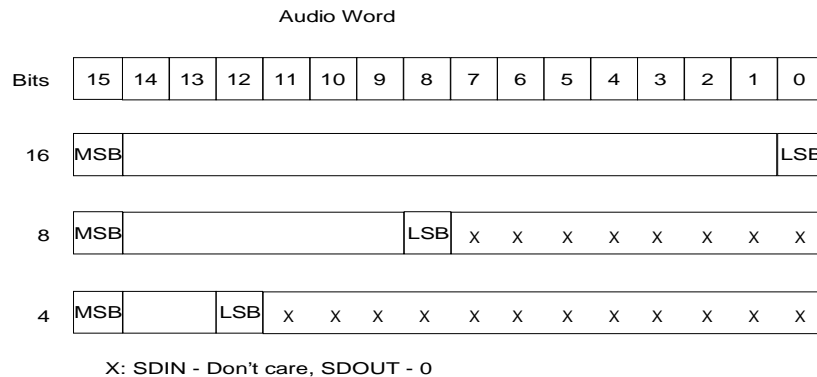
Figure 9. Serial Audio Data Justification

higher frequencies, but any crystal with the above specifications should suffice. The standard crystals for audio are:

XTAL1:   24.576 MHz
         Fundamental Mode
         Parallel Resonant, C_L = 20 pF

XTAL2:   16.9344 MHz
         Fundamental Mode
         Parallel Resonant, C_L = 20 pF

These crystal frequencies support the standard sample frequencies listed in Table 7.

External CMOS clocks may be connected the crystal inputs (XTAL1I, XTAL2I) in lieu of the crystals. When using external CMOS clocks, the XTAL out pins should be left floating. Extreme care should be used when laying out a board using external clocks since coupling between clocks can degrade analog performance.

Power Down - $\overline{PDWN}$

The $\overline{PDWN}$ signal places the CS4231A into maximum power conservation mode. When $\overline{PDWN}$ goes low, any reads of the codec's parallel interface return 80 hex, all analog outputs are muted, and the voltage reference then slowly decays to ground. When $\overline{PDWN}$ is brought high, a full calibration cycle automatically occurs. While the codec is initializing, any reads from the parallel interface will return 80 hex and writes will be ignored. When initialization is completed, the registers will contain their reset value as stated in the register section of the data sheet. The CS4231A contains an internal "Power On Reset" signal that causes a proper initialization at power up time. Therefore, if no power down mode is needed, $\overline{PDWN}$ can be tied permanently to VD3/4.

$\overline{DBEN}$/DBDIR

If needed, the $\overline{DBEN}$ and DBDIR pins can control an external data buffer to the CS4231A. The CS4231A contains 16 mA bus drivers so the external data buffer is only needed when driving a full 24 mA bus. $\overline{DBEN}$ enables the external drivers and DBDIR controls the direction of the data flow. Both signals are normally high, where DBDIR high points the transceiver towards the codec and low points the transceiver towards the data bus. See Figure 1 for a typical connection diagram.

SOFTWARE DESCRIPTION

The CS4231A must be in Mode Change Enable Mode (MCE=1) before any changes to the Interface Configuration register (I9), the Sample Frequency (lower four bits) in the Fs & Playback Data Format register (I8), or the serial port bits (SF1, SF0, SPE) in the Alternate Feature Enable I register (I16) are allowed. The actual audio data formats, which are the upper four bits of I8 for playback and I28 for capture, can be changed by setting MCE (R0) or PMCE/CMCE (I16) high. The exceptions are CEN and PEN which can be changed "on-the-fly" via programmed I/O writes to these bits. All outstanding DMA transfers must be completed before new values of CEN or PEN are recognized.

Power-Down and Initialization

To put the CS4231A into a power-down mode, the $\overline{PDWN}$ pin is pulled low. In this state the host interface reads 80h indicating that it is unable to respond and all analog circuits are turned off.

To let the CS4231A go through its reset initialization the $\overline{PDWN}$ pin should be set high. This

rising edge starts the initialization process in which a full calibration occurs. While the CS4231A is initializing, 80 hex is returned from all reads by the host computer. All writes during initialization of the CS4231A will be ignored. At the end of the initialization, all registers are set to known reset values as documented in the register definition section.

Calibration Modes

The CS4231A has four different calibration modes. The selected calibration occurs whenever the Mode Change Enable (MCE, R0) bit goes from 1 to 0.

The completion of calibration can be determined by polling the Auto-Calibrate In-Progress bit in the Error Status and Initialization register (ACI, I11). This bit will be high while the calibration is in progress and low once completed. The calibration time varies with calibration mode.

The Calibration procedure is as follows:

1) Place the CS4231A in Mode Change Enable using the MCE bit of the Index Address register (R0).
2) Set the CAL1,0 bits in the Interface Configuration register (I9).
3) Return from Mode Change Enable by resetting the MCE bit of the Index Address register (R0).
4) Wait until ACI (I11) cleared to proceed

No Calibration (CAL1,0 = 00)

This is the fastest mode since no calibration is performed. This mode is useful for games which need to change the sample frequency quickly. This mode is also useful when the codec is operating in full-duplex and an ADC data format change is desired. This is the only calibration mode that does not affect the DACs (i.e. mute

the DACs at some point). Changing from any other calibration mode to No Calibration mode will take 40 sample periods to complete; however, subsequent MCE cycles will take 0 sample periods.

Converter Calibration (CAL1,0 = 01)

This calibration mode calibrates the ADCs and DACs but does not calibrate any of the analog mixing channels. This is the second longest calibration mode, taking 136 sample periods, and is software and hardware similar to the CS4231 or CS4248. Since the mixer is not calibrated, any analog signals mixing into the output will be unaffected. The calibration sequence done by the CS4231A is as follows:

> The DACs are muted
> The ADCs are calibrated
> The DACs are calibrated
> The DACs are unmuted

DAC Calibration (CAL1,0 = 10)

This calibration mode only calibrates the DACs' (playback) interpolation filters leaving the ADCs unaffected. This is the second fastest calibration mode (no cal. is the fastest) taking 40 sample periods to complete. The calibration sequence done by the CS4231A is as follows:

> The DACs are muted
> The DAC filters are calibrated
> The DACs are unmuted

Full Calibration (CAL1,0 = 11)

This calibration mode calibrates all offsets, ADCs, DACs, and analog mixers. Full calibration is automatically initiated on power up or anytime the CS4231A exits from a power down state. This is the longest calibration mode and takes 168 sample periods to complete. The calibration sequence done by the CS4231A is as follows:

All outputs are muted (DACs and mixer)
The mixer is calibrated
The ADCs are calibrated
The DACs are calibrated
All outputs are unmuted

Changing Sampling Rate

The internal states of the CS4231A are synchronized by the selected sampling frequency defined in the Fs and Playback Data Format register (I8). The changing of either the clock source or the clock frequency divide requires a special sequence for proper CS4231A operation:

1) Place the CS4231A in Mode Change Enable using the MCE bit of the Index Address register (R0).
2) During a single write cycle, change the Clock Frequency Divide Select (CFS) and/or Clock 2 Source Select (C2SL) bits of the Fs & Playback Data Format register (I8) to the desired value. (The data format may also be changed.)
3) The CS4231A resynchronizes its internal states to the new clock. During this time the CS4231A will be unable to respond at its parallel interface. Writes to the CS4231A will not be recognized and reads will always return the value 80 hex.
4) The host now polls the CS4231A's Index Address register (R0) until the value 80 hex is no longer returned.
5) Once the CS4231A is no longer responding to reads with a value of 80 hex, normal operation can resume and the CS4231A can be removed from MCE.

The CSL and CFS bits cannot be changed unless the MCE bit has been set. Attempts to change the Data Format registers (I8, I28) or Interface Configuration register (I9, except CEN and PEN) without MCE set, will not be recognized.

When fast changing of sample frequency is desired, the XTALE bit (I17) should be set. When set, both crystals are kept running thereby providing the fastest switching time (80h never appears) between sample frequencies. When XTALE is cleared, the unused crystal is powered down to minimize noise coupling. This causes 80h to appear after leaving an MCE cycle until the newly selected crystal is operational. XTALE (and the No Calibration mode, I9) provide the fastest switching time for applications such as games that constantly change the sample frequency.

Changing Audio Data Formats

In MODE 1, MCE must be used to select the audio data format in I8. Since MCE causes a calibration cycle, it is not ideal for full-duplex operation. In MODE 2, individual Mode Change Enable bits for capture and playback are provided in register I16. MCE (R0) must still be used to select the sample frequency, but PMCE (for playback) and CMCE (for capture) allow changing their respective data formats without causing a calibration to occur. Setting PMCE (I16) clears the playback FIFO and allows the upper four bits of I8 to be changed. Setting CMCE (I16) clears the capture FIFO and allows the upper four bits of I28 to be changed.

Audio Data Formats

In MODE 1 operation, all data formats of the CS4231A are in "little endian" format. This format defines the byte ordering of a multibyte word as having the least significant byte occupying the lowest memory address. Likewise, the most significant byte of a little endian word occupies the highest memory address.

The sample frequency is always selected in the Fs and Playback Data Format register (I8). In MODE 1 the same register, I8, determines the audio data format for both playback and capture; however, in MODE 2, I8 only selects the play-

back data format and the capture data format is independently selectable in the Capture Data Format register (I28).

The CS4231A always orders the left channel data before the right channel. Note that these definitions apply regardless of the specific format of the data. For example, 8-bit linear data streams look exactly like 8-bit companded data streams. Also, the left sample always comes first in the data stream regardless of whether the sample is 16- or 8-bit in size.

There are four data formats supported by the CS4231A during MODE 1 operation: 16-bit signed (little endian), 8-bit unsigned, 8-bit companded μ-Law, and 8-bit companded A-Law. See Figures 12 through 15.

Additional data formats are supported in MODE 2 operation: 4-bit ADPCM, and 16-bit signed big endian. See Figures 16 through 19. With the addition of the Big Endian and ADPCM audio data formats, the CS4231A is compliant with the IMA recommendations for digital audio data formats (and sample frequencies).

16-bit Signed

The 16-bit signed format (also called 16-bit 2's complement) is the standard method of representing 16-bit digital audio. This format gives 96 dB theoretical dynamic range and is the standard for compact disk audio players. This format uses the value -32768 (8000h) to represent maximum negative analog amplitude while 32767 (7FFFh) represents maximum positive analog amplitude.

8-bit Unsigned

The 8-bit unsigned format is commonly used in the personal computer industry. This format delivers a theoretical dynamic range of 48 dB. This format uses the value 0 (00h) to represent maximum negative analog amplitude while 255 (FFh) represents maximum positive analog amplitude. The 16-bit signed and 8-bit unsigned transfer functions are shown in Figure 10.

8-bit Companded

The 8-bit companded formats (A-Law and μ-Law) come from the telephone industry. μ-Law is the standard for the United States/Japan while A-Law is used in Europe. Companded audio allows either 64 dB or 72 dB of dynamic range
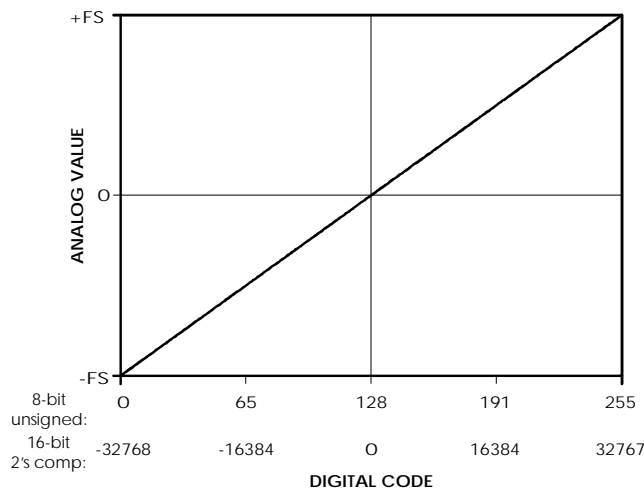
Figure 10. Linear Transfer Functions
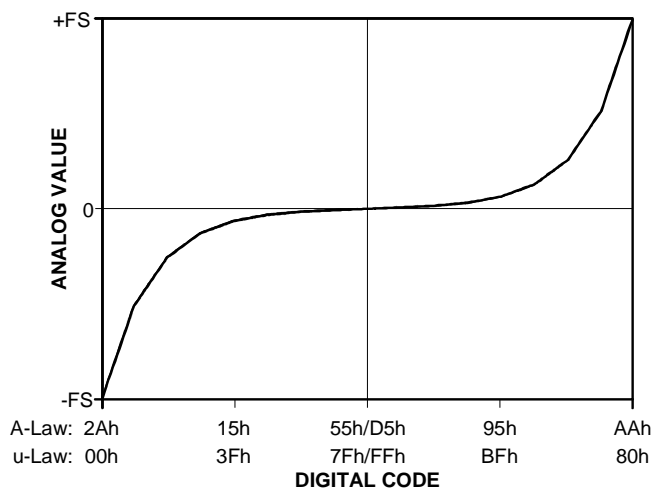
Figure 11. Companded Transfer Functions

32-bit Word

Time

| sample 6 | sample 5 | sample 4 | sample 3 | sample 2 | sample 1 |

| MONO | MONO | MONO | MONO |

31   24 23   16 15   8 7   0
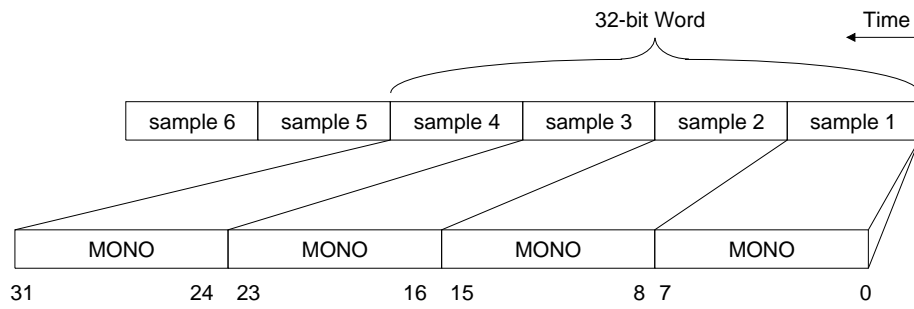
Figure 12. 8-bit Mono, Unsigned Audio Data

32-bit Word

Time

| sample 3 | sample 3 | sample 2 | sample 2 | sample 1 | sample 1 |

| RIGHT | LEFT | RIGHT | LEFT |

31   24 23   16 15   8 7   0
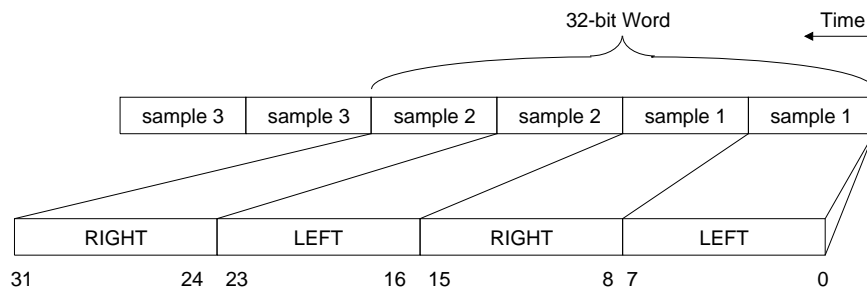
Figure 13. 8-bit Stereo, Unsigned Audio Data

32-bit Word

Time

| sample 6 | sample 5 | sample 4 | sample 3 | sample 2 | sample 1 |

| MONO | MONO |

31   24 23   16 15   8 7   0
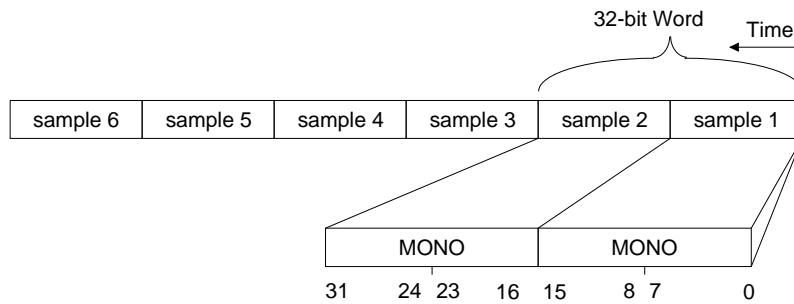
Figure 14. 16-bit Mono, Signed Little Endian Audio Data

32-bit Word

Time

| sample 3 | sample 3 | sample 2 | sample 2 | sample 1 | sample 1 |

| RIGHT | LEFT |

31   24 23   16 15   8 7   0
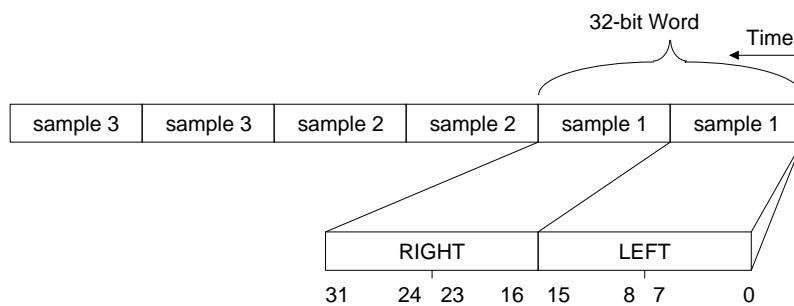
Figure 15. 16-bit Stereo, Signed Little Endian Audio Data
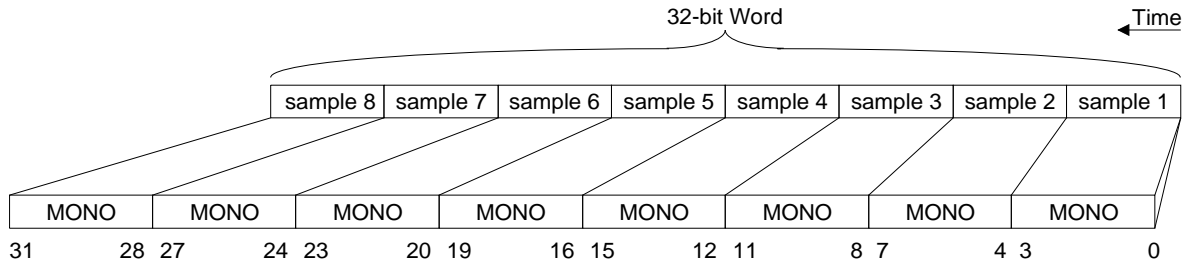
Figure 16. 4-bit Mono, ADPCM Audio Data
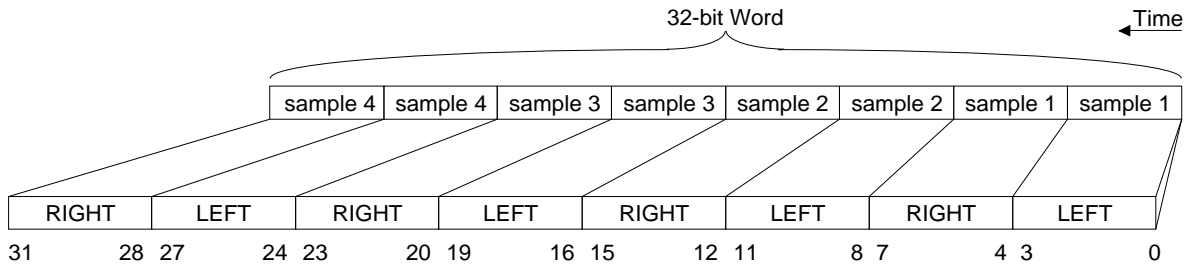
Figure 17. 4-bit Stereo, ADPCM Audio Data
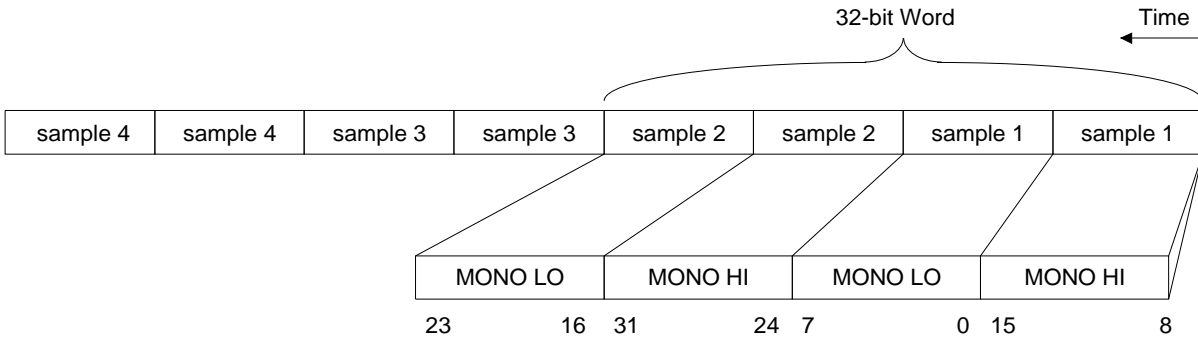
Figure 18. 16-bit Mono, Signed Big Endian Audio Data
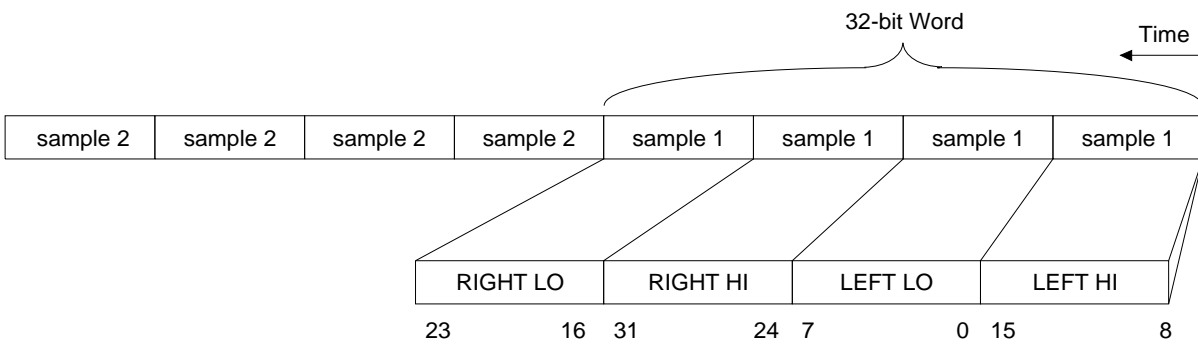
Figure 19. 16-bit Stereo, Signed Big Endian Audio Data

using only 8-bits per sample. This is accomplished using a non-linear companding transfer function which assigns more digitalization codes to lower amplitude analog signals with the sacrifice of precision on higher amplitude signals. The μ-Law and A-Law formats of the CS4231A conform to the CCITT G.711 specifications. Figure 11 illustrates the transfer function for both A- and μ-Law. Please refer to the standards mentioned above for an exact definition.

ADPCM Compression/Decompression

In MODE 2, the CS4231A also contains Adaptive Differential Pulse Code Modulation (ADPCM) for improved performance and compression ratios over μ-Law or A-Law. The ADPCM format is compliant with the IMA standard and provides a 4-to-1 compression ratio (i.e. 4 bits are saved for each 16-bit sample captured). For more detailed information on the IMA ADPCM format contact the IMA at (410) 626-1380. Figures 16 and 17 illustrate the ADPCM data flow.

The ADPCM format is unique with respect to the FIFO depth and the DMA Base register value. The ADPCM format fills the FIFOs completely (64 bytes); therefore, the FIFOs hold 64 stereo samples and 128 mono samples. When samples are transferred using DMA, the DMA request stays active for four bytes, similar to the 16-bit stereo mode. The Status register indicates which of the four bytes is being transferred in PIO mode.

When CEN is 0 (capture disabled), the ADPCM block's accumulator and step size are cleared. When CEN is enabled, the ADPCM block will start converting. The "overrun" condition should never occur, otherwise the data may not be constructed properly upon playback. If pausing the capture sequence is desired, the ADPCM Capture Freeze bit (ACF, I23) should be set. When set, the ADPCM algorithm will continue to oper-

ate until a complete word (4 bytes) is written to the FIFO. Then the ADPCM's block accumulator and step size will be frozen. The user is required to read the FIFO until empty, at which time the requests will stop. When ACF is cleared, the ADPCM adaptation will continue.

When PEN is 0 (playback disabled), the ADPCM block's accumulator and step size are cleared. When PEN is set, the ADPCM block will start converting. When pausing the playback stream is desired, audio data should not be sent to the codec causing an underrun. This can be accomplished by disabling the DMA controller or not sending data in PIO mode. The underrun will be detected by the CS4231A and the adaptation will freeze. As data is sent to the codec, adaptation is resumed. It is critical that all playback ADPCM samples are sent to the codec, since dropped samples will cause errors in the adaptation. Whereas toggling PEN resets the accumulator and step size, the APAR bit (I17) only resets the accumulator without affecting the step size.

DMA Registers

The DMA registers allow easier integration of the CS4231A in ISA systems. Peculiarities of the ISA DMA controller require an external count mechanism to notify the host CPU of a full DMA buffer via interrupt. The programmable DMA Base registers provide this service.

The act of writing a value to the Upper Base register causes both Base registers to load the Current Count register. DMA transfers are enabled by setting the PEN/CEN bit while PPIO/CPIO is clear. (PPIO/CPIO can only be changed while the MCE bit is set.) Once transfers are enabled, each sample that is transferred by a DMA cycle will decrement the appropriate Current Count register (with the exception of the ADPCM format) until zero is reached. The next sample after zero generates an interrupt and re-

loads the Current Count register with the values in the Base registers.

For all data formats except ADPCM, the DMA Base registers must be loaded with the number of samples, minus one, to be transferred between "DMA Interrupts". Stereo data contains twice as many bytes as mono data but the same number of samples. Likewise, 16-bit data contains twice the number of bytes as 8-bit data but the same number of samples. The equation for loading the DMA Base registers is:

DMA Base register$_{16}$ = N$_S$ - 1

Where N$_S$ is the number of samples transferred between interrupts and the "DMA Base register$_{16}$" consists of the concatenation of the upper and lower DMA Base registers.

For the ADPCM data format, the contents of the DMA Base registers are calculated differently from any other data format. In the ADPCM format the data is transferred 4 bytes at a time. Each four byte word transferred, decrements the DMA Current Count register. The Base registers must be loaded with the number of BYTES to be transferred between "DMA interrupts", divided by four, minus one. The same calculation is used whether the data format is stereo or mono ADPCM. The 4-byte word contains 8 mono ADPCM samples or 4 stereo ADPCM samples. The equation for loading the DMA Base registers is:

DMA Base register$_{16}$ = N$_b$/4 - 1

Where N$_b$ is the number of BYTES transferred between interrupts and the "DMA Base register$_{16}$" consists of the concatenation of the upper and lower DMA Base registers.

Playback DMA Registers

The playback DMA registers (I14/15) are used for sending playback data to the DACs in MODE 2. In MODE 1 or when SDC = 1, these registers (I14/15) are used for both playback and capture.

When the playback Current Count register rolls under, the Playback Interrupt bit, PI, (I24) is set causing the INT bit (R2) to be set. The interrupt is cleared by a write of any value to the Status register (R2), or writing a "0" to the Playback Interrupt bit, PI (I24). When SDC = 1, PI reflects the status of I14/I15 for both playback and capture.

Capture DMA Registers

The Capture DMA Base registers (I30/31) provide a second pair of Base registers that allow full-duplex DMA operation. With full-duplex operation, capture and playback can occur simultaneously utilizing different DMA channels. These registers are only used in MODE 2 with SDC = 0. If SDC in I9 is set, I14/I15 are used for Capture DMA Base registers.

When the capture Current Count register rolls under, the Capture Interrupt bit, CI, (I24) is set causing the INT bit (R2) to be set. The interrupt is cleared by a write of any value to the Status register (R2), or by writing a "0" to the Capture Interrupt bit, CI (I24). The CI bit is tied to the Capture DMA base registers; therefore, when SDC = 1, the CI bit is non-functional.

Digital Loopback

Digital Loopback is enabled via the LBE bit in the Loopback Control register (I13). This loopback routes the digital data from the ADCs to the DACs. This loopback can be digitally attenuated via additional bits in the Loopback Control register (I13). Loopback is then summed with DAC data supplied at the digital bus interface. When loopback is enabled, it will "freerun" synchronous with the sample rate. The digital loopback is shown in the CS4231A Block Diagram on the front cover. This loopback can be

used to mix the incoming microphone data with data from the DACs. Since the CS4231A allows selection of different data formats between capture and playback, if the capture channel is set to mono and the playback channel set to stereo, the mono input (mic) data will be mixed into both channels of the output mixer.

If the sum of the loopback and bus data are greater than full scale, CS4231A will send the appropriate full scale value to the DACs (clipping).

Timer Registers

The Timer Base registers are provided for synchronization, watch dog, and other functions where a high resolution time reference is required. This counter is 16 bits and the exact time base, listed in the register description, is determined by the crystal selected.

When the Timer Enable bit TE, in the Alternate Feature Enable register (I16) is clear, the timer does not count. The Timer is set by loading the Upper and then the Lower Base register to the appropriate values and setting TE. When the Timer Lower Base register (I20) is loaded, the entire 16-bit value is loaded into an internal Current Count register which is decremented at approximately a 10 μsec rate. When the value of the Current Count register reaches zero, the Timer Interrupt bit, TI, in I24 is set, and and interrupt is generated if the INT bit (R2) is set. On the next timer clock, the value of the Timer Base registers are automatically loaded into the internal Current Count register which begin counting to zero again. The interrupt is cleared by any write to the Status register (R2) or by writing a "0" to the Timer Interrupt bit, TI, in the Alternate Feature Status register (I24). Since the timer will continue counting down while an interrupt is pending, interrupts will be generated at fixed time intervals regardless of the time required to service the interrupt (assuming the interrupt is

serviced before the next timer interrupt is generated).

Interrupts

The INT bit of the Status register (R2) always reflects the status of the CS4231A internal interrupt state. A roll-over from any Current Count register (DMA playback, DMA capture, or Timer) sets the INT bit. This bit remains set until cleared by a write of ANY value to Status register (R2), or by clearing the appropriate bit or bits (PI, CI, TI) in the Alternate Feature Status register (I24).

The Interrupt Enable (IEN) bit in the Pin Control register (I10) determines whether the interrupt pin responds to the interrupt event in the CS4231A. When the IEN bit is 0, the interrupt is masked and the IRQ pin of the CS4231A is forced low. However, the INT bit in the Status register (R2) always responds to the counter.

Error Conditions

Data overrun or underrun could occur if data is not supplied to or read from the CS4231A in the appropriate amount of time. The amount of time for such data transfers depends on the frequency selected within the CS4231A.

Should an overrun condition occur during data capture, the last whole sample (before the overrun condition) will be read by the DMA interface. A sample will not be overwritten while the DMA interface is in the process of transferring the sample.

Should an underrun condition occur in a playback case, the last valid sample will be output (assuming DACZ = 0) to the DACs which will mask short duration error conditions. When the next complete sample arrives from the host computer the data stream will resume on the next sample clock.

CS4231A REGISTER MAPPING

	Addr.	Register Name
R0	0	Index Address register
R1	1	Indexed Data register
R2	2	Status register
R3	3	PIO Data register

Table 1. Direct Registers

The two address pins of the CS4231A allow access to four 8-bit registers. Two of these registers provide indirect access to more CS4231A registers via an index register. The other two registers provide status information and allow audio data to be transferred to and from the CS4231A without using DMA cycles or indexing.

Physical Mapping

The PIO registers are I/O mapped via four locations. Two address pins provide access to all of the CS4231A's registers. The four direct registers are shown in Table 1. The first two direct registers are used to access 32 indirect registers shown in Table 2. As indicated by the arrows, the Index Address register (R0) points to the indirect register that is accessed through the Indexed Data register (R1).

This section describes all the direct and indirect registers. Table 3 details a summary of each bit in each register with Tables 4 through 10 illustrating the majority of decoding needed when programming the CS4231A and are included for reference. Tables 4 through 8 indicate gain settings at internal nodes. If OLB= 1 then the output will reflect the gain setting. If OLB= 0, the output will be attenuated by 3 dB as indicated in the specifications. The CS4231A powers up into the reset state which is defined as MODE 1. MODE 1 is backwards compatible with the CS4248 and only allows access to the first 16 indirect registers. Setting the MODE2 bit in the MODE and ID register (I12) enables

MODE 2 which allows access to indirect registers 16 through 31 and enables all the features of the CS4231A.
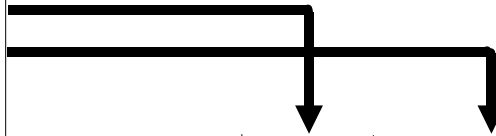
Index	Register Name
I0	Left ADC Input Control
I1	Right ADC Input Control
I2	Left Aux #1 Input Control
I3	Right Aux #1 Input Control
I4	Left Aux #2 Input Control
I5	Right Aux #2 Input Control
I6	Left DAC Output Control
I7	Right DAC Output Control
I8	Fs & Playback Data Format
I9	Interface Configuration
I10	Pin Control
I11	Error Status and Initialization
I12	MODE and ID (MODE2 bit)
I13	Loopback Control
I14	Playback Upper Base Count
I15	Playback Lower Base Count
I16	Alternate Feature Enable I
I17	Alternate Feature Enable II
I18	Left Line Input Control
I19	Right Line Input Control
I20	Timer Low Base
I21	Timer High Base
I22	RESERVED
I23	Alternate Feature Enable III
I24	Alternate Feature Status
I25	Version / Chip ID
I26	Mono Input & Output Control
I27	RESERVED
I28	Capture Data Format
I29	RESERVED
I30	Capture Upper Base Count
I31	Capture Lower Base Count

Table 2. Indirect Registers

Index Address Register (R0)

D7	D6	D5	D4	D3	D2	D1	D0
INIT	MCE	TRD	IA4	IA3	IA2	IA1	IA0

IA3-IA0   Index Address: These bits define the address of the CS4231A register accessed by the Indexed Data register (R1). These bits are read/write.

IA4   Allows access to indirect registers 16 - 31. Only available in MODE 2. In MODE 1,this bit is reserved.

TRD   Transfer Request Disable: This bit, when set, causes DMA transfers to cease when the INT bit of the status register is set. Independent for playback and capture interrupts.

         0 - Transfers Enabled (PDRQ and CDRQ occur uninhibited)
         1 - Transfers Disabled (PDRQ and CDRQ only occur if INT bit is 0)

MCE   Mode Change Enable: This bit must be set whenever the sample frequency,D3-D0 of I8, or the Interface Configuration (I9) register is changed. The exceptions are CEN and PEN which can be changed "on-the-fly". The DAC output is muted when MCE is set. MCE or PMCE (I16) may be used to changed the playback data format, D7-D3 of I8. MCE or CMCE (I16) may be used to change the capture data format, D7-D3 of I28.

INIT   CS4231A Initialization: This bit is read as 1 when the CS4231A is in a state in which it cannot respond to parallel interface cycles. This bit is read-only.

Immediately after RESET (and once the CS4231A has left the INIT state), the state of this register is: 010x0000

During initialization and power down, this register CANNOT be written and always reads 10000000 (80h)

Indexed Data Register (R1)

D7	D6	D5	D4	D3	D2	D1	D0
ID7	ID6	ID5	ID4	ID3	ID2	ID1	ID0

ID7-ID0   Indexed Data register: These bits are the indirect register referenced by the Indexed Address register (R0).

During initialization and power down, this register can NOT be written and is always read 10000000 (80h)

Status Register (R2, Read Only)

D7	D6	D5	D4	D3	D2	D1	D0
CU/L	CL/R	CRDY	SER	PU/L	PL/R	PRDY	INT

INT   Interrupt Status: This indicates the status of the internal interrupt logic of the CS4231A. This bit is cleared by any write of any value to this register. The IEN bit of the Pin Control register (I10) determines whether the state of this bit is reflected on the IRQ pin of the CS4231A. Read States

         0 - Interrupt inactive
         1 - Interrupt active

PRDY   Playback Data Ready. The Playback Data register (R3) is ready for more data. This bit would be used when direct programmed I/O data transfers are desired.

         0 - Data still valid. Do not overwrite.
         1 - Data stale. Ready for next host data write value.

PL/R̄   Playback Left/Right Sample: This bit indicates whether data needed is for the Left channel or Right channel in all audio data formats except ADPCM. In ADPCM it indicates whether the first two or last two bytes of a 4-byte set (8 ADPCM samples) is needed.

         0 - Right or 3/4 ADPCM byte needed
         1 - Left, Mono, or 1/2 ADPCM byte needed

PU/L̄   Playback Upper/Lower Byte: This bit indicates whether the playback data needed is for the upper or lower byte of the channel. In ADPCM it indicates, along with PL/R̄, which one of four ADPCM bytes is needed.

0 - Lower or 1/3 ADPCM byte needed
1 - Upper, any 8-bit mode, or 2/4 ADPCM byte needed

SER   Sample Error: This bit indicates that a sample was not serviced in time and an error has occurred. The bit indicates an overrun for capture and underrun for playback. If both the capture and playback are enabled, the source which set this bit can not be determined. However, the Alternate Feature Status register (I24) can indicate the exact source of the error.

CRDY   Capture Data Ready. The Capture Data register (R3) contains data ready for reading by the host. This bit would be used for direct programmed I/O data transfers.

0 - Data is stale. Do not reread the information.
1 - Data is fresh. Ready for next host data read.

CL/R̄   Capture Left/Right Sample: This bit indicates whether the capture data waiting is for the Left channel or Right channel in all audio data formats except ADPCM. In ADPCM it indicates whether the first two or last two bytes of a 4-byte set (8 ADPCM samples) is waiting.

0 - Right or 3/4 ADPCM byte waiting
1 - Left, Mono, or 1/2 ADPCM byte waiting

CU/L̄   Capture Upper/Lower Byte: This bit indicates whether the capture data ready is for the upper or lower byte of the channel. In ADPCM it indicates, along with CL/R̄, which one of four ADPCM bytes is waiting.

0 - Lower or 1/3 ADPCM byte waiting
1 - Upper, any 8-bit mode, or 2/4 ADPCM byte waiting

Note on PRDY/CRDY: These two bits are designed to be read as one when action is required by the host. For example, when PRDY is set to one, the device is ready for more data; or when the CRDY is set to one, data is available to the host. The definition of the CRDY and PRDY bits are therefore consistent in this regard.

I/O Data Registers

The PIO Data register is two registers mapped to the same address. Writes to this register send data to the Playback Data register. Reads from this register will receive data from the Capture Data register.

During initialization and power down, this register CANNOT be written and is always read 10000000 (80h)

Capture I/O Data Register (R3, Read Only)

D7	D6	D5	D4	D3	D2	D1	D0
CD7	CD6	CD5	CD4	CD3	CD2	CD1	CD0

CD7-CD0   Capture Data Port. This is the control register where capture data is read during programmed I/O data transfers.

The reading of this register will increment the state machine so that the following read will be from the next appropriate byte in the sample. The exact byte which is next to be read can be determined by reading the Status register (R2). Once all relevant bytes have been read, the state machine will point to the last byte of the sample. Once the Status register (R2) is read and a new sample is received from the FIFO, the state machine and Status register (R2) will point to the first byte of the new sample.

During initialization and power down, this register can NOT be written and is always read 10000000 (80h)

Playback I/O Data Register (R3, Write Only)

D7	D6	D5	D4	D3	D2	D1	D0
PD7	PD6	PD5	PD4	PD3	PD2	PD1	PD0

PD7-PD0　　Playback Data Port. This is the control register where playback data is written during programmed IO data transfers.

Writing data to this register will increment the playback byte tracking state machine so that the following write will be to the correct byte of the sample. Once all bytes of a sample have been written, subsequent byte writes to this port are ignored. The state machine is reset after the Status register (R2) is read and the current sample is sent to the DACs via the FIFOs.

Indirect Mapped Registers

These registers are accessed by placing the appropriate index in the Index Address register (R0) and then accessing the Indexed Data register (R1). All reserved bits should be written zero and may be 0 or 1 when read. Indirect registers 16-31 are only available when the MODE2 bit in MODE and ID register (I12) is set.

Left ADC Input Control (I0)

D7	D6	D5	D4	D3	D2	D1	D0
LSS1	LSS0	LMGE	res	LAG3	LAG2	LAG1	LAG0

LAG3-LAG0　　Left ADC Gain. The least significant bit represents +1.5 dB, with 0000 = 0 dB. See Table 4.

LMGE　　Left Mic Gain Enable: This bit enables the 20 dB gain stage of the left mic input signal, LMIC.

LSS1-LSS0　　Left ADC Input Source Select. These bits select the input source for the left ADC channel.

0 - Left Line: LLINE
1 - Left Auxiliary 1: LAUX1
2 - Left Microphone: LMIC
3 - Left Line Output Loopback

This register's initial state after reset is: 000x0000

Right ADC Input Control (I1)

D7	D6	D5	D4	D3	D2	D1	D0
RSS1	RSS0	RMGE	res	RAG3	RAG2	RAG1	RAG0

RAG3-RAG0　　Right ADC Gain. The least significant bit represents +1.5 dB, with 0000 = 0 dB. See Table 4.

RMGE　　Right Mic Gain Enable: This bit enables the 20 dB gain stage of the right mic input signal, RMIC.

RSS1-RSS0　　Right ADC Input Select. These bits select the input source for the right ADC channel.

0 - Right Line: RLINE
1 - Right Auxiliary 1: RAUX1
2 - Right Microphone: RMIC
3 - Right Line Out Loopback

This register's initial state after reset is: 000x0000

Left Auxiliary #1 Input Control (I2)

D7	D6	D5	D4	D3	D2	D1	D0
LX1M	res	res	LX1G4	LX1G3	LX1G2	LX1G1	LX1G0

LX1G4-LX1G0　　Left Auxiliary #1, LAUX1, Mix Gain. The least significant bit represents 1.5 dB, with 01000 = 0 dB. See Table 5.

LX1M　　Left Auxiliary #1 Mute. When set to 1, the left Auxiliary #1 input, LAUX1, to the mixer, is muted.

This register's initial state after reset is: 1xx01000.

Right Auxiliary #1 Input Control (I3)

D7	D6	D5	D4	D3	D2	D1	D0
RX1M	res	res	RX1G4	RX1G3	RX1G2	RX1G1	RX1G0

RX1G4-RX1G0   Right Auxiliary #1, RAUX1, Mix Gain. The least significant bit represents 1.5 dB, with 01000 = 0 dB. See Table 5.

RX1M   Right Auxiliary #1 Mute. When set to 1, the right Auxiliary #1 input, RAUX1, to the mixer, is muted.

This register's initial state after reset is: 1xx01000.

Left Auxiliary #2 Input Control (I4)

D7	D6	D5	D4	D3	D2	D1	D0
LX2M	res	res	LX2G4	LX2G3	LX2G2	LX2G1	LX2G0

LX2G4-LX2G0   Left Auxiliary #2, LAUX2, Mix Gain. The least significant bit represents 1.5 dB, with 01000 = 0 dB. See Table 5.

LX2M   Left Auxiliary #2 Mute. When set to 1, the left Auxiliary #2 input, LAUX2, to the mixer, is muted.

This register's initial state after reset is: 1xx01000.

Right Auxiliary #2 Input Control (I5)

D7	D6	D5	D4	D3	D2	D1	D0
RX2M	res	res	RX2G4	RX2G3	RX2G2	RX2G1	RX2G0

RX2G4-RX2G0   Right Auxiliary #2, RAUX2, Mix Gain. The least significant bit represents 1.5 dB, with 01000 = 0 dB. See Table 5.

RX2M   Right Auxiliary #2 Mute. When set to 1, the right Auxiliary #2 input, RAUX2, to the mixer, is muted.

This register's initial state after reset is: 1xx01000.

Left DAC Output Control (I6)

D7	D6	D5	D4	D3	D2	D1	D0
LDM	res	LDA5	LDA4	LDA3	LDA2	LDA1	LDA0

LDA5-LDA0   Left DAC Attenuator. The least significant bit represents -1.5 dB, with 000000 = 0 dB. See Table 6.

LDM   Left DAC Mute. When set to 1, the left DAC output to the mixer will be muted.

This register's initial state after reset is: 1x000000.

Right DAC Output Control (I7)

D7	D6	D5	D4	D3	D2	D1	D0
RDM	res	RDA5	RDA4	RDA3	RDA2	RDA1	RDA0

RDA5-RDA0   Right DAC Attenuator. The least significant bit represents -1.5 dB, with 000000 = 0 dB. See Table 6.

RDM   Right DAC Mute. When set to 1, the right DAC output to the mixer will be muted.

This register's initial state after reset is: 1x000000.

Fs and Playback Data Format (I8)

D7	D6	D5	D4	D3	D2	D1	D0
FMT1	FMT0	C/L̄	S/M̄	CSF2	CFS1	CFS0	C2SL

C2SL   Clock 2 Source Select: This bit selects the clock source used for the audio sample rates for both capture and playback. If only one crystal is supplied in hardware, it must be XTAL1. CAUTION: C2SL can only be changed while MCE (R0) is set.

        0 - XTAL1   Typically 24.576 MHz
        1 - XTAL2   Typically 16.9344 MHz

CFS2-CFS0   Clock Frequency Divide Select: These bits select the audio sample frequency for both capture and playback. The actual audio sample frequency depends on which clock source (C2SL) is selected and its frequency. Frequencies listed as N/A are not available because their sample frequency violates the maximum specifications; however, the decodes are available and may be used with crystals that do not violate the sample frequency specifications. CAUTION: CFS2-CFS0 can only be changed while MCE (R0) is set.

	XTAL1	XTAL2
Divide	24.576 MHz	16.9344 MHz
0 - 3072	8.0 kHz	5.51 kHz
1 - 1536	16.0 kHz	11.025 kHz
2 - 896	27.42 kHz	18.9 kHz
3 - 768	32.0 kHz	22.05 kHz
4 - 448	N/A	37.8 kHz
5 - 384	N/A	44.1 kHz
6 - 512	48.0 kHz	33.075 kHz
7 - 2560	9.6 kHz	6.62 kHz

S/M̄   Stereo/Mono Select: This bit determines how the audio data streams are formatted. Selecting stereo will result in alternating samples representing left and right audio channels. Mono playback plays the same audio sample on both channels. Mono capture only captures data from the left channel. In MODE 1, this bit is used for both playback and capture. In MODE 2, this bit is only used for playback, and the capture format is independently selected via I28. MCE (R0) or PMCE (I16) must be set to modify S/M̄. See *Changing Audio Data Formats* section for more details.

        0 - Mono
        1 - Stereo

The C/L̄, FMT1, and FMT0 bits set the audio data format as shown below. In MODE 1, FMT1, which is forced low, FMT0, and C/L̄ are used for both playback and capture. In MODE 2, these bits are only used for playback, and the capture format is independently selected via register I28. MCE (R0) or PMCE (I16) must be set to modify the lower four bits of this register. See *Changing Audio Data Formats* section for more details.

FMT1† D7	FMT0 D6	C/L̄ D5	
0	0	0	Linear, 8-bit unsigned
0	0	1	μ-Law, 8-bit companded
0	1	0	Linear, 16-bit two's complement, Little Endian
0	1	1	A-Law, 8-bit companded
1	0	0	RESERVED
1	0	1	ADPCM, 4-bit, IMA compatible
1	1	0	Linear, 16-bit two's complement, Big Endian
1	1	1	RESERVED

† FMT1 is not available in MODE 1 (forced to 0).

This register's initial state after reset is: 0000000.

Interface Configuration (I9)

D7	D6	D5	D4	D3	D2	D1	D0
CPIO	PPIO	res	CAL1	CAL0	SDC	CEN	PEN

PEN   Playback Enable. This bit enables playback. The CS4231A will generate PDRQ and respond to PDAK signals when this bit is enabled and PPIO=0. If PPIO=1, PEN enables PIO playback mode. PEN may be set and reset without setting the MCE bit.

      0 - Playback Disabled (PDRQ and PIO inactive)
      1 - Playback Enabled

CEN   Capture Enabled. This bit enables the capture of data. The CS4231A will generate CDRQ and respond to CDAK signals when CEN is enabled and CPIO=0. If CPIO=1, CEN enables PIO capture mode. CEN may be set and reset without setting the MCE bit.

      0 - Capture disabled (CDRQ and PIO inactive)
      1 - Capture enabled

SDC   Single DMA Channel: This bit will force BOTH capture and playback DMA requests to occur on the Playback DMA channel. The Capture DMA CDRQ pin will be zero. This bit forces the CS4231A to use one DMA channel. Should both capture and playback be enabled in this mode, only the playback will occur. See the DMA section for further explanation.

      0 - Dual DMA channel mode
      1 - Single DMA channel mode

CAL1,0   Calibration: These bits determine which type of calibration the CS4231A performs whenever the Mode Change Enable (MCE) bit, R0, changes from 1 to 0. The number of sample periods required for calibration is listed in parenthesis.

      0 - No calibration (0, 40 the first time)
      1 - Converter calibration (136)
      2 - DAC calibration (40)
      3 - Full Calibration (168)

PPIO   Playback PIO Enable: This bit determines whether the playback data is transferred via DMA or PIO.

      0 - DMA transfers
      1 - PIO transfers

CPIO   Capture PIO Enable: This bit determines whether the capture data is transferred via DMA or PIO.

      0 - DMA transfers
      1 - PIO transfers

CAUTION: This register, except bits CEN and PEN, can only be written while in Mode Change Enable (either MCE or PMCE). See *Changing Sampling Rate* section for more details.

This register's initial state after reset is: 00x01000

Pin Control (I10)

D7	D6	D5	D4	D3	D2	D1	D0
XCTL1	XCTL0	res	res	DEN	res	IEN	res

IEN   Interrupt Enable: This bit enables the interrupt pin. The Interrupt pin will reflect the value of the INT bit of the Status register (R2). The interrupt pin is active high.

          0 - Interrupt disabled
          1 - Interrupt enabled

DEN   Dither Enable: When set, triangular pdf dither is added before truncating the ADC 16-bit value to 8-bit, unsigned data. Dither is only active in the 8-bit unsigned mode.

          0 - Dither disabled
          1 - Dither enabled

XCTL1-XCTL0 XCTL Control: These bits are reflected on the XCTL1,0 pins of the CS4231A.

          0 - TTL logic low on XCTL1,0 pins
          1 - TTL logic high on XCTL1,0 pins

This registers initial state after reset is: 00xx0x0x

Error Status and Initialization (I11, Read Only)

D7	D6	D5	D4	D3	D2	D1	D0
COR	PUR	ACI	DRS	ORR1	ORR0	ORL1	ORL0

ORL1-ORL0   Overrange Left Detect: These bits determine the overrange on the left ADC channel. These bits are updated on a sample by sample basis.

          0 - Less than -1.5 dB from full scale
          1 - Between -1.5 dB and 0 dB
          2 - Between 0 dB and 1.5 dB
             overrange
          3 - Greater than 1.5 dB overrange

ORR1-ORR0   Overrange Right Detect: These bits determine the overrange on the Right ADC channel.

          0 - Less than -1.5 dB from full scale
          1 - Between -1.5 dB and 0 dB
          2 - Between 0 dB and 1.5 dB
             overrange
          3 - Greater than 1.5 dB overrange

DRS   DRQ Status: This bit indicates the current status of the PDRQ and CDRQ pins of the CS4231A.

          0 - CDRQ AND PDRQ are presently
             inactive
          1 - CDRQ OR PDRQ are presently
             active

ACI   Auto-calibrate In-Progress: This bit indicates the state of calibration. The length of time high is dependent on the calibration mode selected.

          0 - Calibration not in progress
          1 - Calibration is in progress

PUR   Playback underrun: This bit is set when playback data has not arrived from the host in time to be played. As a result, if DACZ = 0, the last valid sample will be sent to the DACs. This bit is set when an error occurs and is cleared when the Status register (R2) is read.

COR   Capture overrun: This bit is set when the capture data has not been read by the host before the next sample arrives. The old sample will not be overwritten and the new sample will be ignored. This bit is set when an error condition occurs and is cleared when the Status register (R2) is read.

The SER bit in the Status register (R2) is simply a logical OR of the COR and PUR bits. This enables a polling host CPU to detect an error condition while checking other status bits.

This register's initial state after reset is: 00000000

MODE and ID (I12)

D7	D6	D5	D4	D3	D2	D1	D0
1	MODE2	res	res	ID3	ID2	ID1	ID0

ID3-ID0   Codec ID: These four bits indicate the ID of the codec. Revisions are contained in indirect register 25. These bits are read only.

                            1010

MODE2   MODE 2: Enables the expanded mode of the CS4231A. Must be set to enable access to indirect registers 16-31 and their associated features.

                            0 - MODE 1: CS4248 "look-alike".
                            1 - MODE 2: Expanded features.

This register's initial state after reset is: 10xx1010

Loopback Control (I13)

D7	D6	D5	D4	D3	D2	D1	D0
LBA5	LBA4	LBA3	LBA2	LBA1	LBA0	res	LBE

LBE   Loopback Enable: When set to 1, the ADC data is digitally mixed with data sent to the DACs.

                            0 - Loopback disabled
                            1 - Loopback enabled

LBA5-LBA0   Loopback Attenuation: These bits determine the attenuation of the loopback from ADC to DAC. The least significant bit represents -1.5 dB, with 000000 = 0 dB. See Table 6.

This register's initial state after reset is: 000000x0

Playback Upper Base (I14)

D7	D6	D5	D4	D3	D2	D1	D0
PUB7	PUB6	PUB5	PUB4	PUB3	PUB2	PUB1	PUB0

PUB7-PUB0   Playback Upper Base: This register is the upper byte which represents the 8 most significant bits of the 16-bit Playback Base register. Reads from this register return the same value which was written. The Current Count registers cannot be read. When set for MODE 1 or SDC, this register is used for both the Playback and Capture Base registers.

This register's initial state after reset is: 0000000

Playback Lower Base (I15)

D7	D6	D5	D4	D3	D2	D1	D0
PLB7	PLB6	PLB5	PLB4	PLB3	PLB2	PLB1	PLB0

PLB7-PLB0   Lower Base Bits: This register is the lower byte which represents the 8 least significant bits of the 16-bit Playback Base register. Reads from this register return the same value which was written. When set for MODE 1 or SDC, this register is used for both the Playback and Capture Base registers.

This register's initial state after reset is: 00000000

Alternate Feature Enable I (I16)

D7	D6	D5	D4	D3	D2	D1	D0
OLB	TE	CMCE	PMCE	SF1	SF0	SPE	DACZ

DACZ   DAC Zero: This bit will force the output of the playback channel to AC zero when an underrun error occurs

     1 - Go to center scale
     0 - Hold previous valid sample

SPE   Serial Port Enable. When enabled, audio data from the ADCs is sent out SDOUT and audio data from SDIN is sent to the DACs. MCE must be set before this bit can be changed.

     1 - Enable serial port
     0 - Disable serial port. Parallel port used for audio data.

SF1,SF0   Serial Format. Selects the format of the serial port when enabled by SPE. MCE must be set before these bits can be changed.

     0 - 64-bit enhanced
     1 - 64-bit
     2 - 32-bit
     3 - Reserved.

PMCE   Playback Mode Change Enable. When set, it allows modification of the stereo/mono and audio data format bits (D7-D4) for the playback channel, I8. MCE in R0 must be used to change the sample frequency.

CMCE   Capture Mode Change Enable. When set, it allows modification of the stereo/mono and audio data format bits (D7-D4) for the capture channel, I28. MCE in R0 must be used to change the sample frequency.

TE   Timer Enable: This bit, when set, will enable the timer to run and interrupt the host at the specified frequency in the timer registers.

     0 - Timer Disabled - Does not count
     1 - Timer Enabled - Counts down

OLB   Output Level Bit: Sets the analog output level. When clear, analog line outputs are attenuated 3 dB.

     0 - Full scale of 2 Vpp (-3 dB)
     1 - Full scale of 2.8 Vpp (0 dB)

This register's initial state after reset is: 00000000

Alternate Feature Enable II (I17)

D7	D6	D5	D4	D3	D2	D1	D0
TEST	TEST	TEST	TEST	res	APAR	XTALE	HPF

HPF   High Pass Filter: This bit enables a DC-blocking high-pass filter in the digital filter of the ADC. This filter forces the ADC offset of 0.

     0 - disabled
     1 - enabled

XTALE   Crystal Enable. When set, both crystals are always active. When clear, only the crystal selected by C2SL, I8, is active with the other crystal powered down. This bit is normally set when working with games software that switch sample frequencies often.

APAR   ADPCM Playback Accumulator Reset. While set, the Playback ADPCM accumulator is held at zero. Used when pausing a playback stream.

TEST   Factory Test. These bits are used for factory testing and must remain at 0 for normal operation.

This register's initial state after reset is: 0000x000.

Left Line Input Control (I18)

D7	D6	D5	D4	D3	D2	D1	D0
LLM	res	res	LLG4	LLG3	LLG2	LLG1	LLG0

LLG4-LLG0   Left Line, LLINE, Mix Gain. The least significant bit represents 1.5 dB, with 01000 = 0 dB. See Table 5.

LLM   Left Line Mute. When set to 1, the left Line input, LLINE, to the mixer, is muted.

This register's initial state after reset is: 1xx01000.

Direct Registers: (R0-R3)

	A1	A0	D7	D6	D5	D4	D3	D2	D1	D0
R0	0	0	INIT	MCE	TRD	IA4†	IA3	IA2	IA1	IA0
R1	0	1	ID7	ID6	ID5	ID4	ID3	ID2	ID1	ID0
R2	1	0	CU/L̄	CL/R̄	CRDY	SER	PU/L̄	PL/R̄	PRDY	INT
R3	1	1	CD7	CD6	CD5	CD4	CD3	CD2	CD1	CD0
R3	1	1	PD7	PD6	PD5	PD4	PD3	PD2	PD1	PD0

Indirect Registers: (I0-I31)

IA4-IA0	D7	D6	D5	D4	D3	D2	D1	D0
0	LSS1	LSS0	LMGE	-	LAG3	LAG2	LAG1	LAG0
1	RSS1	RSS0	RMGE	-	RAG3	RAG2	RAG1	RAG0
2	LX1M	-	-	LX1G4	LX1G3	LX1G2	LX1G1	LX1G0
3	RX1M	-	-	RX1G4	RX1G3	RX1G2	RX1G1	RX1G0
4	LX2M	-	-	LX2G4	LX2G3	LX2G2	LX2G1	LX2G0
5	RX2M	-	-	RX2G4	RX2G3	RX2G2	RX2G1	RX2G0
6	LDM	-	LDA5	LDA4	LDA3	LDA2	LDA1	LDA0
7	RDM	-	RDA5	RDA4	RDA3	RDA2	RDA1	RDA0
8 §	FMT1†	FMT0	C/L̄	S/M̄	CSF2	CSF1	CSF0	C2SL
9 §	CPIO	PPIO	-	CAL1	CAL0	SDC	CEN	PEN
10	XCTL1	XCTL0	-	-	DEN	-	IEN	-
11	COR	PUR	ACI	DRS	ORR1	ORR0	ORL1	ORL0
12	1	MODE2	-	-	ID3	ID2	ID1	ID0
13	LBA5	LBA4	LBA3	LBA2	LBA1	LBA0	-	LBE
14 *	PUB7	PUB6	PUB5	PUB4	PUB3	PUB2	PUB1	PUB0
15 *	PLB7	PLB6	PLB5	PLB4	PLB3	PLB2	PLB1	PLB0
16 §	OLB	TE	CMCE	PMCE	SF1	SF0	SPE	DACZ
17	TEST	TEST	TEST	TEST	-	APAR	XTALE	HPF
18	LLM	-	-	LLG4	LLG3	LLG2	LLG1	LLG0
19	RLM	-	-	RLG4	RLG3	RLG2	RLG1	RLG0
20	TL7	TL6	TL5	TL4	TL3	TL2	TL1	TL0
21	TU7	TU6	TU5	TU4	TU3	TU2	TU1	TU0
22	-	-	-	-	-	-	-	-
23	-	-	-	-	-	-	-	ACF
24	-	TI	CI	PI	CU	CO	PO	PU
25	V2	V1	V0	-	-	CID2	CID1	CID0
26	MIM	MOM	MBY	-	MIA3	MIA2	MIA1	MIA0
27	-	-	-	-	-	-	-	-
28 §	FMT1	FMT0	C/L̄	S/M̄	-	-	-	-
29	-	-	-	-	-	-	-	-
30	CUB7	CUB6	CUB5	CUB4	CUB3	CUB2	CUB1	CUB0
31	CLB7	CLB6	CLB5	CLB4	CLB3	CLB2	CLB1	CLB0

† IA4 and FMT2 bits are only available in MODE 2 (I12, bit 6 = 1). In MODE1, IA4 is forced to 0.

* When in MODE 1, the playback base registers (upper and lower) are used for both playback and capture.

§ In I8, MCE must be set to modify the lower 4 bits. MCE or PMCE must be set to modify the upper 4 bits.
In I9, MCE must be set to modify the upper 6 bits. PEN and CEN can be changed anytime.
In I16, MCE must be set to modify the serial port bits: SF1, SF0, and SPE.
In I28, MCE or CMCE must be set to modify the upper 4 bits.

Table 3. Register Bit Summary

NOTE: Output level relative to input level assuming OLB=1.

	AG3	AG2	AG1	AG0	Level
0	0	0	0	0	0.0 dB
1	0	0	0	1	1.5 dB
2	0	0	1	0	3.0 dB
3	0	0	1	1	4.5 dB
.			.		.
.			.		.
.			.		.
12	1	1	0	0	18.0 dB
13	1	1	0	1	19.5 dB
14	1	1	1	0	21.0 dB
15	1	1	1	1	22.5 dB

Table 4. ADC Input Gain

	A5	A4	A3	A2	A1	A0	Level
0	0	0	0	0	0	0	0.0 dB
1	0	0	0	0	0	1	-1.5 dB
2	0	0	0	0	1	0	-3.0 dB
3	0	0	0	0	1	1	-4.5 dB
.			.			.
.			.			.
.			.			.
60	1	1	1	1	0	0	-90.0 dB
61	1	1	1	1	0	1	-91.5 dB
62	1	1	1	1	1	0	-93.0 dB
63	1	1	1	1	1	1	-94.5 dB

Table 6. DAC & Loopback Attenuation

	G4	G3	G2	G1	G0	Level
0	0	0	0	0	0	12.0 dB
1	0	0	0	0	1	10.5 dB
2	0	0	0	1	0	9.0 dB
3	0	0	0	1	1	7.5 dB
4	0	0	1	0	0	6.0 dB
5	0	0	1	0	1	4.5 dB
6	0	0	1	1	0	3.0 dB
7	0	0	1	1	1	1.5 dB
8	**0**	**1**	**0**	**0**	**0**	**0.0 dB**
9	0	1	0	0	1	-1.5 dB
10	0	1	0	1	0	-3.0 dB
11	0	1	0	1	1	-4.5 dB
12	0	1	1	0	0	-6.0 dB
.		.			.
.		.			.
.		.			.
24	1	1	0	0	0	-24.0 dB
25	1	1	0	0	1	-25.5 dB
26	1	1	0	1	0	-27.0 dB
27	1	1	0	1	1	-28.5 dB
28	1	1	1	0	0	-30.0 dB
29	1	1	1	0	1	-31.5 dB
30	1	1	1	1	0	-33.0 dB
31	1	1	1	1	1	-34.5 dB

Table 5. AUX1 & AUX2 & LINE Mixer Gain

	CFS2	CFS1	CFS0	XTAL1 24.576 MHz	XTAL2 16.9344MHz
0	0	0	0	8.0 kHz	5.51 kHz
1	0	0	1	16.0 kHz	11.025 kHz
2	0	1	0	27.42 kHz	18.9 kHz
3	0	1	1	32.0 kHz	22.05 kHz
4	1	0	0	N/A	37.8 kHz
5	1	0	1	N/A	44.1 kHz
6	1	1	0	48.0 kHz	33.075 kHz
7	1	1	1	9.6 kHz	6.62 kHz

Table 8. Sample Frequency Select

	MIA3	MIA2	MIA1	MIA0	Level
0	0	0	0	0	0.0 dB
1	0	0	0	1	-3.0 dB
2	0	0	1	0	-6.0 dB
3	0	0	1	1	-9.0 dB
.			.		.
.			.		.
.			.		.
12	1	1	0	0	-36.0 dB
13	1	1	0	1	-39.0 dB
14	1	1	1	0	-42.0 dB
15	1	1	1	1	-45.0 dB

Table 7. Mono Mixer Attenuation

	FMT1	FMT0	C/$\overline{\text{L}}$	Audio Data Format
0	0	0	0	Linear, 8-bit unsigned
1	0	0	1	μ-Law, 8-bit
2	0	1	0	Linear, 16-bit, 2's C, LEnd.
3	0	1	1	A-Law, 8-bit
5	1	0	1	ADPCM, 4-bit IMA
6	1	1	0	Linear, 16-bit, 2'sC, BEnd.

Table 10. Audio Data Format

	SS1	SS0	ADC Input Multiplexer
0	0	0	Line
1	0	1	Auxiliary 1
2	1	0	Microphone
3	1	1	Line Output Loopback

Table 9. ADC Input Selector

Right Line Input Control (I19)

D7	D6	D5	D4	D3	D2	D1	D0
RLM	res	res	RLG4	RLG3	RLG2	RLG1	RLG0

RLG4-RLG0   Right Line, RLINE, Mix Gain. The least significant bit represents 1.5 dB, with 01000 = 0 dB. See Table 5.

RLM   Right Line Mute. When set to 1, the Right Line input, RLINE, to the mixer, is muted.

This register's initial state after reset is: 1xx01000.

Timer Lower Base (I20)

D7	D6	D5	D4	D3	D2	D1	D0
TL7	TL6	TL5	TL4	TL3	TL2	TL1	TL0

TL7-TL0   Lower Timer Bits: This is the low order byte of the 16-bit timer base register. Writes to this register cause both timer base registers to be loaded into the internal timer; therefore, the upper timer register should be loaded before the lower. Once the count reaches zero, an interrupt is generated, if enabled, and the timer is automatically reloaded with these base registers.

This register's initial state after reset is: 00000000.

Timer Upper Base (I21)

D7	D6	D5	D4	D3	D2	D1	D0
TU7	TU6	TU5	TU4	TU3	TU2	TU1	TU0

TU7-TU0   Upper Timer Bits: This is the high order byte of the 16-bit timer. The time base is determined by the clock source selected from C2SL in I8:

C2SL = 0 - divide XTAL1 by 245 (24.576 MHz - 9.969 μs)

C2SL = 1 - divide XTAL2 by 168 (16.9344 MHz - 9.92 μs)

This register's initial state after reset is: 00000000

RESERVED (I22)

D7	D6	D5	D4	D3	D2	D1	D0
res	res	res	res	res	res	res	res

This register's initial state after reset is: xxxxxxxx

Alternate Feature Enable III (I23)

D7	D6	D5	D4	D3	D2	D1	D0
res	res	res	res	res	res	res	ACF

ACF   ADPCM Capture Freeze. When set, the capture ADPCM accumulator and step size are frozen. This bit must be clear for adaptation to continue. Used when pausing a capture stream.

This register's initial state after reset is: xxxxxxx0

Alternate Feature Status (I24)

D7	D6	D5	D4	D3	D2	D1	D0
res	TI	CI	PI	CU	CO	PO	PU

PU   Playback Underrun: This bit, when set, indicates that the DAC has run out of data and a sample has been missed.

PO   Playback Overrun: This bit, when set, indicates that the host attempted to write data into a full FIFO and the data was discarded.

CO   Capture Overrun: This bit, when set, indicates that the ADC had a sample to load into the FIFO but the FIFO was full. In this case the bit is set and the new sample is discarded.

CU   Capture Underrun: This bit indicates that the host has read more data out of the FIFO than it contained. In this condition, the bit is set and the last valid byte is read by the host.

PI   Playback Interrupt: This bit indicates that an interrupt is pending from the playback DMA count registers. When SDC = 1, this bit responds for both capture and playback.

CI   Capture Interrupt: This bit indicates that an interrupt is pending from the record DMA count registers. When SDC=1, this bit is non-functional.

TI   Timer Interrupt: This bit indicates that an interrupt is pending from the timer count registers

The PI, CI, and TI bits are reset by writing a "0" to the particular interrupt bit or by writing any value to the Status register (R2).

This register's initial state after reset is: x0000000

Version / ID (I25)

D7	D6	D5	D4	D3	D2	D1	D0
V2	V1	V0	res	res	CID2	CID1	CID0

V2-V0   Version number. As enhancements are made to the CS4231A, the version number is changed so software can distinguish between the different versions.

                       100 - All CS4231 revisions. See Appendix A.
                       101 - CS4231A. This Data Sheet.

CID2-CID0   Chip Identification. Distinguishes between this chip and future chips that support this register set.

                       000 - CS4231 or CS4231A

This register's initial state after reset is: 101xx000

Mono Input & Output Control (I26)

D7	D6	D5	D4	D3	D2	D1	D0
MIM	MOM	MBY	res	MIA3	MIA2	MIA1	MIA0

MIA3-MIA0   Mono Input Attenuation. When MIM is 0, these bits set the level of MIN summed into the mixer. MIA0 is the least significant bit and represents 3 dB attenuation, with 0000 = 0 dB. See Table 7.

MBY   Mono Bypass. MBY connects MIN directly to MOUT with an attenuation of 9 dB. When MBY = 1, MIM should be 1.

                       0 - MIM not connected directly to MOUT. Use MIM and MIA bits.
                       1 - MIN connected to MOUT directly.

MOM   Mono Output Mute. The MOM bit will mute the mono mix output, MOUT. This mute is independent of the line output mute.

                       0 - no mute
                       1 - mute

MIM Mono Input Mute. This bit controls the mute function on the mono input, MIN to the mixer. The mono input provides mix for the "beeper" function in most personal computers. When MIM = 0, MBY should be 0.

  0 - no mute
  1 - muted

This register's initial state after reset is: 101x0000.

RESERVED (I27)

D7	D6	D5	D4	D3	D2	D1	D0
res	res	res	res	res	res	res	res

This register's initial state after reset is: xxxxxxxx

Capture Data Format (I28)

D7	D6	D5	D4	D3	D2	D1	D0
FMT1	FMT0	C/$\overline{\text{L}}$	S/$\overline{\text{M}}$	res	res	res	res

S/$\overline{\text{M}}$ Stereo/Mono Select: This bit determines how the capture audio data stream is formatted. Selecting stereo will result with alternating samples representing left and right audio channels. Selecting mono only captures data from the left audio channel.

  0 - Mono
  1 - Stereo

The C/$\overline{\text{L}}$, FMT1, and FMT0 bits set the capture data format in MODE 2. See Table 10 or register I8 for the bit settings and data formats. The capture data format can be different that the playback data format; however, the sample frequency must be the same and is set in I8. MCE (R0) or CMCE (I16) must be set to modify this register. See *Changing Audio Data Formats* section for more details.

This register's initial state after reset is: 0000xxxx

RESERVED (I29)

D7	D6	D5	D4	D3	D2	D1	D0
res	res	res	res	res	res	res	res

This register's initial state after reset is: xxxxxxxx

Capture Upper Base (I30)

D7	D6	D5	D4	D3	D2	D1	D0
CUB7	CUB6	CUB5	CUB4	CUB3	CUB2	CUB1	CUB0

CUB7-CUB0 Capture Upper Base: This register is the upper byte which represents the 8 most significant bits of the 16-bit Capture Base register. Reads from this this register returns the same value that was written.

This register's initial state after reset is: 0000000
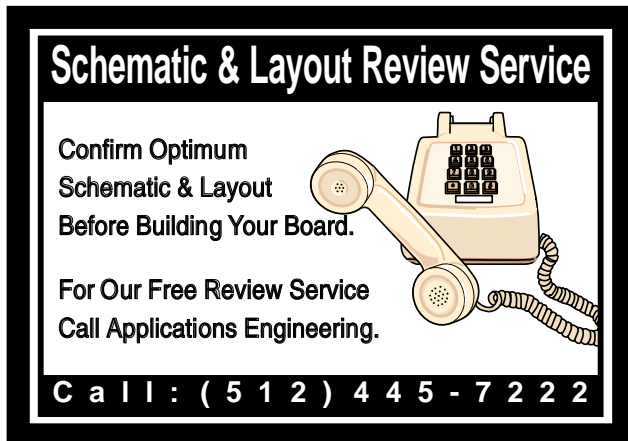
Capture Lower Base (I31)

D7	D6	D5	D4	D3	D2	D1	D0
CLB7	CLB6	CLB5	CLB4	CLB3	CLB2	CLB1	CLB0

CLB7-CLB0 Lower Base Bits: This register is the lower byte which represents the 8 least significant bits of the 16-bit Capture Base register. Reads from this register returns the same value which was written.

This register's initial state after reset is: 00000000

GROUNDING AND LAYOUT

Figure 16 is a suggested layout for the CS4231A. Similar to other Crystal codecs, it is recommended that the device be located on a separate analog ground plane. With the CS4231A's parallel data interface, however, optimum performance is achieved by extending the digital ground plane across pins 65 through 68 and pins 1 through 8. Pins 2 and 8 are grounds for the data bus and should be electrically connected to the digital ground plane which will minimize the effects of the bus interface due to transient currents during bus switching. Figure 17 shows the recommended positioning of the decoupling capacitors. The capacitors must be on the same layer as, and close to, the CS4231A. The vias shown go through to the ground plane layer. Vias, power supply traces, and VREF traces should be as large as possible to minimize the impedance.

Schematic & Layout Review Service

Confirm Optimum Schematic & Layout Before Building Your Board.

For Our Free Review Service Call Applications Engineering.

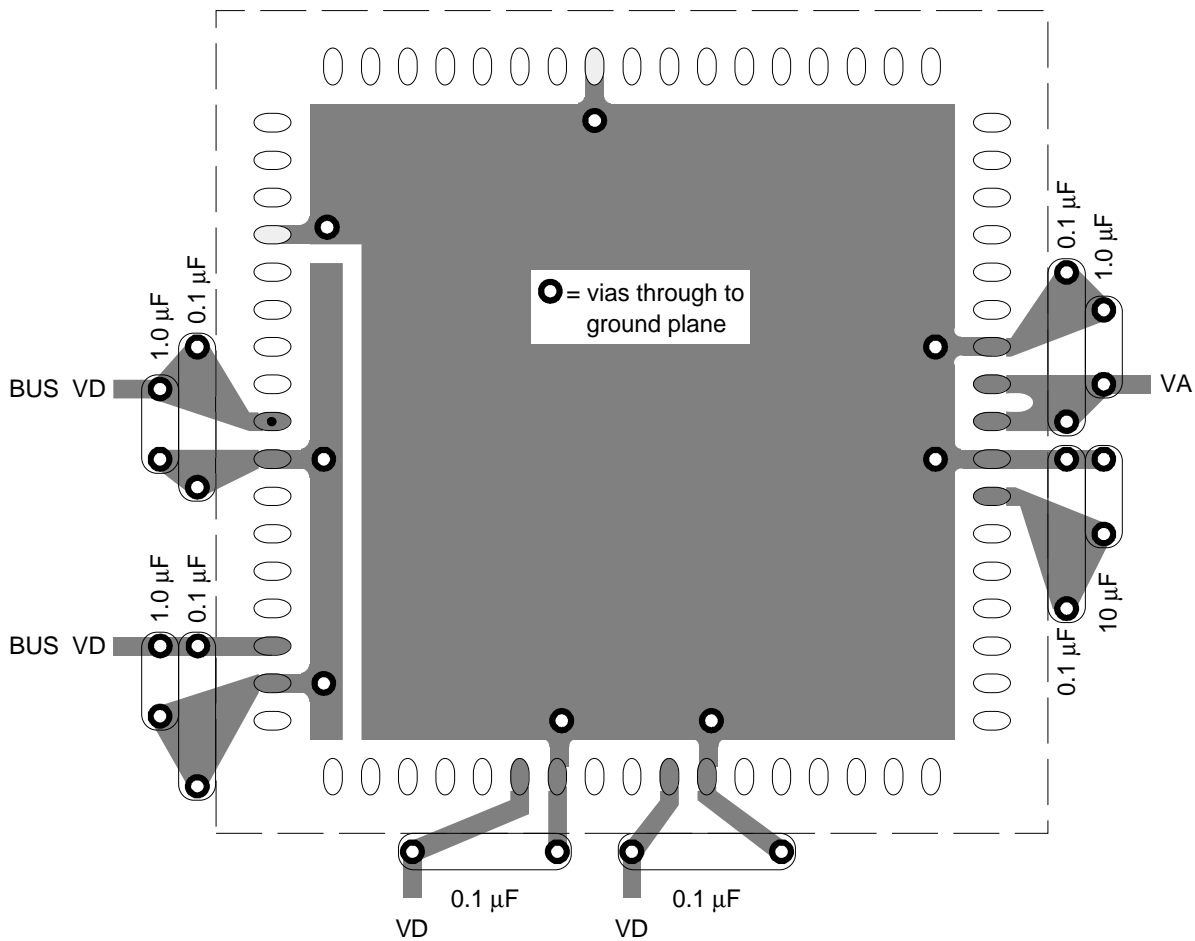**Call: (512) 445-7222**

COMPATIBILITY WITH AD1848

The CS4231A is compatible with the AD1848 rev. J silicon, the CS4231, and the CS4248 in terms of the applications circuit. The AD1848 rev K requires 0.1 µF capacitors (not 1000 pF) on pins 26 and 31. The CS4231A requires 1000 pF NPO-type capacitors on filter pins 26

and 31 (not 0.1 µF). To achieve compatibility with the CS4231A:

1. Correct spacing of pads will ensure that either 0.1 µF capacitors (for the AD1848 rev K) or 1000 pF NPO capacitors (for the CS4231A) may be installed.

2. The CS4231A does not require the input anti-aliasing filters included as an input R/C for the AD1848 (5.1kΩ and 560 pF). The additional R/C's can be used with the CS4231A if desired, with no degradation in performance.

3. Although optimum performance is achieved using the ground plane shown in Figure 16, any ground plane scheme that achieves acceptable performance with the AD1848 should work with the CS4231A.

4. The AD1848 needs extra power and ground pins. The power pins (V_{DD}) are pins 24, 45, and 54. The ground pins (GNDD) are pins 25 and 44. The CS4231A PLCC package does not use these pins and the appropriate power/ground connections can be made.

5. The Mono In/Mono Out pins do not exist on the AD1848.

6. The AD1848 does not contain 16 mA bus drivers. Therefore, buffers must be used.

7. MODE 2 and all associated features do not exist on the AD1848.

8. The AD1848 does not contain the selectable dither (DEN, I10)

9. The AD1848 is not available in a 100-pin TQFP package.

≥1/8"

Digital Ground Plane

CS4231A

65

PINS

Digital Pins

Analog Pins

8

Ground Connection

+5V Ferrite Bead

Analog Ground Plane

CPU & Digital Logic

Codec digital signals

Codec analog signals & Components
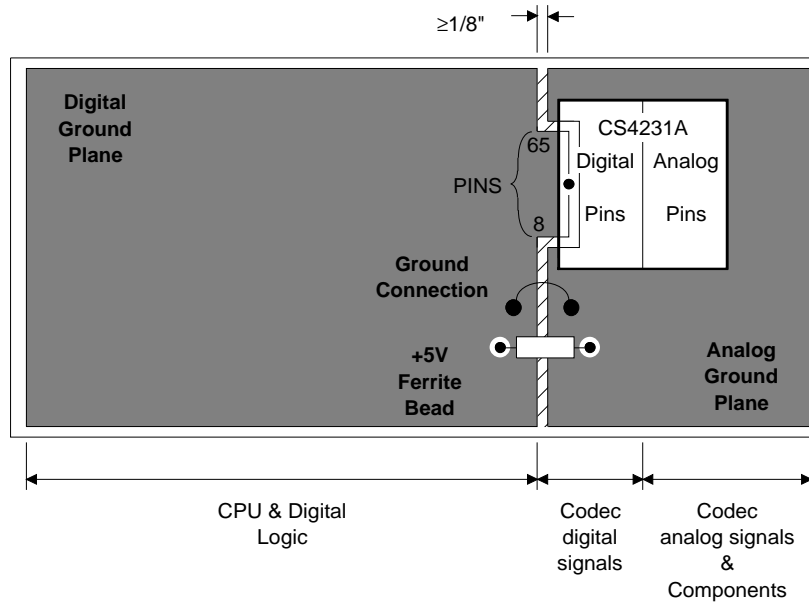
Figure 16. Suggested Layout Guideline

= vias through to ground plane

0.1 μF

1.0 μF

VA

1.0 μF

0.1 μF

BUS VD

1.0 μF

0.1 μF

BUS VD

10 μF

0.1 μF

0.1 μF

VD

0.1 μF

VD

Figure 17. Recommended Decoupling Capacitor Positions

10. The AD1848 does not have any CS4231A specific features. See Appendix A for more details.

11. The TEST pin on the CS4231A must be grounded. This pin is not used or connected on the AD1848. Grounding this pin will support the CS4231A while having no affect on the AD1848.

ADC/DAC FILTER RESPONSE PLOTS

Figures 18 through 23 show the overall frequency response, passband ripple, and transition band for the CS4231A ADCs and DACs. Figure 24 shows the DACs' deviation from linear phase. Since the CS4231A scales filter response based on sample frequency selected, all frequency response plots x-axis' are shown from 0 to 1 where 1 is equivalent to Fs. Therefore, for any given sample frequency, multiply the x-axis values by the sample frequency selected to get the actual frequency.
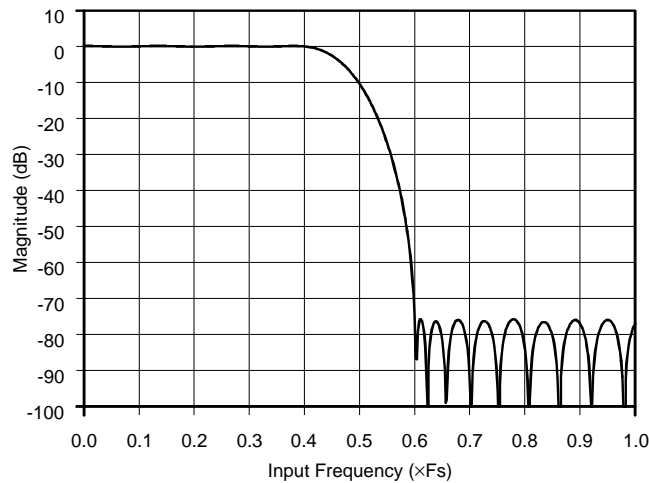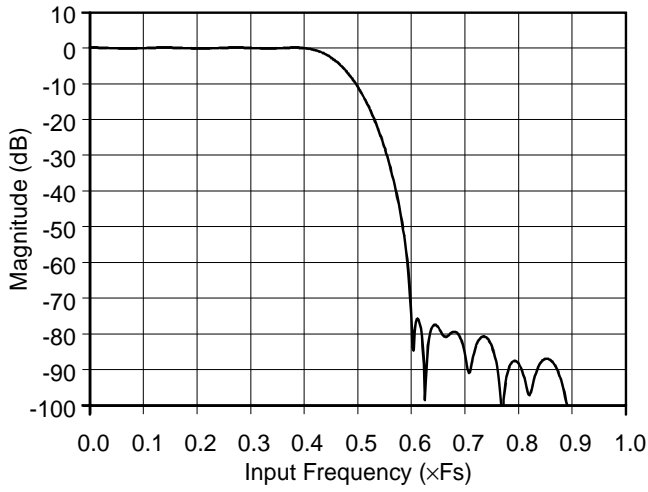

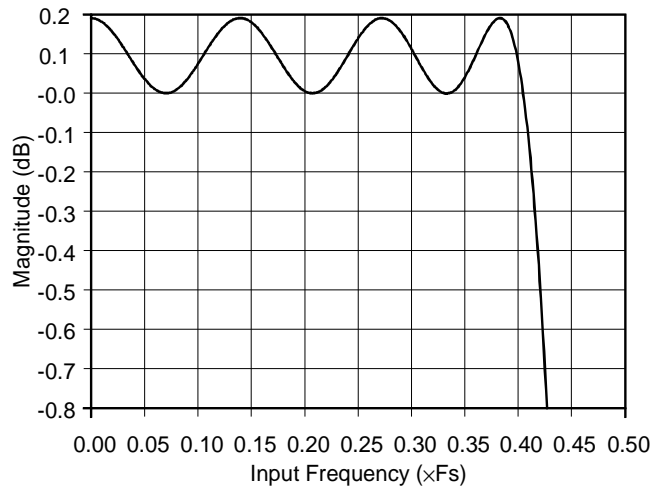**Figure 18. ADC Filter Response.**
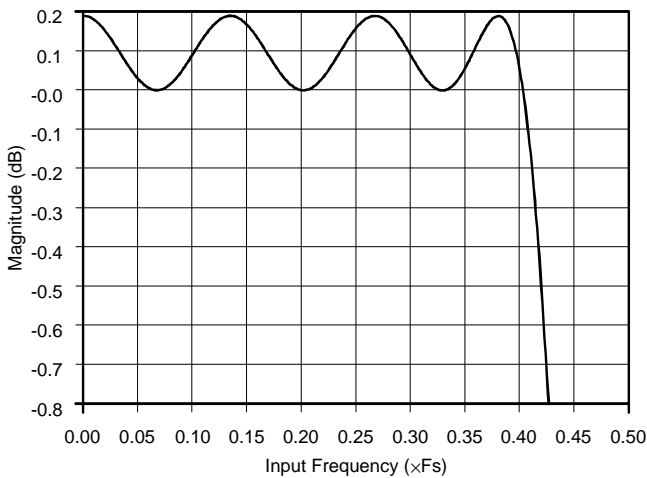
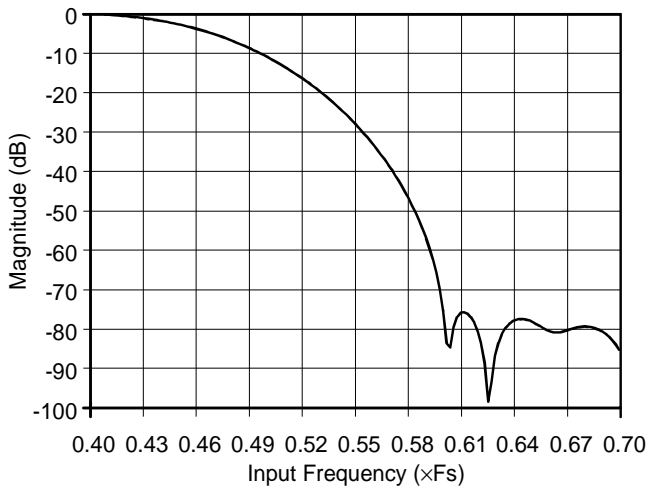
Figure 19. ADC Passband Ripple.
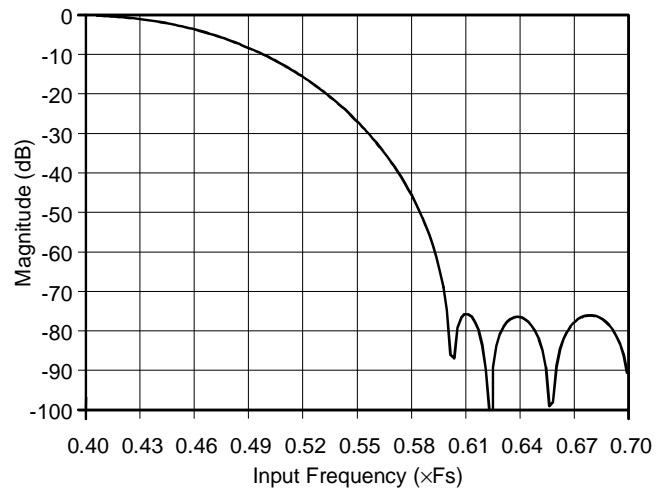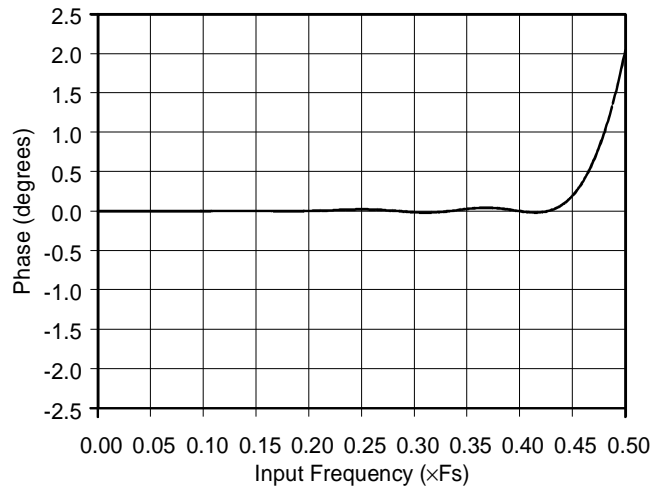

Figure 20. ADC Transition Band.

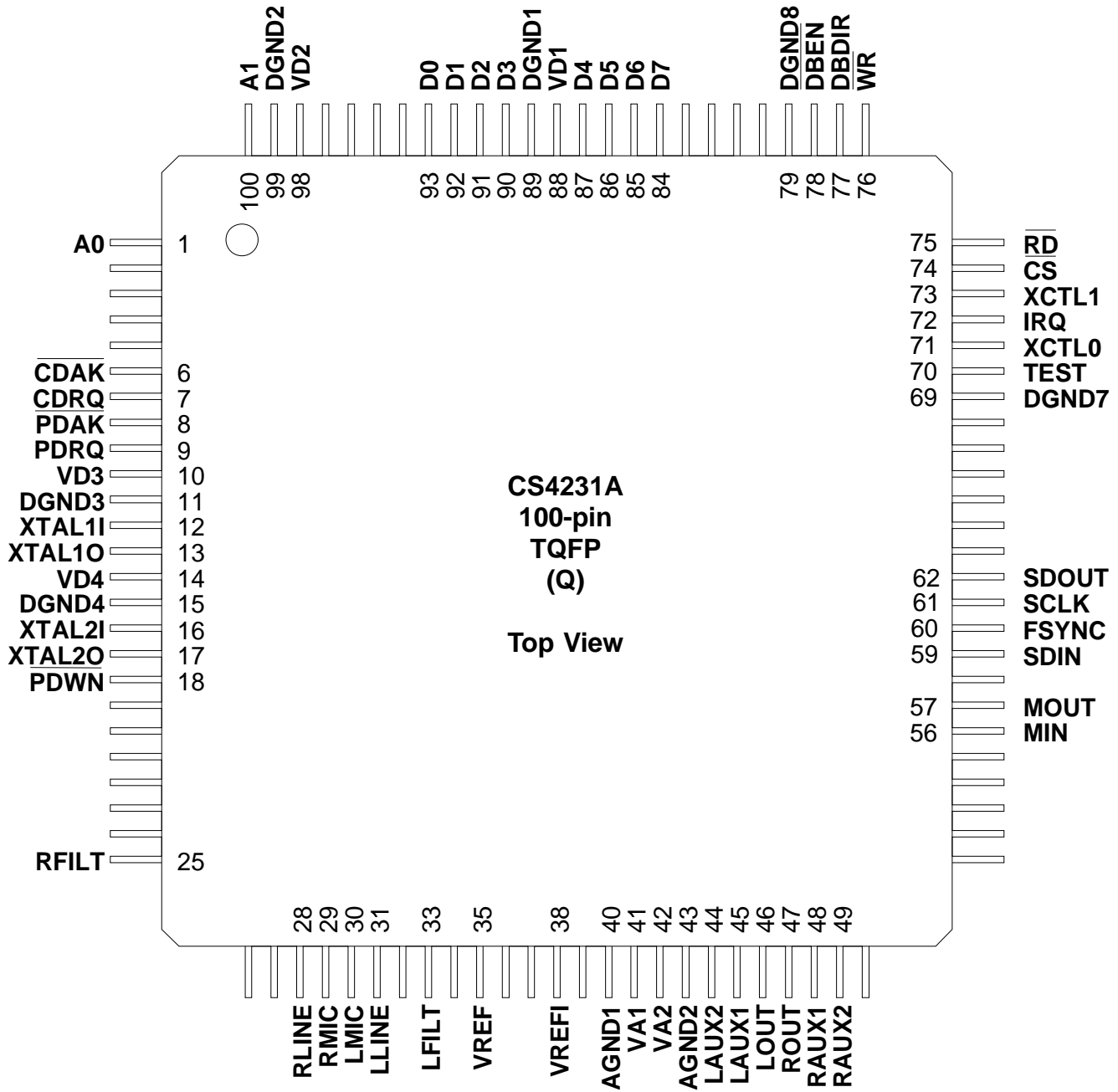**Figure 21. DAC Filter Response.**

Figure 22. DAC Passband Ripple.

Figure 23. DAC Transition Band.

Figure 24. DAC Phase Response.

PIN DESCRIPTIONS

CS4231A
100-pin
TQFP
(Q)

Top View

Top pins (left to right): A1 (100), DGND2 (99), VD2 (98), D0 (93), D1 (92), D2 (91), D3 (90), DGND1 (89), VD1 (88), D4 (87), D5 (86), D6 (85), D7 (84), DGND8 (79), DBEN (78), DBDIR (77), WR (76)

Left pins (top to bottom): A0 (1), CDAK (6), CDRQ (7), PDAK (8), PDRQ (9), VD3 (10), DGND3 (11), XTAL1I (12), XTAL1O (13), VD4 (14), DGND4 (15), XTAL2I (16), XTAL2O (17), PDWN (18), RFILT (25)

Right pins (top to bottom): RD (75), CS (74), XCTL1 (73), IRQ (72), XCTL0 (71), TEST (70), DGND7 (69), SDOUT (62), SCLK (61), FSYNC (60), SDIN (59), MOUT (57), MIN (56)

Bottom pins (left to right): RLINE (28), RMIC (29), LMIC (30), LLINE (31), LFILT (33), VREF (35), VREFI (38), AGND1 (40), VA1 (41), VA2 (42), AGND2 (43), LAUX2 (44), LAUX1 (45), LOUT (46), ROUT (47), RAUX1 (48), RAUX2 (49)

```
                                    CS4231A
                                    68-pin
                                     PLCC
                                      (L)

                                   Top View
```

VD1
DGND1
D3
D2
D1
D0
VD2
DGND2
A1
A0
CDAK
CDRQ
PDAK
PDRQ
VD3
DGND3
XTAL1I
XTAL1O
VD4
DGND4
XTAL2I
XTAL2O
PDWN
* NC (V_DD)
* NC (GNDD)
RFILT
RLINE
RMIC
LMIC
LLINE
LFILT
VREF
VREFI
AGND1

D4
D5
D6
D7
DGND8
DBEN
DBDIR
WR
RD
CS
XCTL1
IRQ
XCTL0
TEST
* NC (V_DD)
DGND7
SDOUT
SCLK
FSYNC
SDIN
NC
MOUT
MIN
* NC (V_DD)
* NC (GNDD)
RAUX2
RAUX1
ROUT
LOUT
LAUX1
LAUX2
AGND2
VA2
VA1

9 7 5 3 1 67 65 63 61
11   59
13   57
15   55
17   53
19   51
21   49
23   47
25   45
27 29 31 33 35 37 39 41 43

* see *Power Supply* section

Parallel Bus Interface Pins

CDRQ - Capture Data Request, Output, Pin 12 (L), Pin 7 (Q).
> The assertion of this signal indicates that the codec has a captured audio sample ready for transfer. This signal will remain asserted until all the bytes from the capture buffer have been transferred.

CDAK - Capture Data Acknowledge, Input, Pin 11 (L), Pin 6 (Q).
> The assertion of this active low signal indicates that the RD cycle occurring is a DMA read from the capture from the buffer.

PDRQ - Playback Data Request, Output, Pin 14 (L), Pin 9 (Q).
> The assertion of this signal indicates that the codec is ready for more playback data. The signal will remain asserted until the bytes needed for a playback sample have been transferred.

PDAK - Playback Data Acknowledge, Input, Pin 13 (L), Pin 8 (Q).
> The assertion of this active low signal indicates that the $\overline{WR}$ cycle occurring is a DMA write to the playback buffer.

A<1:0> - Address Bus, Input, Pin 9, 10 (L), Pin 100, 1 (Q).
> These address pins are read by the codec interface logic during an I/O cycle access. The state of these address lines determines which register (R0-R3) is accessed.

$\overline{RD}$ - Read Strobe, Input, Pin 60 (L), Pin 75 (Q).
> This signal defines a read cycle to the codec. The cycle may be an I/O cycle read, or the cycle could be a read from the codec's DMA sample registers.

$\overline{WR}$ - Write Strobe, Input, Pin 61 (L), Pin 76 (Q).
> This signal indicates a write cycle to the codec. The cycle may be an I/O cycle write, or the cycle could be a write to the codec's DMA sample registers.

$\overline{CS}$ - Chip Select, Input, Pin 59 (L), Pin 74 (Q).
> The codec will not respond to any I/O cycle accesses until this signal goes low. This signal is ignored during the DMA transfers.

D<7:0> - Data Bus, Input/Output, Pin 65-68, 3-6 (L), Pin 84-87, 90-93 (Q).
> These signals are used to transfer data to and from the CS4231A.

$\overline{DBEN}$ - Data Bus Enable, Output, Pin 63 (L), Pin 78 (Q).
> This pin indicates that the bus drivers attached to the CS4231A should be enabled. This signal is active low.

DBDIR - Data Bus Direction, Output Pin 62, (L), Pin 77 (Q).
> This pin indicates the direction of the data bus transceiver. High points to the CS4231A, low points to the host bus. This signal is normally high.

IRQ - Host Interrupt Pin, Output, Pin 57 (L), Pin 72 (Q).
> This active high signal is used to notify the host of events which need servicing.

Serial Audio Port Pins

SDOUT - Serial Data Output, Pin 52 (L), Pin 62 (Q).
> Enabled via SPE in I16, the serial data out pin outputs audio data bits, on the rising edge of SCLK, from the ADCs in the audio data format selected. The serial audio data is always 16 bits wherein the MSB of the different audio formats (16, 8 , 4 bit) is aligned with zero padding after the LSB. When SPE is zero (disabled), this pin is held low.

SCLK - Serial Clock, Output, Pin 51 (L), Pin 61 (Q).
> Enabled via SPE in I16, the serial clock outputs audio data bits on the rising edge of SCLK and receives audio data on the falling edge of SCLK. Two different formats are supported: 64 SCLKs per frame, and 32 SCLKs per frame. When SPE is zero (disabled), this pin is held low.

FSYNC - Frame Sync, Output, Pin 50 (L), Pin 60 (Q).

Enabled via SPE in I16, the frame sync output indicates the start of the data frame. Two different formats are supported: FSYNC high for one bit period before the start of a frame, and FSYNC high during the left word (either 16 or 32 bit periods). When the serial port is disabled, this output is held low.

SDIN - Serial Data In, Input, Pin 49 (L), Pin 59 (Q).

Enabled via SPE in I16, the serial data input accepts data, on the falling edge of SCLK, from an external source and sends the data to the DACs for conversion to analog. The serial port supports three serial formats and supports all audio data formats of the CS4231A. The serial audio data is always 16 bits wherein the MSB of the different audio (16, 8, 4 bit) is aligned with zero padding after the LSB.

Analog Inputs

LLINE- Left Line Input, Pin 30 (L), Pin 31 (Q).

Nominally 1 V$_{RMS}$ max analog input for the Left LINE channel, centered around VREF. The LINE inputs may be selected for an A/D conversion via the input multiplexer (I0). A programmable gain block (I18) also allows routing to the mixer.

RLINE - Right Line Input , Pin 27 (L), Pin 28 (Q).

Nominally 1 V$_{RMS}$ max analog input for the Right LINE channel, centered around VREF. The LINE inputs may be selected for A/D conversion via the input multiplexer (I1). A programmable gain block (I19) also allows routing to the mixer.

LMIC - Left Mic Input, Pin 29 (L), Pin 30 (Q).

Microphone input for the Left MIC channel, centered around VREF. This signal can be either 1 V$_{RMS}$ (LMGE = 0) or 0.1 V$_{RMS}$ (LMGE = 1). The MIC inputs may be selected for A/D conversion via the input multiplexer (I0).

RMIC - Right Mic Input, Pin 28 (L), Pin 29 (Q).

Microphone input for the Right MIC channel, centered around VREF. This signal can be either 1 V$_{RMS}$ (RMGE = 0) or 0.1 V$_{RMS}$ (RMGE = 1). The MIC inputs may be selected for A/D conversion via the input multiplexer (I1).

LAUX1 - Left Auxiliary #1 Input, Pin 39 (L), Pin 45 (Q).

Nominally 1 V$_{RMS}$ max analog input for the Left AUX1 channel, centered around VREF. The AUX1 inputs may be selected for A/D conversion via the input multiplexer (I0). A programmable gain block (I2) also allows routing to the output mixer.

RAUX1 - Right Auxiliary #1 Input, Pin 42 (L), Pin 48 (Q).

Nominally 1 V$_{RMS}$ max analog input for the Right AUX1 channel, centered around VREF. The AUX1 inputs may be selected for A/D conversion via the input multiplexer (I1). A programmable gain block (I3) also allows routing to the output mixer.

LAUX2 - Left Auxiliary #2 Input, Pin 38 (L), Pin 44 (Q).

Nominally 1 V$_{RMS}$ max analog input for the Left AUX2 channel, centered around VREF. A programmable gain block (I4) allows routing of the AUX2 channels into the output mixer.

RAUX2 - Right Auxiliary #2 Input, Pin 43 (L), Pin 49 (Q).

Nominally 1 V$_{RMS}$ max analog input for the Right AUX2 channel, centered around VREF. A programmable gain block (I5) allows routing of the AUX2 channels into the output mixer.

MIN - Mono Input, Pin 46 (L), Pin 56 (Q).

Nominally 1 V$_{RMS}$ max analog input, centered around VREF, that goes through a programmable gain stage (I26) into both channels of the mixer. This is a general purpose mono analog input that is normally used to mix the typical "beeper" signal on most computers into the audio system. On power-up, MIN is connected directly to MOUT, but not to L/ROUT. The default condition can be changed in I26.

Analog Outputs

LOUT - Left Line Level Output, Pin 40 (L), Pin 46 (Q).

Analog output from the mixer for the left channel. Nominally 1 V$_{RMS}$ max centered around VREF when OLB = 1 (I16). When OLB = 0, the output is attenuated 3 dB and is a maximum of 0.707 V$_{RMS}$

ROUT - Right Line Level Output, Pin 41 (L), Pin 47 (Q).

Analog output from the mixer for the right channel. Nominally 1 V$_{RMS}$ max centered around VREF when OLB = 1 (I16). When OLB = 0, the output is attenuated 3 dB and is a maximum of 0.707 V$_{RMS}$

MOUT - Mono Output, Pin 47 (L), Pin 57 (Q).

When OLB=1 (I16), MOUT is nominally 1 V$_{RMS}$ max analog output, centered around VREF. When OLB=0, the maximum output voltage is 3 dB lower, 0.707 V$_{RMS}$. This output is a summed analog output from both the left and right output channels of the mixer. MOUT typically is connected to a speaker driver that drives the internal speaker in most computers. Independently mutable via MOM in I26.

Miscellaneous

XTAL1I - Crystal #1 Input, Pin 17 (L), Pin 12 (Q).

This pin will accept either a crystal with the other pin attached to XTAL1O or an external CMOS clock. XTAL1 must have a crystal or clock source attached for proper operation. The standard crystal frequency is 24.576 MHz although other frequencies can be used. The crystal should be designed for fundamental mode, parallel resonance operation.

XTAL1O - Crystal #1 Output, Pin 18 (L), Pin 13 (Q).

This pin is used for a crystal placed between this pin and XTAL1I.

XTAL2I - Crystal #2 Input, Pin 21 (L), Pin 16 (Q).
> If a second crystal is used, it should be placed between this pin and XTAL2O. The standard crystal frequency is 16.9344 MHz although other frequencies can be used. The crystal should be designed for fundamental mode, parallel resonance operation.

XTAL2O - Crystal #2 Output, Pin 22 (L), Pin 17 (Q).
> This pin is used for a crystal placed between this pin and XTAL2I.

$\overline{\text{PDWN}}$ - Power Down, Input, Pin 23 (L), Pin 18 (Q).
> Places CS4231A in lowest power consumption mode. All sections of the CS4231A, except the digital bus interface which reads 80h, are shut down and consuming minimal power. The CS4231A is in power down mode when this pin is logic low.

XCTL0, XCTL1 - External Control, Output, Pin 56, 58 (L), Pin 71, 73 (Q).
> These signals are controlled by the register bits XCTL0 and XCTL1 in register I10. They can be used to control external logic via TTL levels.

VREF - Voltage Reference, Output, Pin 32 (L), Pin 35 (Q).
> All analog inputs and outputs are centered around VREF which is nominally 2.1 Volts. This pin may be used to level shift external circuitry, although any AC loads should be buffered. High internal-gain microphone inputs S/N ratio can be slightly improved by placing a 10µF capacitor on VREF.

VREFI - Voltage Reference Internal, Input, Pin 33 (L), Pin 38 (Q).
> Voltage reference used internal to the CS4231A must have a 0.1 µF + 10 µF capacitor with short fat traces to attach to this pin. No other connections should be made to this pin.

LFILT - Left Channel Antialias Filter Input, Pin 31 (L), Pin 33 (Q).
> A 1000 pF NPO capacitor must be attached between this pin and analog ground.

RFILT - Right Channel Antialias Filter Input, Pin 26 (L), Pin 25 (Q).
> A 1000 pF NPO capacitor must be attached between this pin and analog ground.

TEST - Test, Pin 55 (L), Pin 70 (Q).
> This pin must be tied to ground for proper operation.

Power Supplies

VA1, VA2 - Analog Supply Voltage, Pin 35, 36 (L), Pin 41, 42 (Q).
> Supply to the analog section of the codec.

AGND1, AGND2 - Analog Ground, Pin 34, 37 (L), Pin 40, 43 (Q).
> Ground reference to the analog section of the codec. Internally, these pins are connected to the substrate as are DGND3/4/7/8; therefore optimum layout is achieved with the AGND pins on the same ground plane as DGND3/4/7/8 (see Figure 17). However, other ground arrangements should yield adequate results.

VD1, VD2 - Digital Supply Voltage, Pin 1, 7 (L), Pin 88, 98 (Q).

 Digital supply for the parallel data bus section of the codec.

VD3, VD4 - Digital Supply Voltage, Pin 15, 19 (L), Pin 10, 14 (Q).

 Digital supply for the internal digital section of the codec (except for the parallel data bus).

DGND1, DGND2 - Digital Ground, Pin 2, 8 (L), Pin 89, 99 (Q).

 Digital ground reference for the parallel data bus section of the codec. These pins are isolated from the other digital grounds and should be connected to the digital ground section of the board (see Figure 17).

DGND3, DGND4, DGND7, DGND8 - Digital Ground, Pin 16, 20, 53, 64(L), Pin 11, 15, 69, 79 (Q).

 Digital ground reference for the internal digital section of the codec (except the parallel data bus). These pins are connected to the substrate of the die as are the AGND pins. Optimum layout is achieved by placing DGND3/4/7/8 on the analog ground plane with the AGND pins as shown in Figure 17. However, other ground arrangements should yield adequate results.

*NC (V$_{DD}$) - No Connect, Pins 24, 45, 54 (L)

 These pins are no connects for the CS4231A. When compatibility with the AD1848 is desired, these pins should be connected to the digital power supply. For other compatibility issues, see the *Compatibility with AD1848* section of the data sheet.

*NC (GNDD) - No Connect, Pins 25, 44 (L)

 These pins are no connects for the CS4231A. When compatibility with the AD1848 is desired, these pins should be connected to digital ground. For other compatibility issues, see the *Compatibility with AD1848* section of the data sheet.

PARAMETER DEFINITIONS

Resolution

The number of bits in the input words to the DACs, and in the output words in the ADCs.

Differential Nonlinearity

The worst case deviation from the ideal code width. Units in LSB.

Total Dynamic Range

TDR is the ratio of the rms value of a full scale signal to the lowest obtainable noise floor. It is measured by comparing a full scale signal to the lowest noise floor possible in the codec (i.e. attenuation bits for the DACs at full attenuation). Units in dB.

Instantaneous Dynamic Range

IDR is the ratio of a full-scale rms signal to the rms noise available at any instant in time, without changing the input gain or output attenuation settings. It is measured using S/(N+D) with a 1 kHz, -60 dB input signal, with 60 dB added to compensate for the small input signal. Use of a small input signal reduces the harmonic distortion components to insignificance when compared to the noise. Units in dB.

Total Harmonic Distortion (THD)

THD is the ratio of the test signal amplitude to the rms sum of all the in-band harmonics of the test signal.

Interchannel Isolation

The amount of 1 kHz signal present on the output of the grounded input channel with 1 kHz 0 dB signal present on the other channel. Units in dB.

Interchannel Gain Mismatch

For the ADCs, the difference in input voltage that generates the full scale code for each channel. For the DACs, the difference in output voltages for each channel with a full scale digital input. Units in dB.

Offset Error

For the ADCs, the deviation in LSBs of the output from mid-scale with the selected input grounded. For the DACs, the deviation in volts of the output from VREF with mid-scale input code.

APPENDIX A

This data sheet describes the CS4231A which is backwards compatible with the CS4231 - both hardware and software. The CS4231A uses four pins that were "No Connects", on the CS4231 (for the audio serial port). Since the CS4231 defines these pins as "No Connects", the CS4231A will drop into a CS4231 socket and function properly, although the serial port will not be connected.

There are also software additions to the CS4231A. New bits have been defined to enhance the operation of the CS4231A. These added bits were reserved in the CS4231. The data sheet states that reserved bits should be written as 0 and may read back as 0 or 1; therefore, properly written software is forwards compatible with the CS4231A. The version bits V2-V0 (upper three bits of I25) distinguish between the CS4231 and the CS4231A. The additions to the CS4231A are as follows:

1. **Interface Configuration register (I9):** The CAL1 bit does not exist in the CS4231. The CAL0 bit was labeled ACAL in the CS4231 but the function was the same. The extra calibration modes in the CS4231A better support full duplex and games software.

2. **Alternate Feature Enable I register (I16):** The PMCE and CMCE bits do not exist in the CS4231. These bits were added to enhance full-duplex operation.

   The serial audio data port and associated bits - SF1, SF0, SPE - do not exist on the CS4231. The serial audio data port was added to the CS4231A to allow DSP's and ASIC's to act as an audio coprocessor to the CS4231A.
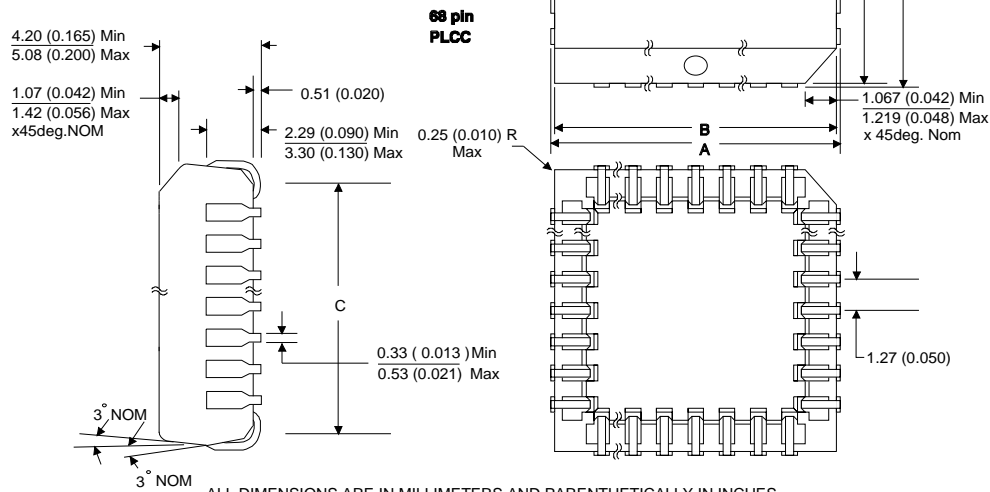
3. **Alternate Feature Enable II register (I17):** The APAR and XTALE bits do not exist in the CS4231. The APAR bit was added better support the ADPCM playback mechanism.

   The XTALE bit was added to better support software that switches sample frequencies often, e.g. games.
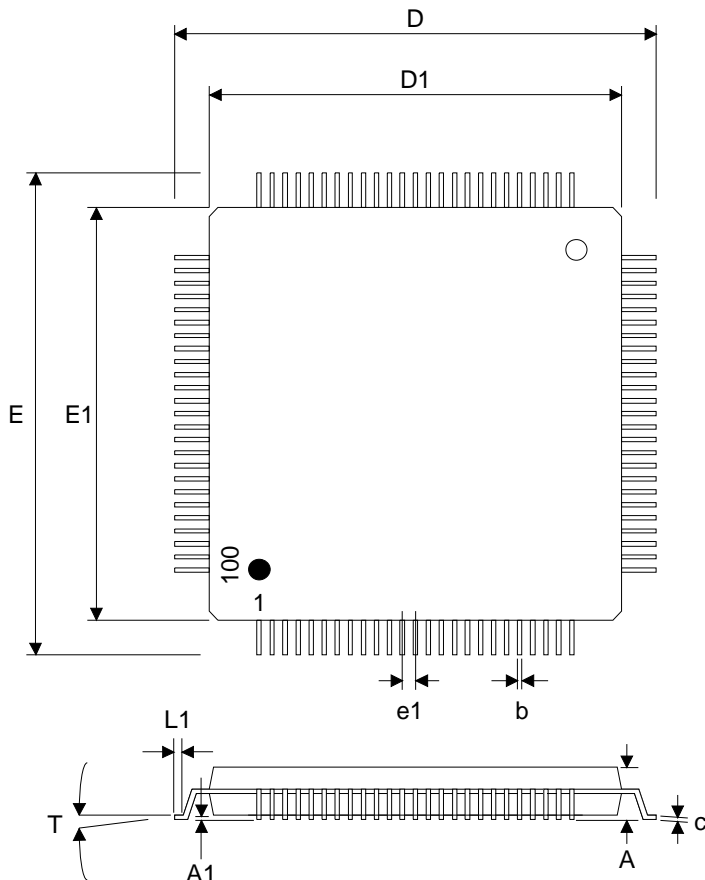
4. **Alternate Feature Enable III register (I23):** The ACF bit does not exist on the CS4231. This bit better supports the ADPCM capture mechanism.

5. **Version / ID register (I25):** The Version number bits - V2, V1, V0 - were modified (changed to 101) to allow software to uniquely identify the CS4231A.

6. **Mono Input & Output Control register (I26):** The MBY bit does not exist in the CS4231. The power up default value of this register was also changed. The extra bit and the changes will approximate the CS4231 at power-up. The difference is that the MIN pin (normally the PC beeper) is directed to the MOUT pin - but not to the L/ROUT pins.

PACKAGE DIMENSIONS

	A		B		C	
	MIN	MAX	MIN	MAX	MIN	MAX
68	25.02 (0.985)	25.27 (0.995)	24.13 (0.950)	24.33 (0.958)	22.61 (0.890)	23.62 (0.930)

68 pin PLCC

4.20 (0.165) Min
5.08 (0.200) Max

1.07 (0.042) Min
1.42 (0.056) Max
x45deg.NOM

0.51 (0.020)

2.29 (0.090) Min
3.30 (0.130) Max

0.25 (0.010) R Max

1.067 (0.042) Min
1.219 (0.048) Max
x 45deg. Nom

0.33 (0.013) Min
0.53 (0.021) Max

C

B
A

B
A

3° NOM

3° NOM

1.27 (0.050)

ALL DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES.

100-pin TQFP

Symbol	Description	MIN	NOM	MAX
N	Lead Count		100	
A	Overall Height			1.66
A1	Stand Off	0.00		
b	Lead Width	0.14	0.20	0.26
c	Lead Thickness	0.077	0.127	0.177
D	Terminal Dimension	15.70	16.00	16.30
D1	Package Body		14.0	
E	Terminal Dimension	15.70	16.00	16.30
E1	Package Body		14.0	
e1	Lead Pitch	0.40	0.50	0.60
L1	Foot Length	0.30	0.50	0.70
T	Lead Angle	0.0°		12.0°

D

D1

E

E1

100

1

e1

b

L1

T

A1

C

A

Notes:
1) Dimensions in millimeters.
2) Package body dimensions do not include mold protrusion, which is 0.25 mm.
3) Coplanarity is 0.004 in.
4) Lead frame material is AL-42 or copper, and lead finish is solder plate.
5) Pin 1 identification may be either ink dot or dimple.
6) Package top dimensions can be smaller than bottom dimensions by 0.20 mm.
7) The "lead width with plating" dimension does not include a total allowable dambar protrusion of 0.08 mm (at maximum material condition).
8) Ejector pin marks in molding are present on every package.

CRYSTAL
Semiconductor Corporation

CS4231/4248 Evaluation Board

Features

- PC ISA Plug-In Card

- Serial Audio Data Port Header for CS4231A Support

- Mono In / Mono Out Support

- Microphone Pre-Amplifier

- Line Out / Headphone Circuit

- Microsoft Windows™ 3.1 Software Support

General Description

The CDB4231/4248 evaluation board supports all the features of the CS4231A, CS4231, and CS4248. The DMA, IRQ, and base address are all selectable via on-board jumpers. Four stereo jacks provide MIC in, AUX1 in, LINE in, and Line/Headphone out. In addition, on-board headers provide an internal analog CD-ROM interface via the AUX2 inputs, and support for the mono in and mono out capabilities of the CS4231. The CDB4231 also includes a serial port header to support the expanded features of the CS4231A.

Software that runs under Microsoft Windows™ 3.1 is also provided along with an extensive diagnostics program.

ORDERING INFORMATION: CDB4231, CDB4248
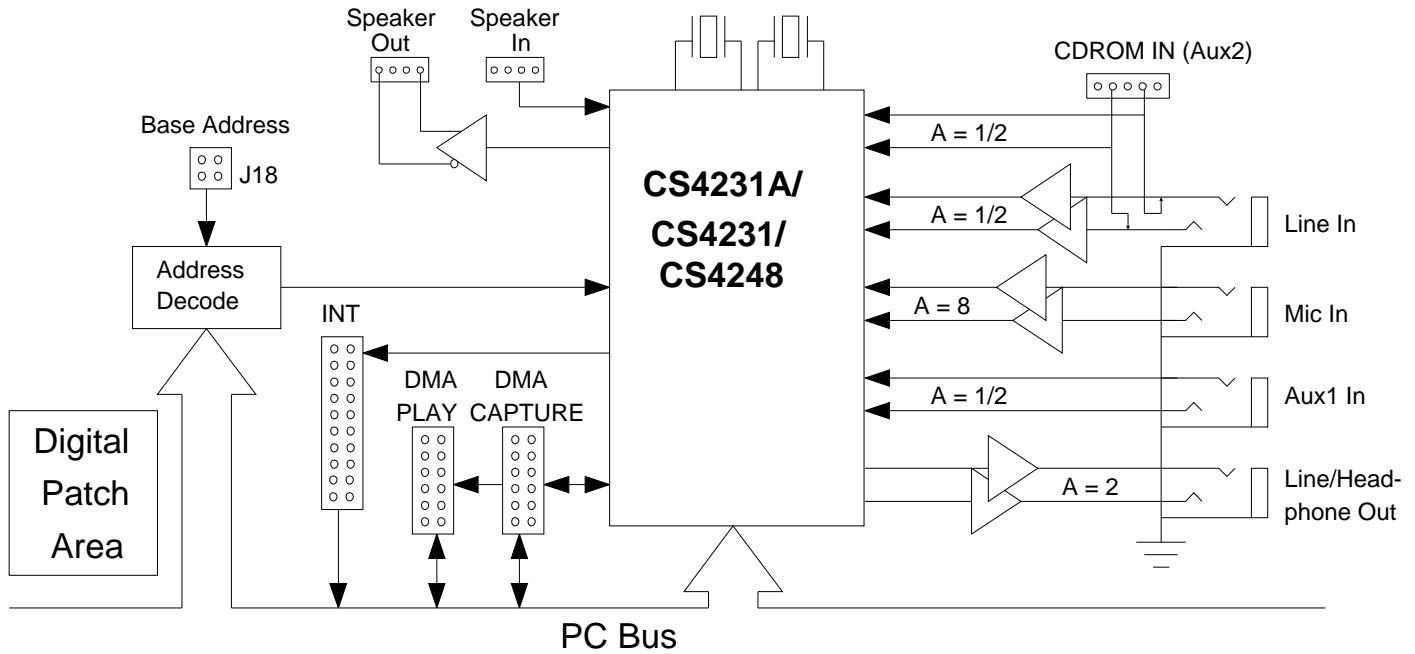
GENERAL INFORMATION

The CDB4231/4248 is designed to provide an easy platform for evaluating the performance of the CS4231A, CS4231, or CS4248 Parallel Interface, Multimedia Audio Codecs in a PC environment. This board is not a reference design, although many aspects of the design should be incorporated in reference designs. The board is optimized for performance and ease of modification for testing purposes. For those interested in a reference design, the CRD4231 provides most of the capabilities of the CDB4231, plus games support.

Software that operates under the Microsoft Windows™ environment is also included with applets that control all the CS4231 or CS4248 features. This software also provides full Windows™ 3.1 compatibility with extensions to utilize the more powerful CS4231 features in custom code.

Four stereo jacks, externally accessible, allow connection to Microphone inputs, Auxiliary 1 inputs, Line inputs, and Line/Headphone outputs. Headers allow internal connections to a CD-ROM analog output (using the codec's Auxiliary 2 inputs), and speaker pass-through and control via the **SPEAKER IN** (Mono In) and **SPEAKER OUT** (Mono Out) headers.

Additional headers on the board allow the setting of the Base Address, DMA channel, and IRQ for the CS4231. The factory default for the CDB4231 is base address 530h, DMA playback channel 3, DMA capture channel 0 and IRQ 7. The CDB4248 is the same with the exception of the DMA capture header which is not used and has both shorting jumpers removed.

The software must be configured to match the settings on the evaluation board headers for proper operation.

STEREO ANALOG INPUTS

Three of the four external $^{1}/_{8}$" stereo jacks are for analog inputs. The stereo **Mic I**, Microphone Input, (Figure 2) contains an op-amp buffer with a gain of 18 dB providing a maximum full scale input to the evaluation board of 12 mV (with the 20 dB boost inside the codec enabled). For microphones that output signals larger than 12 mV, the 20 dB gain block inside the codec can be disabled in software (the "Boost" button in the input applet). With the 20 dB gain block disabled, the maximum full-scale value is 120 mV. The microphone circuit is designed for single-ended microphones which are the most common type available. The J35 header, close to the mic input jack allows selection of a stereo microphone when the jumper is in the 'S' position, or mono input where the jumper is in the 'M' position. In the mono position, a mono mic input would go to both the left and right mic input pins on the codec.

The second input jack is **Ax1 I**, Auxiliary 1 In, (Figure 1) which has an input impedance of approximately 10 kΩ with a maximum full scale into the **Ax1 I** jack of 2 V$_{RMS}$.

The third stereo input jack is **Line I**, Line In, (Figure 4) which also has a maximum full scale of 2 V$_{RMS}$ and provides a typical audio input impedance of 47 kΩ.

An internal header, labeled **CDROM IN (AUX2)**, (Figure 4) may be used by any internal device for analog mixing into the codec's output mixer via the Auxiliary 2 inputs, AUX2. Since the AUX2 inputs don't have a path to the ADCs, when nothing is plugged into the **Line I** jack, the analog contained on the **CDROM IN** header is summed into the Line inputs of the codec as well as the AUX2 inputs. When a plug is inserted into the **Line I** jack, the **CDROM IN** header is disconnected from the Line inputs (but is still connected to the AUX2 inputs).

STEREO ANALOG OUTPUTS

The CDB4231/4248 contains one stereo analog output labeled **Ln/Hp O**, Line/Headphone Out, (Figure 5) with a maximum full-scale output of 2 V$_{RMS}$. This output provides a high-quality line out for use with external power amps or other equipment containing line-level inputs. It is also designed to drive headphones directly with exceptional quality.

MONO INPUT AND OUTPUT

The CS4231 contains a MIN (mono in) pin and a MOUT (mono out) pin that are typically placed in between the internal PC speaker and the beeper chip. The CDB4231 comes with a cable that should be connected between the PC beeper chip and the **SPEAKER IN** header (Figure 1) on the CDB4231 board. The cable wire, pin 1, should be placed on pin 1 of the **SPEAKER IN** header and pin 1 of the beeper header. If the PC beeps do not mix into the codec, try reversing the beeper header connector. This connects the beeper to the MIN pin on the CS4231 and allows traditional PC beeps to be mixed into the audio path.

The **SPEAKER OUT** header (Figure 3) should be connected to the PC speaker. The MOUT pin on the CS4231 is a mix of both left and right channels and has an independent software mute. The quality of this circuit is limited to the quality of the speaker used. Much higher fidelity can be achieved by using a higher quality speaker.

Since the CS4248 does not have MIN and MOUT pins, the CDB4248 board does not provide a cable, and the **SPEAKER IN** and **SPEAKER OUT** headers are non-functional.

SERIAL AUDIO DATA PORT

The CS4231A contains a serial audio data port that can pass audio data from the ADCs and to the DACs across the serial port. All control data must still be transferred via the ISA bus. The CDB4231 supports the CS4231A by providing a header, labeled J34, that is connected to the serial audio data port on the CS4231A. The even pins are connected to ground and the rest of the header pins are defined as follows:

    1 - not used
    3 - SDOUT
    5 - SDIN
    7 - SCLK
    9 - FSYNC

Twisted pair ribbon cable should be used when connecting to this header. Since the CS4231 and CS4248 do not support the serial audio data port, these pins are non-functional on the CDB4248 and when using a CS4231.

BASE ADDRESS

The base address is set using header J18 (Figure 6) and must match the software selected base address. The CDB4231/4248 evaluation board uses 8 I/O addresses. The first four are used to read the board ID of 04. Writes to the first four addresses are ignored. The board ID is output from the ID31 PLD and indicates that the board is Windows Sound System, WSS, compatible (see limitations listed in the *SOFTWARE COMPATIBILITY* section).

The second four addresses are used by the codec. The default for the evaluation board and the software is 530h - no jumpers. The following table lists the available base addresses (along with the associated codec address), with a "1" defined as no shorting jumper and a "0" defined as a shorting jumper installed:

X1	X0	Base Address	Codec Address	
1	1	530h	534h	(default)
1	0	604h	608h	
0	1	E80h	E84h	
0	0	F40h	F44h	

INTERRUPT

Although the hardware supports a wide selection of interrupts, software may have limitations in the available options. See the *SOFTWARE COMPATIBILITY* section for more information.

The interrupt is set using header J2, also labeled **INT**, (Figure 7) and must also match the software selected interrupt. The default for the evaluation board and the software is 7.

DMA SELECTION

Although the hardware supports a wide selection of DMA channels for playback and capture, software may have limitations in the available options. See the *SOFTWARE COMPATIBILITY* section for more information.

The CDB4231 contains two headers for DMA selection: one determines the playback channel and the other, if used, determines the capture channel for full duplex operation. Two shorting jumpers are needed for the selected DMA channel, one for the DRQ and one for the DACK. Header J20, labeled **DMA PLAY**, (Figure 7) is the primary DMA channel used for both playback and capture on the CS4248 or CS4231 in SDC

mode, as well as playback on the CS4231 in full-duplex operation.

Half Duplex - Single DMA Channel

The default configuration for the CDB4231 is full duplex. When the evaluation board is configured for half duplex, both jumpers on the **DMA CAPTURE** header J1, (Figure 7) SHOULD BE REMOVED. Otherwise, contention with other system resources may occur.

The CS4248 does not contain the second set of DMA base registers; therefore, it must be operated in half duplex mode. Since only one DMA channel is needed at any particular time, the CS4248 is usually operated in Single DMA Channel, SDC, mode.

If only one DMA channel is available, the CS4231 can be programmed for SDC mode wherein the playback channel, selected on the **DMA PLAY** header is used for both playback and capture. The default setting for the evaluation board for the **DMA PLAY** header DRQ3/DACK3.

Full Duplex - Two DMA Channels

Full duplex is only supported on the CS4231 (MODE 2 operation) which contains independent capture and playback DMA Base registers.

The J1 header, labeled **DMA CAPTURE**, (Figure 7) is used to support simultaneous capture in the CS4231 full-duplex mode. The default for the CDB4231 evaluation board **DMA CAPTURE** header, J1, is DRQ0/DACK0.

To support full-duplex operation, a unique DMA channel from each header must be selected.

SOFTWARE COMPATIBILITY

The CDB4231/4248 comes with two sets of software: diagnostics and Windows 3.1 drivers. The diagnostics will support all hardware jumper settings. The Windows software will support all hardware settings when configured for generic hardware. When the included Windows software (or any software) is configured or designed for 100% Windows Sound System compatibility, limitations in the hardware selections exist.

The CDB4231/4248 evaluation board includes a board ID PLD, ID31, that indicates to software that the board is Windows Sound System, WSS, compatible. This read-only register is located at the first four addresses (the second four are for the codec). This ID will read back 0x04 from the lower six bits. Although the evaluation board is WSS compatible from the codec register perspective, the auto-select hardware of the WSS board is not included. The DMA and IRQ settings must be configured via on-board jumpers. The four base addresses supported by the evaluation board are the same as specified for WSS hardware.

Windows software, such as the included drivers and applets, that check for a WSS board will read the board ID and assume that the auto-select register needs to be loaded. The auto-select register only allows certain combinations which must be adhered to when using the evaluation board with this software.

Therefore, to run 100% compatible Windows Sound System, WSS, software, the IRQ and DMA selection must be made from the following:

> INT: 7   (default)
>   10
>   11

Half Duplex: DMA PLAY:
>   0
>   1
>   3   (CDB4248 default)
>   DMA CAPTURE:
>   No jumpers (CDB4248 default)

Full Duplex: PLAY CAPTURE
>   0   1
>   1   0   (CDB4231 default)
>   3   0

Note in full duplex, only the three combinations listed are allowed with the last combination being the default for the CDB4231. If the software does not support full duplex, remove the jumpers on the **DMA CAPTURE** header, J1 (Figure 7).

The Crystal Windows software provided with the evaluation board can be configured for 100% WSS compatible hardware and will load the Auto-Select register with the proper DMA and IRQ settings. In 100% WSS mode, the Crystal software will not allow improper settings for the DMA and IRQ.

Some hardware, including the CDB4231/4248, allow selection of DMA and IRQ via on-board jumpers. These jumpers allow a wider selection of configuration options since it is not limited by the Auto-Select register options listed above.

The Crystal Windows 3.1 software (version 1.04) supports a "generic hardware" switch that forces the software to use the DMA and IRQ settings in the SYSTEM.INI file and assume no Auto-Select register exists. With this switch on, all combinations of DMA and IRQ, supported by the hardware, are allowed. To use this option, the SYSTEM.INI file must contain:

```
[CSBusAud]
GenericHardware=On      ; either On or Off
                        ; Off is default
```

This switch is added to the SYSTEM.INI file by the installation software when the "Generic Hardware" option is selected from the Windows Sound System screen.

WSS SOFTWARE COMPATIBILITY

The CS4231/4248 is compatible with Microsoft Windows Sound System software (version 2.0) with respect to wave audio data support. Since the evaluation board does not contain a synthesizer, the MIDI portion of WSS will not function. When installing the Microsoft software, select Custom Installation and set the base address, IRQ, and DMA channel consistent with the evaluation board jumper settings. Since the board does not contain the extra hardware needed for software configuration of the IRQ and DMA channel, the Auto Installation mode of the Microsoft WSS software is not supported.

The Microsoft WSS hardware and software drivers do not use all the analog inputs. The only hardware supported by the Microsoft WSS hardware and software are a mono microphone input (set jumper on J35 to M), and the stereo Line input jack, **Line I**.

CRYSTAL ENHANCED WSS 2.0 DRIVERS

Crystal also provides enhanced Windows Sound System drivers that support software written to the Windows Sound System standard. These drivers, currently version 1.0, were designed to support the CRD4231 reference design, but will also support the CDB4231. When using the Enhanced WSS 2.0 drivers, the following settings in the SYSTEM.INI file must be set to:
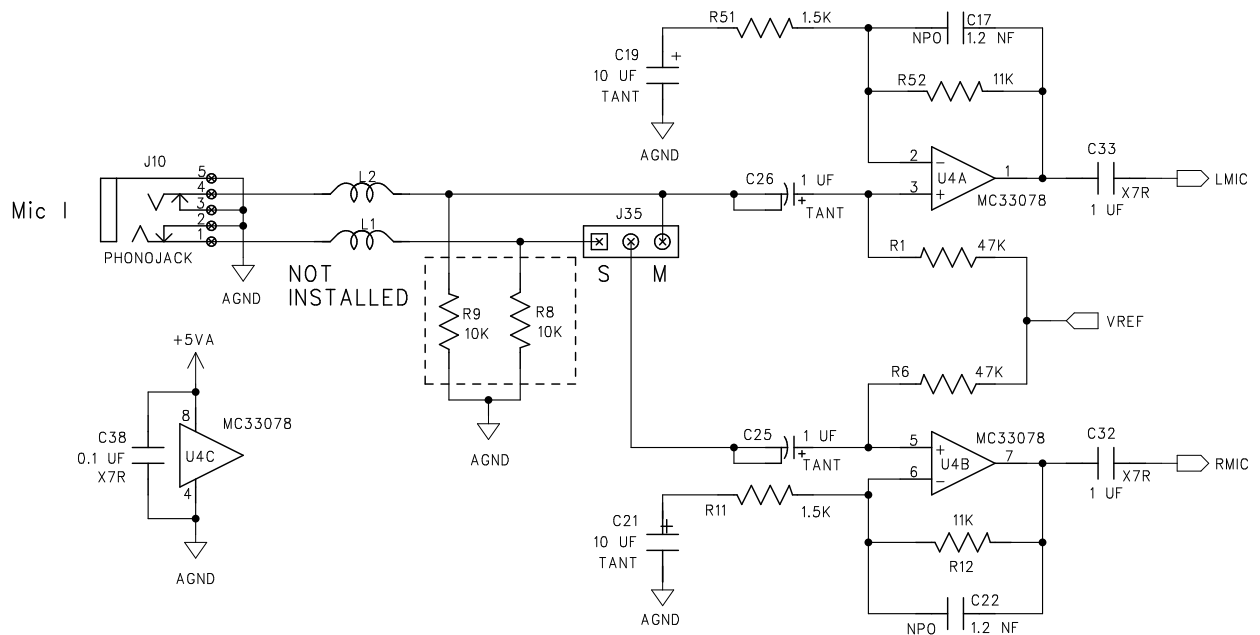
```
OldMSDosGameCompatibility=0
BlasterSupport=SWEmulation
Msft Hardware=0
Auto Select=0
Midi Play=0
```
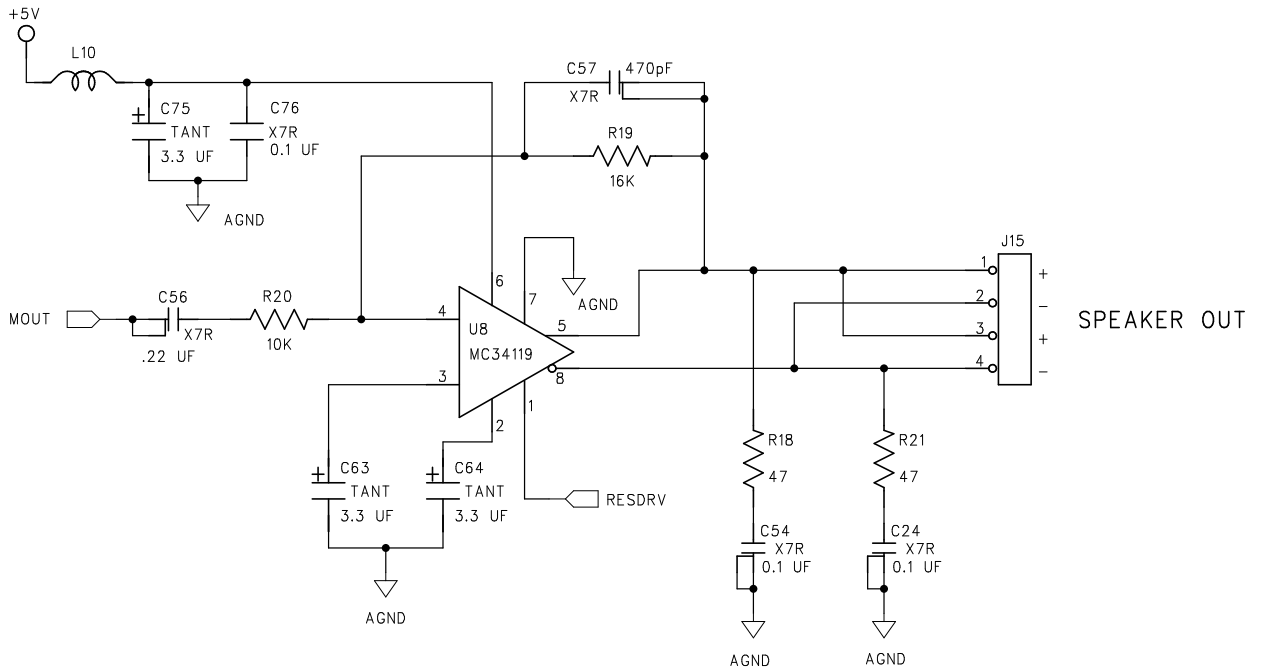
SCHEMATICS

The following pages contain the full schematics for the CDB4231/4248, the PLD equations, and layout plots of each PCB layer.

Windows and Windows Sound System are registered trademarks of Microsoft Corporation
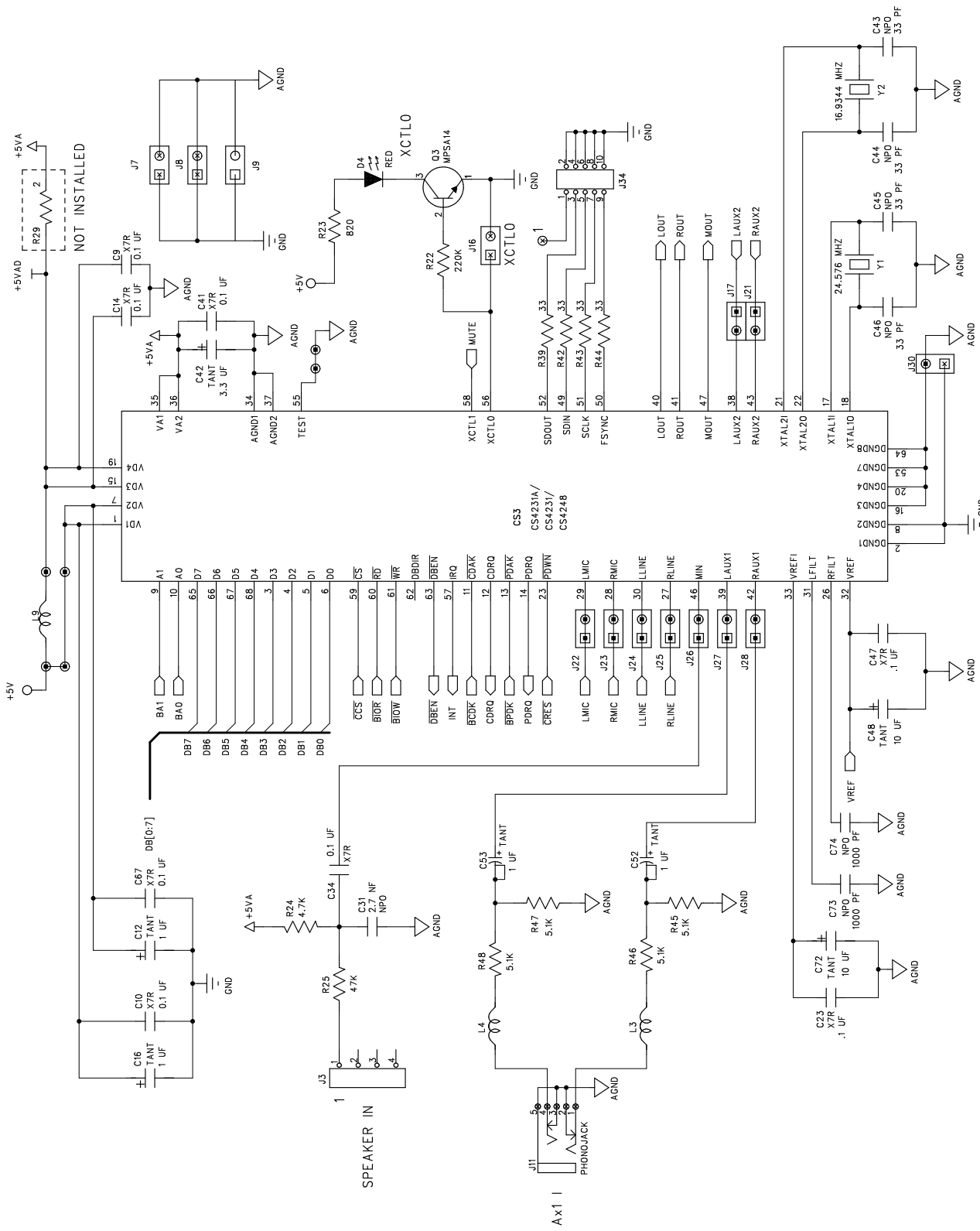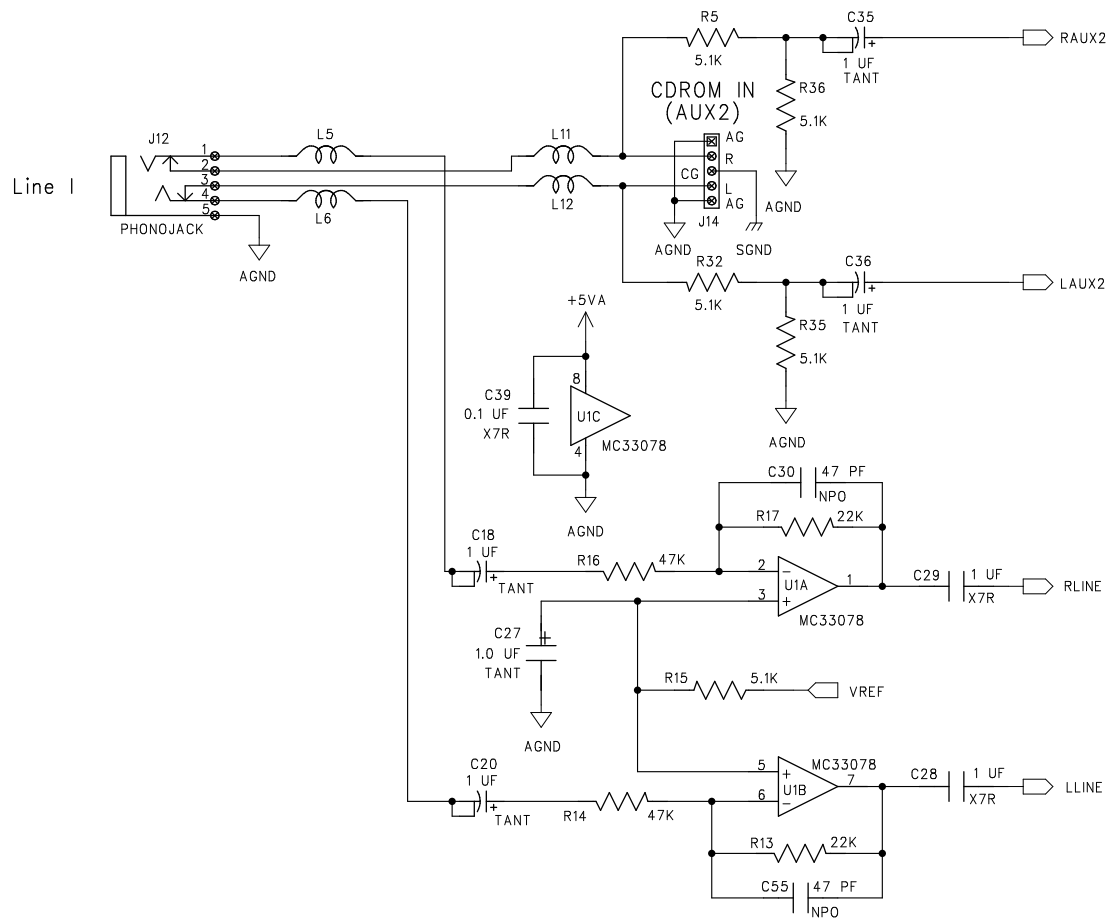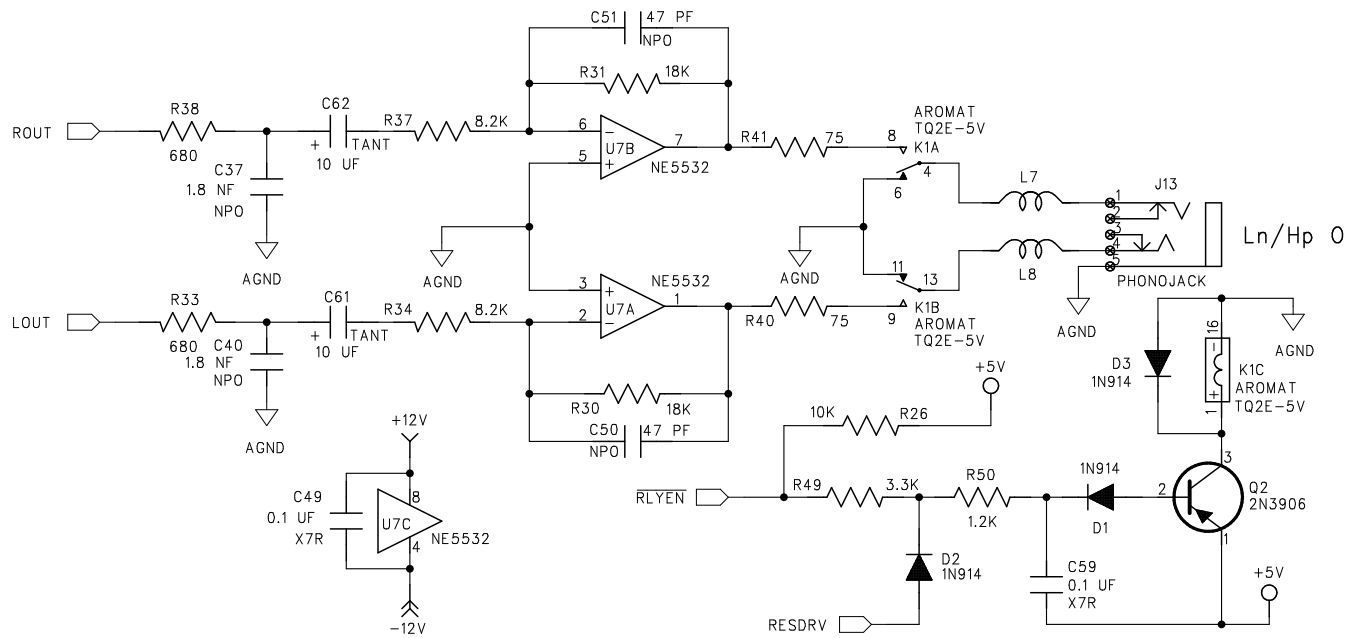
Figure 1. CS4231 & Aux1 In
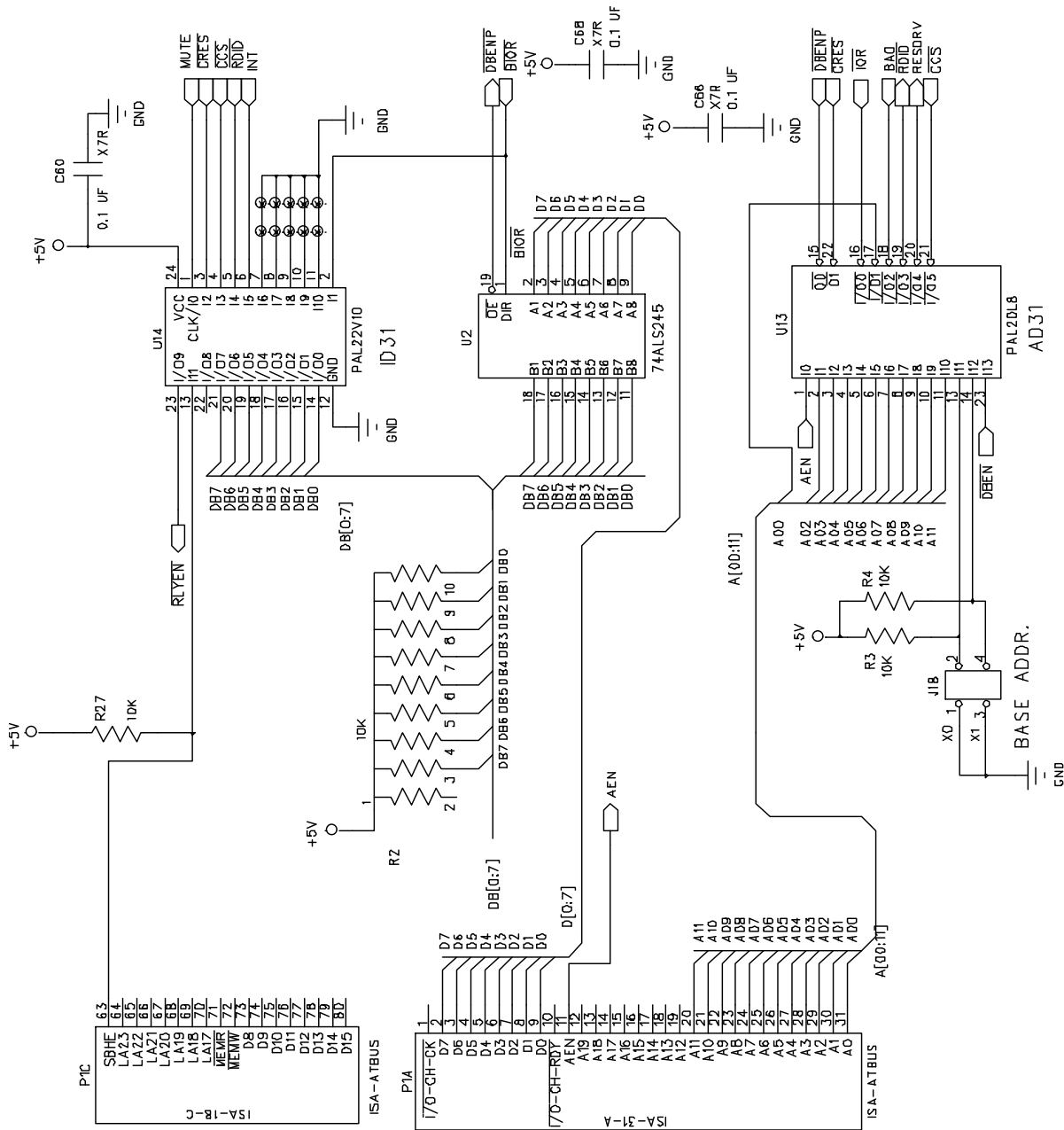
Figure 2. Microphone In

Figure 3. Mono Speaker Out

Figure 4. Line In & CDROM In (Aux2)

Figure 5. Line/Headphone Out
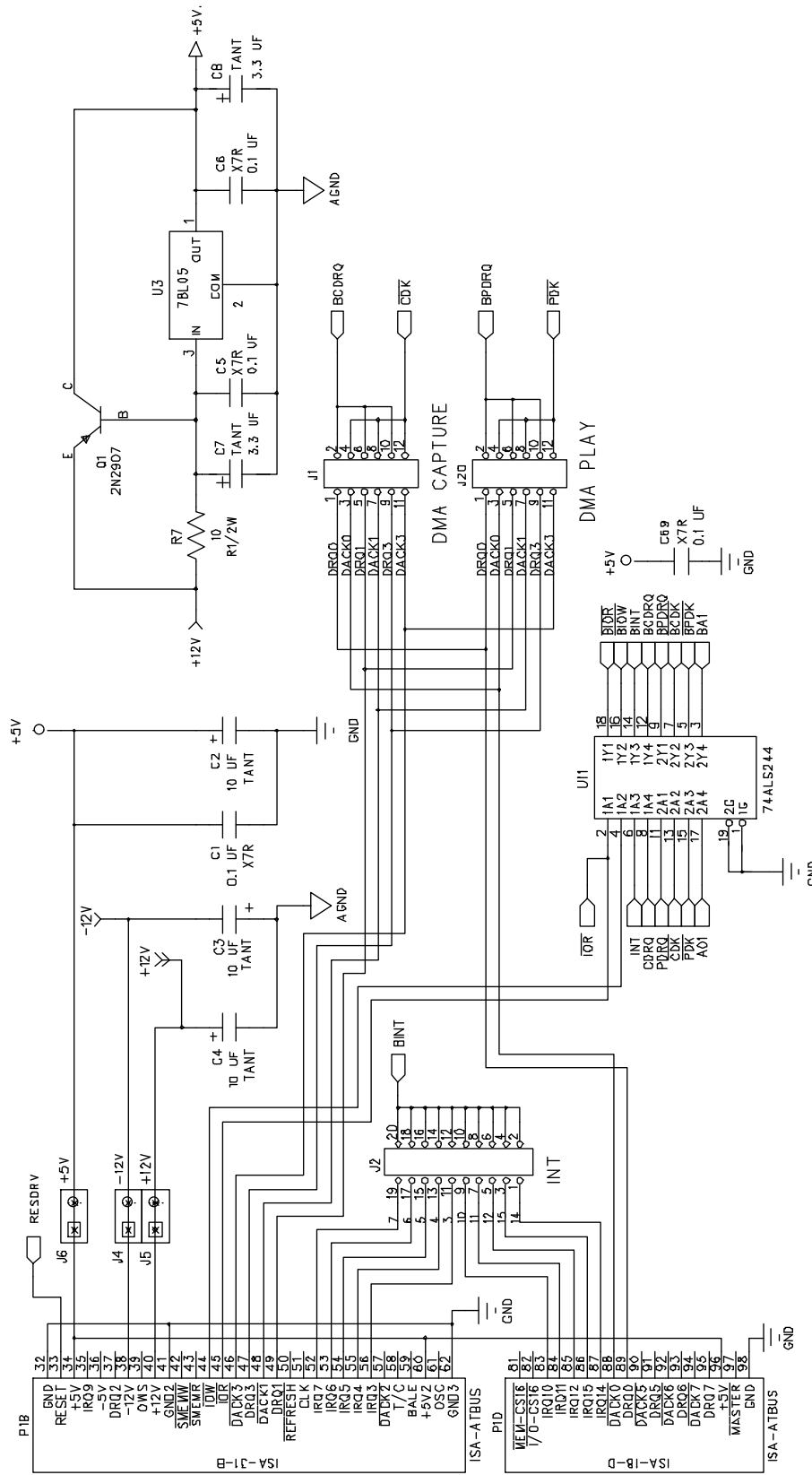
Figure 6. Address Decode and Board ID

Figure 7. Analog Power & Buffer

```
;PALASM Design Description
; CDB4231 Rev. D
;------------------------------ Declaration Segment ------------
TITLE     Address Decode for CS4231 and Read ID
PATTERN   AD31.PDS
REVISION 2.0
AUTHOR    Clif Sanchez
COMPANY   Crystal Semiconductor
DATE      10/15/93


CHIP   _AD31   PAL20V8


;------------------------------ PIN Declarations --------------
PIN  1           AEN              ; Eight addresses in all.
PIN  2           A2               ; The first four addresses are used by the
PIN  3           A3               ;     board PLD ID31 - address select RDID.
PIN  4           A4               ; The second four addresses are used by the
PIN  5           A5               ;     CS4231/4248.
PIN  6           A6
PIN  7           A7               ; Base Address: X1,X0 (header J18)
PIN  8           A8               ;               1  1   530-537, codec 534
PIN  9           A9               ;               1  0   604-60B, codec 608
PIN  10          A10              ;               0  1   E80-E87, codec E84
PIN  11          A11              ;               0  0   F40-F47, codec F44

PIN  13          X0               ; I - Address selector X1,X0:
PIN  14          X1               ; I -
PIN  15          /DBENP           ; O - Data Bus Enable Prime for 245 chip
PIN  16          /IOR             ; I - Qualifies Read ID enable
PIN  17          A0               ; I - from bus
PIN  18          BA0              ; O - Buffered A0 (PLD just used for buffer)
PIN  19          /RDID            ; O - Read ID register enable
PIN  20          RESDRV           ; I - Global Reset
PIN  21          /CCS             ; O - Chip Select for Codec
PIN  22          /CRES            ; O - Inverted RESDRV - to codec PWDN pin
PIN  23          /DBEN            ; I - Data Bus Enable from codec

;------------------------------ Boolean Equation Segment ------
EQUATIONS


/BA0     = /A0

RDID     =  /A11*A10*/A9* A8*/A7*/A6* A5* A4*/A3*/A2*/AEN*IOR* X1* X0 ; 530-533
         + /A11*A10* A9*/A8*/A7*/A6*/A5*/A4*/A3* A2*/AEN*IOR* X1*/X0 ; 604-607
         +  A11*A10* A9*/A8* A7*/A6*/A5*/A4*/A3*/A2*/AEN*IOR*/X1* X0 ; E80-E83
         +  A11*A10* A9* A8*/A7* A6*/A5*/A4*/A3*/A2*/AEN*IOR*/X1*/X0 ; F40-F43

CCS      =  /A11*A10*/A9* A8*/A7*/A6* A5* A4*/A3* A2*/AEN* X1* X0 ; 534-537
         + /A11*A10* A9*/A8*/A7*/A6*/A5*/A4* A3*/A2*/AEN* X1*/X0 ; 608-60B
         +  A11*A10* A9*/A8* A7*/A6*/A5*/A4*/A3* A2*/AEN*/X1* X0 ; E84-E87
         +  A11*A10* A9* A8*/A7* A6*/A5*/A4*/A3* A2*/AEN*/X1*/X0 ; F44-F47

DBENP    = DBEN
         + /A11*A10*/A9* A8*/A7*/A6* A5* A4*/A3*     /AEN* X1* X0 ; 530-537
         + /A11*A10* A9*/A8*/A7*/A6*/A5*/A4*/A3* A2*/AEN* X1*/X0 ; 604-607
         + /A11*A10* A9*/A8*/A7*/A6*/A5*/A4* A3*/A2*/AEN* X1*/X0 ; 608-60B
         +  A11*A10* A9*/A8* A7*/A6*/A5*/A4*/A3*     /AEN*/X1* X0 ; E80-E87
         +  A11*A10* A9* A8*/A7* A6*/A5*/A4*/A3*     /AEN*/X1*/X0 ; F40-F47


CRES     = RESDRV
```

Address PLD - AD31

```
;PALASM Design Description
;------------------------------- Declaration Segment ------------
TITLE     Read ID + relay enable
PATTERN   ID31.PDS
REVISION 2.0
AUTHOR    Clif Sanchez
COMPANY   Crystal Semiconductor
DATE      10/28/93

CHIP  _ID31  PAL22V10

;------------------------------- PIN Declarations --------------
PIN   1             MUTE            ; I - from Codec XCTL1 pin, Software Mute
PIN   2             /BIOR           ; I - buffered /IOR from 244
PIN   3             /CRES           ; I - inverted RESDRV from the AD31 PLD
PIN   4             /CCS            ; I - codec chip select, used for ACCESS
PIN   5             /RDID           ; I - Read ID chip select, from the AD31 PLD
PIN   6             INT
PIN   7             NC
PIN   8             NC
PIN   9             NC
PIN   10            NC
PIN   11            NC

PIN   13            SBHE            ; I
PIN   14            D0              ; O - Data Bus, Enabled for /RDID
PIN   15            D1              ; O    Places Read on the data bus
PIN   16            D2              ; O
PIN   17            D3              ; O
PIN   18            D4              ; O
PIN   19            D5              ; O
PIN   20            D6              ; O
PIN   21            D7              ; O
PIN   22            ACCESS          ; O - True after first read of the codec
PIN   23            /RLYEN          ; O - Relay Enable
;------------------------------- Boolean Equation Segment ------
EQUATIONS

D0 = GND
D0.TRST = RDID

D1 = GND
D1.TRST = RDID

D2 = VCC
D2.TRST = RDID

D3 = GND
D3.TRST = RDID

D4 = GND
D4.TRST = RDID

D5 = GND
D5.TRST = RDID

D6 = /INT
D6.TRST = RDID

D7 = SBHE
D7.TRST = RDID
```
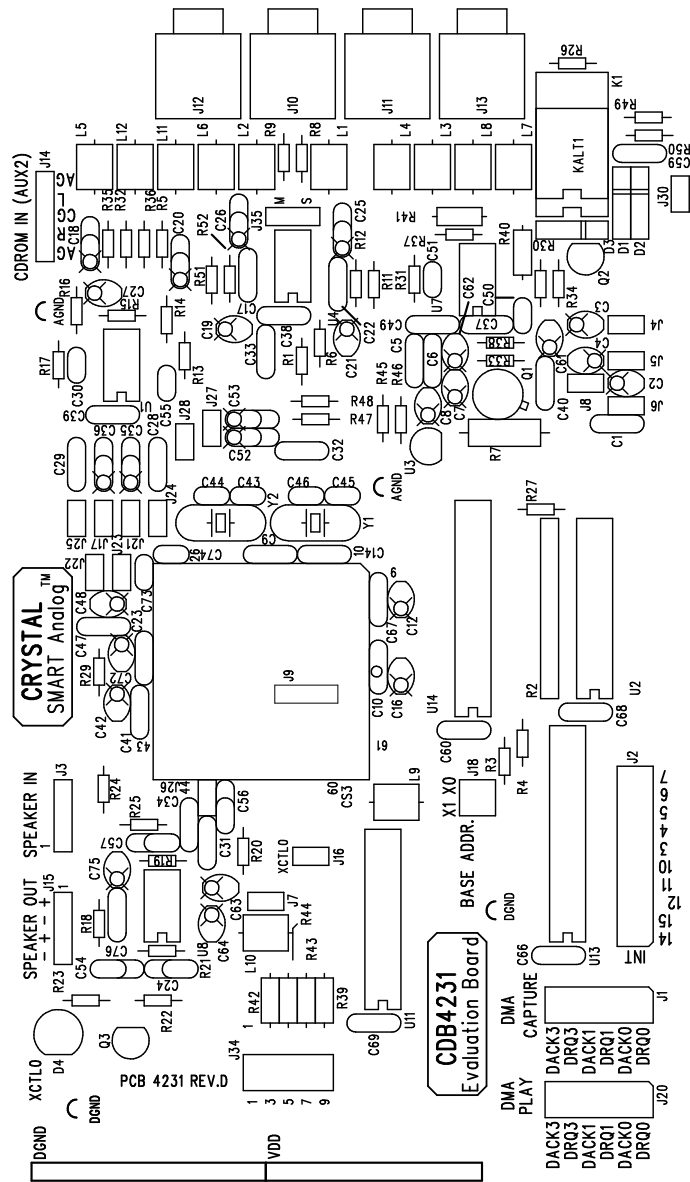
Board ID PLD - ID31

```
ACCESS  = ACCESS * /CRES
         + CCS * BIOR * /CRES

RLYEN = ACCESS * /MUTE
```

Board ID PLD - ID31 (continued)

Figure 8. Silk Screen
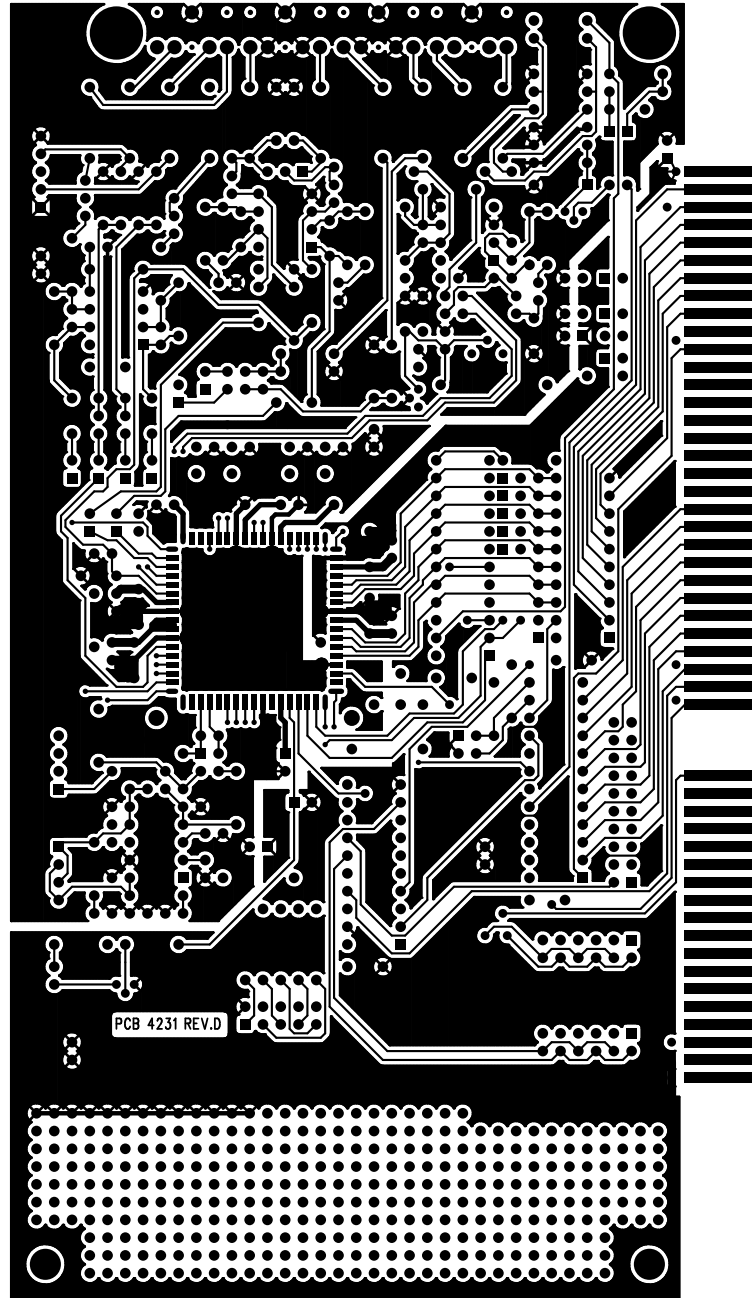
Figure 9. Component Side (Top , 1st Layer)
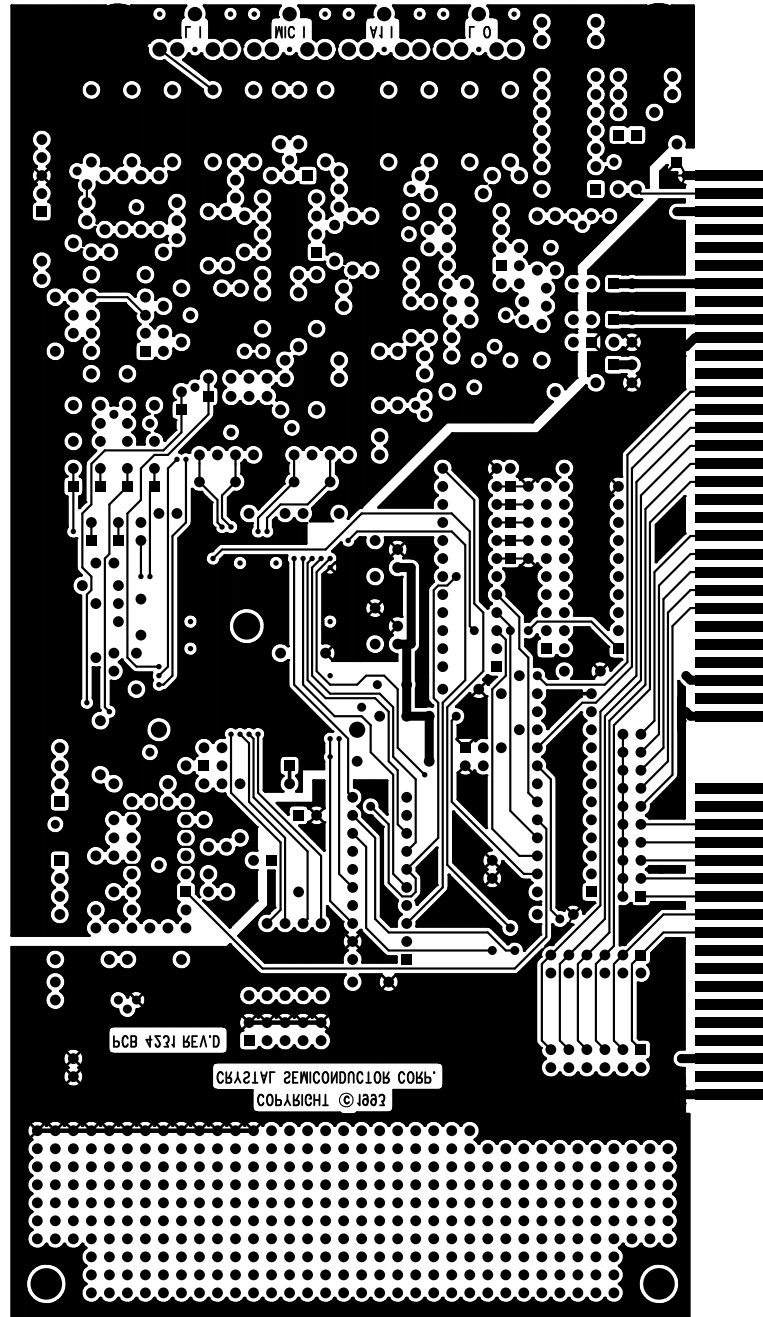
PCB 4231 REV.D
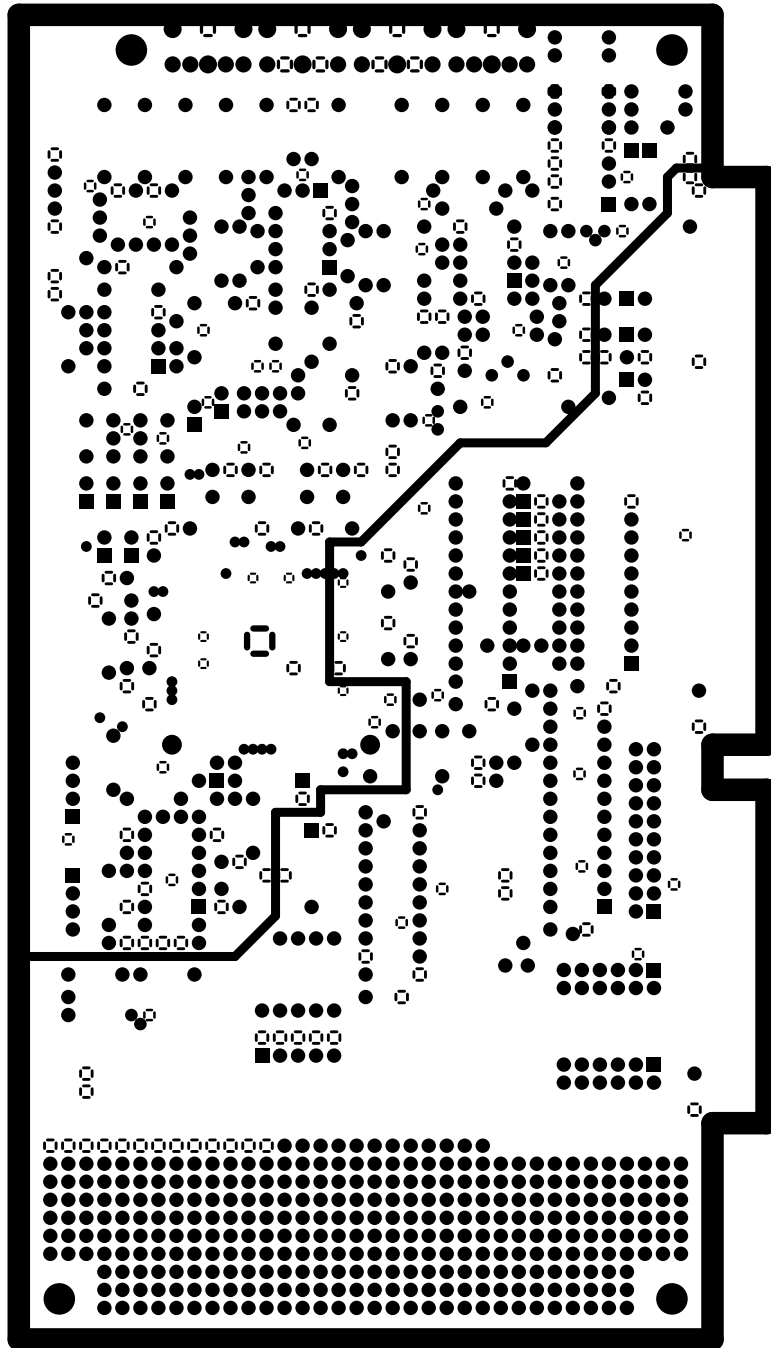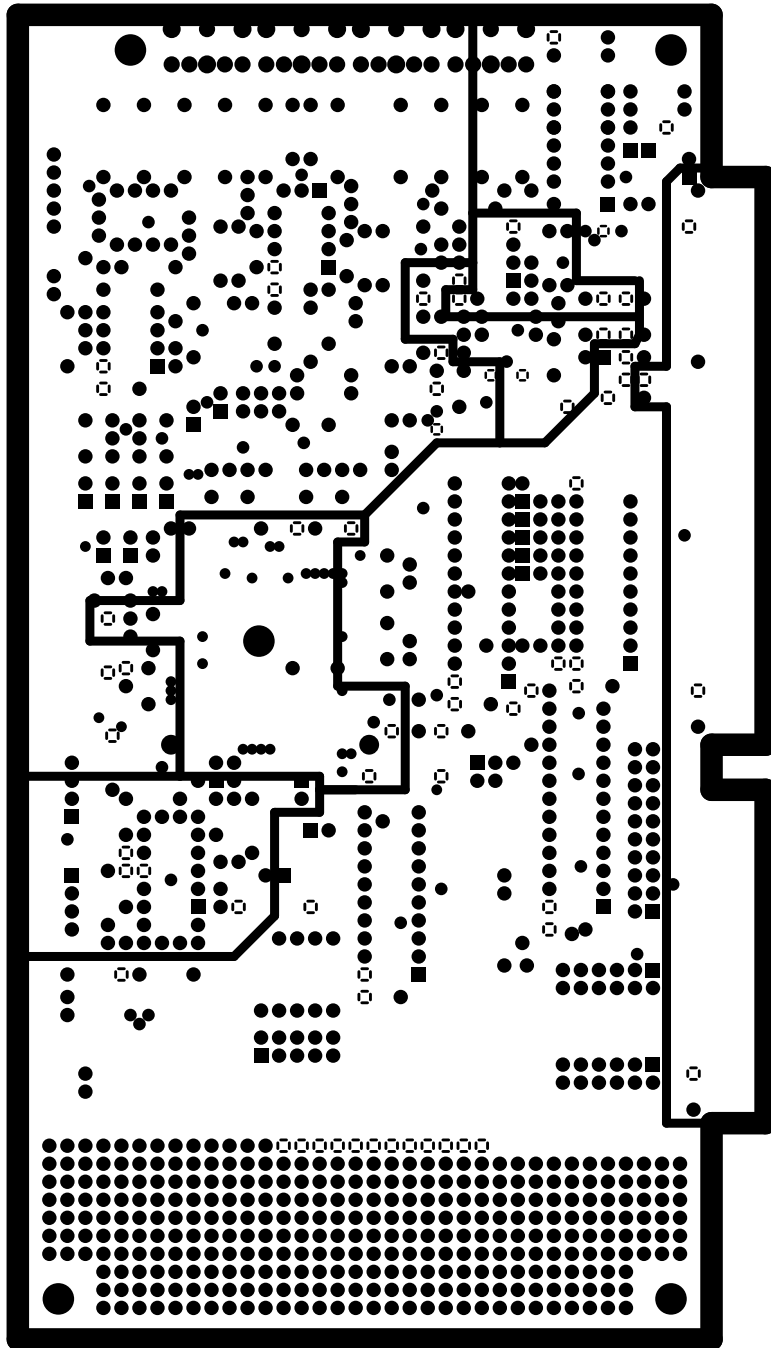
Figure 10. Solder Side (Bottom, 4th Layer)

Figure 11. Ground (2nd Layer - Inverse)

Figure 12. Power (3rd Layer - Inverse)