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PRELIMINARY INFORMATION

CS8230 AT/386 CHIPSET DATASHEET
ADDENDUM

A) CORRECTIONS
B) CS8230-25 TIMING SPECIFICATION: 25 MHz SPEC
C) INTERFACING 80386 TO 80387
D) CS8230 PRODUCT UPDATES
E) 82C302 REV C CHANGES
F) DK8230 ANOMALY SHEETS

JANUARY 27, 1989
PA062.1/1-89
REV. 1.0

Followings are the addendum to the CS8230: AT/386 CHIPSet preliminary data sheet.

The addendum is broken into six sections;

A) Corrections to the existing preliminary data sheet
B) 25 MHz timing parameters and timing diagrams
C) Interfacing the 80386 to 80387 NPU
D) Latest CS8230 AT/386 CHIPSet product update.
E) Changes to 82C302 rev. C.
F) Current DK8230 anomaly sheets

2

SECTION A

CORRECTIONS TO THE EXISTING PRELIMINARY DATA SHEET

3

The following section provides the corrections to the CS8230 data sheet (preliminary).

Page 2, Icc worst case is 20 mamps and not 20 Amps.

Page 5, IOW ADDRESS BUFFERS should be LOW ADDRESS BUFFERS.

Page 7, in the READY- signal description, the external pull up resistor should be 10K Ohms instead of 1K Ohms.

Page 8, in IOCHRDY description, lowW should be low,.

Page 12, pin numbers for the XMEMR- and XMEMW- signals are reversed. The XMEMR- signal should be on pin 35 and the XMEMW- signal should be on pin 36.

Page 12, in the HIROM- signal description, A<31:A24> should be A<31:24>.

Page 14, pin 62 is VDD and should be tied to Vcc (+5V).

Page 25, in the last paragraph of column 1, 82C302 should be 82C301.

Page 27, table 1-1 should be as follow:

CLK2IN	SCLK	Ratio	BCLK	SYSCLK
24	12	/2	12	6
32	16	/2	16	8
32	16	/3	10.7	5.4
40	20	/2	20	10
50	25	/3	16.7	8.4

Page 30, in figure 1-3, the IO ADDR for port B should be 61 instead of 62.

Page 34, on t101, CLK should be CLK2.

Page 34, t106 (min) is 1 ns and t106 (max) is 6 ns at 16 and 20 MHz.

Page 34, t109 (min) is 2 ns.

Page 35, t127 (min) and t128 (min) are both 3ns at 16 and 20 MHz.

Page 35, t131 (min) and T133 (min) are both 25 ns at 16 and 20 MHz.

Page 35, on t135 and t136, SBHE- should be XBHE- at 16 and 20 MHz.

Page 35, t138 (min) is 0 ns at 16 and 20 MHz.

Page 35, t139 (min) is 3 ns and t139 (max) is 15 ns at 16 and 20 MHz.

Page 35, t140 (min) is 3 ns for both 16 and 20 MHz.

page 35, t148 (min) is 25 ns for both 16 and 20 MHz. The 17 ns typical value is not correct and should be taken away.

4

Page 38, the timing diagram is missing the HOLD signal. The timing diagram should be as shown in figure 1.

Page 40, that timing diagram is missing several parameters and labels. It should be as shown in figure 2. Also, MALE- is not shown in the right phase.

Page 41, in the second timing diagram, 0WS should be 0WS-.

Page 43, in 82C301 timing diagram, REF should be REF-.

Page 46, Row and Column address generation logic for 1 M DRAM is changed in the 82C302 rev C. Section E of this addendum sheet will show the new address generation for the row and column addresses.

Page 52, REG8 bit 3, the function of 1 and 0 is reversed. When REG8<3>=0, then the boot/BIOS ROM located just below 16MB is disabled. The boot/BIOS ROM below 16MB is enabled when REG8<3>=1.

Page 52, REG8 bit is supposed to be used to write protect the middle boot space. However, this bit doesn't function properly. Regardless of this bit set to zero or one, the 256KB RAM located above 0FC0000 is readable and writeable.

The following table shows the result of different setting of REG8<4:3>:

REG8<3>	REG8<4>	RESULT
0	0	Read and Write to the RAM located at 256K below 16M is possible.
0	1	Read and Write to the RAM located at 256K below 16M is possible.
1	0	Read ROM and Write to the RAM located at 256K below 16M is possible.
1	1	Read ROM and Write to the RAM located at 256K below 16M is possible.

Page 53, Index 9, bit 3,2,1 and 0 default values are 0,0,0 and 1 respectively. That is, only the ROM at 960K F0000-FFFFFH (BIOS) is enabled.

Page 56, the DC characteristics of the 82C302 is missing. It is shown in table 1.

Page 56, t221 is not a valid parameter and needs to be removed from the data book

Page 57, t227 is not a valid parameter and needs to be removed from the data book

Page 59, second t272 should be t273.

Page 59, on t276 description, MALE- should be ADS-.

Page 59, t293 and t294 parameters are missing. They should be as follow:

t293 IOCHRDY going low from XMEMR- or XMEMW-   32 ns (max)
t294 IOCHRDY going high from CAS- (read cycle)   1/2 CLK2 + 8 ns (max)
t295 IOCHRDY going high from CAS- (write cycle)   9 ns (max)

Page 60, the second S2 should be Si

Page 60, on IOCHRDY signal, t293 doesn't have a right arrow. It should be as shown in figure 3.

Page 60, on IOCHRDY signal, t225 should be t295.

Page 60, HLDA1 doesn't finish. It should be as shown in figure 3.

Page 61, ADS should be ADS-.

Page 61, on the READY- timing, t237 is shown incorrectly. It is READY- input setup time to CLK2 low and it is from the time that the READY- goes active til the falling edge of CLK2 in phase 2 of last Tw.

Page 62, the labels on some those timing diagram doesn't show a right polarity. It should be as shown in figure 4.

Page 62, on the 82C302 refresh timing,the errow on RAS1- should be t243.

Page 66, there is an extra arrow on the CASi- timing diagram.

Page 67, the 82C302 write miss cycle with RAS low, the ADS- for the second pipeline cycle is not shown correctly. ADS- should go active in the first T1w and stay active til READY- for the previous cycle has come.

Page 68, the 82C302 DRAM write hit cycle, the ADS- for the second pipeline cycle is not shown correctly. ADS- should go active in the T1w and stay active til READY- for the previous cycle has come.

Page 68, there are arrows with no label on the MALE- timing, they need to be removed.

Page 69, the 82C302 DRAM read cycle with RAS being high, the ADS- for the second and third pipeline cycle is not shown correctly. ADS- should go active in the first T1w and stay active til READY- for the previous cycle has come. And then, ADS- sould go active again in the second T1w and stay active until the next ready.

Page 71, in table 3-1. decode conditions for the HIROM- signal should be A<31:24> = FFH.

Page 82, in the decoder section of 82A304, XDIR should be XDIR-.

Page 84, all the labels are scrambled. It should be as shown in figure 5.

Page 86, in the 82C304 DC characteristics, Icc should be 100 mA and NOT 1000 uA.

page 94, the write to 8 bit device diagram is missing some labels. It should be.as shown in figure 6.

Section A

Page 99, in the 82C305 DC characteristics, Icc should be 20 mA and NOT 100 uA.

Page 99, at the bottom of the page in the NOTES section, PP<3:> should be PP<3:0>.

Page 106, t626 is missing. It should read as follow:

t626   SMEMW- (or SMEMR-) LO to HI-Z transition delay from low to high transition of LMEGCS   t626 (min)=6 ns, t626 (max)=28 ns

Page 107, ALT signal on t648 should be ALE.

Page 108, ALT signal on t649 should be ALE.

7

Section A

In addition to these corrections, in the preliminary data book, functionality of register 2A was not defined. Register 2A resides in the 82C302 and only one bit is used (bit 0). It is defined as follow:

REG2A<0>: Enable/Disable the lowest 256K RAM on the local memory bus.

        0   Disable. AF32- = 1
        1   Enable (default). AF32- = 0

When this bit is set (REG2A<0>=1), any access to the lower 256K of memory will be a local memory cycle and will result in generation of AF32-.

When this bit is zero (REG2A<0>=0), any access to the lower 256K of memory will be considered as a AT bus cycle and therefore, AF32- will not be generated.

Following timing specifications are to be added to the current data book.

82A303/304

ATEN- to data valid	30 ns
MASTER- to data valid	30 ns
HLDA1 to data valid	30 ns
ATEN- to data tristate	30 ns
MASTER- to data tristate	30 ns
HLDA1 to data tristate	30 ns

82A305

SDIR to data valid	30 ns
ATEN- to data valid	30 ns
MRD- to data valid	30 ns
SDIR to data tristate	30 ns
ATEN- to data tristate	30 ns
MRD- to data tristate	30 ns

8

Figure 1.

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82C301 TIMING DIAGRAMS

9

Figure 2.

CHIPS

82C301 TIMING DIAGRAMS

10
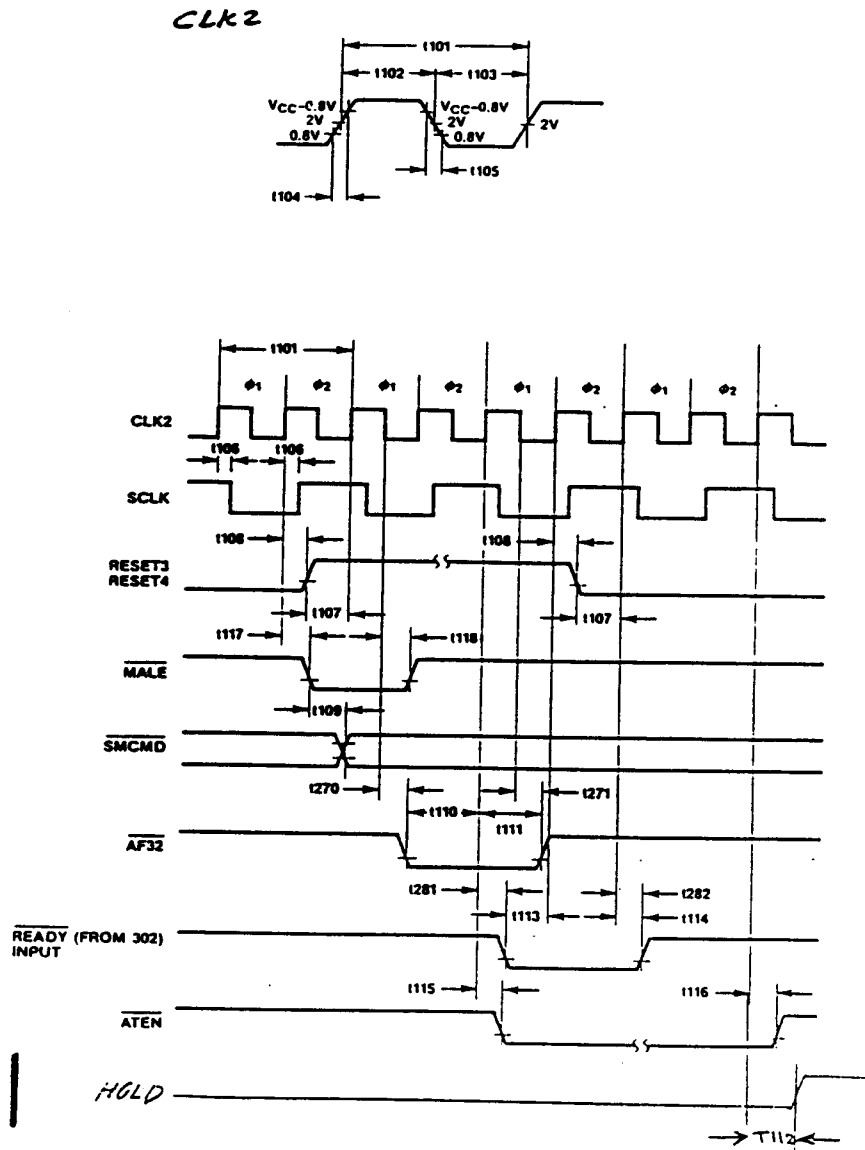
CHIPS

82C302 Absolute Maximum Ratings

Parameter	Symbol	Min.	Max.	Units
Supply Voltage	V_{CC}	—	7.0	V
Input Voltage	V_I	-0.5	5.5	V
Output Voltage	V_O	-0.5	5.5	V
Operating Temperature	T_{op}	-25	85	C
Storage Temperature	T_{stg}	-40	125	C

NOTE: Permanent device damage may occur if Absolute Maximum Ratings are exceeded. Functional operation should be restricted to the conditions described under Operating Conditions.

82C302 Operating Conditions

Parameter	Symbol	Min.	Max.	Units
Supply Voltage	V_{CC}	4.75	5.25	V
Ambient Temperature	T_A	0	70	C

82C302 DC Characterisites

Parameter	Symbol	Min.	Max.	Units
Input Low Voltage	V_{IL}		0.8	V
Input High Voltage	V_{IH}	2.0		V
Output Low Voltage I_{OL}=8mA (Note 1)	V_{OL}		0.45	V
Output High Voltage I_{OH}=-200 μA	V_{OH}	2.4		V
Input Current $0 < V_{IN} < V_{CC}$	I_{IL}		±10	μA
Output Short Circuit Current V_O=0V	I_{OS}	TBD	TBD	mA
Input Clamp Voltage	V_{IC}		TBD	V
Power Supply Current @ 8 MHz Clock	I_{CC}		20	mA
Output Hi-Z Leak Current $0.45 < V_{OUT} < V_{CC}$	I_{OZ1}		±10	μA

NOTE:
1. SYSCLK, $\overline{DWE}$, $\overline{RAS<3:0>}$, $\overline{CAS}$, $\overline{CAS<3:0>}$ have I_{OL} = 8mA. All other outputs and I/O pins have I_{OL} = 4mA. In all cases all I_{OL} = I_{OH} for the pin.

82C302

11

Figure 3.

CHIPS

82C302 TIMING DIAGRAM (RESET SEQUENCE)

82C302 DMA Cycle

82C302

60

12
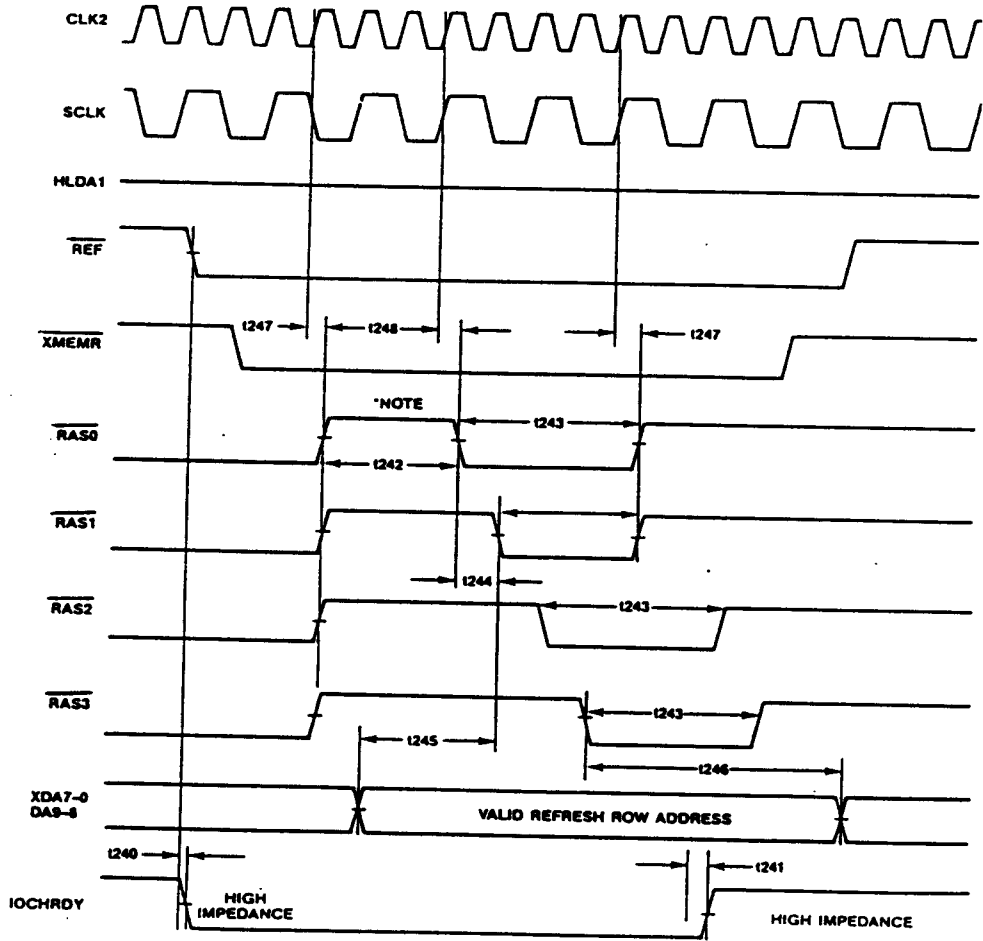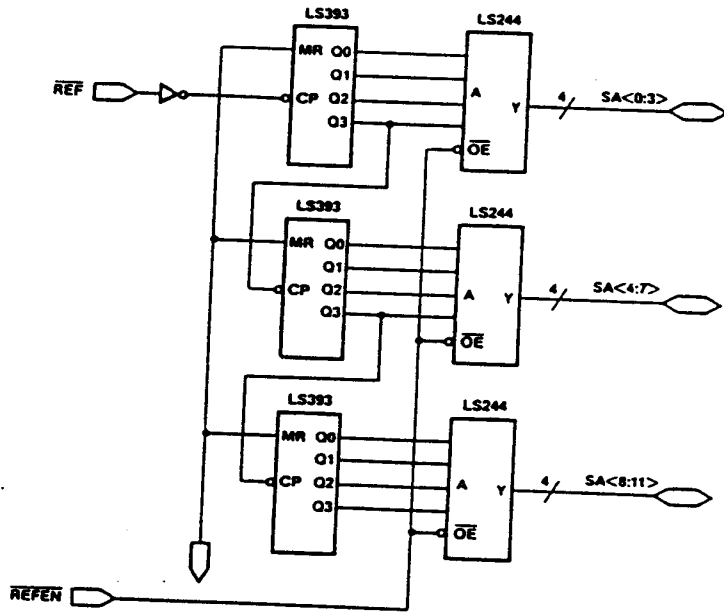
Figure 4.

CHIPS

82C302 REFRESH CYCLE WAVEFORM

*NOTE: Add 2 more clock cycles if either Bit 7 of register 11 is 1 or Bit 7 of register 13 is 1.
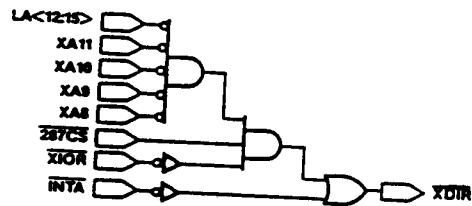
13

Figure 5.

CHIPS

82A304 AT Bus Refresh Address Generation Circuitry

82A304 TTL Equivalent XDIR Generation Logic
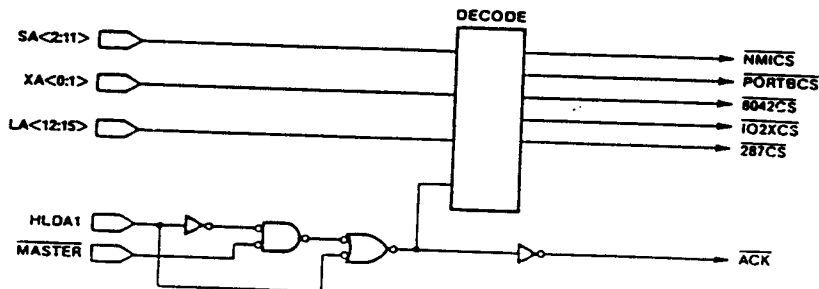
82A304 TTL Equivalent Chip Select Generation Circuitry

82A304

84

14

Figure 6.

CHIPS

CPU Read from 8-Bit Devices

AC<3:0> = 5,6,7,8
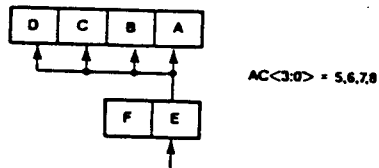
CPU Read from 32-Bit Device

AC<3:0> CH
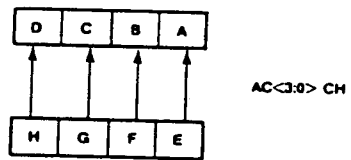
CPU Read from 16-Bit Devices

AC<3:0> 9,A

Write to 32-Bit Device

AC<3:0> = 4H

ENABLE A,B,C,D
ENABLE E,F,G,H

Write to 8-Bit Device

ENABLE C,D,E,F

AC<3:0> = 2

ENABLE D,E,F

AC<3:0> = 3

AC<3:0> = 0
ENABLE A,B,E,F

AC<3:0> = 1
ENABLE C,D,E,F

Write to 16-Bit Device

ENABLE A,B,E,F

AC<3:0> = 0

ENABLE SWAP
ENABLE B,E,F
AC<3:0> = 1

82A305

94

15
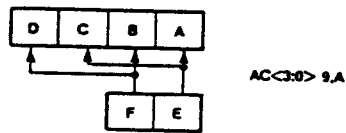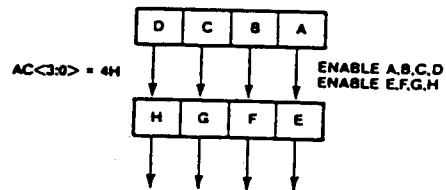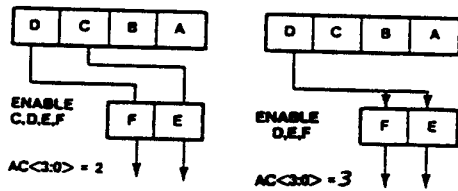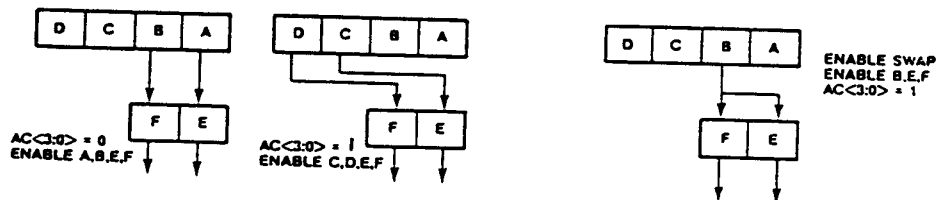
SECTION B

CS8230 -25 TIMING SPECIFICATION

CHIPS

Chips and Technologies, Incorporated

May 27, 1988

Dear Customer:

Attached is an addendum to the CS8230 Data Book which includes the preliminary specifications for the 25 MHz CS8230 CHIPSet. This data is based on CHIPS' best estimate of the timing requirements for a 25 MHz system. These estimates are based on extensive engineering lab work and testing. The timing specifications are subject to change when specific information relating to Intel's 25 MHz 80386 data sheet becomes publicly available.

Sincerely,

Nelson C. Chan
Product Manger
Systems Logic

NC/kls

Attachment

17

Following section provides the timing characteristics of the critical signals for the 25 MHz CS8230 AT/386 CHIPSet. The enclosed timing specifications need to be used in conjunction with the published CS8230 Data Book (preliminary).

Sym	Description	25 MHz	
		min	max
t101	CLK2 period	20 ns	125 ns
t102	CLK2 low time	7 ns	
t103	CLK2 high time	7 ns	
t104	CLK2 rise time		7 ns
t105	CLK2 fall time		7 ns
t109	SMSMD- delay from MALE- active	7 ns	
t110	AF32- setup time to CLK2	9 ns	
t113	READY- input setup time from CLK2	11 ns	
t191	MALE- active delay from ADS- falling		13 ns
t192	MALE- active delay from READY- low		17 ns
t270	AF32- active delay from CLK2		19 ns
t273	CASi- inactive delay from CLK2	17 ns	
t283	RASi- active delay from CLK2		16 ns
t286	CASi- active delay from CLK2		12 ns

To run the DK8230 AT/386 development board at 25 MHz, the following steps must be taken prior to changing the crystal from 32/40 MHz to 50 MHz (16/20 MHz system to 25 MHz system):

1) Change number of wait states for the local memory.
2) AT bus clock should be ATCLK input pin.
3) Might have to increase the number of wait states for I/O command delay and 8/16 bit command delay.

If you have access to the SETUP386 program, follow the following procedures:

1) Replace all required parts with the 25 MHz parts except the crystal and power up the system.
2) Run SETUP386
3) Select the "CHIP SETUP FOR THE 82C301".
4) Change the AT bus clock source to ATCLK input pin
5) Press ESC and return to the main menu.
6) Select the "CHIP SETUP FOR THE 82C302"
7) Change the number of wait states to 1 WS for banks 0,1,2,3.
8) Press ESC and return to the main menu.
9) Select the "POWER ON RESET"
10) Turn the power off and replace the 32/40 MHz crystal with the 50 MHz one.
11) Turn the system back on.
12) If you experience any difficulty with reading the hard disk or other AT expansion cards, Power down.
13) Replace the crystal back to the old one, and power up.
14) Run SETUP386.

18

Section B

15) Select the "CHIP SETUP FOR THE 82C301".
16) Increase the number of wait states for the IO command delay and 8/16 bit command delay.
17) Go back to step 8.

The main timing differences between the 20 MHz and 25 MHz CS8230 are in their local memory cycles. Following timing diagrams illustrates most of the local memory cycles for 20 and 25 MHz and point out the differences.

Figure 7 A&B show the timing diagrams for read cycle, page hit, non-pipelined mode for 20 and 25 MHz respectively.

Figure 8 A&B show the timing diagrams for read cycle, page hit, pipelined mode for 20 and 25 MHz respectively.

Figure 9 A&B show the timing diagrams for read cycle, RAS being inactive, non-pipelined mode for 20 and 25 MHz respectively.

Figure 10 A&B show the timing diagrams for read cycle, page miss, non-pipelined mode for 20 and 25 MHz respectively.

Figure 11 A&B show the timing diagrams for write cycle, page hit, pipelined mode for 20 and 25 MHz respectively.

Figure 12 A&B show the timing diagrams for write cycle, page miss, non-pipelined mode for 20 and 25 MHz respectively.

19

FIGURE 7 A: READ CYCLE, PAGE HIT, NON-PIPELINED MODE, 1 WS, 20 MHz.
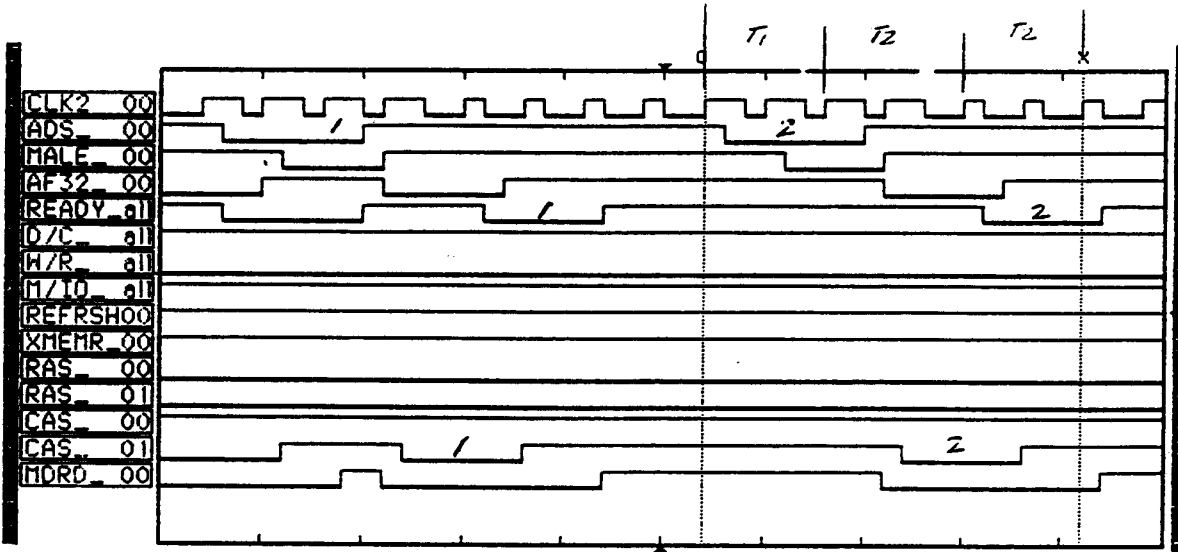
FIGURE 7 B: READ CYCLE, PAGE HIT, NON-PIPELINED MODE, 2 WS, 25 MHz.
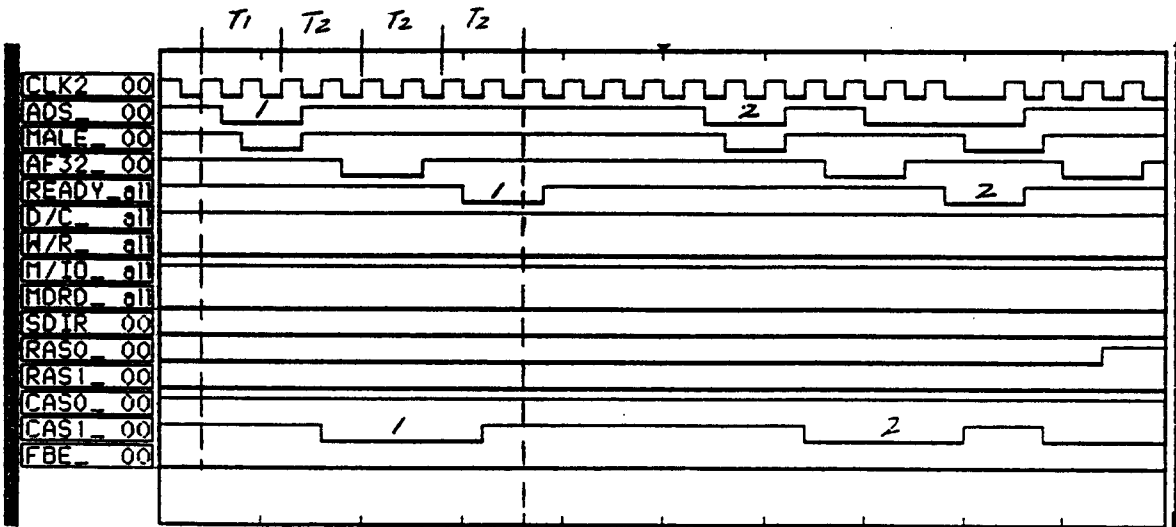
FIGURE 8 A: READ CYCLE, PAGE HIT, PIPELINED MODE, 0 WS, 20 MHz.

FIGURE 8 B: READ CYCLE, PAGE HIT, PIPELINED MODE, 1 WS, 25 MHz.

21

Section B

FIGURE 9 A: READ CYCLE, RAS BEING INACTIVE, NON-PIPELINED MODE, 2 WS, 20 MHz.
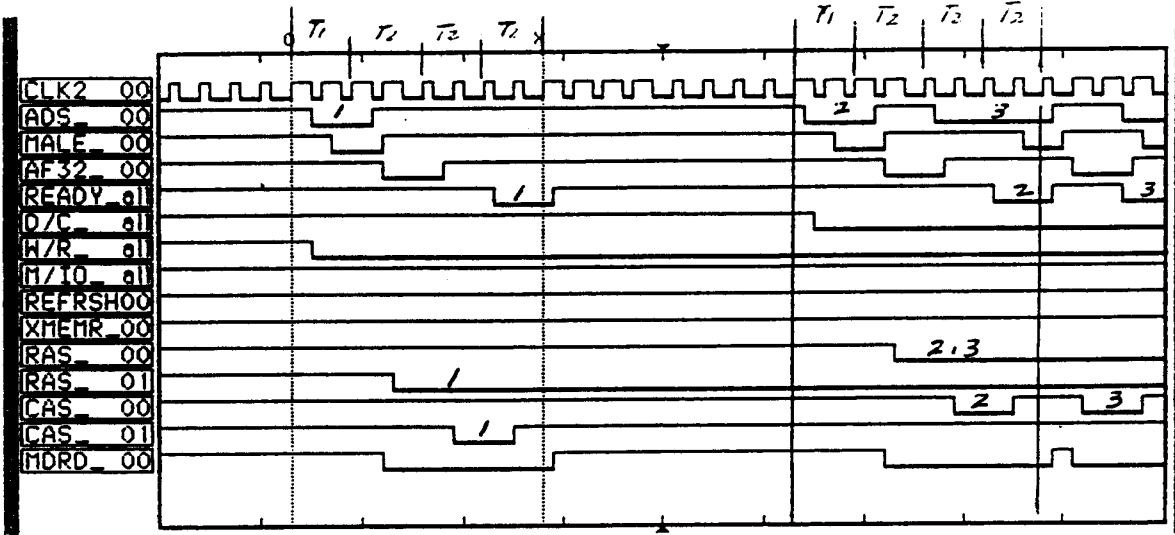
FIGURE 9 B: READ CYCLE, RAS BEING INACTIVE, NON-PIPELINED MODE, 3 WS, 25 MHz.

22
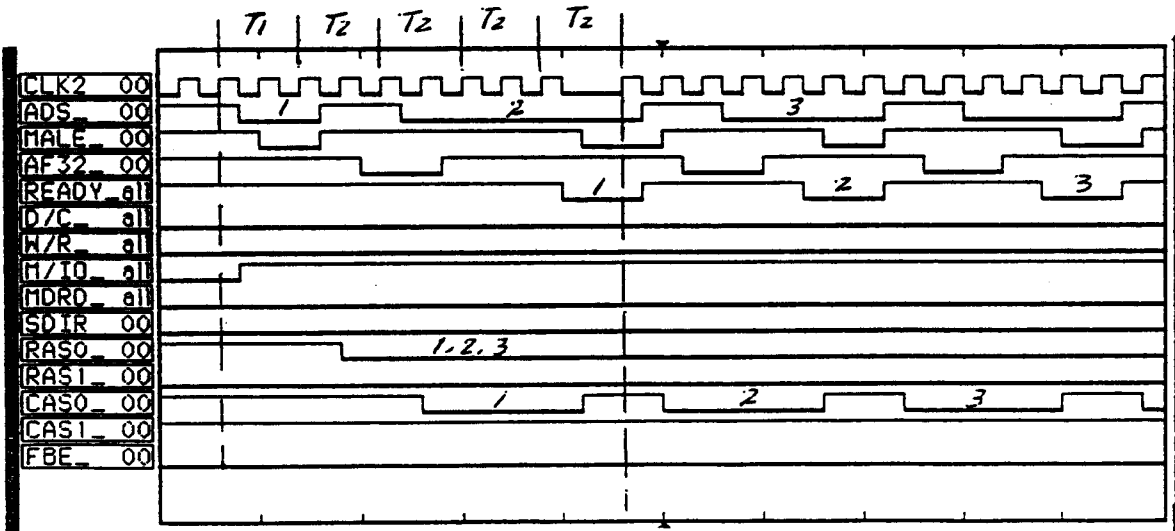
FIGURE 10 A: READ CYCLE, PAGE MISS, NON-PIPELINED MODE, 4 WS, 20 MHz.
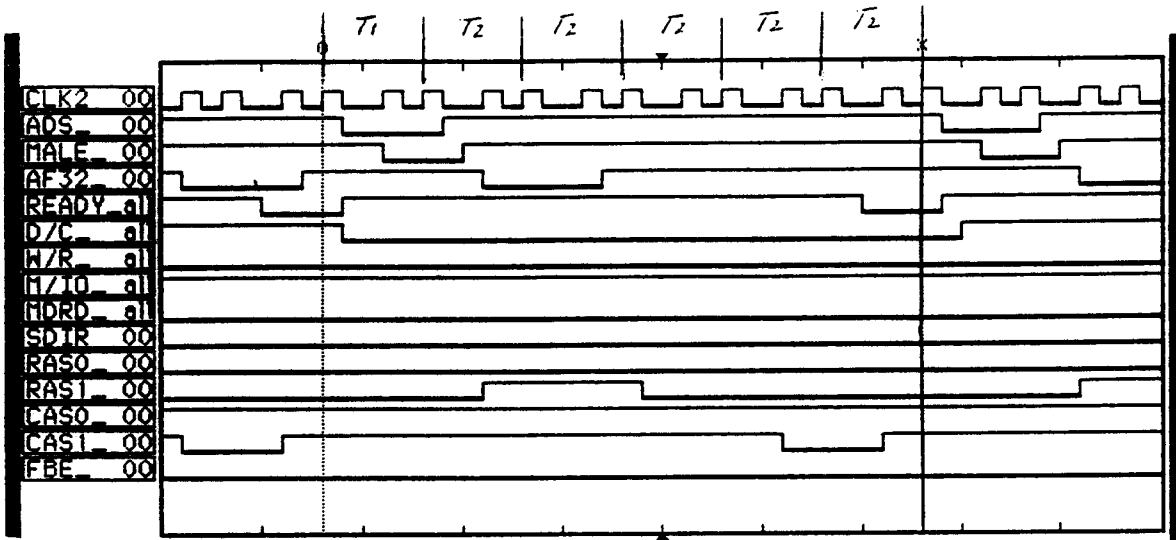
FIGURE 10 B: READ CYCLE, PAGE MISS, NON-PIPELINED MODE, 5 WS, 25 MHz.

23
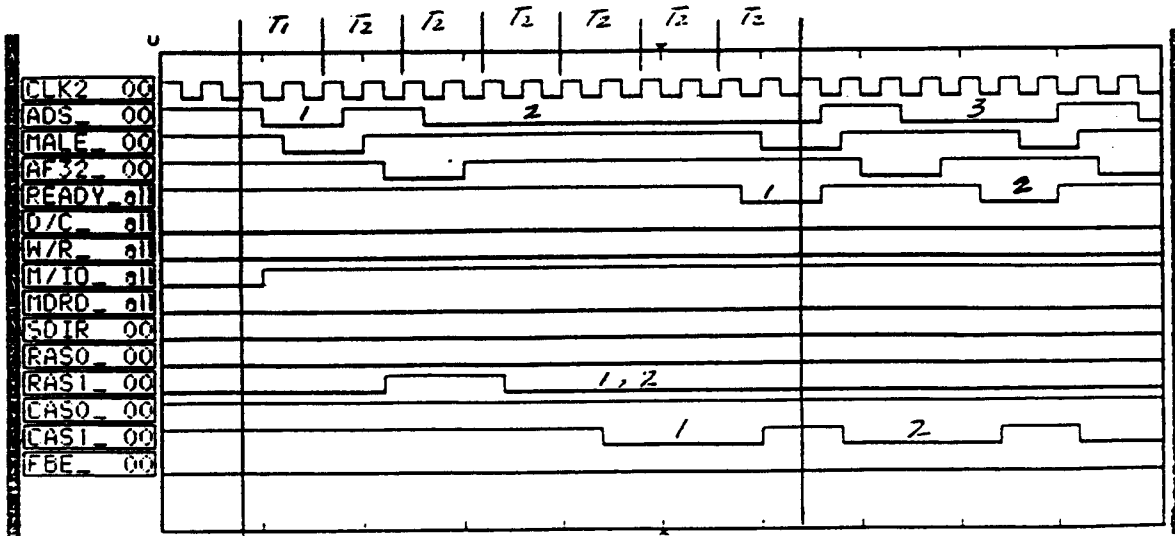
FIGURE 11 A: WRITED CYCLE, PAGE HIT, PIPELINED MODE, 1 WS, 20 MHz.
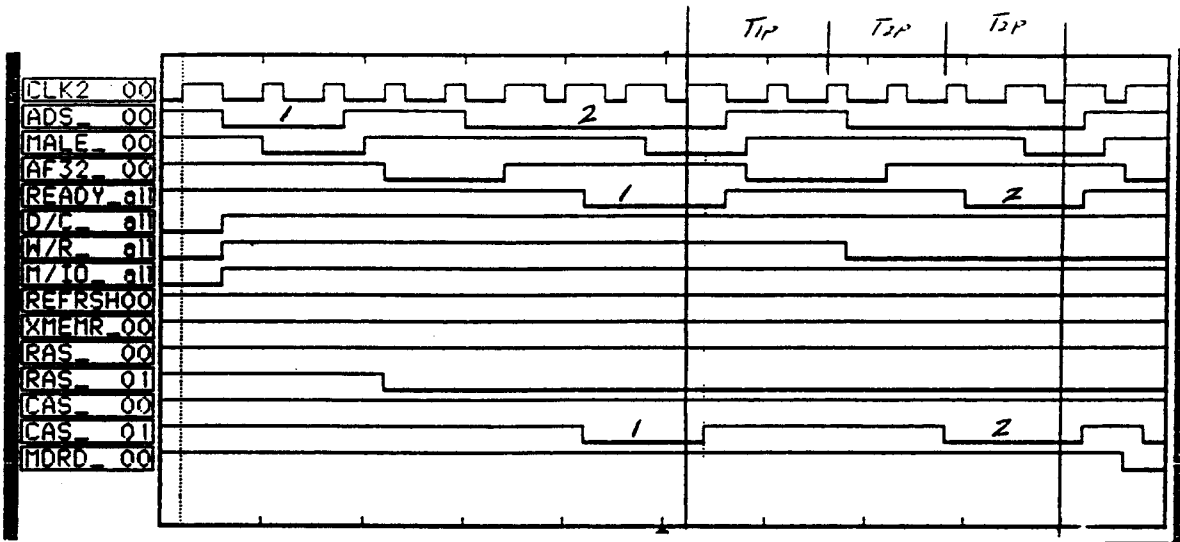
FIGURE 11 B: WRITE CYCLE, PAGE HIT, PIPELINED MODE, 2 WS, 25 MHz.

24
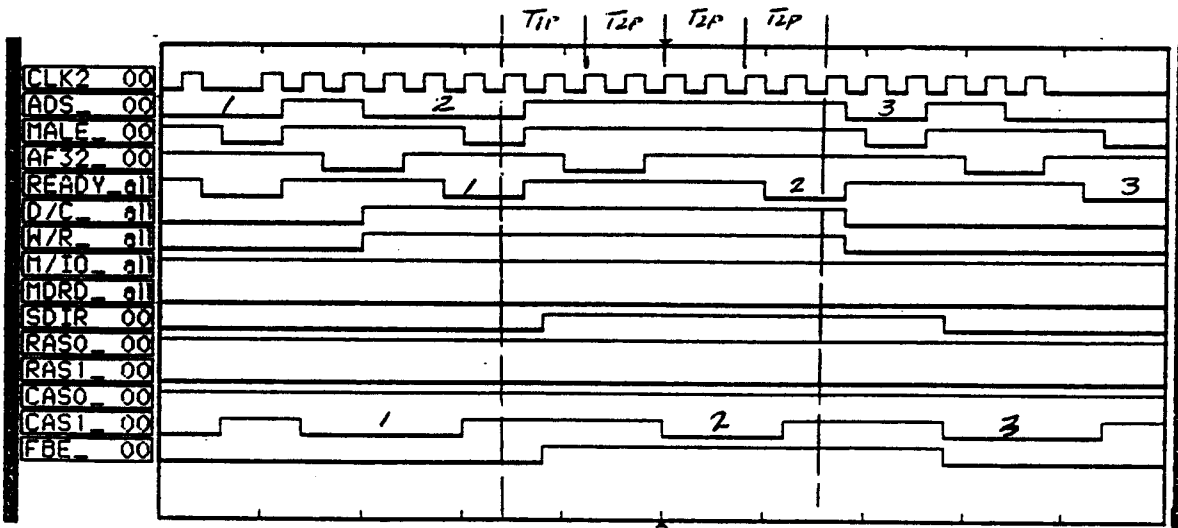
FIGURE 12 A: WRITE CYCLE, PAGE MISS, NON-PIPELINED MODE, 4 WS, 20 MHz.
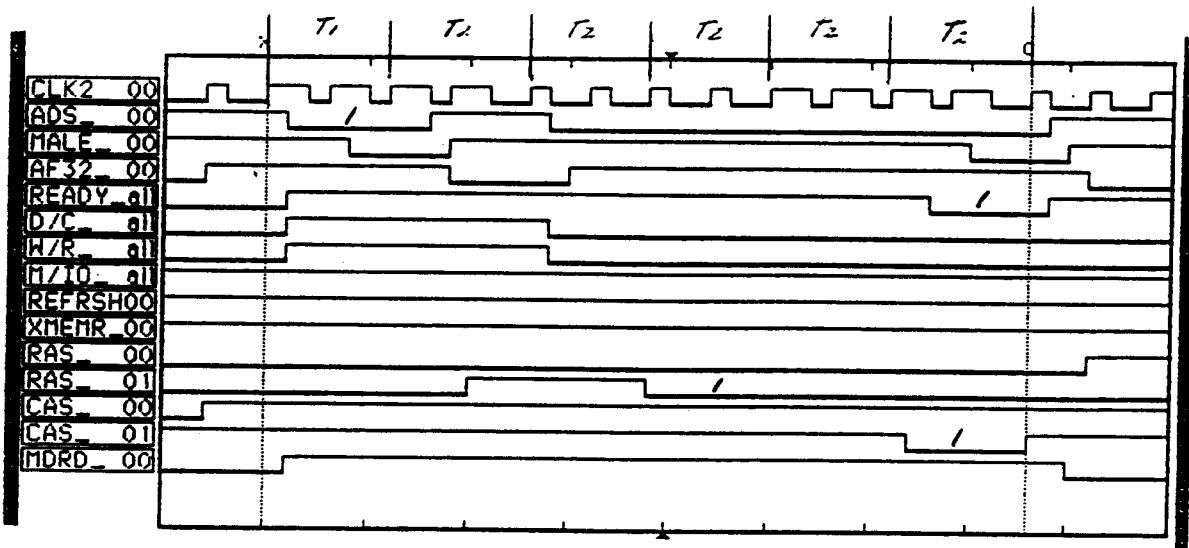
FIGURE 12 B: WRITE CYCLE, PAGE MISS, NON-PIPELINED MODE, 5 WS, 25 MHz.

25
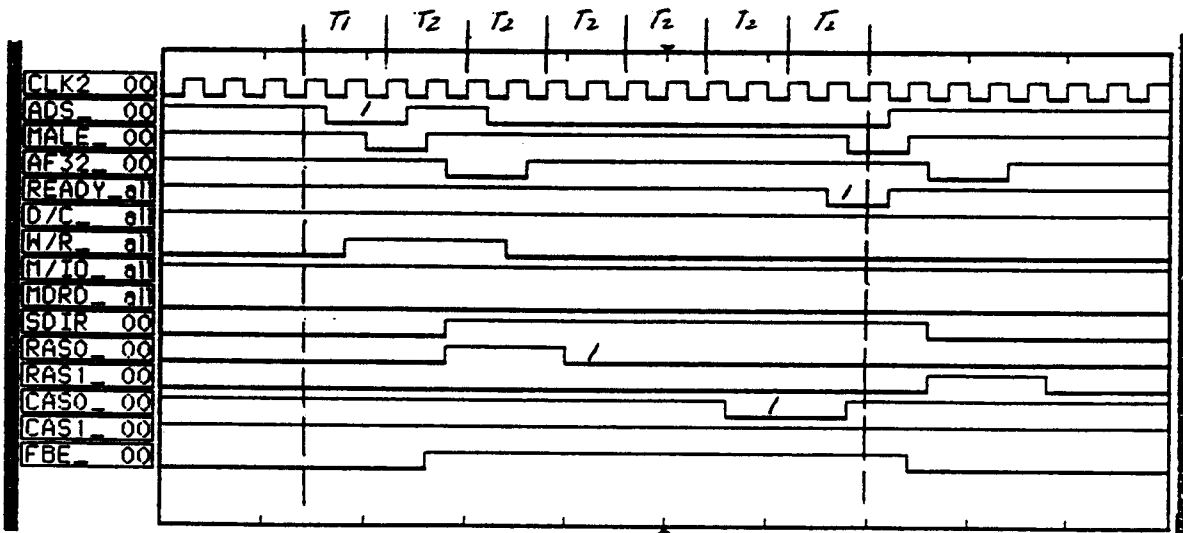
Following are the worst case timing analysis for the CS8230-25 and -20 MHz.

NOTE: DK8230 Rev C schematics is used to calculate the following timing.

Calulation for Tcac during the page hit cycle;

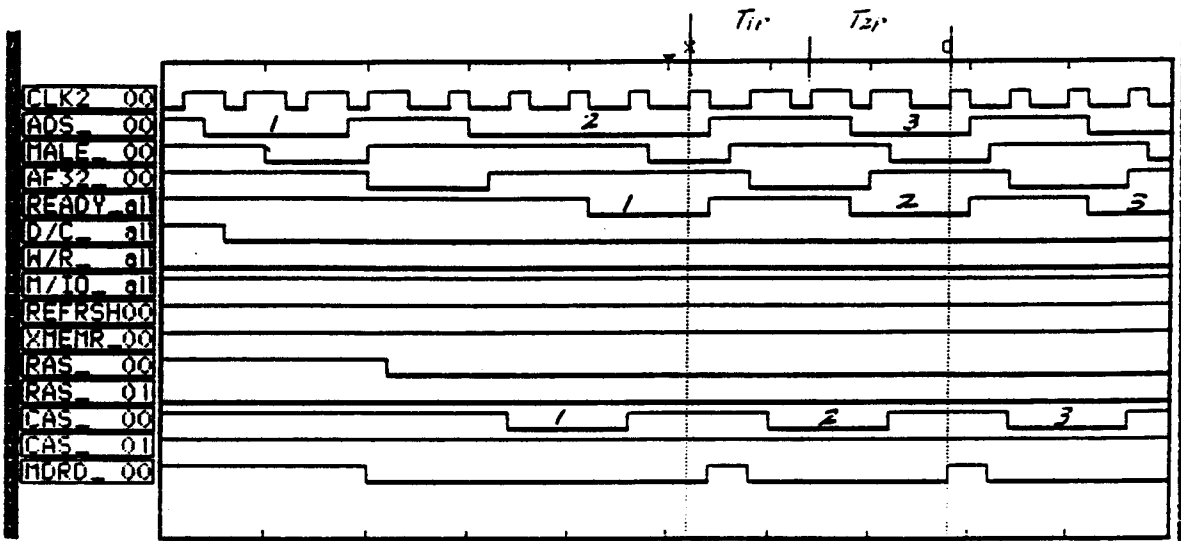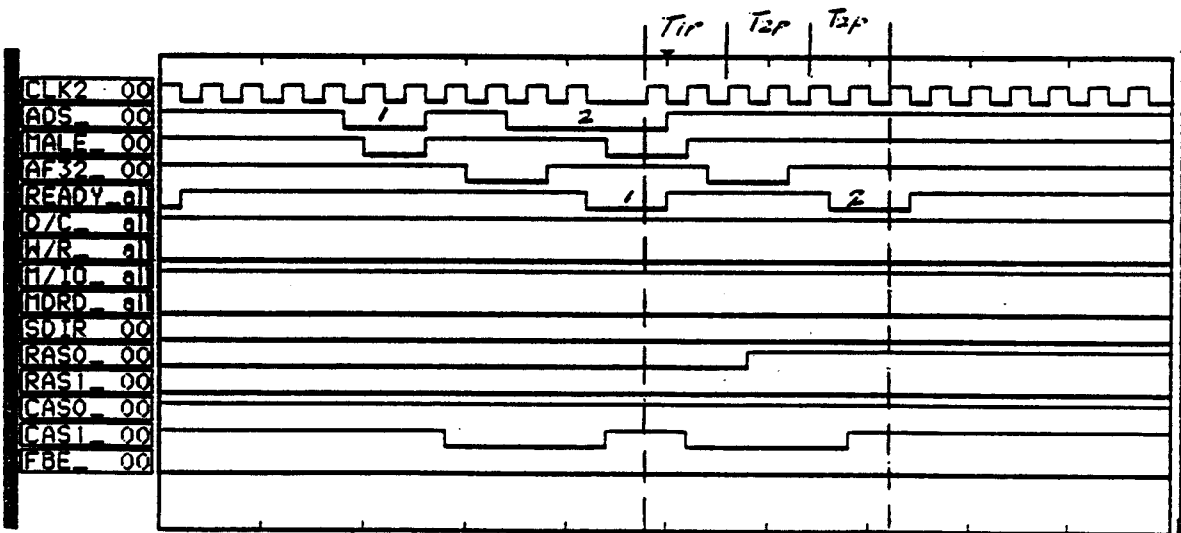| | 20MHz | | |
	0 WS	1 WS	0WS W/25 MHz Parts
Memory cycle (3CLK2 @ 0WS, 5CLK2 @ 1WS)	75	125	75
CASi active delay from CLK2	-18	-18	-12
74F32 Prop Delay	-6	-6	-6
LD data valid from MD data valid (t504 max)	-13	-13	-13
80386 data setup time	-10	-10	-10
	----	----	----
Tcac for 20 MHz	28	78	34

| | 25MHz | |
	0 WS	1 WS
Memory cycle (3CLK2 @ 0WS, 5CLK2 @ 1WS)	60	100
CASi active delay from CLK2	-12	-12
74F32 Prop Delay	-6	-6
LD data valid from MD data valid (t504 max)	-13	-13
80386 data setup time	-6	-6
	----	----
Tcac for 25 MHz	23	63

26

Caiulation for Trac during the page miss, RAS being inactive cycle;

	20MHz	
	0 WS	1 WS
Memory cycle (5CLK2 @ 0WS,7CLK2 @ 1WS)	125	175
74F244 prop delay	-6	-6
RASi active delay from CLK2 (t283 max)	-16	-16
LD data valid from MD data valid (t504 max)	-13	-13
80386 data setup time	-10	-10
	----	----
Trac for 20 MHz	80	130

	25MHz	
	0 WS	1 WS
Memory cycle (5CLK2 @ 0WS,7CLK2 @ 1WS)	100	140
74F244 Prop Delay	-6	-6
RASi active delay from CLK2 (t283)	-16	-16
LD data valid from MD data valid (t504)	-13	-13
80386 data setup time	-6	-6
	----	----
Trac for 25 MHz	59	99

27

INTERFACING THE 80386 TO NUMERIC COPROCESSOR 80387

USING THE CS8230 CHIPSET

REV. 3.0
JAN 11, 1989

28

INTERFACING THE 80386 TO THE NUMERICS COPROCESSORS
1. INTRODUCTION

Numeric processors extend the register and instruction set of the 80386 microprocessor architecture and adds numeric capability as well as support for floating point, extended integer and BCD data types. The numeric co-processor enhances the overall system performance by executing numeric instructions in parallel with the 80386 microprocessor.

The 80386 communicates with the numeric co-processors through I/O addresses 800000F8H and 800000FCH. The I/O addresses are automatically generated by the 386 when it encounters a numeric instruction. Communication of instructions and data operand transfers between the 80386 and the numeric coprocessor are handled by three control signals:

1. BUSY#, when active, indicates that the coprocessor is busy executing a command.

2. PEREQ# when active, indicates that the numeric coprocessor is ready to initiate data transfer.

3. ERROR# when active, indicates that an unmasked error condition exists.

The 80386 supports two numeric co-processors:

- The 80287 performs 16-bit data transfers and interfaces directly to the 80286 microprocessor. It can interface to the 80386 with additional glue logic.

- The 80387 performs 32-bit data transfers and interfaces directly to the 386 microprocessor. The 80386/80387 interface offers two to three times the performance of the 80386/80287 interface.

This Application-Brief discusses the 386/387 and 386/287 AT compatible hardware interface when using Chips and Technology's CS8230-AT CHIPSet. The first section provides a brief overview of the numeric co-processor implementation on the PC-AT. The section also discusses the differences between the 80387 and the 80287 coprocessor and the differences between the 80386 and the 286 microprocessor when interfacing to numeric co-processors. Those who are familiar with the PC-AT numeric co-processor implementation may wish to skip this section. The second section provides a detailed design description of the 80386/80387 PC-AT compatible interface. The 386/287 interface is discussed in section 3. Detailed schematics and PAL codes have been included in the Appendix.

1.1. PC-AT Numeric Co-processor Hardware Interface Description

The PC-AT uses Intel's 80287 numeric co-processor. The co-processor derives its clock input from the processor clock. This clock is internally divided by three to generate the co-processor clock. The 80287 is accessed as an I/O device at location 00F8H, 00FAH and 00FCH. The communication between the processor and the numeric co-processor is through these I/O addresses.

The 80287 uses the BUSY# output to inform the host processor that it is currently executing a numeric instruction.

In the event of an error during a numeric operation, the BUSY# signal from the numerics is extended (by latching BUSY# during an error condition) to prevent the processor from executing new numeric instruction before the error handling routine is invoked.

The error signal generates a hardware interrupt (INT 13H). The error handler routine is then invoked, which in turn clears the BUSY latch by an 8-bit write to the I/O port address F0H with D0~ D7 equal to zeros. The control is then transferred to the NMI interrupt handler routine.

The 80287, like the 80286 and the 80386 microprocessors, support two modes of operation : the Real Address mode, and the Protected mode. Following power on reset or an I/O write operation to port F1H, the 287 operates in the Real Address mode. The 287 can be programmed to operate in the protected mode by executing an SETPM ESC instruction.

1.2. Differences Between the 387 and the 287 Numeric Co-processor

1. 80287 performs 16-bit data transfers while the 387 performs 32-bit data transfers. The 386 can interface to the 287 with additional logic. However, the 286 supports only the 287.

2. The 387 requires a longer RESET pulse width.

3. The phase of the 387's internal bus controller clock must be the same phase as the 386's internal clock. This enables the 387 to monitor all bus cycles to determine if the 386 is operating in the pipelined or the non-pipelined mode. The 80287 does not monitor CPU bus cycles.

4. The 287 ERROR# output is activated during an unmasked error condition. In the PC-AT implementation, the ERROR# input to the processor is strapped high. When an error occurs during a numeric operation, external logic is used to generate an INT 13H. The interrupt service routine then performs the error processing and reporting.

    The 387 ERROR# output on the otherhand serves two functions:

    a. The 387 activates the ERROR# output when a error occurs of the type not masked by the coprocessor's control register

    b. Following RESET, the ERROR# input is used to inform the 80386 if it is interfacing to the 80387 or the 80287. If the 386 ERROR# input is held low following the falling edge of RESET until the 386 receives the READY# for the first cycle, the 386 assumes a 387 is installed. Otherwise a 287 is assumed.

    The current PC-AT implementation has to be modified when using the 387 to allow proper numeric coprocessor interface recognition.

1.3. Differences between the 80386 and the 80286 when interfacing to co-processors

The 80287 supports a PEACK# signal, that in conjunction with the PREQ signal provides the hand-shake mechanism for data transfers between the processor and the numerics

30

interface.

The 80386 does not support a PEACK signal because it knows the exact length of the operand being transferred. After the ESC instruction has been sent to the numeric co-processor, the 80386 processor expansion channel will initiate a data transfer when it receives a PEREQ from the numeric interface.

One direct impact of this operand transfer mechanism in an AT compatible environment is that when an error occurs, the 387/287 will flag the error condition and abort the execution of the instruction. The 386 on the other hand is waiting to complete the requested operand transfers.

To prevent the 386 from idling during the error condition, the following sequence of events should be initiated:

1. When ERROR# goes active, the PEREQ is extended to allow the 386 to complete the operand transfer.

2. The 80287/80387 outputs are tri-stated by either activating NPCS2 (80287) or the STEN input (80387). This ensures that there is no bus contention problem.

This protocol permits the 386 to complete the operation, even after an error occurs. The data transfer process is automatically terminated by the 386.

2.0.   386/387 PC-AT COMPATIBLE INTERFACE

The previous section described the AT compatible numeric hardware interface requirements and the differences between the 386 and the 286 in terms of co-processor interface. This section will describe the techniques of realizing an AT compatible 386/387 interface.

The 386/387 AT compatible interface circuitry is shown in the Appendix along with the PAL codes. Figure 1.0a illustrates the interface in a block diagram form. A brief circuit description is given below:

2.1.   PEREQ, STEN, INT13 and BUSY generation circuit

The circuitry required to generate the PEREQ, BUSY, STEN and INT13 is shown in Figure 1.0. The PEREQ and BUSY# is latched on the leading edge of the error signal by a 74F74. The Q (INT13) output of the flip-flop is used to generate the interrupt to the 82C206 Integrated Peripheral Controller. The INT13 output is 'Ored' with the 387 BUSY# to generate BUSY output to the 386. 386 PEREQ is generated by 'Oring' the 387 PEREQ with INT13H. The Q# output of the flip-flop is used to generate the STEN output to the 387 (the 387's STEN input may optionally be strapped high). The 74F74 flip-flop is cleared by either a I/O write to port F0H, an INTA# cycle, or by activating RESET3.

2.2.   Reset Generation Logic

In an PC-AT compatible design, the 80387 is reset by performing a write to I/O port F1H with D0~D7 equal to zeros. The CS8230: AT/386 CHIPSet executes a write to this I/O address location as a AT emulation cycle, allowing extension of the cycle with IOCHRDY#.
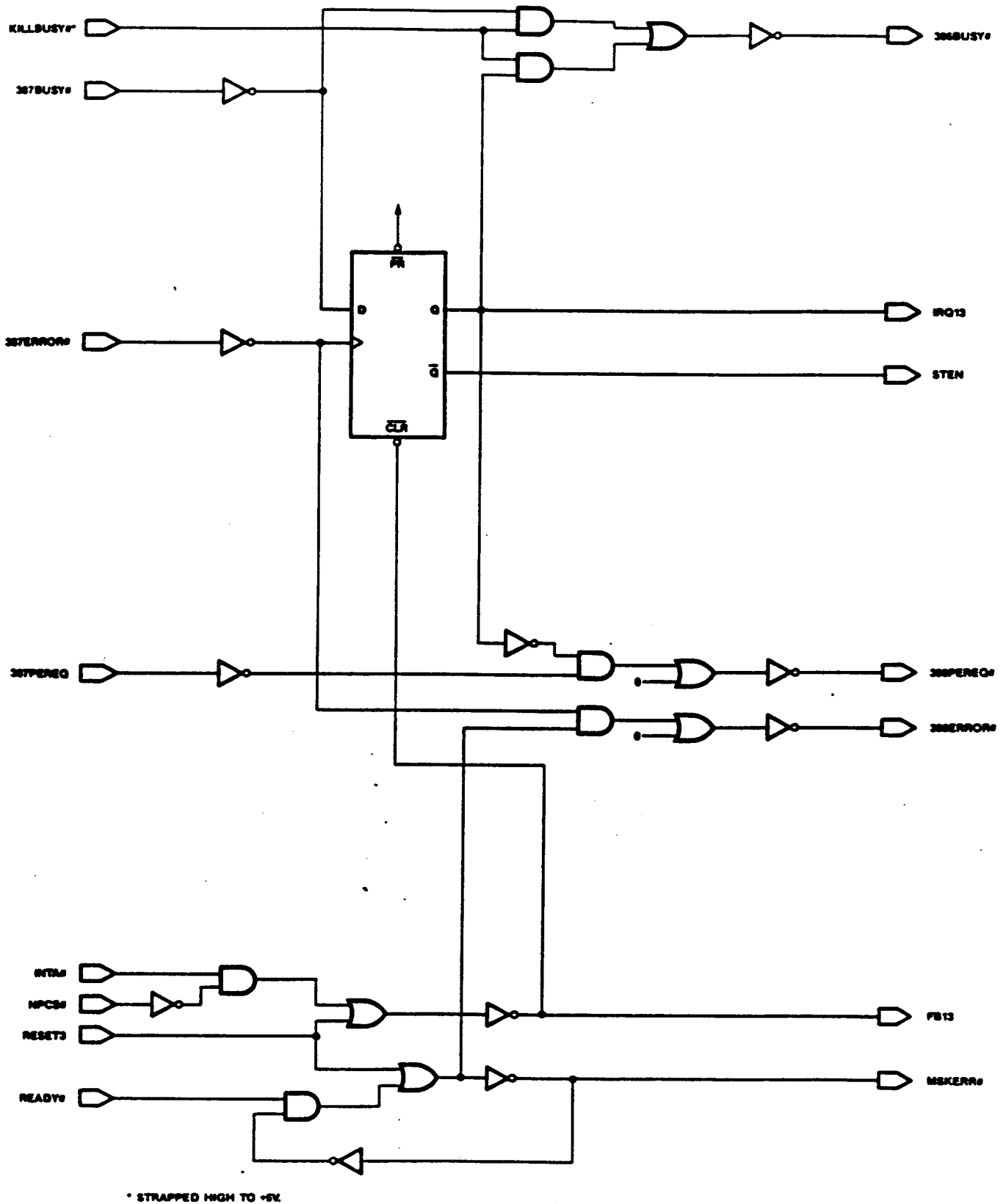
Figure 1.0 BUSY#, PEREG, STEN, IRQB and ERROR# Generation Logic

* STRAPPED HIGH TO +5V.

32
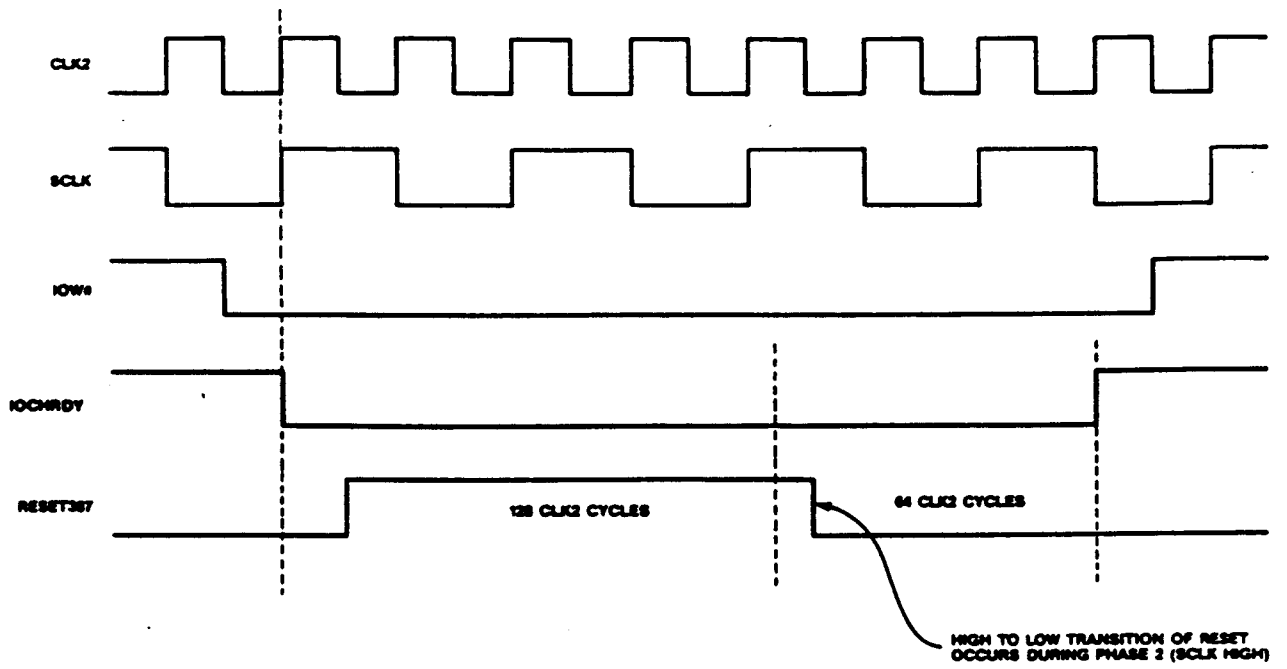
Figure 2.0 Timing Relationship Between IOW#, RESET and IOCHRY
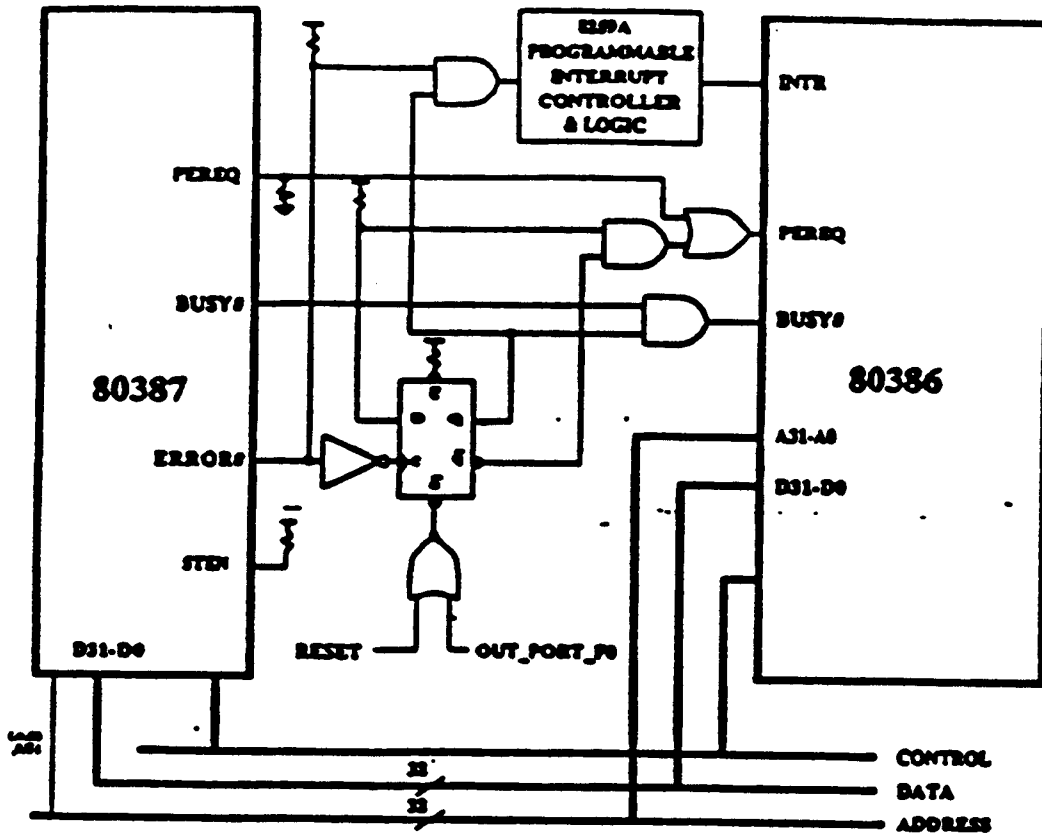
Figure 1.0a PC-AT Compatible 386/387 Interface as recommended by Intel (B0-step 80387 Stepping Information)

The RESET generation and synchronization logic extends the cycle sufficiently to meet the reset pulse width requirement of the 387 and allow sufficient time for synchronization. The timing relationship between the IOW, RESET and IOCHRDY is shown in Figure 2.0 and the logic required to satisfy the timing relationship is illustrated in Figure 3.0.

Three conditions have to be satisfied to properly reset the 387 and re-synchronize the 387 to the 386:

1. RESET to the 80387 has to be held high for at least 78 CLK2 cycles

2. The high to low transition of reset should occur during phase 2 of the 386 CLK2. This is to ensure that the internal bus controller clock of the 387 is in phase with the 386 internal clock.

3. After RESET is de-activated, at least 50 CLK2 cycles are required before a new numeric instruction can be executed. This delay is also generated by the logic in Figure 3.0).
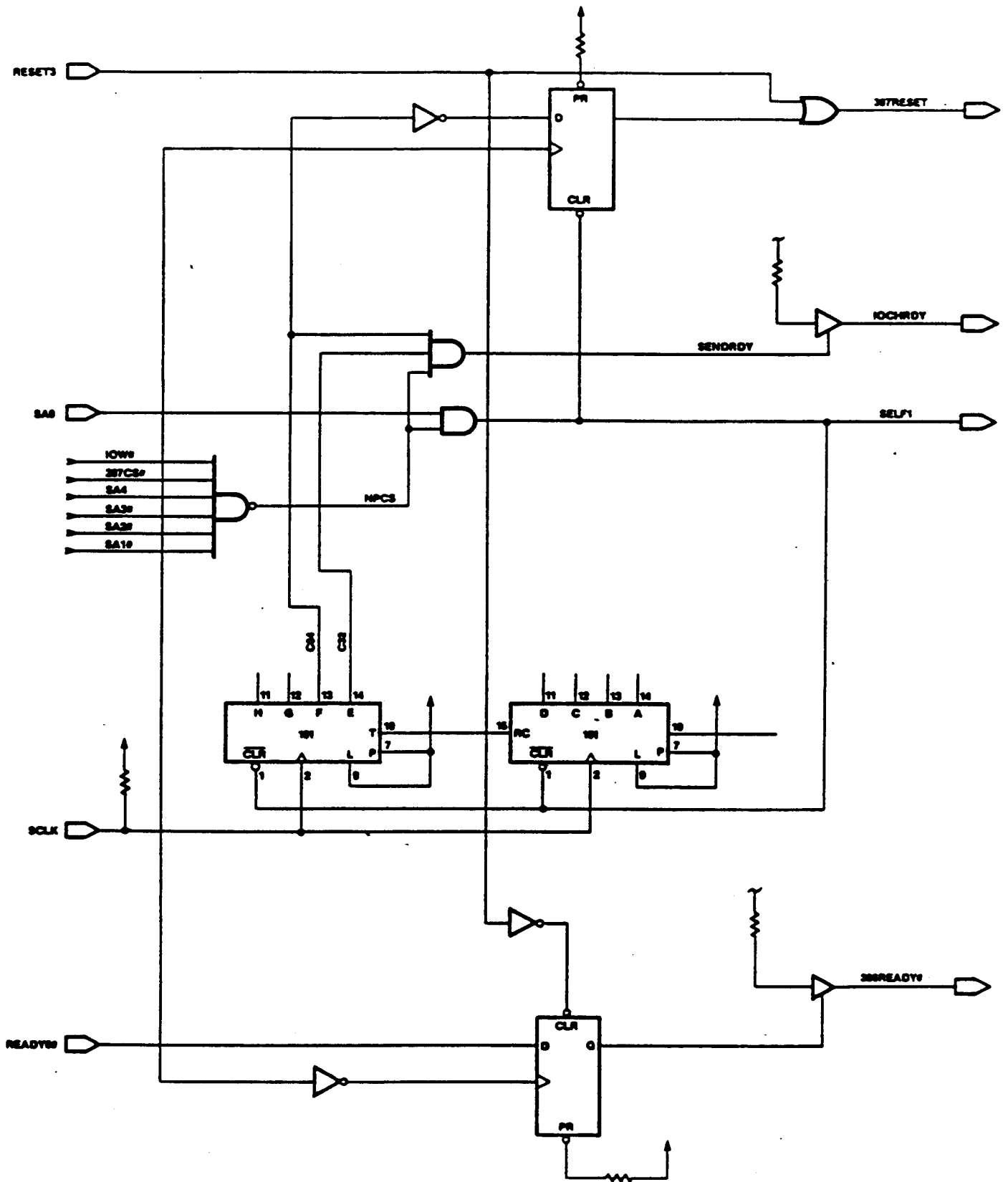
Figure 3.0 80387 RESET Generation Logic

35

2.2.1. OPERATION

When an I/O write to the port F1 is performed, the SELF1 output is activated, which clears the cascaded counter. The C64 output (see Figure 3.0) is inverted and synchronized to SCLK to generate the SRESET. This output is high for 64 SCLK cycles following a write to port address F1H. The falling edge of SRESET occurs during the high to low transition of SCLK, thereby ensuring that reset occurs during Phase 2 of the 386 internal clock. This enables the 387 to maintain synchronization with the 386. The circuit also ensures that following a write to I/O port F1, the reset to the 387 is held high for at least 64 SCLK (128 386 CLK2 cycles) cycles, thereby satisfying the reset high time requirements of the 387 (>> 78 CLK2 cycles). The IOCHRDY# output is forced low until C64 and C32 goes active (after 32 SCLK cycles). This prevents the processor from executing a numeric instruction till 32 SCLK (64 387 CLK2 cycles) cycles following the de-activation of SRESET (Note: The 387 requires at least 50 387 CLK2 cycles for initialization) After 96 SCLK cycles, the IOCHRDY# is released, allowing the processor to resume execution of instructions.

NOTE 1:

During the reset synchronization sequence, the 386 will not honor any refresh requests. The worst case refresh delay is:

$$192 \times 386 \text{ CLK2 period}$$

$$@ 16 \text{ MHz, 386 CLK2 period is 62.5 ns.}$$

$$= 192 \times 62.5$$

$$= 12 \text{ microseconds.}$$

The worst case refresh cycle delay is 12 microseconds. The DRAMs require 128 rows to be refreshed every 2 ms. The PC-AT implements a distributed refresh scheme whereby each row is refreshed every 15 microseconds.

Therefore 128 rows are refreshed every 128 x 15 = 1920 or 1.92 microseconds. Even if one refresh cycle is delayed by 12 microseconds (hopefully we will not have more than one numeric error in 2 ms) the 2 ms requirement is still not violated (1920 + 12 = 1.932 < 2 ms).

The number of RESETs required within a 2 ms interval to violate the refresh requirements can be computed as follows:

The refresh can be delayed by approximately 12 microseconds (worst case : refresh request coincides with an error condition) during an error condition. The refresh implementation on the PC-AT can tolerate a refresh delay of 80 microseconds (2.0 - 1.920 = 0.080 milliseconds). Therefore, if more than six numeric errors occur during a 2 millisecond interval, the DRAM refresh requirement will be violated.

NOTE 2:

Intel recommends that 386/387 should be reset simultaniously. The asynchronous reset feature can easily be disabled by removing the SRESET term in the RES387 generation logic. This is illustrated below:

The present RES387 equation is as follows:

RES387 = SRESET # RESET3; SRESET is the asynch reset input.

To disable asynchronous reset, the following modification is recommended:

RES387 = RESET3;

NOTE3:

Forcing AF32 during pipelined operation

The AF32# to the 82C301 should be active during the start of all local bus accesses (including accesses to the 387 co-processors). The AF32 allows the 82C301 to determine which state machine should be invoked for the current access, ie. either CPU or AT state machine. The 82C306 AF32# is activated during numeric co-processor accesses. The 82C306 AF32# generation circuit functions properly during non-pipelined accesses. In the non-pipelined mode, the AF32# is activated during 32-bit memory accesses as well as 387 accesses. But, when operating in the pipe-lined mode, AF32# is not activated during the third cycle, during back to back accesses. This is due to a race condition induced during pipe-lined accesses. When AF32# is not detected during the third access, the 82C301 attempts to initiate the AT state machine causing improper operation. The above anomaly can easily be corrected, provided the following modifications are made to the numeric co-processsor interface:

Forced AF32# generation during numeric co-processor access:

!306AF32 :=!MALE & SCLK & A31 & !MIO;   activate AF31 during A31 & !MIO
      # !306AF32 & !SCLK;   keep AF32 active till SCLK is high

if(!306AF32) !301AF32 = V_{CC}; buffered AF32 to 301

2.3.   Error Generation Logic .

The ERROR input to the 386 should be low following the reset sequence till the first ready is detected to allow for proper numeric interface recognition. After READY is detected, the ERROR to the 386 must remain high till the next soft reset or system reset.

The circuit that satisfies the above condition is illustrated in Figure 1.0. When RESET3 is activated, the 386ERROR# output is activated. The 386ERROR# is held active till the first ready is detected.

3.   386/287 PC-AT COMPATIBLE NUMERIC INTERFACE

If the ERROR# input to the 386 is sampled high following the high to low transition of reset, the 386 assumes it is interfacing either to the 287 co-processor or no co-processor interface exists. It is the responsibility of the software to exercise the numeric interface to determine the presence of a 287 numeric co-processor.

The 80386 performs all the necessary bus cycles to transfer data to or from the 287 on the lower half of the data bus. The 80386 automatically converts 32 bit data transfers into two sixteen bit 287 data transfers. When the 386 detects a numeric instruction, it generates one or more I/O cycles to port address 800000F8H and 800000FCH.

37

External bus control logic is required to translate 386 bus signals to 287 compatible signals. When using Chips and Technology Chipset, the bus controller function is automatically performed by the 82C301 bus controller. The only additional logic required is the BUSY#, PEREQ, RESET, ERROR#, IOCS16#, NPCS# and IRQ13 generation logic. This logic can be integrated into a single 82S153 PAL.

Figure 4 illustrates the 386/287 interface circuitry. The PEACK# output of the 287 is strapped high. The 287 data bus D0~D15 is connected to RD0~RD15 out of the 82C305. The XIOR# and the XIOW# out of the 82C301 connects directly to the 80287 NPRD# and NPWR# inputs.

3.1.   80287 Clock Generation

The 82C301 generates the 386 processor clock (CLK2), the SCLK and the ATS clock. CLK2 is derived from the CLK2IN input of the 82C301 (If CLK2IN is 32 MHz then CLK2 equals 32 Mhz). The 82C301 provides software controlled selection of the ATSCLK clock used for the AT state machine. The ATSCLK provides the clock input to the 287. This clock input is divided by three to generate the internal clock.

3.2.   OPERATION

1. 386 PEREQ is activated when either 287 PEREQ or IRQ13 is active.

2. 287 RESET is acticvated when either the system reset (RESET4) or an I/O write to port F1H is performed. When interfacing the 386 to the 287, reset synchronization is not required as the 287 does not monitor 386 bus cycles.

3. IRQ13 is generated when BUSY and ERROR from the 287 occur at the same time. The IRQ13 will then remain active until RESET or I/O write to port F1 is executed.

4. The 82C304 activates 287CS. for addresses 0E0H to FFH. This output has to be qualified with A3 to ensure that the 287CS is activated only for port accesses to addresses F8H or FCH. The NPCS is not activated during IRQ13.

5. The 386 ERROR# input is strapped high and COPEN# is strapped low..

6. The 386 BUSY# is activated if any of the following conditions hold true:

   1. 287 BUSY# and COPEN# are both active
   2. IRQ13 and COPEN# are both active
   3. NPCS and COPEN# are both inactive

7. IOCS16# to the 82C301 is activated when the 287 is accessed to inform the byte conversion logic on the 82C301 that it is interfacing to a sixteen bit I/O peripheral.

If the design does not use the Chips and Technology CHIPSet, then an external bus controller should be used to generate the numeric co-processor interface. The Bus controller logic should guarantee 80287 timing requirements, particularly the minimum command inactive time (Tcmdi). Using Chips 80386 chipset, AT compatible interface can be realized using a single 82S153 PAL (16L8 PAL can also be used).

38
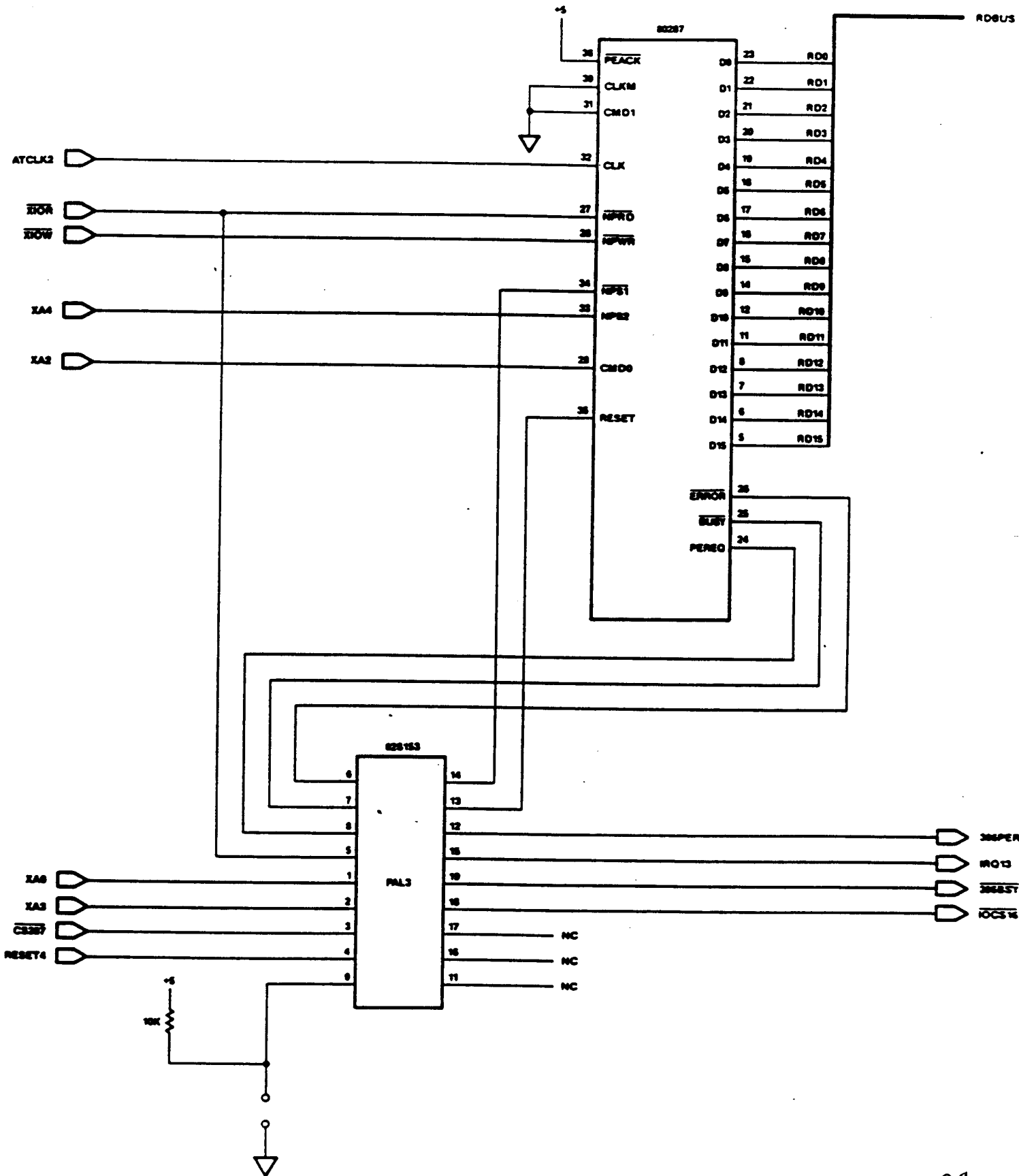
Figure 4.0 80386/80287 PC-AT Compatible Numeric Interface

39

Section C

Adding the 80387 Coprocessor to DK8230

Attached is the information required to implement the 80387 coprocessor in the DK8231 development board. This package contains:

1) Revised 80387 interface schematics.
2) Updated PAL equations for U83, U80 in the DK8231.
3) A software patch for old versions of BIOS that don't support the 80387 coprocessor. This software patch is not required if BIOS version 3.07 or higher is used.

Notes:

Jumper 3 & 4 must be in place when 387 is installed.
Use "B" type PALs for the 80387 interface logic.
Updated PAL equations will correct the 80386 toggle-busy problem.
This design will work with both CS8230 and CS8231 CHIPSets.

40

```
 1:NAME              387BUS;
 2:DATE              12/27/88;
 3:REV               00;
 4:DEVICE            P16L8;
 5:DESIGNER          MEHDI ASNAASHARI;
 6:COMPANY           Chips and Technologies Inc.;
 7:ASSEMBLY          80387 BUSY LATCHING;
 8:LOCATION          U83;
 9:
10:/******************************************************************/
11:/* This device controls BUSY latching, PEREQ, ERROR, BUSY, and */
12:/* IRQ13 generation to the processor.                          */
13:/******************************************************************/
14:/* Allowable Target Device Types:  PAL 16L8                    */
15:/******************************************************************/
16:
17:/** Inputs **/
18:
19:PIN 2  = N_87PRS           ;/* 387 PRESENT           */
20:PIN 4  = N_READY           ;/* READY#                */
21:PIN 5  = N_REF             ;/* REF# for toggle busy  */
22:PIN 6  = 87PRQ             ;/* PEREQ from 387        */
23:PIN 7  = RESET3            ;/* CPU RESET             */
24:PIN 8  = N_87ERR           ;/* ERROR from 387        */
25:PIN 9  = N_87BSY           ;/* BUSY from 387         */
26:PIN 17 = IRQ13             ;/* Latched IRQ from FF   */
27:
28:/** Outputs **/
29:
30:PIN 12 = !86BSY            ;/* BUSY# to  386         */
31:PIN 13 = !86ERR            ;/* ERROR# to 386         */
32:PIN 15 = 86PRQ             ;/* PEREQ to 386          */
33:PIN 19 = !ERRFF            ;/* ERROR to Flip-Flop    */
34:
35:/** Declarations and Intermediate Variable Definitions **/
36:
37:
38:/** Logic Equations **/
39:
40:86BSY  = !N_87BSY
41:       # IRQ13
42:       # !N_REF & N_87PRS;
43:
44:86ERR  = !N_87ERR & RESET3
45:       # 86ERR & N_READY;
46:
47:86PRQ  = 87PRQ
48:       # IRQ13 & N_87BSY;
49:
50:ERRFF  = N_87ERR;
51:
Jedec Fuse Checksum      (2F43)
Jedec Transmit Checksum  (B87C)
```

41

```
 1:NAME              387RST;
 2:DATE              12/27/88;
 3:REV               00;
 4:DEVICE            P16L8;
 5:DESIGNER          MEHDI ASNAASHARI;
 6:COMPANY           Chips and Technologies Inc.;
 7:ASSEMBLY          80387 RESET IRQ13;
 8:LOCATION          U80;
 9:
10:/*****************************************************************/
11:/* This device resets IRQ13 and generates the AF32 signal      */
12:/* for the coprocessor cycles.                                 */
13:/*****************************************************************/
14:/* Allowable Target Device Types:  PAL 16L8                    */
15:/*****************************************************************/
16:
17:/** Inputs **/
18:
19:PIN 1   = N_287CS              ; /*287 Chipselect       */
20:PIN 2   = N_IOW               ; /*IO write             */
21:PIN 3   = SA4                 ; /*                     */
22:PIN 4   = SA3                 ; /*                     */
23:PIN 5   = SA2                 ; /*                     */
24:PIN 6   = SA1                 ; /*                     */
25:PIN 7   = SA0                 ; /*                     */
26:PIN 8   = A31                 ; /*Address line 31      */
27:PIN 9   = N_MIO               ; /*Memory / IO          */
28:PIN 11  = N_MALE              ; /*                     */
29:PIN 15  = N_INTA              ; /*Interrupt Ack.       */
30:PIN 18  = RESET3              ; /*                     */
31:
32:/** Outputs **/
33:
34:PIN 16  = !CLR                ; /*CLR IRQ13 latch      */
35:PIN 17  = !AF32FF             ; /*                     */
36:
37:/** Declarations and Intermediate Variable Definitions **/
38:
39:
40:/** Logic Equations **/
41:
42:CLR     = RESET3
43:     # N_INTA & !N_IOW & !N_287CS & SA4 & !SA3 & !SA2
44:     & !SA1 & !SA0;
45:
46:AF32FF      = !N_MIO & !N_MALE & A31;
47:
48:
Jedec Fuse Checksum      (12A9)
Jedec Transmit Checksum   (829C)
```
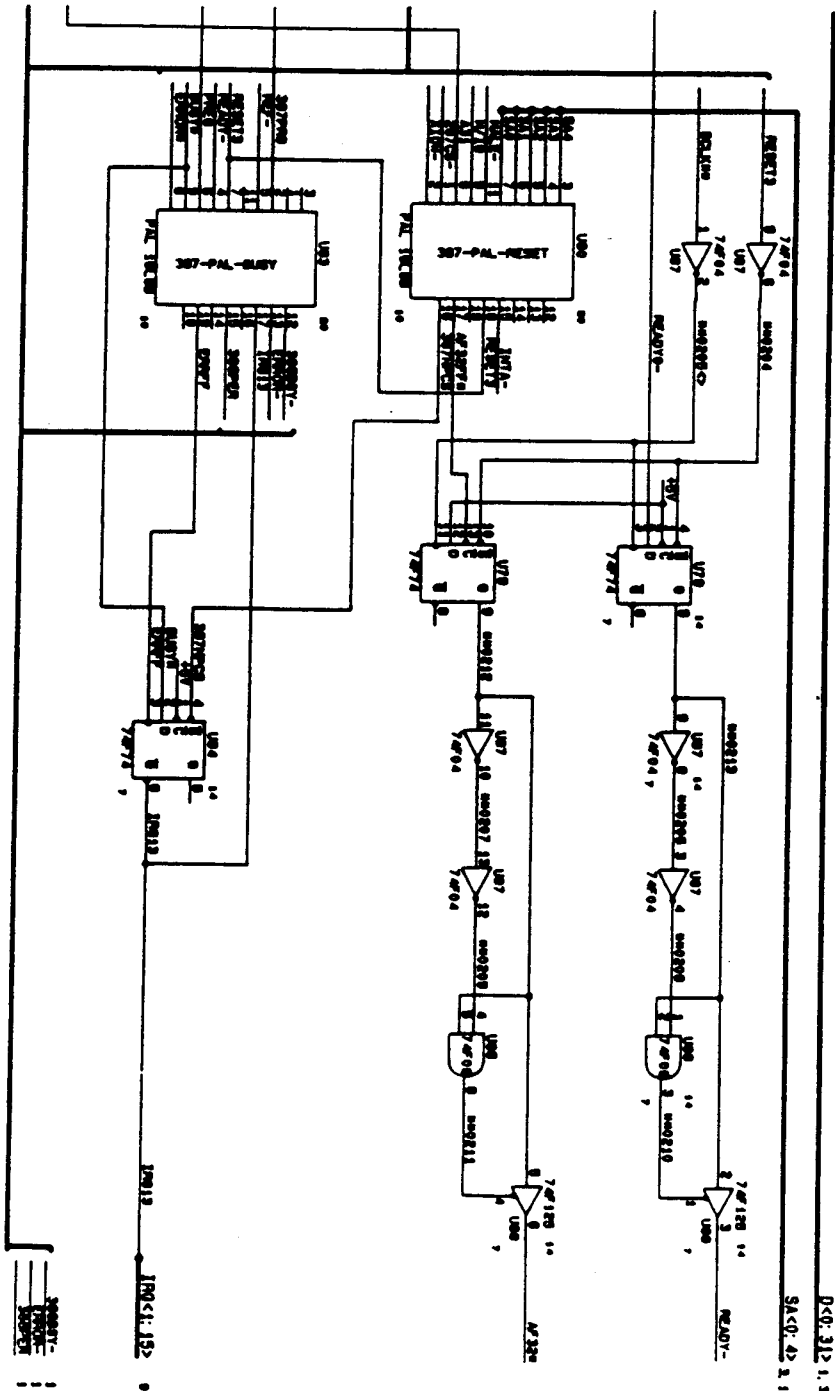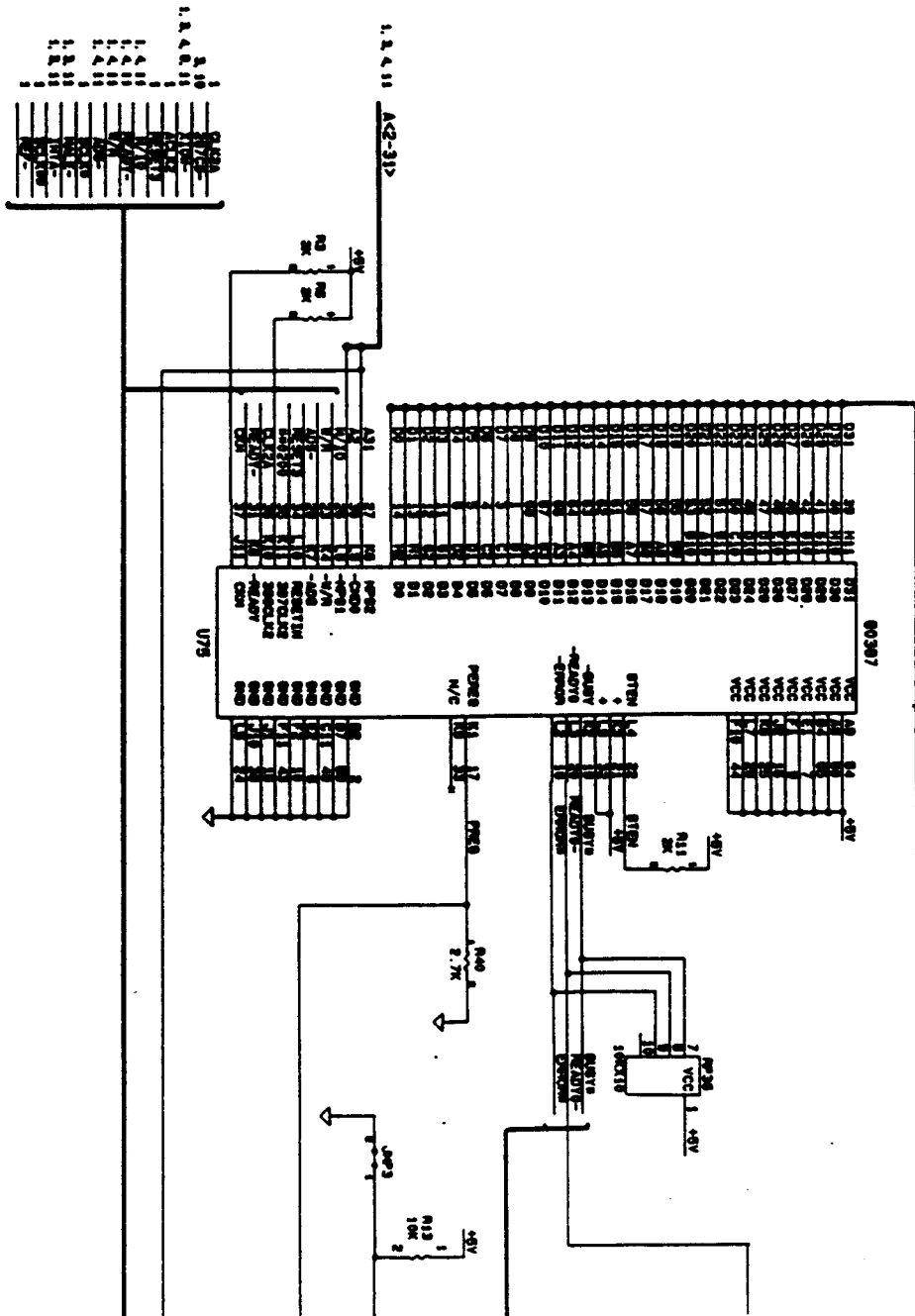
42

43

44

SECTION D

CS8230 PRODUCT UPDATES

45

CS8230 AT/386 CHIPSet ERRATA HISTORY

The revision history of the CS8230 and CS8282 CHIPSet is as follows:

CHIP PART #	PART IDENTIFICATION ON PART	STATUS
P82C301	TC19G032-AT004 7034-004	1st Samples/Initial Version; First Shipments: 10/20/86 Parts no longer being shipped.
	7034-0010	Second Silicon Parts; First Shipments: 3/13/87
	P82C301 C 7034-0044	Current production Parts; First Shipment: 3/15/88
P82C302	TC19G042-AT004 7035-004	1st Samples/Initial Version; First ˇ Shipments: 10/20/86 Parts no longer being shipped.
	7035-0008	Current Production Parts; First Shipments: 3/13/87
P82A303	MB113T317P or MB113F317	1st Samples and Current Production Parts; First Shipments: 10/20/86 MB113T317P and MB113F317 are identical parts.
P82C303	MB623301	1st samples and Current Productin Parts; First Shipment: 11/87
P82A304	MB113T318P	1st Samples/Initial Version; First Shipments: 10/20/86 Parts no longer being shipped.

46

SECTION D

CHIP PART #	PART IDENTIFICATION ON PART	STATUS
P82A304	MB113F323	Current Production Parts; First Shipments: 3/13/87
P82C304	MB623303U	1st Samples and Current Production Parts; First Shipment: 11/87
P82A305	MB113T319	1st Samples and Current Production Parts; First Shipments: 10/20/86
P82B305	D67010L-017	1st Samples and Current Production Parts; First Shipment: 7/87
P82C305	MB623302U	1st Samples and Current Production Parts; First Shipments: 11/87
P82A306	MB113T320P	1st Samples/Initial Version; First Shipments: 10/20/86 Parts no longer being shipped.
	MB113F324	2nd Silicon; First Shipments: 3/13/87 Parts no longer being shipped.
	P82A306 A MB113F326	Current Production Parts; First Shipments: 11/16/87
P82C306	MB623304	1st Samples and Current Production Parts; First Shipment: 11/87

47

Following is the list of the parts shipped with each CHIPSet:

CS8230-16	CS8230-20	CS8230-25
82C301	82C301-20	82C301-25
82C302	82C302-20	82C302-25
82A303	82A303	82A303
82A304	82A304	82A304
82A305	82B305	82B305
82A306	82A306	82A306

CS8232-16	CS8232-20	CS8232-25
82C301	82C301-20	82C301-25
82C302	82C302-20	82C302-25
82C303	82C303	82C303
82C304	82C304	82C304
82C305	82B305	82B305
82C306	82C306	82C306

LISTED BELOW ARE THE ANOMALIES IDENTIFIED FOR EACH REVISION OF EACH CHIP OF THE CS8230 AT/386 CHIPSet. A TEMPORARY FIX HAS BEEN PROVIDED FOR EACH ANOMALY WITH AN INDICATION IF THE NEXT REVISION OF THAT PARTICULAR CHIP WILL BE CORRECTED OR NOT.

CHIP PART #: P82C301

PART IDENTIFICATION ON PART: TC19G032-AT004 7034-004

STATUS: 1st Samples/Initial Revision; First Shipments: 10/20/86; Parts no longer being shipped.

ANOMALY LIST:

(1) Anomaly: SDIR generation is incorrect and causes the buffers to be in the wrong direction on the local and AT bus for some access cycles.

  Fix: The following circuit shows the fix needed for correct SDIR signal generation.

  Plan: Corrected in the next revision of silicon.

48
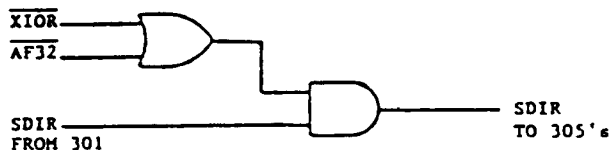
(2)   Anomaly: PCLK generation during RESET: PCLK is inhibited during the reset which causes keyboard controller not to reset correctly.

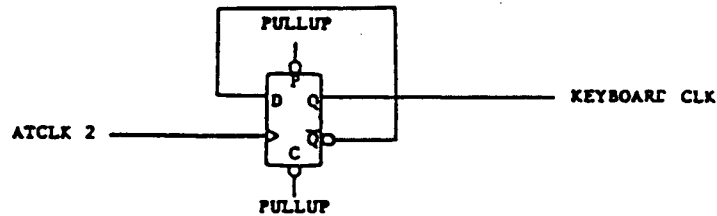   Fix: The following external fix should be provided so that devices such as the keyboard controller can be reset correctly. Note that this fix assumes the use of asynchronour AT clock: if AT clock is derived from the CLK2, a divide down from CLK2 would be needed.

        Plan: Corrected in the next revision of silicon.

(3)   Anomaly: ATEN* reset after shutdown: ATEN* remains active following a CPU shutdown which causes incorrect subsequent system operation.

        Fix: The circuit shown below will reset ATEN* after shutdown.

        Plan: Corrected in the next revision of silicon.

49
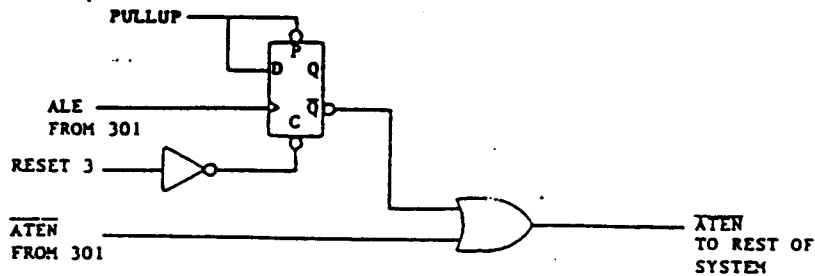
(4)   Anomaly: IO Channel 8 and 16 bit transfer: The 8-bits data transfer
                    between 8 bit and 16 bit IO Channel devices are not supported.
                    This results in incorrect DMA data transfer between an 8 bit IO
                    device and a 16 bit IO device.

      Fix: See item 1 of 82A305 for the external fix.

      Plan: There is NO plan to incorporate this fix in future revisions of the
                    82C301.

CHIP PART #:   P82C301

PART IDENTIFICATION ON PART: 7034-0010

STATUS: Current Production Parts; First Shipments: 3/13/87

ANOMALY LIST: None

CHIP PART #:   P82C302

PART IDENTIFICATION ON PART: TC19G042-AT004   7035-004

STATUS: 1st Samples; First shipments: 10/20/86; parts no longer being shipped.

ANOMALY LIST:

(1)   Anomaly: ROMCS* generation: The ROMCS* coming out of 82C302 is too
                    short for ROM access on the AT bus if the configuration register
                    REG08H is set to 07H. This results in incorrect ROM accesses.

      Fix: The following circuit provides a fix to this anomaly. The fix is
                    not needed if the bit 2 of the internal configuration register 08H
                    is set to 0.

      Plan: Corrected in the next revision of silicon.
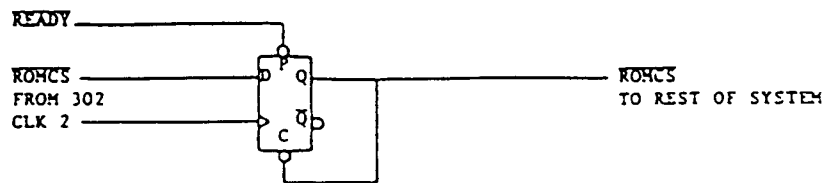
(2)   Anomaly: Configuration register decode anomaly: The configuration register decode incorrectly responds to indices 00H to 07H. This may cause unexpected reprogramming of the 82C302.

        Fix: The following circuit shows a temporary fix to this anomaly by preventing 82C302 from responding to accesses to index registers 00H to 07H.

        Plan: ,   Corrected in the next revision of silicon.
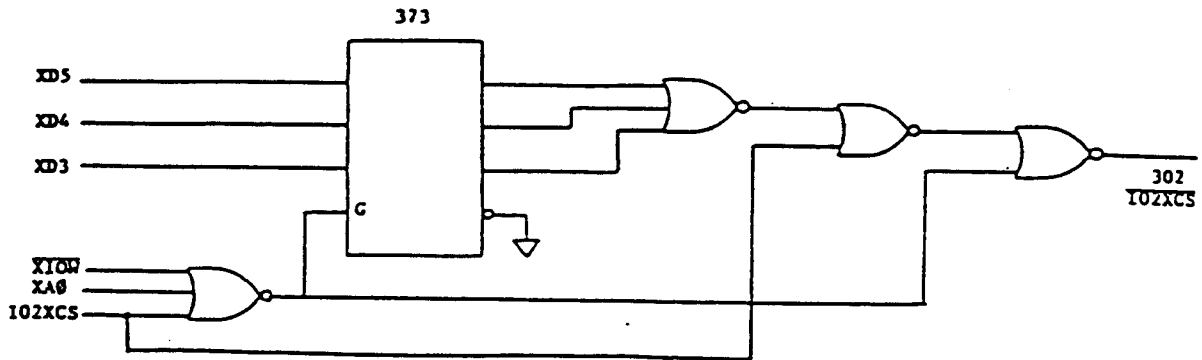
(3)   Anomaly: The ready signal generated from the 82C302 is too early in some access cycles, such as DMA, and confuses both the 80386 and 80C301.

        Fix: The following figure shows the external circuit required to correct this problem.

        Plan: Corrected on the next revision of silicon.

51

CHIP PART #:   P82C302

PART IDENTIFICATION ON PART: 7035-0008

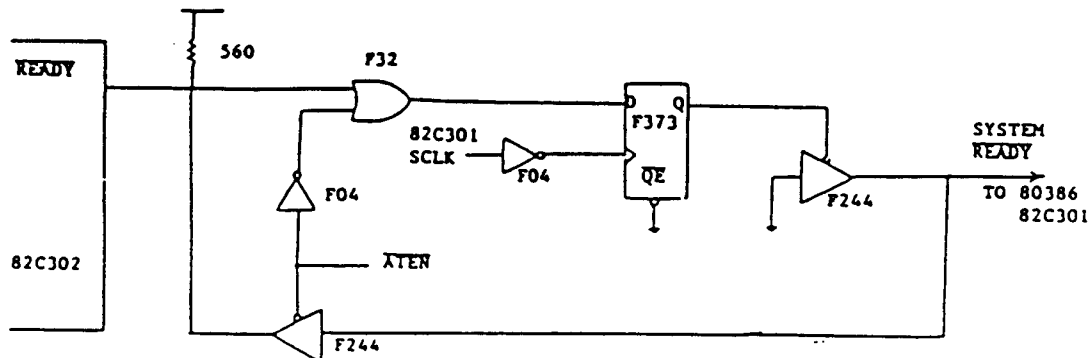STATUS: Current Production Parts; First Shipments: 3/13/87

ANOMALY LIST: None

CHIP PART #:   P82A303

PART IDENTIFICATION ON PART: MB113T317P or MB113F317

STATUS: 1st Samples and Current Production Parts;
First Shipments: 10/20/86

ANOMALY LIST: None

CHIP PART #:   P82A304

PART IDENTIFICATION ON PART: MB113T318P

STATUS: 1st Samples/Initial Version; First Shipments: 3/13/87
Parts no longer being shipped.

ANOMALY LIST:

(1)   Anomaly: Pin 56 ACK* output signal is not qualified by the REF* signal. As
a result some devices on the IP Channel may operate incorrectly.

Fix: The ACK* signal must be generated externally by the circuit
shown below.

Plan: Corrected in the next revision of silicon.

52

CHIP PART #:   P82A304

PART IDENTIFICATION ON PART: MB113F323

STATUS: Current Production Parts; First Shipments: 3/13/87

ANOMALY LIST: None

CHIP PART #:   P82A305

PART IDENTIFICATION ON PART: MB113T319P or MB113T319

STATUS: 1st Samples and Current Production Parts;
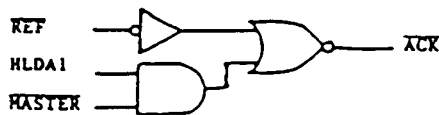   First Shipments: 10/20/87

ANOMALY LIST:

    (1)   Anomaly: IO Channel 8 and 16 bit transfer: The 8-bits data transfer
between 8 bit and 16 bit IO Channel devices are not supported.
This results in incorrect DMA data transfer between an 8 bit IO
device and a 16 bit IO device.

             Fix: The following circuit is required to do this operation correctly.

             Plan: There is NO plan to incorporate this fix in future revisions of the
82A305
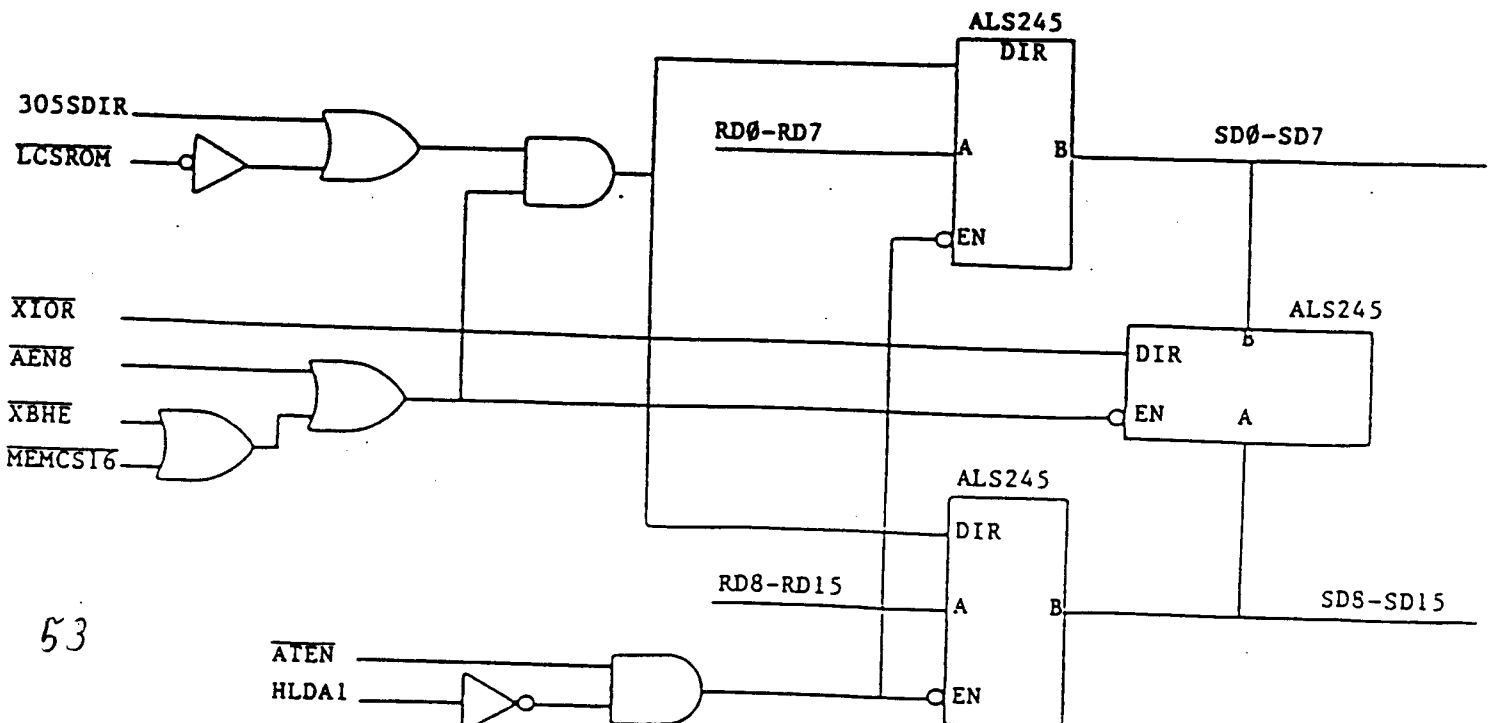
53

CHIP PART #: P82A306

PART IDENTIFICATION ON PART: MB113T320P

STATUS: 1st Samples/Initial Version; First Shipments: 10/20/86
Parts no longer being shipped.

ANOMALY LIST:

(1) Anomaly: The timing diagram on page 101 and the timing descriptions on page 97 of the data sheet are incorrect. The rising and falling edges of the signals REF* and LMEGCS* are reversed for the signal timing t626 to t633.

Fix: Please make a note of this in your data sheet.

Plan: Corrected in the next revision of data sheet.

(2) Anomaly: The BALE signal generated from the 82A306 is not properly qualified with REF*. As a result the BALE is not asserted during refresh cycles.

Fix: The following figure shows the external circuit required to correct this problem.

Plan: Corrected in the last revision and current production parts.

SPECIAL NOTE: If you decide to incorporate the fix into your system design now, your modified boards will work with Rev. 3 silicon (the next silicon) when it becomes available.

54

CHIP PART #:   P82A306

PART IDENTIFICATION ON PART: MB113F324

STATUS: 2nd Silicon; First Shipments: 3/13/87; Parts no longer being shipped.

ANOMALY LIST:

(1)   Anomaly: The BALE signal generated from the 82A306 is not properly qualified with REF*. As a result the BALE is not asserted during refresh cycles.

   Fix: The following figure shows the external circuit required to correct this problem.

   Plan: Corrected in the next revision of silicon.

SPECIAL NOTE: If you decide to incorporate the fix into your system design now, your modified boards will work with Rev. 3 silicon (the next silicon) when it becomes available.
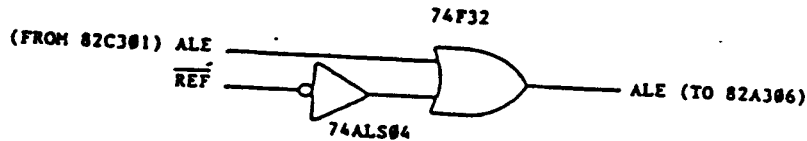
CHIP PART #:   P82A306

PART IDENTIFICATION ON PART: P82A306 A
                                      MB113F326

STATUS: Current Production Parts; First Shipments: 11/161/88

ANOMALY LIST: None

65

CLARIFICATIONS AND CHANGES TO DATA SHEET

(1)   Reference: Data Sheet - Advance Information.
      Change: Configuration register 09H default value is changed from 0FH
                                to 01H. Thus only accesses to the 64KB block from 960KB to 1MB
                                will generate ROMCS* by default.
      Impact: System configuration program for 82C302 may be affected if
                                your BIOS uses more that 64KB.

(2)   Reference: Data Sheet - Advance Information.
      Change: A new configuration register 2AH is added. This is a R/W register with
only the bit 0 defined. This bit is used to control the access to the low
256KB of memory address space. If the bit is 1 the 82C302 will take
control of themeory access by asserting AF32*. If the bit is 0, 82C302
will not issues AF32* and thus allows the address space to be controlled
by other devices. This bit defaults to 1.
      Impact: This is a new feature and should not affect your system unless this feature
is to be used.

(3)   Reference: Data Sheet - Advance Information.
      Change: IOCHRDY instead of READY* will be activated during DMA cycles.
IOCHRDY will become low if the memory address is specified as system
DRAM memory access in the memory map and if either XMEMR* or
XMEMW* is active. The duration of IOCHRDY low time is
approximately 2 SCLK cycles.
      Impact: This rectifies potential problems which can arise in AT-386 systems.
NO changes should be required in your system design.

(4)   Reference: Data Sheet - Advance Information.
      Change: For system DRAM memory access resulting in page-hit, CASn* and
CAS* will be synchronized with CLK2 rising edge instead of CLK2
falling edge. This results in CASn* and CAS* to be shifted from the
falling edge to the next rising edge.
      Impact: This should result in more stable memory subsystem operation and should
not affect your system design.

(5)   Reference: Data Sheet - Advance Information.
      Change: Pin 58 of 82A306 is changed from OUT1 to NC (No Connect).
Previously this is an output of a buffer.
      Impact: If you used this buffer as specified, your system design will be affected.

(6)   Reference: Data Sheet - Advance Information.
      Change: Pin 63 of 82A306 is changed from IN1 to LBOP (Latched-Byte-enable-Option)
If this pin is tied to VCC, LBE<3:0>* will be changed at the falling
edge of SCLK while MALE* is low. If the pin is tied to GND,
LBE<3:0>* will be latched at the rising edge of MALE*. An internal pull
up is provided for this pin so that it is high as a default.
      Impact: If you used this buffer as specified, your system design will be affected.

(7)   Reference: Data Sheet - Advance Information.   56

| | Change: | Pin 11 of 82A306 AF32* signal is latched by SCLK falling edge while MALE* is low. This is to allow for interfaces to 80387 like devices. |
| | Impact: | This will provide you a cleaner interface to 80387. |

(8)   Reference: Data Sheet - Advance Information.

         Change: The timing diagram on page 101 and the timing descriptions on page 97 of the data sheet are incorrect. The rising and falling edges of the signals REF* and LMEGCS* are reversed for the signal timing t626 to t633.
Please make a note of this in your data sheet.

         Impact: Corrected in the next revision of data sheet.

If you have any questions or concerns on anything contained in this document, please contact our sales representatives or field applications engineers.

Ref.:   PA01/2-87
            PA03/3-87

57

CS8230 AT/386 CHIPSet PRODUCT UPDATE

CHIP PART #:   P82C301

PART IDENTIFICATION ON PART: TC19G032-AT004 (Initial Version)
                                                          and
                                                          7034-0010 (First Revision and Current Production Parts)

STATUS: A new P82C301 with the following part identification on the part: "82C301   C" will become available (in production) toward the end of March 1988. This new P82C301 will replace the current production part. The following changes have been made to the "82C301   C":

1.   CHANGE: Change the design to accommodate add-on cards that generate IOCS16# by gating address decode with IOR# and IOW#.

        REASON FOR CHANGE: A detail description of this anomaly is attached.

2.   CHANGE: Change the design to support non-pipelined 0 wait state cycles.

        REASON FOR CHANGE: In the old 82C301, the AF32# signal was sampled too late into the cycle and therefore did not allow for 0 wait state non-pipelined operation. In order to allow the 386/AT cache controller (82C307) to operate in zero wait state non-pipeline operation with the data cache (SRAMs), AF32# is now sampled earlier. This change is done only to allow the 82C301 to work more efficiently with the cache controller and is transparent to all current designs.

3.   CHANGE: Change the design to disallow any MALE# signal during CPU reset (RESET3).

        REASON FOR CHANGE: MALE# was becoming active during reset. However, since the rest of the CHIPSet was in a reset state, it did not affect the functionality of the system. In order to avoid any potential future problems, we have changed the part to not allow the MALE# signal to go active when the CPU reset (RESET3) signal is active. This change should be transparent to all current designs.

4.   CHANGE: Change the design to disallow HLDA and CPU reset (RESET3) to occur at the same time.

        REASON FOR CHANGE: In order to change from protected mode to real mode in a 286-based system, reset had to be generated. Therefore, with 286-based software, a potential problem could occur if another bus master is performing DMA at the same time reset is being generated. This very rare problem occurs because of a potential interlock problem between the reset and the HLDA. In order to avoid this rare interlock problem, the 82C301 has been changed so that the CPU reset (RESET3) signal and the HLDA signal cannot both be active at the same time. This change should be transparent to all current designs.

58

5.   <u>CHANGE:</u>   Delay sampling of the IOCHRDY signal by a quarter of a T state.

     <u>REASON FOR CHANGE:</u> This is a fix for certain AT add-on cards that have been poorly designed. On these particular AT add-on cards, the IOCHRDY signal is generated too late. The new 82C301 has been modified to allow the part to sample the IOCHRDY signal later into the cycle. This will allow enough time for the add-on card to generate its IOCHRDY signal on time. This change should be transparent to all current designs.

6.   <u>CHANGE:</u>   Change the version number (bits 7, 6 of register 04H) from 00 to 01.

     <u>REASON FOR CHANGE:</u> This change is done so that the version number of the part can be identified by reading register 04H.

59

CHIP PART #:   P82C301

PART IDENTIFICATION ON PART: TC19G032-ATOO4   7034-004 (Initial Version)
and
7034-0010 (First Revision)

STATUS: Both the initial version and the first revision parts exhibit this anomaly.

ANOMALY: Novell's Disk Co-Processor board does not work correctly with the CS8230 CHIPSet (or
specifically the P82C301 of the CS8230 CHIPSet). The Novell Disk Co-Processor board is a
sixteen bit card that generates IOCS16# by gating address decode with IOR# and IOW#. This
causes IOCS16# to be generated too late for the CS8230 CHIPSet to recognize it, and incorrect
bus conversion will occur. A detailed analysis of the problem is attached.

CHIPS investigation of current sixteen bit cards in the marketplace reveals that only the Novell
Disk Co-Processor board fails to function correctly with the CS8230 CHIPSet. Other 16-bit
cards, such as the Western Digital Hard/Floppy Disk Controller Card, and the Ungerman Bass
Ethernet Controller Card, work correctly with the CS8230 CHIPSet.

FIX: Novell was notified of the problem and has found a solution. The fix requires that one of the
PALs on the Novell Co-Processor board be replaced with a new PAL. The PALs are pin
compatible and the only difference is the equations which reside in the PALs. Novell will
support customers wishing to use their Disk Co-Processor boards with the CS8230 CHIPSet. In
fact, customers can contact Richard Buhler of Novell Service Division, Provo, Utah 1-800-526-
7937 to obtain the new PAL. This new PAL will only be supported if used in a manufacturer's
386 machine validated by Novell's Service Division. Use of this PAL in a non-qualified 386 PC
will void warranty of the Disk Co-Processor Board. 386 designs using the CS8230 CHIPSet
should have no problems getting validated by Novell.

PLAN: CHIPS has found an internal fix to the problem which is currently being implemented in the
P82C301 silicon. The next revision silicon, which will be identified as "P82C301   C", will
correct the problem and will be available (in production) towards the end of March 1988. This
new revision will not require the use of the new PAL from Novell.

60

CS8230 IOCS16# OPERATION:

IOCS16# sampling on an IBM PC/AT

The "IOCS16#" signal, when active, informs the system board that the current transfer is a sixteen bit, 1 wait state I/O access. This signal must be driven active by a 16-bit I/O device after decoding a valid address select from SA0-SA15. It is an active low, open collector tri-state output.

It is possible that IOCS16# will be active during a memory cycle or that MEMCS16# will be active during an I/O cycle. The logic on the system board will know whether a memory or an I/O cycle is active and will only sample the appropriate input. (Note: Even if MEMCS16# is activated during an I/O cycle, it is ignored. There is no need to gate the IOCS16# with either the IOR# or the IOW# signals, as it is redundant).

Figure 1.0. illustrates the setup and hold requirements for IOCS16# signal and Table 1.0 specifies the timing parameters that have to be met to ensure that IOCS16# is sampled active.
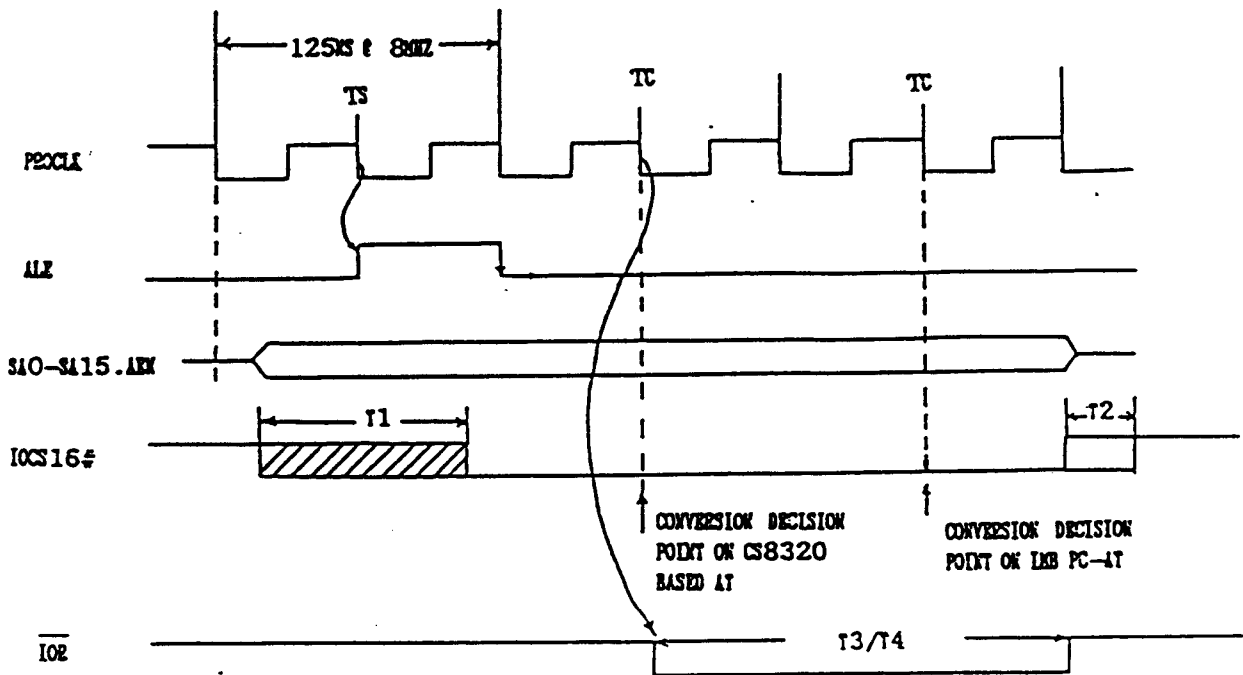

Figure 1.0. IOCS16# sampling

Sym	Parameter Description	Min	Typ	Max
T1	IOCS16# active from valid address	0	--	90
T2	IOCS16# inactive from address change	0	--	90
T3	Fast I/O cycle command pulse width	175	350	600
T4	Slow I/O cycle command pulse width	540	630	1000

Table 1.0. IOCS16# Timing

61

IOCS16# is sampled in the middle of T_C cycle. If IOCS16# is sampled active on this clock edge (ie. IOCS16# meets the setup timing requirement) then a sixteen bit cycle is invoked and the corresponding bus conversion cycle is performed (ie. If the CPU performs a sixteen bit operation, then only one cycle is performed. If on the other hand, a 32 bit write is initiated by the CPU, then two sixteen-bit write cycles are performed).

IOCS16# sampling on the CS8230 CHIPSet

The IOCS16# is sampled twice on the CS8230 CHIPSet.

1. IOCS16# is sampled on the falling edge of ALE to determine if the current access is to an eight or a sixteen bit I/O device and to determine the number of wait states.

2. The IOCS16# is again sampled at the start of the T_C cycle to decide the bus conversion algorithm to be used.

Three different techniques can be employed by add on card vendors to generate IOCS16# signal:

1. Generating IOCS16# from unlatched SA<0:15>

On the CS8230 CHIPSet, there is no need to latch SA<0:15> as they are valid throughout the I/O cycle. If unlatched addresses are used to generate IOCS16#, then the setup timing requirement are met as shown by the timing analysis carried out below:.

2TCLCL - ATEN active delay - SA addresses valid from ATEN# active - propagation delay for the address decode - IOCS16# setup time >> 0 ns

@ 8MHz

125 - t115 - t406 - tPD (decode logic) - t131 >> 0 ns

125 - 20 - 33 - tPD (address decode logic) - 35 >> 0ns

tPD(address decode logic) << 37ns

This allows the use of two levels of fast TTL gates to generate IOCS16# and still meet the IOCS16# setup requirements.

2. Generating IOCS16# from latched SA<0:15>

If the sixteen bit I/O cards use a transparent latch to latch the SA<0:15> addresses then the IOCS16# setup requirement of 35 ns will be violated if the propagation delay of the address decode circuitry exceeds:

@8MHz

61.25ns-tPD(74ALS373)-tPD(decode circuit)-IOCS16# setup time >>0 ns

61.25 - 23 - tPD (decode circuit) - 35 >> 0ns

tPD (decode circuit) << 3.25 ns.

62

This time is not sufficient to decode the addresses and generate IOCS16# and meet the IOCS16# setup time.

IOCS16# will be sampled inactive on the falling edge of ALE. The programmed number of wait states for 8-bit I/O device will be used for this access.

IOCS16# will again be sampled at the start of the TC cycle. IOCS16# has to be sampled low for the correct bus conversion. Unless the decode logic propagation delay is greater than 61.25 ns, the IOCS16# will be sampled active on this clock edge and the correct bus conversion will be used.

In conclusion, if IOCS16# is generated using latched SA<0:15>, sixteen bit transfers will be performed and the cycle will terminate correctly. But, the number of wait states will be that programmed for eight bit I/O device. The default number of wait states for an 8-bit I/O access is 5 wait states. This can be programmed to 2 wait states by programming Bits (3:2) of Reg 06H to 11 respectively.

3. Generating IOCS16# by gating address decode with IOR# and IOW#

IBM PC/AT specification states that IOCS16# has to be activated no later than 90 ns following valid addresses on SA<0:15> (Refer to Table 1). If IOR# or IOW# is factored into the IOCS16# generation logic, then IOCS16# is activated much later than 90 ns, thereby violating the IOCS16# specification.

Cards that factor IOR# or IOW# into IOCS16# generation logic will work in the IBM PC/AT environment as they are sampled in the middle of the second TC cycle (Refer to Figure 1.).

These cards however will not operate on PC/AT compatible machines based around the CS8230 CHIPSet, as IOCS16# is activated past the second sampling window. As IOCS16# is not sampled active, INCORRECT BUS CONVERSION WILL OCCUR, THEREBY RESULTING IN IMPROPER OPERATION.

CONCLUSION

We have currently found only one 16-bit board, the Novell Disk Co-processor board, which factor IOR# and IOW# to generate IOCS16# and therefore fail to function correctly with the CS8230 CHIPSet. It is violating the IBM/PC AT IOCS16# specification. However, the card will work in an IBM PC/AT environment but will not work on CS8230 based compatible machines. The reason for this is that IBM PC/AT machines are very lenient in terms of their timing parameters.

Novell was notified of the problem and has found a solution. The fix requires one PAL. Novell will support manufacturers wishing to use their Disk Co-Processor boards with the CS8230 CHIPSet. In fact, customers can contact Richard Buhler of Novell Service Division, Provo, Utah 1-800-526-7937 to obtain the equations for the PAL.

CHIPS has found an internal fix and it is currently being implemented in the P82C301 silicon. This fix will allow the CHIPS' CS8230 CHIPSet to function correctly regardless of whether IOCS16# is generated from:

1.   Unlatched SA<0:15>
2.   Latched SA<0:15>, or
3.   Gating address decode with IOR# or IOW#

Specifically, the 82C301 will be modified to accommodate the card(s) that violate the IOCS16# specification.

As was stated initially, parts with the fix incorporated in them will be available (in production) towards the end of March 1988.

63

SECTION E

82C302 REV C CHANGES

64

Features of 82C302 Rev C.

The default state of the 82C302 Rev C is similar to Rev B except for the 3 non-programmable features listed at the bottom of this page.

In addition to the registers which the 82C302 version B has, a new register at location 20H is implemented in version C, and is accessible through I/O ports 22H and 23H. This new register allows the user to enable the additional features that we have incorporated into the 82C302 Rev C.

4 bits are used in this byte and they are defined as follow:

REG20<7>: Deassert RAS- for non-pipelined cycles.

     0   default value, same as version B.
     1   All 4 CPU DRAM control state machines will be reset to idle when a pipelined
              cycle is followed by a non-pipelined cycle. Therefore, all RAS-'s will be deasserted
              and the minimum RAS- precharge time could be 75ns at 20 MHz system speed.

REG20<6>: Disable stagger RAS- refresh mode.

     0   default value, Staggered refresh.
     1   All 4 RAS-'s will be active at the same time.

REG20<5,4>: Fast CAS- precharge time.

     0   default value
     1   CAS- precharge time can be 1 CLK2 cycle. This will eliminate the extra wait state
              of a read cycle immediately following a write cycle to the same bank. REG20<5>
              controls CAS<1:0> and REG20<4> controls CAS<3:2> precharge timings.

REG20<3,2,1,0>: These bits are not used.

Non-programmable features of 82C302 version C include

1)   1 wait state non-pipelined write cycle instead of 2 wait states.

2)   Bits 7 and 6 of register 08 will read 01 instead of 00.

3)   The page size of 1MEG DRAM is 4KB instead of 2KB.

65

Section E

The 82C302 Rev C has 2KB page size for 256K type DRAM's and 4K page size for 1M type DRAM's. Following table shows the address multiplexing for different organizations:

	ADDRESS ASSIGNMENT	ROW ADDR MA9-MA0	COLUMN MA9-MA0
One bank	256K DRAM's	A<19:11>	A<10:2>
	1M DRAM's	A<21:12>	A<11:2>
Inter-leave	256K DRAM's	A<20:12>	A<10:2>
	1M DRAM's	A<22:13>	A<11:2>

In interleaved memory cases, for 256K DRAM's, address bit A<11> determines which bank is accessed. Address bit A<12> is used in 1M DRAM's to determine which bank is accessed.

The Column addresses shown in the above table are in sequence, however, the row addresses shown are not necessarily in sequence. Following table shows the row address multiplexing:

ROW ADDRESS MA9-MA0

	ROW ADDRESS MA9-MA0
One bank, 256K DRAM	19.18,17,16,15,14,13,12,11
One bank, 1M DRAM's	21,19,18,17,16,15,14,13,12,20
Interleave, 256K DRAM	19.18,17,16,15,14,13,12,20
Interleave, 1M DRAM's	21,19,18,17,16,15,14,13,22,20

Following timing diagrams illustrate the new features of the 82C302 Rev C.

Figure 13: Deassertion of RAS- signals for non-pipelined cycle.

Figure 14 A&B: Staggered and non-staggered RAS- refresh.

Figure 15 A&B: Fast CAS- precharge time.

Figure 16: 1 WS non-pipelined write cycle.

66

FIGURE 13: Deassert RAS- for non-pipeline cycles.

REG20<7>=1

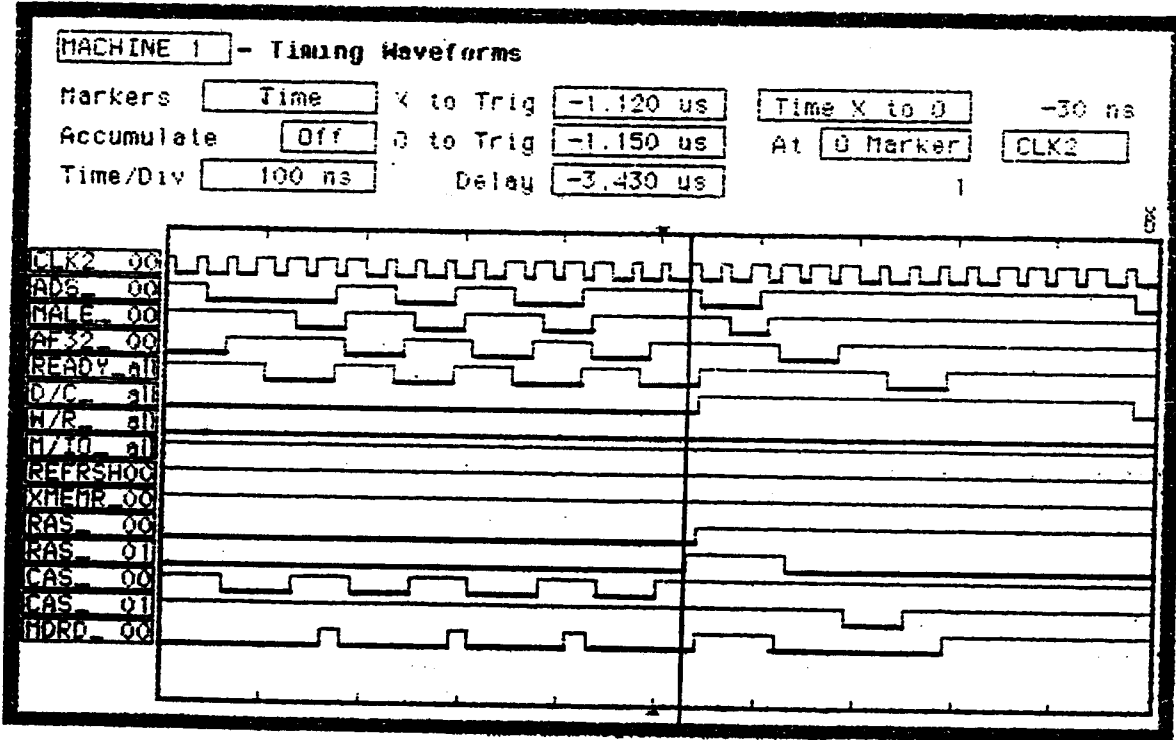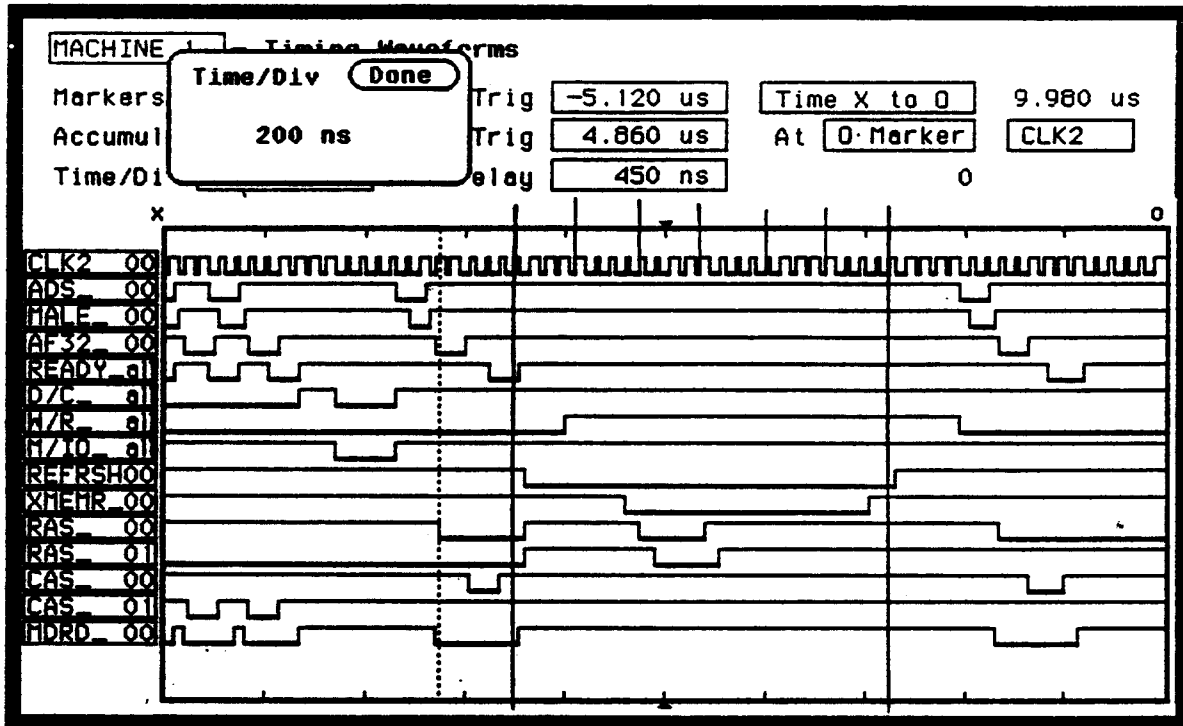FIGURE 14 A: Staggered refresh   REG20<6>=0.

FIGURE 14 B: Non-staggered refresh   REG20<6>=1.
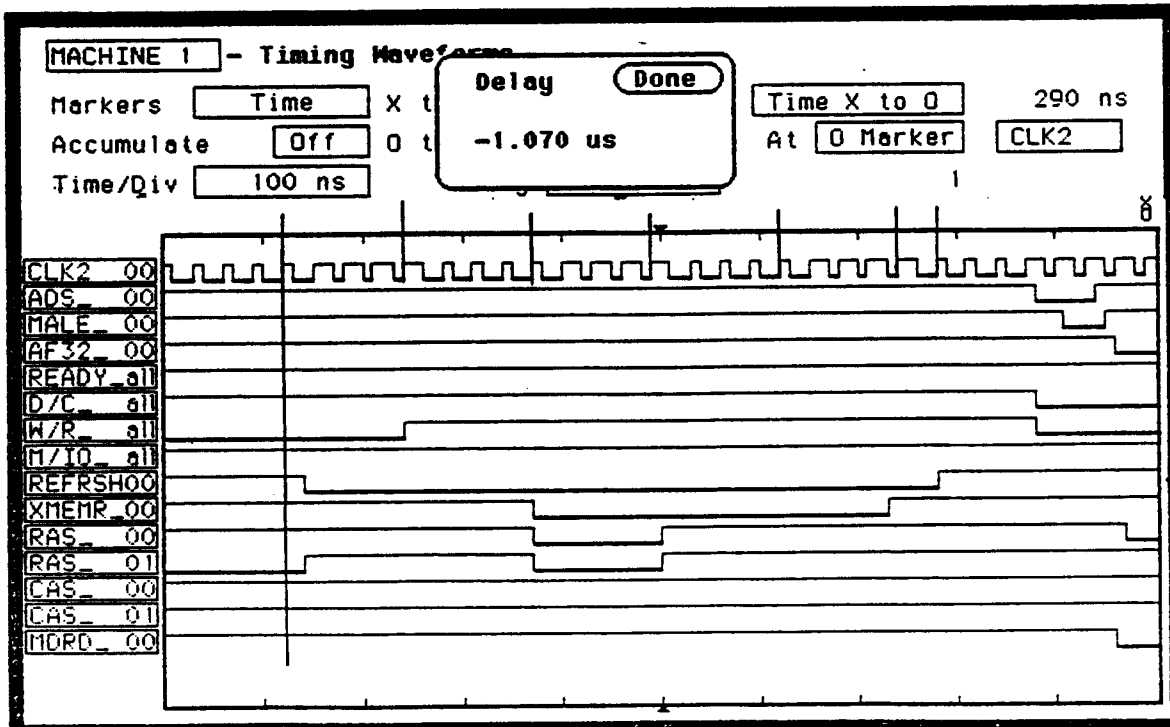

68

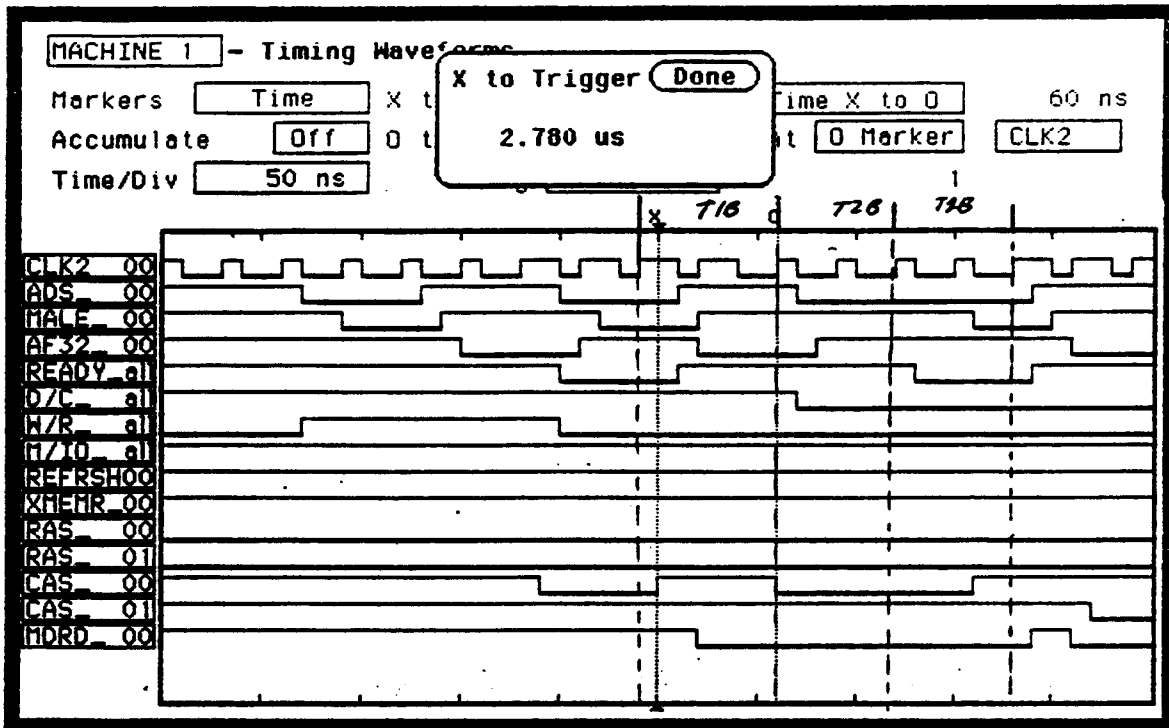**FIGURE 15 A: CAS- precharge time   REG20<5>=0.**
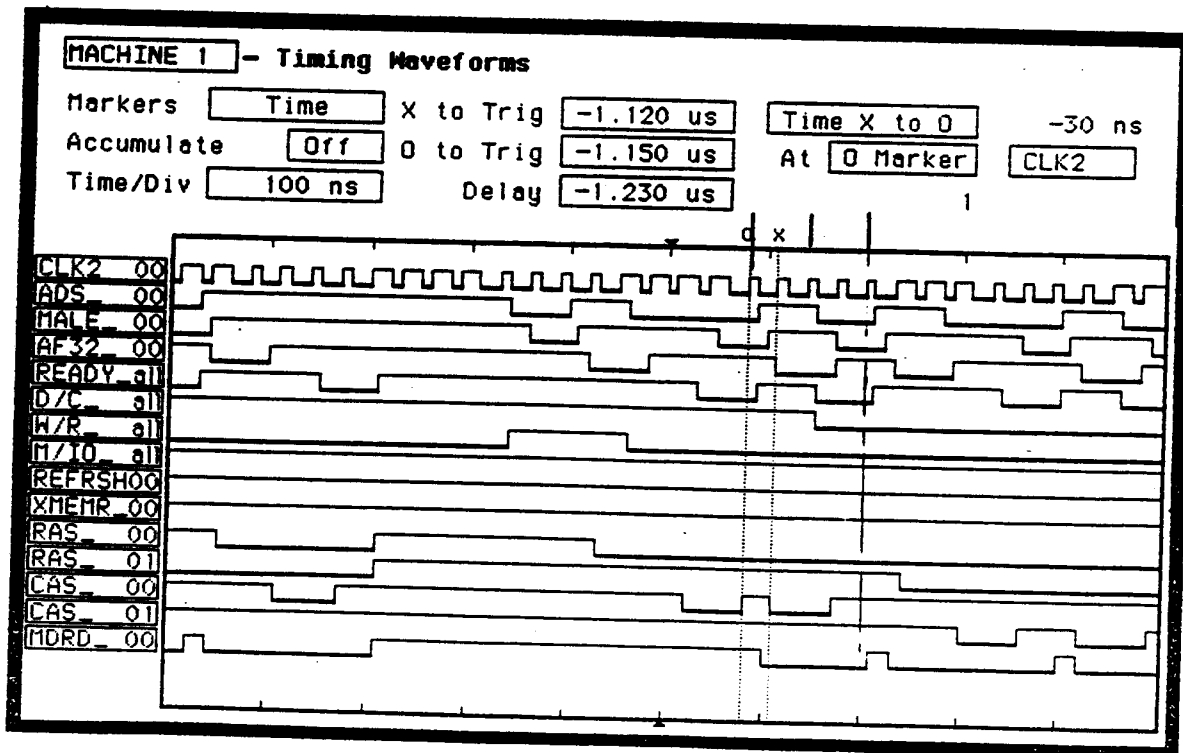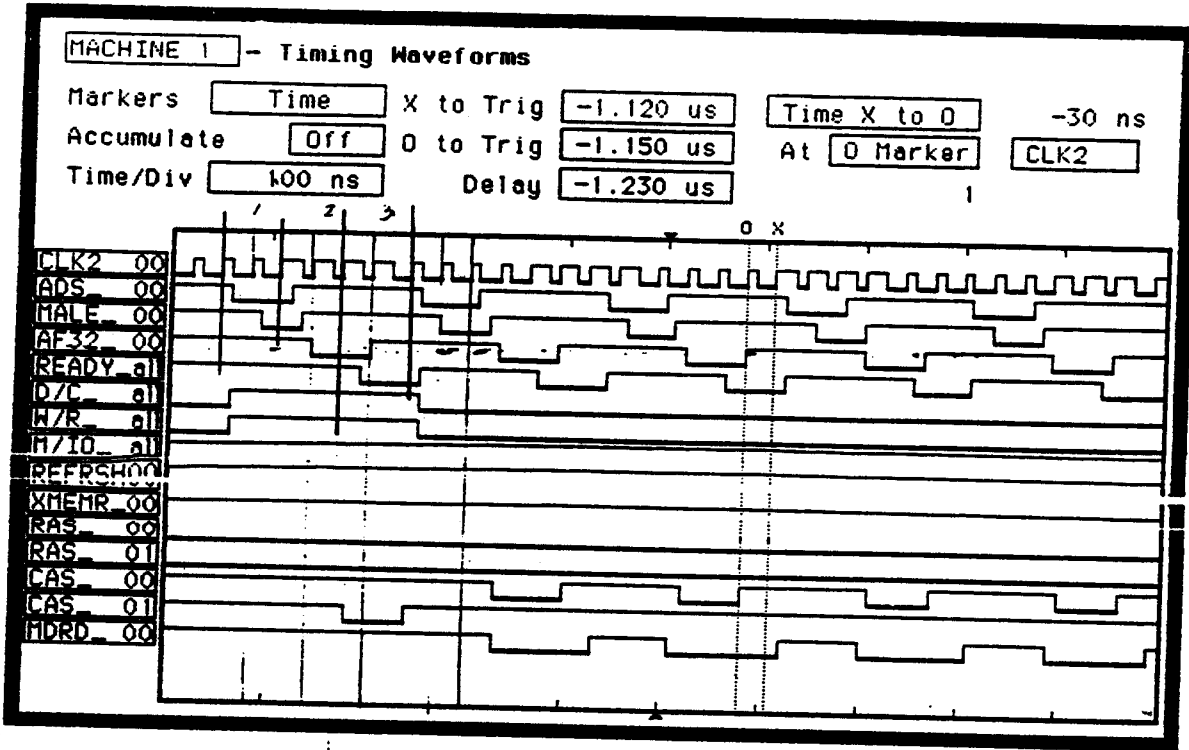

FIGURE 15 B: CAS- precharge time   REG20<5>=1.

FIGURE 16: 1 wait state Non-pipeline write cycle.

70

SECTION F

DK8230 ANOMALY SHEETS

Parity Error Anomaly

82A306 generates the parity bits during the write cycles and checks the parity bits during the read cycles. At high frequencies, due to late arrivall of the Byte Enable bits (BE0- thru BE3-), the parity logic generates parity error during the partial_double_word read cycles. To avoid this problem, connect the FBE- from 82C302 to the FBE- of 82A306. By doing this, all the read cycles will be a 32-bit read and the BE- bits will be ignored by the parity logic.

72

SA<17:19> Bus contention anomaly

Since the SA<17:19> and LA<17:19> are not isolated in the DK8230 board, there is a possibility of bus contention when a master card is on the I/O channel. A master card such as an intelligent Network controller may drive both LA<17:19> and SA<17:19> independently and cause bus contention.

Work Around

One way to solve this problem is to isolate the LA<17:19> lines from the SA<17:19>. This can be accomplished by using a 74ALS244 buffer and using the inverted MASTER- signal to control the direction of the buffer.

73
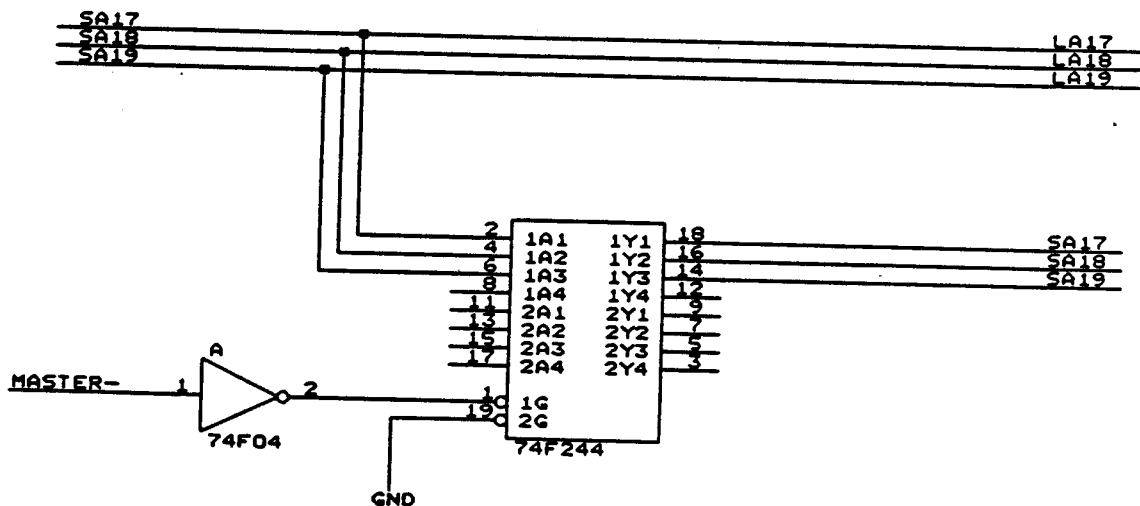
DMA problem with AST cards

The AST memory card in Expanded mode and 8 bit DMA transfer fails in a DK8230 system. The reason is that the AST activates MEMCS16- for onboard memory accesses; consequently, the CS8230 chipset recognizes the DMA cycle as 16 bit transfer and activates the 8-bit to 16-bit transfer.

Following PAL equations should resolve the AST RAM card problem.

```
PAL16L8
IBUSCTL   CHIPS 386 BUS CONTROL PAL
CHIPS AND TECHNOLOGIES   SAN JOSE, CA


/LCSROM SDIR /287CS HLDA1 /ATEN /AEN8 /XBHE /MEMCS16 /XIOR
GND
NC NC NC /AF32 NC NC /ENHLB /SBUSEN DIR245 VCC


/DIR245 =   /LCSROM * /SDIR */287CS
          + /LCSROM * /SDIR */XIOR

SBUSEN =    ATEN
         + HLDA1

ENHLB =  AEN8  * XBHE * MEMCS16 * /AF32


DESCRIPTION
```