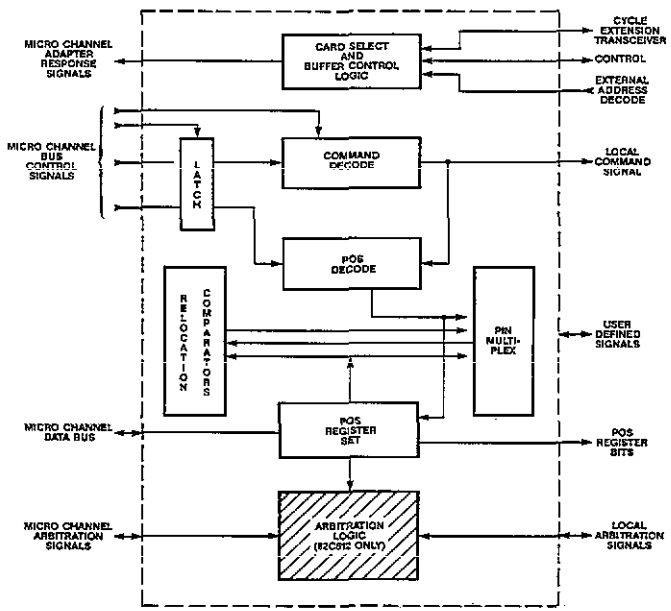
82C611, 82C612
MicroCHIPS™: Micro Channel™ Interface Parts

- **Implements 100% IBM® PS/2™ Compatible Micro Channel Adapters**
- **82C611 Supports Multi-function, I/O and Memory Adapters.**
- **82C612 Supports Controller-type Adapters Including All DMA Slave Arbitration Functions.**
- **Programmable Option Select (POS) Support Including:**
  - **Adapter ID Support**
  - **Flexible I/O and Memory Relocation Support**
  - **POS Port Decode Logic and Handshaking**
- **Full Micro Channel Interface Including:**
  - **Command and Status Decoding**
  - **Response Signal Generation**
  - **Full DMA Slave Arbitration and Handshake (82C612 only)**
- **Meets all IBM specified Timing and Drive Specifications.**
- **Simplifies migration of XT/AT adapter designs to the Micro Channel.**
- **Available as 68-pin PLCC or 80-pin PFP components.**

Description

The MicroCHIPS (Micro Channel Interface Parts) family of components integrates most of the interface logic required on an adapter card for the Micro Channel—IBM's new high speed bus for its latest generation of PCs. MicroCHIPS provide many benefits to designers of add-in adapters for the Micro Channel: Space savings because of the single-chip VLSI approach, cost savings because of the integration of many components into one, and time savings because of the ease of design.

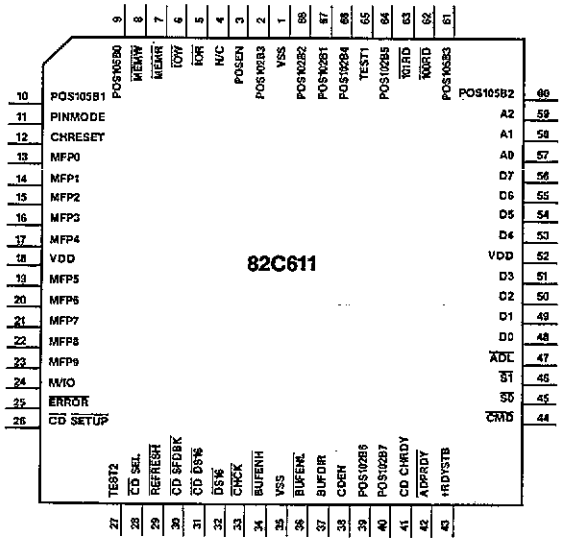


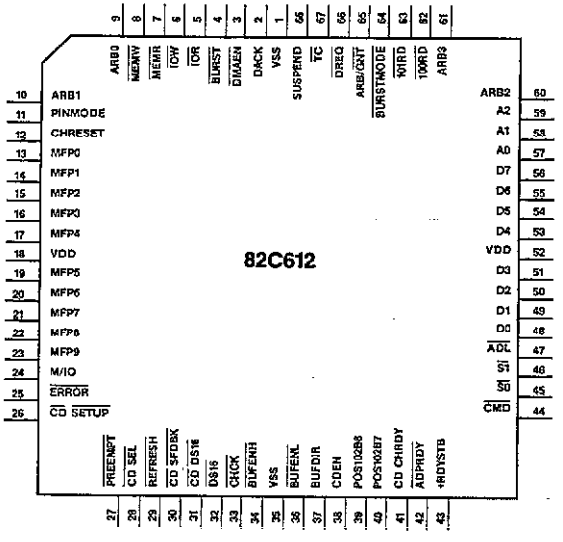
Simplified Block Diagram of the 82C611/612

There are currently two members of the MicroCHIPS family: The 82C611 is optimized for memory and I/O interfaces such as those on multi-function cards. It does not support the DMA arbitration and handshaking signals. The 82C612 adds full support for DMA arbitration and handshaking including single cycle and burst modes. It also supports both "preempt" and "fairness" modes as defined by IBM. Both chips are available in either a 68-pin PLCC (plastic leadless chip carrier) or 80-pin PFP (plastic flat pack) packages.

In addition to the standard functions supplied by the 82C611 and 82C612, CHIPS has the capability to customize these standard devices for dedicated high-volume applications. The macrocells for these parts can be integrated into custom controller designs.

Note: IBM uses a leading minus sign (-) to indicate an active low signal. The convention used in this data sheet is the overbar. Therefore a signal such as -ADL in th IBM documentation would be represented as $\overline{ADL}$ herein.


82C611
10 POS105B1
11 PINMODE
12 CHRESET
13 MFP0
14 MFP1
15 MFP2
16 MFP3
17 MFP4
18 VDD
19 MFP5
20 MFP6
21 MFP7
22 MFP8
23 MFP9
24 M/IO
25 ERROR
26 CD SETUP
9 POS105B0
8 MEMW
7 MEMR
6 IOW
5 IOR
4 H/C
3 POSEN
2 POS102B3
1 VSS
88 POS102B2
87 POS102B1
86 POS102B4
85 TEST1
84 POS102B5
83 IORD
82 IOWR
81 POS105B3
80 POS105B2
59 A2
58 A1
57 A0
56 D7
55 D6
54 D5
53 D4
52 VDD
51 D3
50 D2
49 D1
48 D0
47 ADL
46 SI
45 SO
44 CMD
27 TEST2
28 CD SEL
29 REFRESH
30 CD SFDBK
31 CD DS16
32 DS16
33 CHCK
34 BUFENH
35 VSS
36 BUFENL
37 BUFDIR
38 CDEN
39 POS102B6
40 POS102B7
41 CD CHRDY
42 ADRDY
43 +RDYSTB


82C612
10 ARB1
11 PINMODE
12 CHRESET
13 MFP0
14 MFP1
15 MFP2
16 MFP3
17 MFP4
18 VDD
19 MFP5
20 MFP6
21 MFP7
22 MFP8
23 MFP9
24 M/IO
25 ERROR
26 CD SETUP
9 ARB0
8 MEMW
7 MEMR
6 IOW
5 IOR
4 BURST
3 DMAEN
2 DACK
1 VSS
66 SUSPEND
67 TC
68 DREQ
65 ARB/GNT
64 BURSTMODE
63 IORD
62 IOWR
61 ARB3
60 ARB2
59 A2
58 A1
57 A0
56 D7
55 D6
54 D5
53 D4
52 VDD
51 D3
50 D2
49 D1
48 D0
47 ADL
46 SI
45 SO
44 CMD
27 PREEMPT
28 CD SEL
29 REFRESH
30 CD SFDBK
31 CD DS16
32 DS16
33 CHCK
34 BUFENH
35 VSS
36 BUFENL
37 BUFDIR
38 CDEN
39 POS102B6
40 POS102B7
41 CD CHRDY
42 ADRDY
43 +RDYSTB

Pin Description

Pin No.	Pin Type	Symbol	Pin Description
Micro Channel Bus Pins			
The pins in this group connect directly to the pins of the same name on the Micro Channel Bus. They meet all timing and drive specifications so no external buffers are required. For more information on the Micro Channel Architecture, please consult the IBM Technical References for either the PS/2 Models 50/60™ or the Model 80™. Another excellent document is the IBM Personal System/2™ Seminar Proceedings, Volume 5, Number 3.			
47	I	$\overline{ADL}$	**Address Decode Latch.** This signal is used to latch address and status information from the Micro Channel. It connects directly to the Micro Channel $\overline{ADL}$ pin.
24	I	M/$\overline{IO}$	**Memory/Input Output.** This signal indicates whether a memory or I/O cycle is in progress. It connects directly to the Micro Channel M/$\overline{IO}$ pin. Its state is latched internally with $\overline{ADL}$.
45	I	$\overline{S0}$	**Status Bit 0.** This signal, in conjunction with M/$\overline{IO}$ and $\overline{S1}$, indicates the type of cycle that is in progress. It connects directly to the Micro Channel $\overline{S0}$ pin. It is latched internally with $\overline{ADL}$. See Table 1.0 for details on how M/$\overline{IO}$, $\overline{S0}$ and $\overline{S1}$ are decoded.
46	I	$\overline{S1}$	**Status Bit 1.** This signal, in conjunction with M/$\overline{IO}$ and $\overline{S0}$, indicates the type of cycle that is in progress. It connects directly to the Micro Channel $\overline{S1}$ pin. It is latched internally with $\overline{ADL}$. See Table 1.0 for details on how M/$\overline{IO}$, $\overline{S0}$ and $\overline{S1}$ are decoded.

Table 1.0

M/$\overline{IO}$	$\overline{S0}$	$\overline{S1}$	Function
0	0	0	Reserved A
0	0	1	I/O Write
0	1	0	I/O Read
0	1	1	Reserved B
1	0	0	Reserved C
1	0	1	Memory Write
1	1	0	Memory Read
1	1	1	Reserved D

Pin Description (Continued)

Pin No.	Pin Type	Symbol	Pin Description
44	I	$\overline{\text{CMD}}$	**Command.** This signal is the generalized data strobe. It signifies when data is valid on the bus for write cycles, and when valid data should be placed on the bus for read cycles. In the 82C611/612 it is used with the status information to generate internal and external read and write strobes. It connects directly to the Micro Channel $\overline{\text{CMD}}$ pin.
30	O	$\overline{\text{CD SFDBK}}$	**Card Selected Feedback.** Each memory or I/O slave card on the Micro Channel drives this line low to indicate that it has been selected (address space decode is true). It is a function of the $\overline{\text{CD SEL}}$ input. It is not driven during configuration (POS) or DMA cycles. This output is a standard totem-pole output per the IBM specification. It connects directly to the Micro Channel $\overline{\text{CD SFDBK}}$ pin.
31	O	$\overline{\text{CD DS16}}$	**Card Data Size 16.** This line is driven low to provide an indication that a memory, I/O or DMA slave is capable of 16 bit data transfers. It is not driven by slaves that are only capable of 8 bit transfers. It is a function of the $\overline{\text{DS16}}$ input. This output is a standard totem-pole output per the IBM specification. It connects directly to the Micro Channel $\overline{\text{CD DS16}}$ pin.
41	O	CD CHRDY	**Card Channel Ready.** This line is used by a memory or I/O slave to indicate whether or not it is ready to complete the current bus cycle. It is normally held high (ready) and pulled low (not ready) to extend the current bus cycle. This line is generated as a function of the +RDYSTB and $\overline{\text{ADPRDY}}$ inputs. The 82C611/612 supports both the "asynchronous extended" and the "synchronous extended" ready modes through a programmable option bit. This output is a standard totem-pole output per the IBM specification. It connects directly to the Micro Channel CD CHRDY pin.
59 58 57	I I I	A2 A1 A0	**Address Bits 0 through 2.** The three low order address lines from the bus. They are latched internally and used to select between the POS registers. They connect directly to the Micro Channel A0, A1 and A2 pins.
12	I	CHRESET	**Channel Reset.** This line is asserted high to reset or initialize all adapters to their power-up state. All internal registers in the 82C611/612 are reset to 0 on CHRESET. The mode of the multi-function pins are also established at CHRESET. This line connects directly to the Micro Channel CHRESET pin.

Pin Description (Continued)

Pin No.	Pin Type	Symbol	Pin Description
26	I	CD SETUP	**Card Setup.** This line is driven low to place the card in set-up mode. The system logic provides a separate CD SETUP signal to each connector slot. While this line is low, the POS registers are accessed. The card's status and ID are read at this time and initialization bytes are written. When this line is high, the POS registers may no longer be accessed. This line connects directly to the Micro Channel CD SETUP pin.
29	I	REFRESH	**Refresh.** This line goes low to indicate a refresh cycle is occurring on the Micro Channel bus, which looks like a normal bus memory read cycle. The 82C611/612 does not provide the CD SFDBK (card selected feedback) signal and the buffer enable signals (BUFENH and BUFENL) are held inactive while REFRESH is low. This line connects directly to the Micro Channel REFRESH pin.
33	O	CHCK	**Channel Check.** This signal is used to indicate a serious error (such as a memory failure) on an adapter card. It is a function of the ERROR input. This line is cleared when the 82C611/612 receives a CHRESET. It connects directly to Micro Channel CHCK pin.

DMA/Arbitration Pins (82C612 Only)

Note: The following pin descriptions apply only to the 82C612. The pins have different functions in the 82C611.

61 60 10 9	B B B B	ARB3 ARB2 ARB1 ARB0	**Arbitration Bus Priority Level.** These lines are used by DMA slaves and Bus Masters to arbitrate for control of the bus. They represent an encoded priority level from 0 (highest priority) to F hex (lowest priority). The 82C612 monitors and drives these lines when competing for the bus. It provides an indication to the adapter logic (via the DACK signal) that it has won the bus. These lines connect directly to the Micro Channel ARB3:0 pins.
65	I	ARB/GNT	**Arbitrate/Grant.** A rising edge on this line indicates the start of an arbitration interval, during which all adapters requesting control of the bus compete via the ARB3:0 lines. The falling edge of this signal indicates the end of the arbitration interval and the grant of the bus to the winner. This line connects directly to Micro Channel ARB/GNT pin.

Pin Description (Continued)

Pin No.	Pin Type	Symbol	Pin Description
27	B	PREEMPT	**Preempt.** This line is driven low by DMA slaves and bus masters to request the use of the bus. It must also be monitored by them in case another device also wants the bus. The 82C612 drives PREEMPT low when the adapter logic requests a DMA transfer (via DREQ). It will raise PREEMPT after it detects that it has won the bus. It also monitors PREEMPT while it has the bus and BURSTMODE is active to signal the adapter logic (via SUSPEND) that another device has requested the bus. This pin connects directly to the Micro Channel PREEMPT pin.
67	I	TC	**Terminal Count.** A low going pulse on this line indicates that the current DMA cycle is the last one of a series of transfers. Upon detection of a TC pulse, the 82C612 will release DACK and BURST at the end of the current DMA cycle. This line connects directly to the Micro Channel TC pin.
64	I	BURSTMODE	**Burst Mode.** This signal is driven low by the adapter logic to indicate that a "burst" DMA cycle is requested. The 82C612 will assert BURST on the Micro Channel when DREQ is asserted and monitor PREEMPT when BURSTMODE is active.
66	I	DREQ	**DMA Request.** This signal is driven low by the adapter logic when a DMA transfer is requested. It causes the 82C612 to request the bus and compete in the arbitration cycle. For single cycle transfers, the adapter logic should raise DREQ in response to the rising edge of DACK. For burst transfers, the adapter logic should raise DREQ in response to a TC pulse or the SUSPEND signal. For more information, see the "DMA Operations" section of this data sheet.
2	O	DACK	**DMA Acknowledge.** An active high signal from the 82C612 that indicates to the adapter logic that it has won the arbitration and has been granted the bus. DACK will bracket the entire DMA transfer. It will be dropped by the 82C612 when a TC is detected or in response to DREQ becoming inactive, at the end of the current DMA cycle.
68	O	SUSPEND	**Suspend.** An active high signal from the 82C612 that indicates to the adapter logic that another device has preempted a burst transfer currently in progress, and has not yet completed.
3	I	DMAEN	**DMA Enable.** This signal should be tied low to enable the DMA functions of the 82C612. Improper operation of the chip will result unless this pin is tied low.

Pin Description (Continued)

Pin No.	Pin Type	Symbol	Pin Description
Adapter Logic Pins			
The pins in this group, in addition to the Multi-Function Pins, provide the interface between the adapter logic circuits and the 82C611/612.			
7	O	$\overline{\text{MEMR}}$	**Memory Read.** This signal is an active low memory read strobe. It is active for any memory read cycle. It is also active during $\overline{\text{REFRESH}}$.
8	O	$\overline{\text{MEMW}}$	**Memory Write.** This signal is an active low memory write strobe. It is active for any memory write cycle.
5	O	$\overline{\text{IOR}}$	**I/O Read.** This signal is an active low I/O read strobe. It is active for any I/O read cycle.
6	O	$\overline{\text{IOW}}$	**I/O Write.** This signal is an active low I/O write strobe. It is active for any I/O write cycle.
28	I	$\overline{\text{CD SEL}}$	**Card Select.** The adapter logic drives this signal low to indicate that it has been addressed. It should be a composite select of both I/O and memory addresses if applicable. It must reflect unlatched addresses. The 82C611/612 latches this signal internally in order to generate stable strobes and enables.
32	I	$\overline{\text{DS16}}$	**Data Size 16.** The adapter logic drives this signal low to indicate a 16 bit data path. Conversely, a high on this line indicates an 8 bit data path. This signal should be based on a decode of the unlatched addresses if both 8 and 16 bit data paths are to be supported on the same card.
25	I	$\overline{\text{ERROR}}$	**Error.** The adapter logic drives this signal low to indicate that an error condition has occurred. A low level on $\overline{\text{ERROR}}$ causes the $\overline{\text{CHCK}}$ line to be asserted on the Micro Channel bus. It will go inactive when the card is disabled by writing a 1 to bit 0 of POS register 102 or during channel reset. None of these actions will actually clear the error. The $\overline{\text{ERROR}}$ line must be raised by the adapter logic. The fact that an error occurred is latched internally and made available as bit 7 of set-up register 105. This bit will stay at 0 (indicating an error occurred) even after the $\overline{\text{ERROR}}$ line is raised. It is set by writing a 1 to the same location.
42	I	$\overline{\text{ADPRDY}}$	**Adapter Ready.** An active low signal from the adapter logic indicating that the addressed portion of the adapter is slow and will require the cycle to be extended. This signal should be based on an un-latched decode of the address information. A low condition causes the 82C611/612 to lower the CD CHRDY line on the Micro Channel bus. It is removed by +RDYSTB for asynchronous extended cycles and by the leading edge of $\overline{\text{CMD}}$ for synchronous extended cycles.

Pin Description (Continued)

Pin No.	Pin Type	Symbol	Pin Description
43	I	+RDYSTB	**Ready Strobe.** The adapter logic causes a rising a edge on this line to tell the 82C611/612 that it is ready to complete the cycle. In response to this edge, the 82C611/612 will raise the CD CHRDY line on the Micro Channel bus.
38	O	CDEN	**Card Enabled.** This signal reflects the state of bit 0 in POS register 102. When high it indicates to the adapter logic that the card has been enabled for normal operation. According to the Micro Channel specification, all outputs to the Micro Channel (except those necessary for POS operation) should be de-gated when this signal is low. The 82C611/612 does this for all its applicable lines that are tied directly to the Micro Channel bus. This line will be set low following a CHRESET.
39 40	O O	POS102B6 POS102B7	**POS Register 102 Bits 6 and 7.** These lines reflect the state of POS register 102 bits 6 and 7. They are available for general purpose use by the adapter logic. They are reset to 0 by CHRESET.
63 62	O O	$\overline{101RD}$ $\overline{100RD}$	**POS Register 100 and 101 Read.** These signals are active low read strobes corresponding to POS registers 100 and 101. These are the registers that return the 16 bit CARD ID. These registers do not exist in the 82C611/612, so these lines must be used to gate external ID information onto the data bus. $\overline{100RD}$ corresponds to the low byte and $\overline{101RD}$ is the high byte.
36	O	$\overline{BUFENL}$	**Buffer Enable Low Byte.** This output is used to enable an external transceiver which isolates the low order data lines from the adapter logic (and the 82C611/612) from the Micro Channel data bus pins.
34	O	$\overline{BUFENH}$	**Buffer Enable High Byte.** This output is used to enable an external transceiver which isolates the high order data lines from the adapter logic (and the 82C611/612) from the Micro Channel data bus pins. The high byte transceiver is only enabled when the adapter logic has indicated (via $\overline{DS16}$) that a 16-bit data area has been addressed.
37	O	BUFDIR	**Buffer Direction.** This output controls the direction of the external data bus transceivers. A high on this pin indicates that a write cycle is being performed on the Micro Channel and the data transceivers should allow data to flow onto the adapter card.

Pin Description (Continued)

Pin No.	Pin Type	Symbol	Pin Description
56	B	D7	**Data Bus Bits 7 through 0.** This is the bidirectional data bus used to communicate data to and from the 82C611/612. They must be isolated from the Micro Channel with a transceiver, which would normally be the same transceiver used to isolate the low order data bus on the rest of the adpater logic.
55	B	D6	
54	B	D5	
53	B	D4	
51	B	D3	
50	B	D2	
49	B	D1	
48	B	D0	

Additional POS Register Output Pins (82C611 Only)

In addition to POS register pins available on the multi-function pins, the following POS register pins are available for general purpose use. Note that these pins are available on the 82C611 ONLY! In order to provide the designer with maximum flexibility, some of these lines have been implemented as open collector lines. They are not pulled up internally.

61	O (OC)	POS105B3	**POS Register 105 Bits 0 through 3.** These open-collector outputs reflect the state of POS register 105 bits 0 through 3. If applicable, they should be pulled up externally. They are reset to 0 on CH RESET.
60	O (OC)	POS105B2	
10	O (OC)	POS105B1	
9	O (OC)	POS105B0	
64	O	POS102B5	**POS Register 102 Bits 1 through 5.** These outputs reflect the state of POS register 102 bits 1 through 5. They are reset to 0 on CH RESET.
66	O	POS102B4	
2	O	POS102B3	
68	O	POS102B2	
67	O	POS102B1	
3	I	POSEN	**POS Register Output Enable.** This input should be tied to Vdd to enable the extra POS register outputs. Improper operation of the 82C611 will result if this pin is not tied to Vdd.
65	I	TEST1	**TEST INPUTS 1 and 2.** These two pins are used at the factory to test the 82C611. They should be tied to +5 volts through a 10K ohm pull-up resistor (may be the same resistor). Improper operation of the 82C611 will result if these pins are not connected properly.
27	I	TEST2	

Multi-Function Pins

The multi-function pins (MFP0:9) are a group of 10 pins whose functions are changed by a strapping option. Fot the most part, the function of these pins is related to POS support. Depending on the mode, varying amounts of relocation support are provided.

11	O	PINMODE	**Pin mode.** This pin is tied one of three ways to determine which mode the multi-function pins are in. If this input is tied to Vss, pin mode 0 will be selected. If tied to Vdd, pin mode 1 will be selected. If tied to CHRESET, pin mode 2 will be selected. Note that the state of this pin is sampled at power-up and CHRESET and is not intended to be changed "on-the-fly". Errors in the operation of the 82C611/612 will result.

82C611, 82C612 AC Characteristics (Continued)

Sym	Parameter			Min	Max	Units
23	O	MFP9	**Multi-function Pins 0-9.** The function of these pins in the various pin modes is described in the Pin Modes section of this data sheet.			
22	O	MFP8				
21	O	MFP7				
20	O	MFP6				
19	O	MFP5				
17	O	MFP4				
16	O	MFP3				
15	O	MFP2				
14	O	MFP1				
13	O	MFP0				
Power Supply						
18,52		Vdd	**Power Supply.**			
1,35		Vss	**Ground.**			

1. FEATURES

1.1 Features Common to Both the 82C611 and 82C612.

The 82C611 and 82C612 are VLSI components designed to provide the adapter card designer with a quick, easy and cost-effective means of interfacing to the Micro Channel bus. They provide a direct interface to the bus command and status signals, and decode them into a set of general purpose signals for use by the adapter logic. These signals include memory read and write strobes, I/O read and write strobes, and data buffer control lines. These signals have purposely been made to resemble XT/AT bus signals to aid the designer in moving existing designs from those buses to the Micro Channel.

The 82C611 and 82C612 also provide support for the Programmble Option Select (POS) system implemented on the Micro Channel. The POS system consists of up to 8 registers located on each adapter card. These registers are used to set board parameters such as addressing, interrupt level and to read the board's ID. A goal of the POS system is to eliminate jumpers and switches on the adapter card. This means that board resources should be relocatable through the POS registers.

The 82C611/612 fully decodes these registers and provides varying amounts of relocation support depending on a strapping option. Ten multi-function pins are used to support relocation. Their functions vary depending on the strapping option.

1.2 The 82C611

The 82C611 is intended for I/O, memory and multi-function cards. It does not provide support for DMA Slaves.

1.3 The 82C612

The 82C612 is intended for use on DMA Slave cards. A DMA slave is one which uses the DMA controller in the system to generate addresses, status information and strobes. In addition to the features described above, the 82C612 provides full support for DMA arbitration and handshaking. The arbitration level is programmable through the POS system. The 82C612 supports both single-cycle and burst modes of operation. In burst mode, it supports the fairness algorithm as defined by IBM. Fairness is also programmable.

1.4 Functions Not Supported By the 82C611 or 82C612

The 82C611/612 are intended for both 8 and 16 bit applications. No support is provided for 32 bit operations. The 82C611/612 does not support matched memory cycles. These have been designated by IBM for 32 bit memory cycles only. Lastly, the chips do not provide any interrupt logic, but this is easily implemented externally.

2. FUNCTIONAL DESCRIPTION

This section decribes the major functional blocks of the 82C611/612.

2.1 The Bus Interface

The 82C611/612 provide a complete interface to the Micro Channel bus. Since the chips meet the timing and bus drive requirements, most lines (with the exception of the data bus) connect directly to the Micro Channel bus pins. The designer does not need to do anything special with these lines, just connect them. The exact function of these signals is described in the Pin Descriptions section of this data sheet, and also in the IBM Technical References.

2.2 The Adapter Logic Interface

The 82C611/612 decodes the signals from the bus into a set of adapter logic signals. These signals include memory and I/O read and write strobes, data bus buffer control signals and a master "card enabled" signal. Inputs are also provided so that the adapter logic may control the type of cycle being run (either 8 or 16 bits), extend the cycle, and signal error conditions. A card select input is driven by an external address decoder. The exact function of these signals are described in the Pin Descriptions section of this data sheet. General descriptions follow:

2.2.1 I/O and Memory Read and Write Strobes

The 82C611/612 provides four strobes—one each for memory reads and writes and I/O reads and writes. They are based on a decode of the status and the $\overline{CMD}$ line from the Micro Channel and are active for all bus cycles.

2.2.2 Data Bus Buffer Control Signals

The 82C611/612 provides two enable signals and one direction signal for controlling external data buffers on the adapter. These buffers are used to isolate the adapter logic and the 82C611/612 from the Micro Channel data bus.

These buffers are usually implemented with '245 transceivers. Only one transceiver is required for an adapter that only supports 8 bit transfers. The $\overline{BUFENL}$ signal enables the low order data transceiver and the $\overline{BUFENH}$ signal enables the high order data transceiver (if required). BUFDIR is connected to the direction control of the transceivers, and the "A" bus of the '245 is connected to the Micro Channel data bus with the "B" bus connected to the internal adapter data bus.

2.2.3 Ready Signals

If the adapter design needs more time to transfer data on the Micro Channel, it can request that the cycle be extended. This is commonly known as a wait state, but on the Micro Channel it is called an extended cycle.

The Micro Channel supports two types of "extended" cycles: Asynchronous Extended and Synchronous Extended. The difference between the two is when the CD CHRDY signal is removed. In the asynchronous case, CD CHRDY is removed by the adapter at any time. In the synchronous case, CD CHRDY is removed synchronous within 30 nanoseconds of the falling edge of $\overline{CMD}$. The synchronous extended cycle will consist of one wait state. The asynchronous extended cycle may consist of one or more wait states.

The 82C611/612 supports both types of extended cycles through a bit programmed during POS (POS register 105, bit 5).

The 82C611/612 causes an extended cycle when the $\overline{ADPRDY}$ signal is pulled low by the adapter logic. This is caused by an unlatched decode of the portion of the adapter circuitry that is slow. For an asynchronous extended cycle (Register 105, bit 5 low) a rising edge on the +RDYSTB line removes CD CHRDY causing the extended cycle to complete. For a synchronous extended cycle, CD CHRDY is removed by the 82C611/612 immediately following the falling edge of $\overline{CMD}$. Therefore the +RDYSTB signal need not be used and may be tied low.

Note that CD CHRDY must not be held low for more than 3 microseconds. It is up to the adapter logic to ensure that this condition is met.

2.2.4 Data Size

The $\overline{DS16}$ input to the 82C611/612 is used to tell the Micro Channel what data path size this card (or card section) is capable of handling. It is also used by the 82C611/612 to properly control the data bus buffers. If this is an 8 bit or 16 bit only card, this signal should be tied high or low respectively. If different sections of this board support different transfer sizes (for example a multi-function card with 8 bit I/O and 16 bit memory) then this line should be switched depending on which section of the board is addressed. It should be based on a decode of the unlatched addresses.

2.2.5 Card Select and Card Enable

The $\overline{CD\ SEL}$ line is the card select input to the 82C611/612. It should go low when this adapter is selected. It should be based on an unlatched address decode. For cards with both memory and I/O address spaces, this signal must be a composite of all of the address decodes. If the relocation functions of the 82C611/612 are being used, the "match" outputs must be part of the external decode—they are not combined internally with $\overline{CD\ SEL}$.

The POS system must have the ability to turn off or disable a non-functioning card, or one whose address conflicts cannot be resolved. It does this by setting or resetting the card enabled bit (POS register 2, bit 0). The state of this bit is brought out of the 82C611/612 on the CDEN line. When high, the card is enabled. This signal should qualify the address decoders for the card.

2.2.6 Error Condition Reporting

When the adapter logic detects an error condition (like a memory parity error), it pulls the $\overline{\text{ERROR}}$ line low. This will cause the $\overline{\text{CHCK}}$ line to be asserted on the Micro Channel. The fact that an error occurred is latched inside the 82C611/612 and can be read as bit 7 of POS register 105. For more information, see the Pin Description section of this data sheet.

2.2.7 Multi-Function Pins

This set of 10 pins are used to support relocation and other POS operations. For more information, see the Pin Modes section of this data sheet.

2.2.8 DMA Support (82C612 only)

The 82C612 fully supports DMA slave operations. It contains the bus arbitration logic and DMA handshaking signals. The adapter functions have been designed to resemble the signals on the XT/AT bus (which are essentially those of the 8237). For a more complete description of the DMA protocol and signal functions, see the DMA Operations section of this data sheet.

3. POS SUPPORT

The POS (programmable option select) registers allow the system microprocessor to poll each card and determine its characteristics, as well as write configuration data to it. Ideally, all card resources should be relocatable through this mechanism so that addressing conflicts between cards can be eliminated without the need for jumpers or switches. In addition, each card is required to have a unique card ID so that the POS system knows how to configure it. This section describes how the 82C611/612 supports the POS.

3.1 POS Mechanism

Each connector in the Micro Channel has a unique signal called $\overline{\text{CD SETUP}}$, that when low, puts a card resident in that slot into the setup mode. During the POST (power-on self test) the system microprocessor puts each slot in turn into the set-up mode, reads its ID, and sends it configuration data. During set-up, each card has a set of registers that appear at I/O addresses 100 to 107H (called the POS registers). Since only one card at a time is in set-up mode, no address conflicts occur. The 82C611/612 has differing types of support for these registers, depending on the pin mode selected. The 82C611/612 also handles all of the mechanisms required by the POS system, such as set-up mode decoding and driving/not driving the proper signals. In addition to saving valuable board real estate, it allows the designer to concentrate on other aspects of the adapter design.

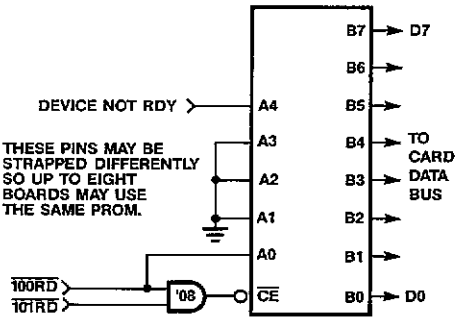
3.2 Card ID

The IBM specification for the Micro Channel states that each adapter type from a manufacturer must have a unique card ID. This is a 16 bit value. IBM recommends that adapter IDs be chosen according to the following table:

ID	Definition
0000	Device not ready
0001 to 0FFF	Bus Master
5000 to 5FFF	Direct Memory Access Devices
6000 to 6FFF	Direct Program Control (including memory-mapped I/O)
7000 to 7FFF	Storage (multiple-function adapters containing storage typically respond as storage).
8000 to 8FFF	Video
FFFF	Device not attached.

One can only assume that ID ranges not specified are reserved by IBM, but this is not stated.

The ID bytes are accessed in POS registers 100 and 101, with the least significant byte corresponding to register 100. The 82C611/612 provides two read strobes, 100RD and 101RD that are used to gate the ID bytes onto the data bus. The ID may be held in a PROM or other programmable logic device, or be hardwired and implemented with tri-state or open collector drivers. Figure 3.1 shows an example implementation with a 32 × 8 PROM, and Figure 3.2 shows an example implemented with tri-state driver. The PROM solution offers the most flexibility as any ID may be programmed and the "device not ready" ID of 0000H is also easily implemented. The driver solution offers the lowest cost at the expense of limited ID choices.



74S288
32 × 8 PROM

PROM PROGRAMMING

Address	Data	
00H	LO ID BYTE	> THIS ADAPTER
01H	HI ID BYTE	
02H	LO ID BYTE	> OTHER ADAPTERS
.	HI ID BYTE	
.	etc.	
.		
1EH	00H	> "DEVICE NOT READY" ID
1FH	00H	

Figure 3.1

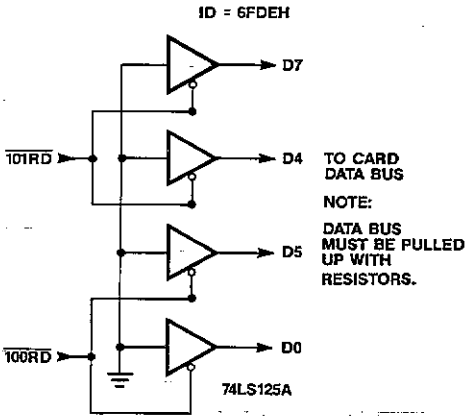


Figure 3.2

3.3 Register 102

Only Bit 0 of register 102 has a defined function in the IBM specification. It is the Card Enable bit. Writing a 0 to this bit disables the card. Conversely, writing a 1 to this bit enables the card. Typically, this is handled by the POS configuration routines. When this bit is 0, none of the "normal mode" signals are generated by the 82C611/612. The state of this bit is available to the adapter logic as the signal CDEN. When CDEN is high, the card is enabled. This bit and CDEN are reset to 0 on a CHRESET.

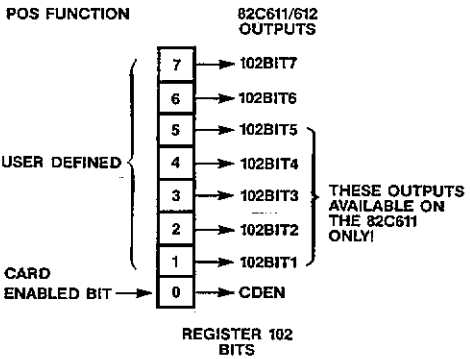


Figure 3.3

The remaining bits of register 102 are user-defined. Bits 6 and 7 are available externally for use by the card designer. They are available on 102BIT6 and 102BIT7. They are both reset to 0 on CHRESET.

The 82C611 also has the remaining bits available from register 102. These are Bits 1-5 and appear on 102BIT1:5. They are all reset to 0 on CHRESET. Note that these bits are not available externally on the 82C612. A block diagram of register 102 is shown in Figure 3.3.

3.4 Register 103

In pin modes 0 and 1, register 103 is implemented internal to the 82C611/612. These two modes are used to support relocation. In pin mode 2, register 103 is implemented external to the 82C611/612 and may be used for any function the designer wishes.

Figure 3.4 shows the function of register 103 in pin modes 0 and 1. For more explanation, see the Pin Modes section of this data sheet.

3.5 Register 104

In pin mode 0, register 104 is implemented internal to the 82C611/612 and is used to support relocation. In pin modes 1 and 2, register 104 is implemented external to the 82C611/612 and may be used for whatever function the designer wishes. Figure 3.4 shows the function of register 104 in pin mode 0. For more explanation, see the Pin Modes section of this data sheet.

3.6 Register 105

Register 105 is always internal to the 82C611/612. Bits 5, 6 and 7 have the same function in both the 82C611 and 82C612, however the remaining bits have different functions depending on which part is being used.

As stated above, the functions of bits 5, 6 and 7 of register 105 are the same in both the 82C611 and 82C612.

Bit 5 is the SYNC READY bit. When high, it tells the 82C611/612 to remove CD CHRDY synchronously with the leading edge of the $\overline{\text{CMD}}$ signal. This causes the system to perform a "synchronous extended" transfer. When low, CD CHRDY will be removed asynchronously.

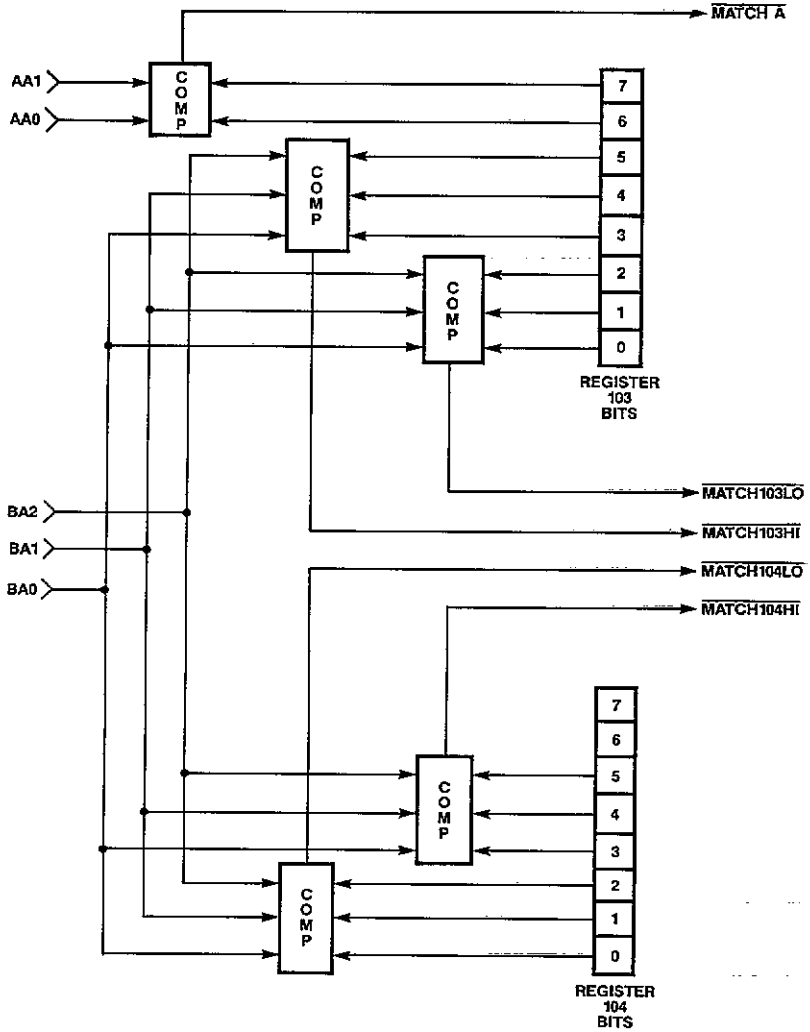
Bit 6 is the $\overline{\text{STAT AVAIL}}$ bit. This read-only bit may be provided by the adapter logic when it signals an error condition. When low, this bit signals the system that the adapter has additional status information available at POS registers 106 and/or 107. Note that this bit and function are only available when the 82C611/612 is operating in pin mode 2. In other modes, this bit always reads 0. For more explanation, see the Pin Modes section of this data sheet.

Bit 7 is the $\overline{\text{CHCK ACTIVE}}$ bit. When low, it indicates that the adapter logic has signaled an error condition via the $\overline{\text{ERROR}}$ input. This bit is set to one upon reset. For more information, see the $\overline{\text{ERROR}}$ pin description. In the 82C612, the remaining bits of register 105 are used for DMA operations. Note that the following descriptions do not apply to the 82C611.

Bits 0 through 3 represent the arbitration level for this adapter. These bits are normally set by the POS system. For a discussion of arbitration, see the DMA Operations section of this data sheet.

Bit 4 is the FAIRNESS bit. When low, this bit enables the fairness algorithm as defined by IBM. This prevents high priority arbiters from excluding lower priority arbiters. For a discussion of fairness mode, see the DMA Operations section of this data sheet.

Since the 82C611 does not support DMA operations, bits 0 through 3 of register 105 have been made available externally for use as the designer wishes. They are available on the 105BIT0:3 pins. To give the designer a maximum amount of flexibility, these pins have been implemented as high current (24mA) open collector drivers. They are suitable for use as LED or relay drivers, or for other applications. If these signals are to be used as normal outputs, they must be pulled up externally. The size of the pull-up resistor



BLOCK DIAGRAM OF REGISTERS 103 and 104 FOR PIN MODE 0. IN PIN MODE 1, REGISTER 104 IS IMPLEMENTED EXTERNALLY, AND ALL BITS BECOME "USER DEFINED".

Figure 3.4

will depend on the desired rise time and current loading on any particular output. Bit 4 of register 105 can be written to and read from, but is not available externally. Block diagrams of the functions of register 105 for the 82C611 and 82C612 are shown in Figures 3.5 and 3.6.

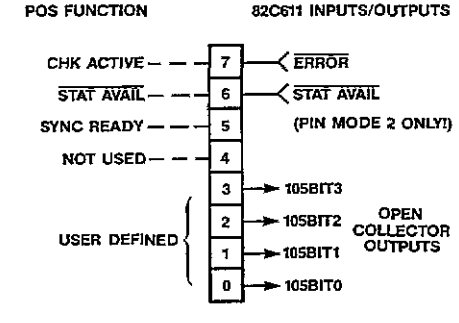


Figure 3.5

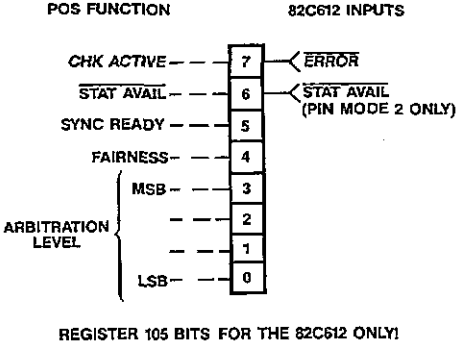


Figure 3.6

3.7 Registers 106 and 107

Registers 106 and 107 are implemented external to 82C611/612. Read and write strobes are available for these registers in pin mode 2. For more explanation, see the Pin Modes section of this data sheet.

4. PIN MODES

This section describes the three pin modes available on the 82C611/612. They are selected by strapping the PINMODE input to Vss for pin mode 0, Vdd for pin mode 1 or CHRESET for pin mode 2.

4.1 Pin Mode 0

This mode provides the most amount of support for POS controlled relocation of the adapter resources. The functions of the pins in Mode 0 are described below:

MFP9:	I	AA1
MFP8:	I	AA0
MFP7:	O	MATCH A
MFP6:	I	BA2
MFP5:	I	BA1
MFP4:	I	BA0
MFP3:	O	MATCH 103HI
MFP2:	O	MATCH 103LO
MFP1:	O	MATCH 104HI
MFP0:	O	MATCH 104LO

Two address fields (AA1:0 and BA2:0) are provided to input external address bits. The AA bits are continually compared with POS register 103 bits 7 and 6. The result of the compare is output on the MATCH A pin, with a low signifying a match. Similarly, the BA bits are continuosly compared to four different register fields: Bits 5:3 and bits 2:0 of both POS registers 103 and 104. The results of the comparisons are output as follows: A match between BA2:0 and POS register 103 bits 5:3 is signified by a low on MATCH 103HI. A match between BA2:0 and POS register 103 bits 2:0 is signified by a low on MATCH 103LO. A match between BA2:0 and POS register 104 bits 5:3 is signified by a low on MATCH 104HI. A match between BA2:0 and POS register 104 bits 2:0 is signified by a low on MATCH 104LO.

The address inputs may be tied to any address lines depending on the size of the block being decoded. For example, if a 1 megabyte memory block was desired to be relocated at any of the first four 1 megabyte boundaries, one would tie A20 and A21 to AA1:0. By writing the proper bit pattern to POS register 103 in bits 6 and 7, the block could be relocated to one of four possible 1 megabyte boundaries (in the first four megabytes). The BA lines could be used on the same board to specify relocation addresses for I/O ports. This would allow four different blocks of I/O ports to be relocated to any of eight possible address locations in the range reflected in the choice of address bits for BA2:0. Of course, additional logic would be required externally to further qualify and decode these addresses.

Note that if these Match outputs are intended to remain stable throughout the cycle, they, or the address lines that generate them, must be latched externally. The AA and BA lines are not latched internally.

4.2 Pin Mode 1

This pin mode is very similar to pin mode 0, except that only register 103 is used to support relocation internally. This means that only two blocks are decoded from the BA lines. The AA lines work as in pin mode 0. Instead of using register 104 internally, the active low read and write strobes are brought out as 104RD and 104WR. The designer may then implement register 104 external to the 82C611/612. The functions of the pins in pin mode 1 are described below:

MFP9:	I	AA1
MFP8:	I	AA0
MFP7:	O	$\overline{\text{MATCH A}}$
MFP6:	I	BA2
MFP5:	I	BA1
MFP4:	I	BA0
MFP3:	O	$\overline{\text{MATCH 103HI}}$
MFP2:	O	$\overline{\text{MATCH 103LO}}$
MFP1:	O	$\overline{\text{104RD}}$
MFP0:	O	$\overline{\text{104WR}}$

4.3 Pin Mode 2

In this mode, no relocation support is provided internally. Instead, active low read and write strobes for POS registers 103, 104, 106 and 107 are brought out so that the designer may implement these registers external to the 82C611/612.

MFP9:	I	$\overline{\text{STAT AVAIL}}$
MFP8:	O	+$\overline{\text{BADL}}$
MFP7:	O	$\overline{\text{107RD}}$
MFP6:	O	$\overline{\text{107WR}}$
MFP5:	O	$\overline{\text{106RD}}$
MFP4:	O	$\overline{\text{106WR}}$
MFP3:	O	$\overline{\text{103RD}}$
MFP2:	O	$\overline{\text{103WR}}$
MFP1:	O	$\overline{\text{104RD}}$
MFP0:	O	$\overline{\text{104WR}}$

The $\overline{\text{STAT AVAIL}}$ input may be provided by the card adapter logic when it signals an error condition. When the system reads this bit as a logic 0 (in POS register 105 bit 6) it indicates that the card will have additional status information available in POS registers 106 and 107. Note that this mode of operation is only available when the 82C611/612 is operating in pin mode 2. Otherwise this bit will always be read as a 0.

The +$\overline{\text{BADL}}$ is a buffered and inverted version of the $\overline{\text{ADL}}$ pin on the Micro Channel bus.

5. DMA OPERATIONS

The 82C612 has complete support for DMA transfers on the Micro Channel. It handles DMA arbitration, single cycle and burst modes, and supports the fairness algorithm as defined by IBM. Note that the 82C612 is not intended for a "Bus Master" application. It is intended for a DMA slave application—the difference primarily is that the DMA controller on the system board still provides address, status and command signals to the bus.

5.1 DMA Arbitration

A DMA slave requests the use of the Micro Channel by activating the PREEMPT line. The Central Arbitration Control Point (CACP) then raises the ARB/GNT line signifying the start of an arbitration interval. During this time, the DMA slave drives its arbitration level onto the 4 ARB pins. There are 16 possible levels, with 0000 having the highest priority.

If any other device also requested the bus, it or they also assert their priority level on the ARB pins. Each competing device compares the levels it is driving on the pins with the levels already on the pins. If the device's priority level is higher than what is on the bus, that device is declared the winner. If the device sees a higher priority level on a the bus than it is trying to assert, then it is declared a loser. The result is that the highest priority level will remain on the bus.

At the end of the arbitration cycle (signified by the CACP dropping the ARB/GNT line) each device that participated in the arbitration will know if it won or lost the bus. If the device won, it raises the PREEMPT line.

5.2 Single Cycle and Burst Mode Transfers

If this was a single-cycle transfer, the device completes a transfer and the CACP will raise ARB/GNT again. If this was a burst transfer, the device would have asserted the BURST line along with PREEMPT. If it won the bus, it would continue to assert BURST until it was done transferring. It signifies the end of transfer by raising the BURST line.

During burst transfers, other devices may request the use of the bus by asserting PREEMPT. The device that currently owns the bus must release it within 7.5 microseconds by raising the BURST line. The device relinquishing the bus is allowed to compete for it again. If it still has the highest priority, it will win the bus back, only having been off the bus during the arbitration interval.

5.3 Fairness

One can see that a high priority device could lock out all other devices if it wished. Therefore, IBM has specified a "fairness" mode. If a device is "fair" it would not compete for the bus again until all requesters who were also competing for the bus have gotten a chance to run their cycles. If everyone is being fair then all devices that were competing will get the bus in order of their priority.

5.5 DMA Cycle Termination

The Micro Channel has a bus line named TC for Terminal Count. A low pulse on this pin signifies that the number of transfers programmed into the DMA controller has been reached. A DMA slave can use this signal to terminate the transfer and/or cause an interrupt to the CPU. If this was a burst transfer, the DMA slave must raise BURST in response to a TC. This is known as "DMA Controller Terminated". A DMA slave can also raise BURST on its own. This is known as "DMA Slave Terminated".

5.6 Priority Levels

With four lines, there should be 16 available priority levels. In fact, there are 18 levels, 15 of which can be used by adapter cards. The priority levels are shown below:

Priority Level	Used For
-2	Memory Refresh
-1	Error Recovery
0	DMA Port 0*
1	DMA Port 1
2	DMA Port 2
3	DMA Port 3
4	DMA Port 4*
5	DMA Port 5
6	DMA Port 6
7	DMA Port 7

8	SPARE
9	SPARE
A	SPARE
B	SPARE
C	SPARE
D	SPARE
E	SPARE
F	System Processor

* DMA ports 0 and 4 may be reassigned to respond to any priority level. For example, DMA port 0 could be reassigned to respond to level B, and a Bus Master could then be assigned to level 0.

Level -2 is reserved is reserved for memory refresh operations. Level -1 is used by the system processor when it absolutely needs to take control of the bus, such as during error recovery operations. These two "super-levels" have the highest priority. In fact, their levels never appear on the ARB pins. Thus, these two levels are guaranteed to win over anything on the bus.

The system processor normally has a priority level of F, or the lowest. Therefore, this level may not be used by a DMA slave.

So, out of 18 levels, only 15 are actually available to DMA slave cards.

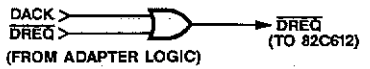
5.7 DMA Adapter Logic Signals

All of this can sound pretty complicated, but don't worry. The 82C612 takes care of most of this for you. Now that you have an idea how DMA transfers occur, here is how the 82C612 handles them:

The 82C612 has four signals that interface to the adapter logic. They are $\overline{\text{DREQ}}$, DACK, BURST MODE and SUSPEND. The designer familiar with the XT/AT buses and/or the 8237 will recoginize $\overline{\text{DREQ}}$ and DACK. They work in essentially the same manner.

To initiate a transfer, the adapter logic drives $\overline{\text{DREQ}}$ low. The 82C612 then handles all of the DMA arbitration functions on the bus.

Once the adapter has won the arbitration, the 82C612 will respond with DACK going high.



CIRCUIT TO GATE $\overline{\text{DREQ}}$ FOR SINGLE-CYCLE DMA

Figure 5.1

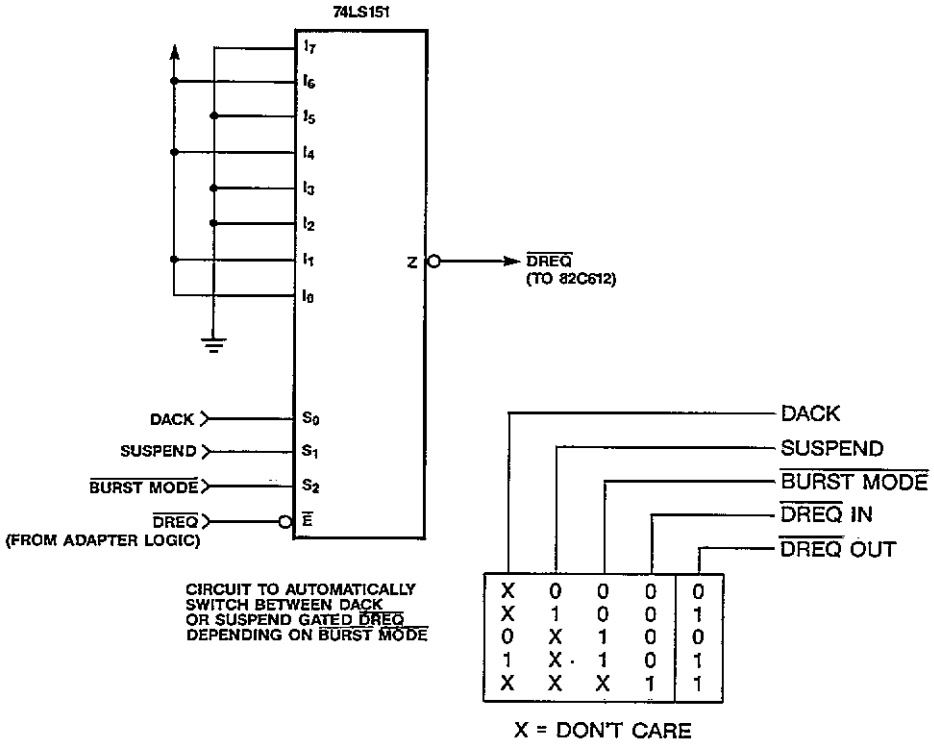
For single cycle transfers, the adapter logic should raise $\overline{\text{DREQ}}$ as soon as DACK goes high. This can be accomplished with a simple OR gate as shown in Figure 5.1. For burst mode transfers, the adapter logic should first drive BURST MODE and then $\overline{\text{DREQ}}$ low. BURST MODE will be latched internally by the leading edge of $\overline{\text{DREQ}}$. It must precede $\overline{\text{DREQ}}$ by 15 nanoseconds. Transfers will start when DACK goes high. The logic should continue to assert $\overline{\text{DREQ}}$ until one of the following events ocurr:

1. The adapter decides to terminate the cycle itself (DMA Slave terminated), in which case it would raise the $\overline{\text{DREQ}}$ line.
2. A $\overline{\text{TC}}$ pulse occurs signifying the end of the transfer (DMA Controller terminated). The adapter logic should raise the $\overline{\text{DREQ}}$ line.
3. The SUSPEND signal goes high, signifying that another device has requested the bus. Since the device does not have to relinquish the bus for 7.5 microseconds, the adapter logic can decide to do something intelligent in response to SUSPEND. It can decide to complete many more transfers and then relinquish the bus (as long as it does not violate the 7.5 microsecond limit), or it can give up the bus immediately. In the latter case, the adapter logic may simply gate $\overline{\text{DREQ}}$ with SUSPEND as shown in Figure 5.2.

CIRCUIT TO GATE $\overline{\text{DREQ}}$ FOR BURST MODE DMA

Figure 5.2

The following circuit may be used to handle DREQ for both single cycle and burst transfer modes. Its mode changes based on the state of BURST MODE. It assumes that the adapter logic will hold BURST MODE low until the entire transfer is complete.



Truth Table

Figure 5.3

82C611, 82C612 Absolute Maximum Ratings

Parameter	Symbol	Min.	Max.	Units
Supply Voltage	V_{DD}	V_{SS}-0.5	6.0	V
Input Voltage	V_I	V_{SS}-0.5	V_{DD}+0.5	V
Output Voltage	V_O	V_{SS}-0.5	V_{DD}+0.5	V
Operating Temperature	T_{OP}	-25	85	°C
Storage Temperature	T_{STG}	-40	125	°C

Note: Permanent device damage may occur if Absolute Maximum Ratings are exceeded. Functional operation should be restricted to the conditions described under Operating Conditions.

82C611, 82C612 Operating Conditions

Parameter	Symbol	Min.	Max.	Units
Supply Voltage	V_{DD}	4.75	5.25	V
Ambient Temperature	T_A	0	70	°C

82C611, 82C612 DC Characteristics

Parameter	Symbol	Min.	Max.	Units
Input Low Voltage	V_{IL}		0.8	V
Input High Voltage	V_{IH}	2.0		V
Output Low Voltage I_{OL1} = 3.2mA I_{OL2} = 8mA I_{OL3} = 24mA } see note 1	V_{OL}		0.5	V
Output High Voltage I_{OH} = 0.4mA	V_{OH}	4.2		V
Input Leakage Current*	I_{IL}	-100	100	μA
Power Supply Current	I_{CC}		100	mA
Output High Impedance Leakage $0.45 < V_{PIN} < V_{DD}$	I_{OZ}	-100	+100	μA

Note 1: All outputs are I_{OL1} (3.2mA) except the following

I_{OL2} (8mA) Outputs	I_{OL3} (24mA) Outputs	
$\overline{\text{CD SFDBK}}$	ARB3	POS105B1
CD DS16	ARB2	POS105B0
CD CHRDY	ARB1	
	$\overline{\text{ARB0}}$	
	$\overline{\text{PREEMPT}}$	
	$\overline{\text{BURST}}$	
	$\overline{\text{CHCK}}$	
	POS105B3	
	POS105B2	

82C611, 82C612 AC Characteristics

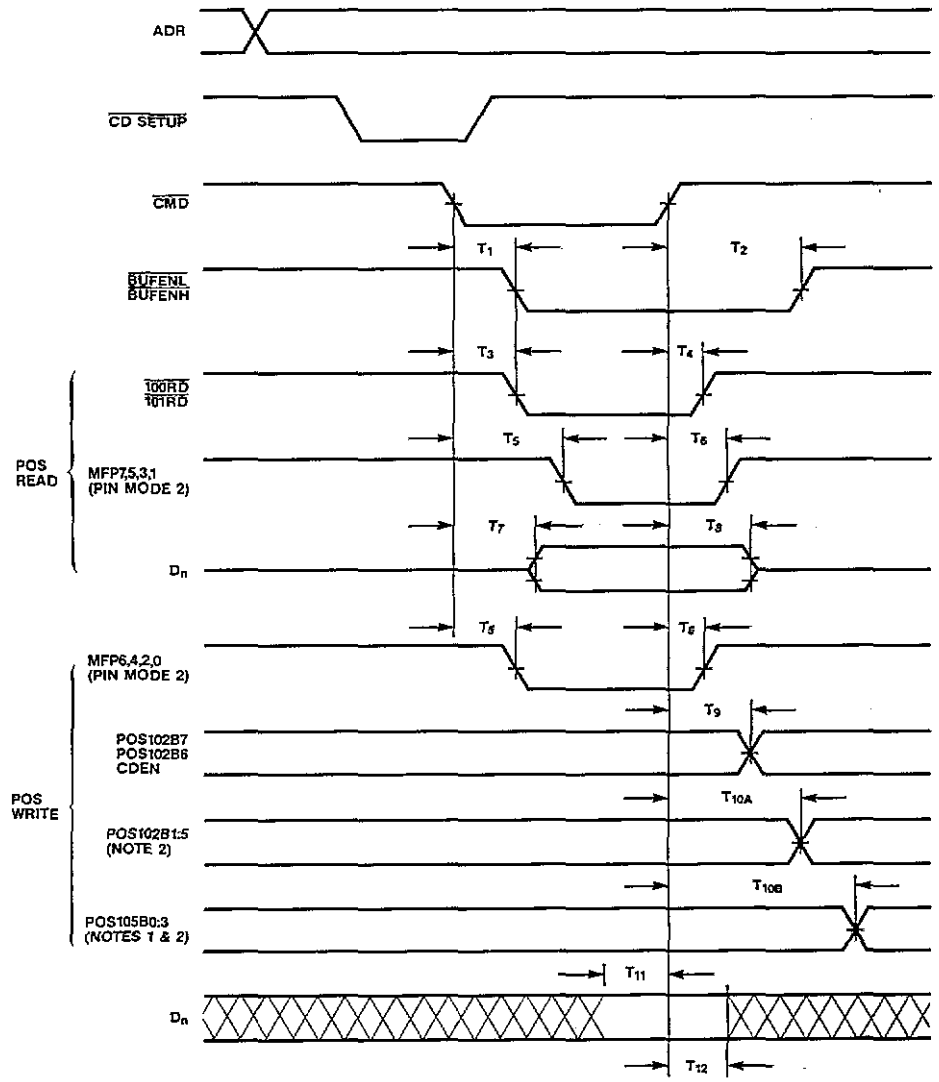
Sym	Parameter	Min	Max	Units
POS Read/Write				
t1	$\overline{CMD}$ Active → BUFENL, H Active		15	ns
t2	$\overline{CMD}$ Active → BUFENL, H Inactive	15	35	ns
t3	$\overline{CMD}$ Active → $\overline{100RD}$, $\overline{101RD}$ Active		18	ns
t4	$\overline{CMD}$ Inactive → $\overline{100RD}$, $\overline{101RD}$ Inactive		18	ns
t5	$\overline{CMD}$ Active → Read/Write Strobes Active		20	ns
t6	$\overline{CMD}$ Inactive → Read/Write Strobes Inactive		20	ns
t7	$\overline{CMD}$ Active → Read Data Valid		22	ns
t8	$\overline{CMD}$ Active → D_n Hi-Z		30	ns
t9	$\overline{CMD}$ Inactive → POS Outputs Valid		20	ns
t10A	$\overline{CMD}$ Inactive → POS Outputs Valid		30	ns
t10B	$\overline{CMD}$ Intactive → POS Outputs Valid		50	ns
t11	Write Data Setup → $\overline{CMD}$ Inactive		20	ns
t12	$\overline{CMD}$ Inactive → Write Data Invalid		10	ns
Channel Ready				
t13	$\overline{ADPRDY}$ Active → CD CHRDY Inactive		15	ns
t14	$\overline{S0}$ ($\overline{S1}$) Active → CD CHRDY Inactive		20	ns
t15	$\overline{CMD}$ Active → CD CHRDY Active		20	ns
t16	+RDYSTB Active → CD CHRDY Active		20	ns
Address Match				
t17	AA_n → $\overline{MATCH\ A}$ Valid		15	ns
t18	BA_n → $\overline{MATCH\ B}$ Valid		18	ns
Command Signals				
t19	$\overline{CMD}$ Active → IO/MEM CMD Active		18	ns
t20	$\overline{CMD}$ Inactive → IO/MEM CMD Inactive		18	ns
Response Signals				
t21	$\overline{CD\ SEL}$ Active → $\overline{CD\ SFDBK}$ Active		12	ns
t22	$\overline{DS16}$ Active → $\overline{CD\ DS16}$ Active		12	ns

82C611, 82C612 AC Characteristics (Continued)

Sym	Parameter	Min	Max	Units
Miscellaneous				
t23	$\overline{ADL}$ Active → +BADL Active		15	ns
t24	$\overline{ADL}$ Inactive → +BADL Inactive		15	ns
t25	$\overline{ERROR}$ Active → $\overline{CHCK}$ Active		25	ns
t26	$\overline{ADL}$ Active → BUFDIR Valid		20	ns
Arbitration Cycle				
t27	$\overline{DREQ}$ Active → $\overline{PREEMPT}$ Active		30	ns
t28	ARB/$\overline{GNT}$ High → ARB_n Low		50	ns
t29	ARB_n Drive from High Order Match		50	ns
t30	ARB_n Off from High Order Mismatch		50	ns
t31	ARB/$\overline{GNT}$ Low → $\overline{PREEMPT}$ Inactive		50	ns
t32	ARB/$\overline{GNT}$ Low → DACK Active		22	ns
Burst Mode				
t33	$\overline{BURSTMODE}$ Setup Time	15		ns
t34	$\overline{BURSTMODE}$ Hold Time	15		ns
t35	ARB/$\overline{GNT}$ Low → $\overline{BURST}$ Active		40	ns
t36	$\overline{TC}$ Active → $\overline{BURST}$ Inactive		25	ns
t37	$\overline{CMD}$ Inactive → DACK Inactive		25	ns
t38	$\overline{DREQ}$ Release Setup Time	15		ns
t39	$\overline{CMD}$ Active → $\overline{BURST}$ Inactive		35	ns
t40	$\overline{PREEMPT}$ Recognition Setup Time	15		ns
t41	$\overline{CMD}$ Inactive → SUSPEND Active		20	ns
t42	IDLE STATUS → SUSPEND Inactive		25	ns
t43	$\overline{CMD}$ Inactive → SUSPEND Inactive		25	ns

82C611/12 Timing Diagrams

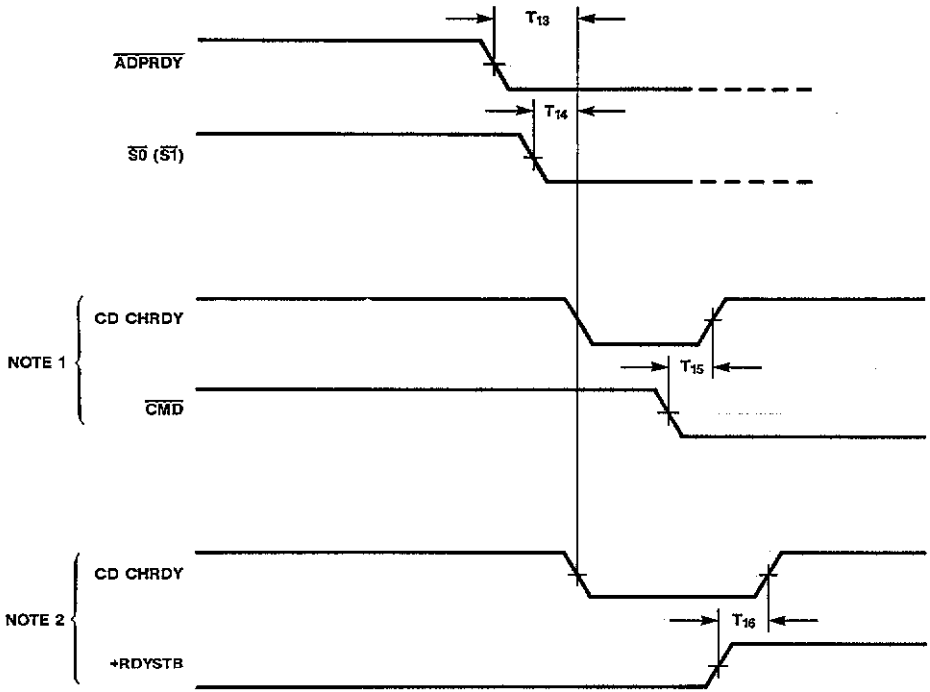
POS Read/Write



NOTE 1: MEASURED WITH 4.7K PULL-UP RESISTORS TO VCC ON OUTPUTS POS105B0:3
NOTE 2: SIGNALS AVAILABLE ON 82C611 ONLY.

82C611/12 Timing Diagrams (Continued)

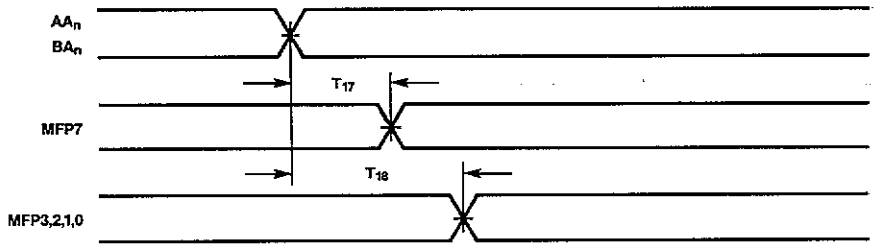
Channel Ready



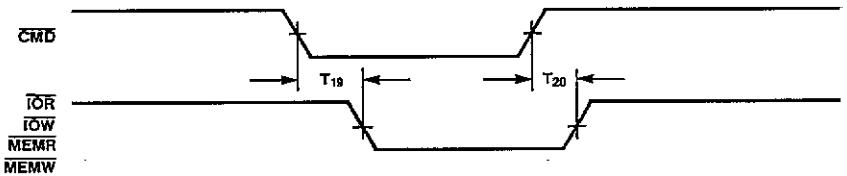
NOTE 1: POS REGISTER 105 BIT 5 = 1 (SYNCHRONOUS EXTENDED CYCLE)
NOTE 2: POS REGISTER 105 BIT 5 = 0 (ASYNCHRONOUS EXTENDED CYCLE)

82C611/12 Timing Diagrams (Continued)

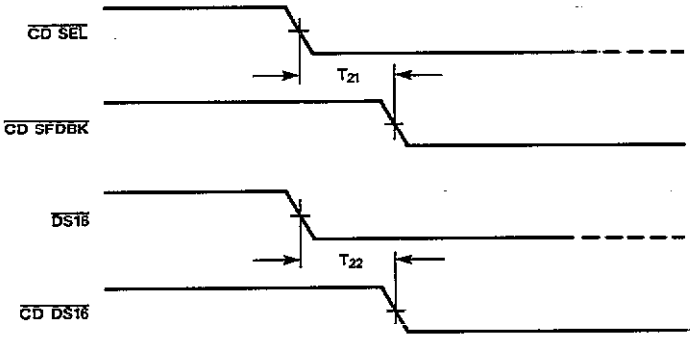
Address Match



Command Signals

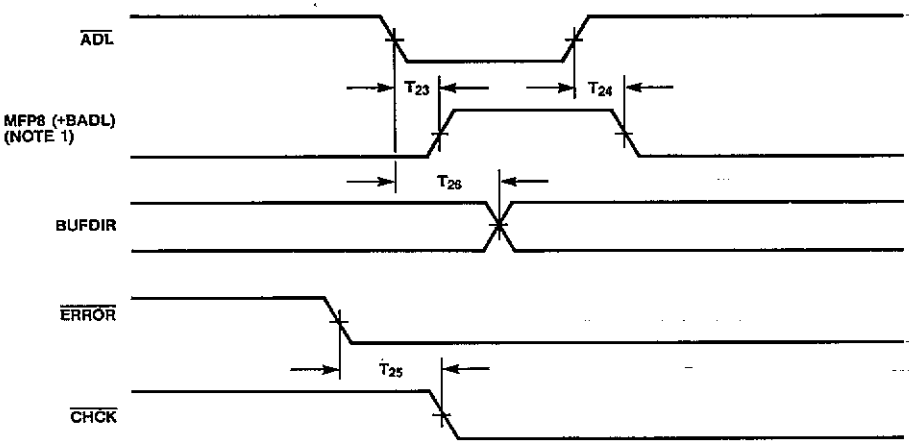


Response Signals



82C611/12 Timing Diagrams (Continued)

Miscellaneous

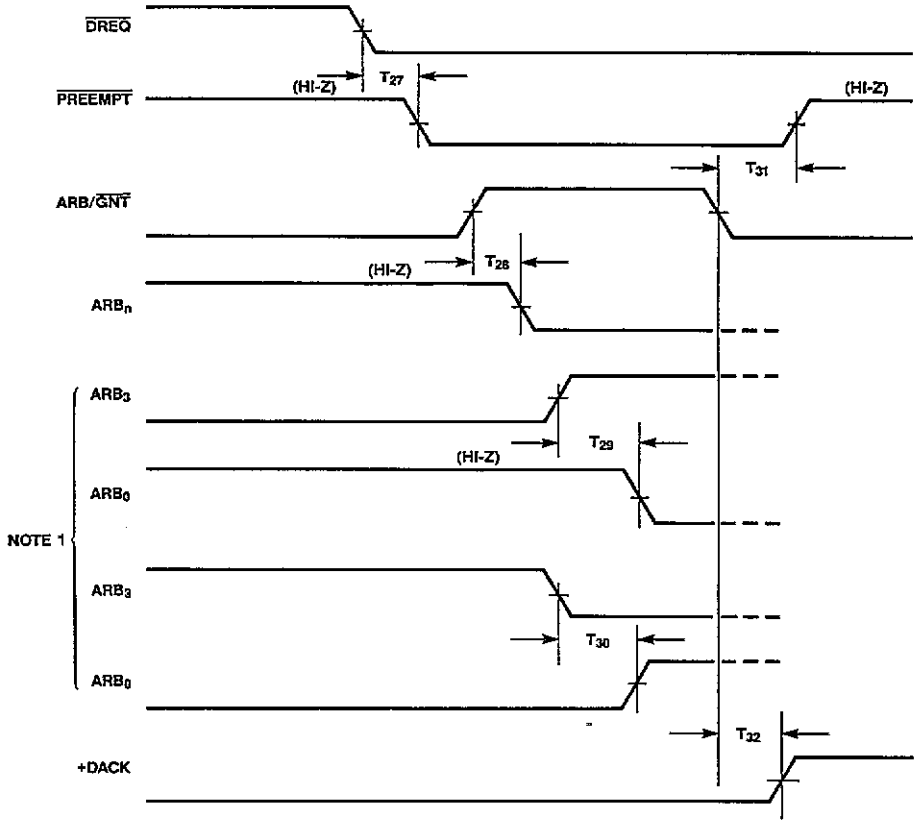


NOTE 1: PIN MODE 2 ONLY.

82C611/12 Timing Diagrams (Continued)

Note: The signals in the following diagrams are applicable to the 82C612 only.

Arbitration Cycle

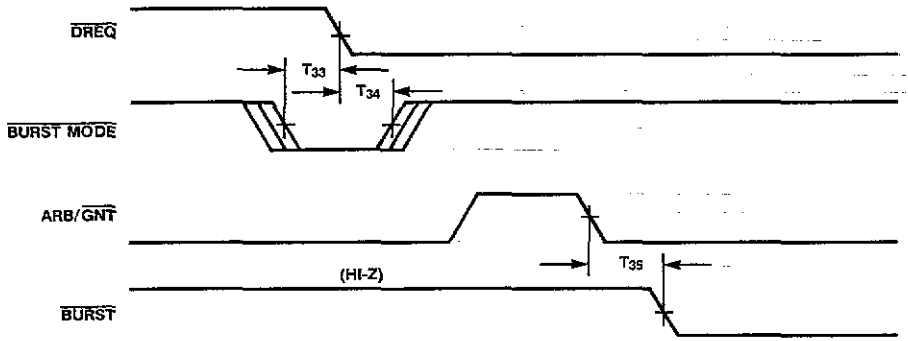


NOTE:

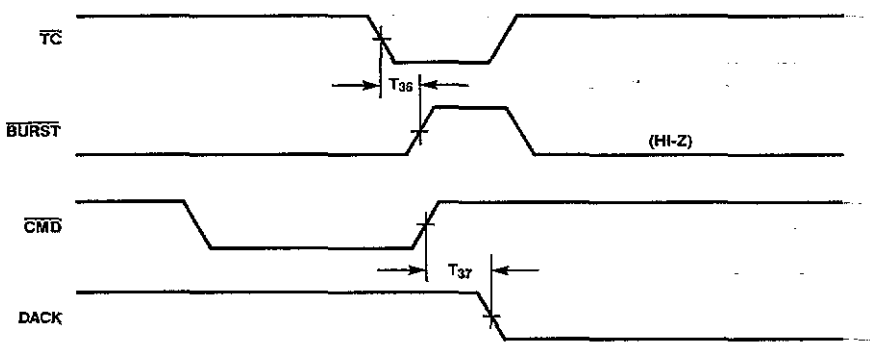
1. ARB3 driven by, or released by another competing device. These waveforms show ripple-through delay of arbitration logic to enable and disable low-order ARB bus line.

82C611/12 Timing Diagrams (Continued)

Burst Mode

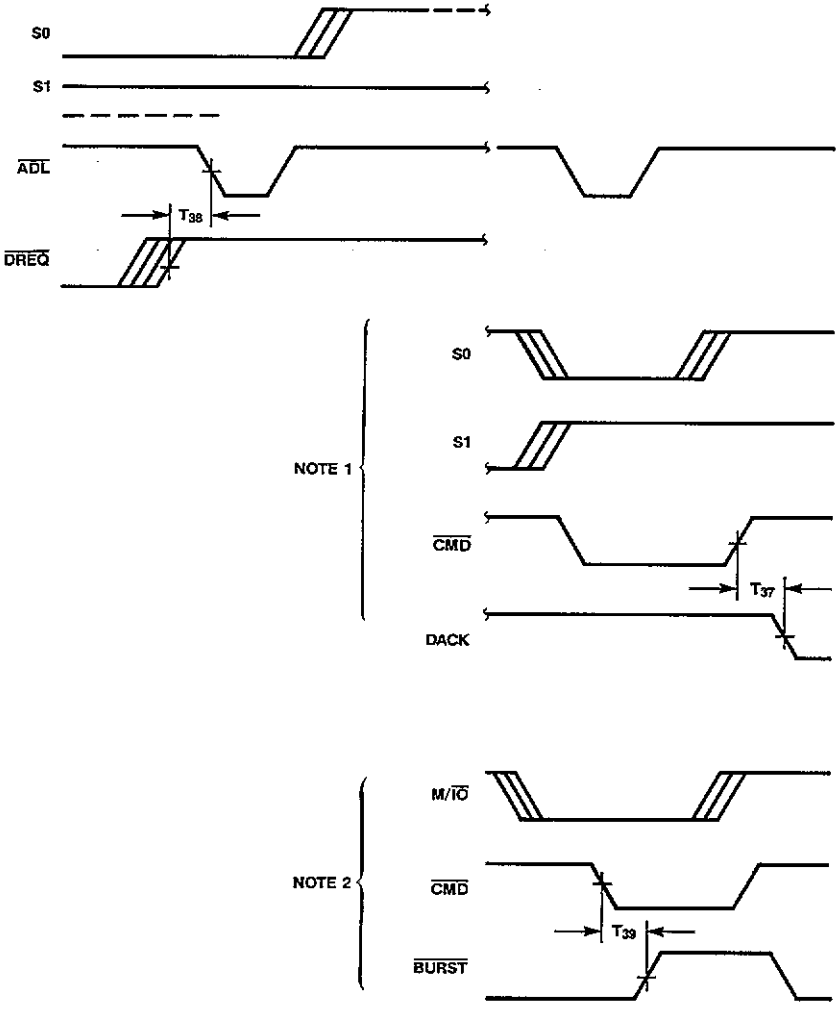


Burst Cycle Termination (DMAC Controlled)



82C611/12 Timing Diagrams (Continued)

Burst Cycle Termination (Slave Controlled)

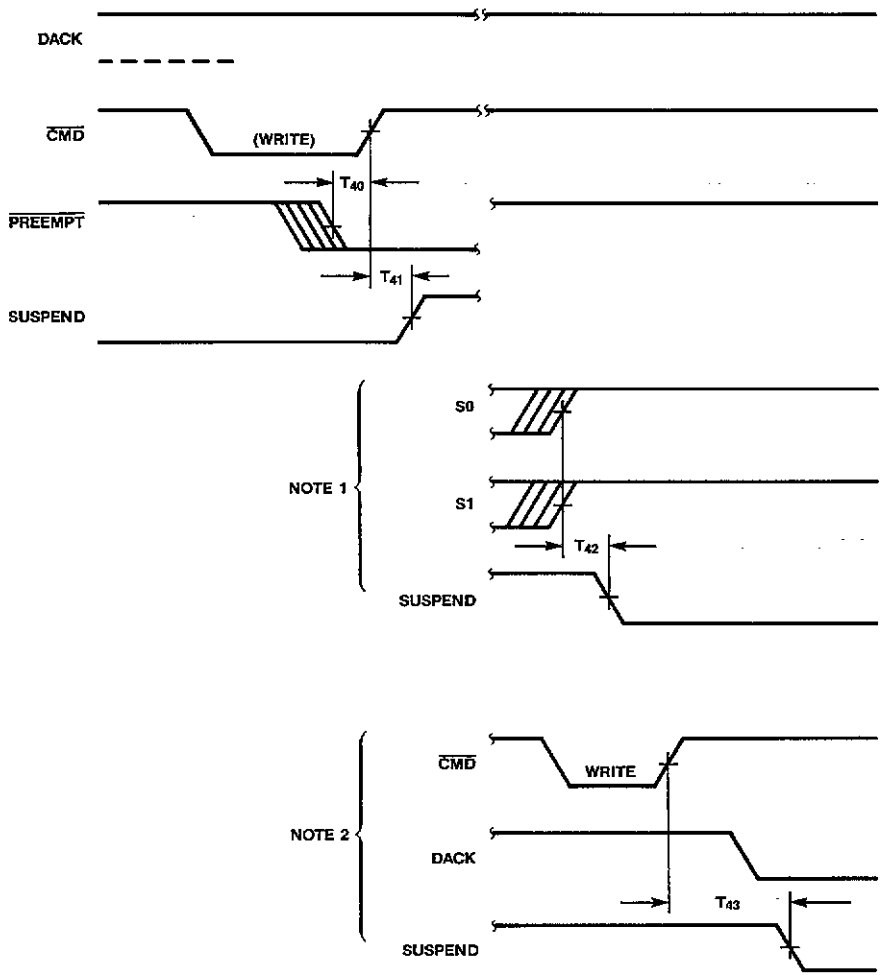


NOTES:

1. DACK is negated following the trailing edge of the first WRITE CMD pulse after DREQ is removed meeting the setup conditions shown.
2. BURST is removed following the leading edge of the first IO CMD pulse after DREQ is removed meeting the setup conditions shown.

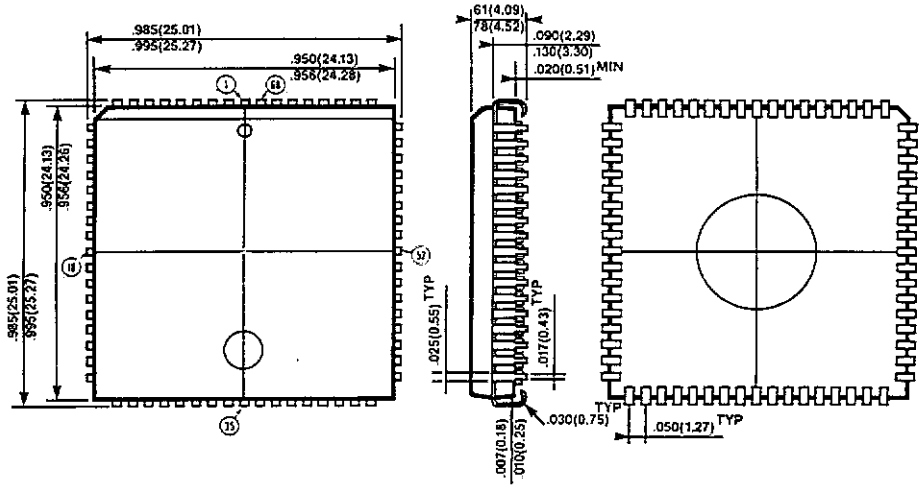
82C611/12 Timing Diagrams (Continued)

Suspend Timing



NOTES:
1. Bit 4 of POS Register I05 set to 0 ("FAIRNESS" enabled).
2. Bit 4 of POS Register I05 set to 1 ("FAIRNESS" disabled).

68-PIN PLASTIC LEADED CHIP CARRIER



Ordering Information

Order Number	Package Type
P82C611	PLCC-68
P82C612	PLCC-68

Note:
1. PLCC = Plastic Leaded Chip Carrier

NOTES

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