Data Sheet
November 1991

AT&T Microelectronics

T7213 Dual Interface Station Chip

Features

- Compatible with IEEE 802.3 standards for Attachment Unit Interface (AUI)
- Compatible with IEEE 802.3 10BASE-T draft standards for Twisted-Pair (TP) Interface
- Software selectable media interface between AUI and TP
- On-chip clock oscillator
- Digital phase-locked loop (DPLL) timing recovery and data decoding
- Encodes NRZ data to Manchester data and supplies the associated predistortion signals needed for TP transmission
- Generates IDL pulse at end of transmit packet
- Detects Manchester code violations and collisions
- Selectable link-integrity test and status indicator for TP Interface
- Interfaces with industry-standard LAN controllers
- Long line length capability for twisted-pair interface

Description

The T7213 Dual Interface Station Chip is a CMOS device which supports both 802.3 AUI and 10BASE-T TP Interface media connections through external isolation transformers. The T7213 includes timing recovery, data encoding/decoding for data conversion, and a local loopback (LLB). It interfaces easily to most popular Carrier Sense Multiple Access with Collision-Detect Local Area Network (CSMA/CD LAN) controllers: AT&T, Intel, AMD, and National Semiconductor. The T7213 not only provides the AUI transceiver paths, but also the predistortion, link integrity, LLB, jabber, and signal quality error (SQE) functions for TP Interface transmission and reception. The device is available in a 28-pin, plastic DIP or SOJ package for surface mounting.

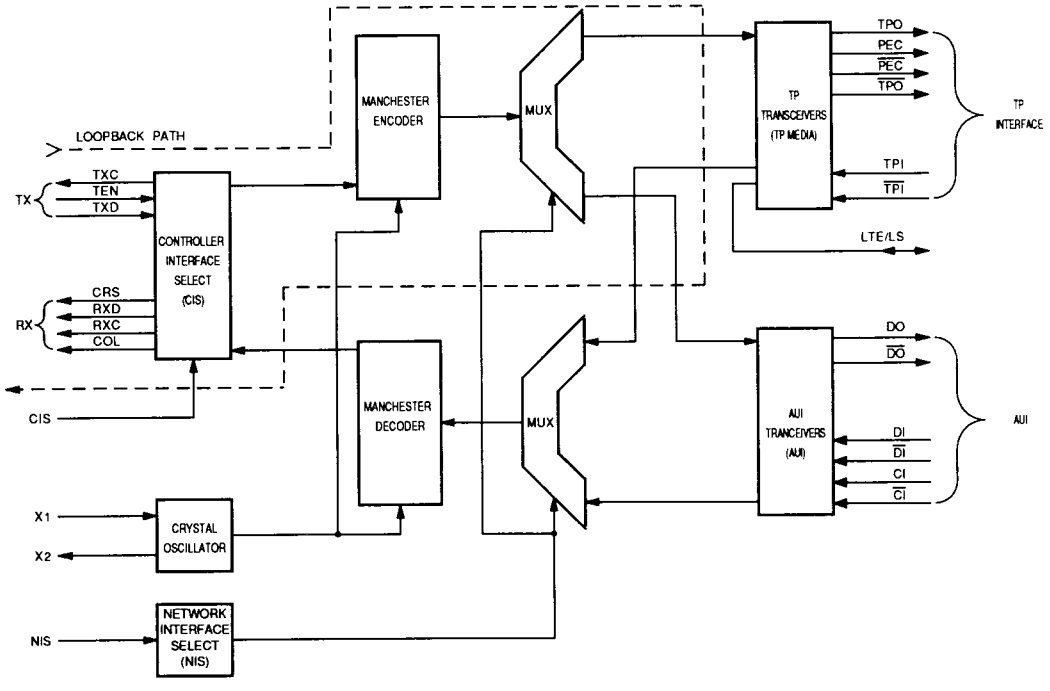


Figure 1. Block Diagram

Pin Information

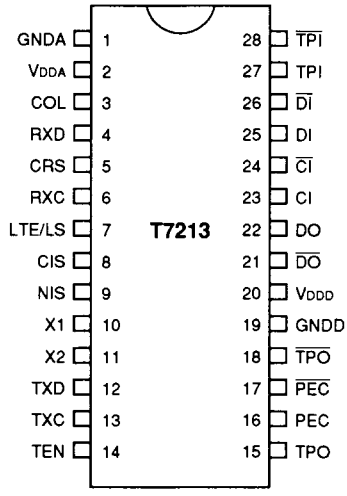


Figure 2. Pin Diagram

Table 1. Pin Descriptions

Pin	Symbol	Type	Name/Function
1	GNDA	—	**Analog Ground.** Ground.
2	V_{DDA}	—	**Analog Power.** +5 V (±10%) supply.
3	COL	O	**Collision Detect.** Connected directly to the CSMA/CD controller, this pin signifies a collision has occurred on the network, a heartbeat signal was received, the watchdog timer has expired, or a Manchester code violation was detected.
4	RXD	O	**Receive Data.** Connected directly to the CSMA/CD controller, this pin is the NRZ data which represents the decoded Manchester data from the TP media or AUI DI circuit.
5	CRS	O	**Carrier Sense.** Connected directly to the CSMA/CD controller, this pin signifies there is activity on the TP media or AUI DI circuit. If an AT&T or Intel controller is selected (CIS is high), CRS is asserted with CI activity. When coupled with RXC, it signals the beginning and end of the received data packet.
6	RXC	O	**Receive Clock.** Connected directly to the CSMA/CD controller, this recovered clock is derived from the received Manchester data and has a nominal period of 100 ns.
7	LTE/LS	I/O	**Link Test Enable/Link Status.** To enable link test for TP media, force this pin high through a 1 kΩ resistor. To show link status, put an LED in series with this resistor. The LED is lit when the link is up. To disable the link test function, force this pin below V_{DDD} – 1.7 V. (See Figure 13.)
8	CIS	I	**Controller Interface Select.** When high, the T7213 interfaces with AT&T and Intel controllers; when left floating, AMD and National controllers. Low is reserved for future use.
9	NIS	I	**Network Interface Select.** When high, the T7213 configures for TP mode; when floating, LLB mode; when low, AUI mode. In LLB mode, the T7213 behaves as if TP mode is selected, except no signal is placed on the TP media, and any received signal from the TP media (including link integrity) is ignored. At least 20 ms must elapse after an NIS change for the T7213 to function correctly. Any data sent to or from the T7213 before this time expires may be lost or garbled.

Pin Information (continued)

Table 1. Pin Descriptions (continued)

Pin	Symbol	Type	Name/Function
10	X1	I	**Crystal 1.** A MTRON #465-160 crystal or equivalent must be mounted closely to this pin to achieve the required 20 MHz ± 100 ppm clock which drives the T7213. An 82 pF ± 5% capacitor to ground must also be connected. (See Table 2.)
11	X2	I	**Crystal 2.** See X1. An 82 pF ± 5% capacitor to ground must be connected to this pin along with the other leg of the 20 MHz crystal.
12	TXD	I	**Transmit Data.** Connected directly to the CSMA/CD controller, this pin provides the serial output data to be put on the TP media or AUI DO circuit.
13	TXC	O	**Transmit Clock.** This signal is a 10 MHz clock connected directly to the CSMA/CD controller. TXD and TEN are clocked out of the CSMA/CD controller synchronously to this signal.
14	TEN	I	**Transmit Enable.** This signal indicates that the data on TXD from the CSMA/CD controller is valid and begins the transmission on the TP media or AUI DO circuit. This signal also starts the watchdog timer. Deassert after the last bit to be transmitted has been clocked out of the CSMA/CD controller. The T7213 will then append an IDL to the output data.
15	TPO	O	**Twisted-Pair Transmit Data.** This differential signal must be transformer coupled to the TP media. The signal is the Manchester-encoded data derived from the NRZ data presented to the TXD input, including IDL at the end of the transmitted packet.
16	PEC	O	**Pre-Equalization Control.** This differential signal mirrors the TPO output except during the second half of a wide pulse; in which case, the output is $\overline{\text{TPO}}$, reducing the amount of receive jitter by preventing overcharge of the TP media.
17	$\overline{\text{PEC}}$	O	**Pre-Equalization Control.** The inverse of PEC.
18	$\overline{\text{TPO}}$	O	**Twisted-Pair Transmit Data.** The inverse of TPO.
19	GNDD	—	**Digital Ground.** Ground.
20	V_{DDD}	—	**Digital Power.** +5 V ± 10% supply.
21	$\overline{\text{DO}}$	O	**AUI Transmit Data.** The inverse of DO.
22	DO	O	**AUI Transmit Data.** This differential signal must be transformer coupled to the AUI DO circuitry. This signal is the Manchester-encoded data derived from the NRZ data presented to the TXD input, including IDL at the end of the transmitted packet.
23	CI	I	**AUI Collision.** This differential input, connected to the AUI collision presence pair of the AUI cable through an isolation transformer, should be a 10 MHz ± 15% square wave.
24	$\overline{\text{CI}}$	I	**AUI Collision.** The inverse of CI.
25	DI	I	**AUI Receive Data.** This differential input, connected to the receive pair of the AUI wire through an isolation transformer, can have up to ±18 ns of timing jitter.
26	$\overline{\text{DI}}$	I	**AUI Receive Data.** The inverse of DI.
27	TPI	I	**TP Receive Data.** This differential input, connected to the receive pair of the TP wire through an isolation transformer, can have up to ±18 ns of timing jitter.
28	$\overline{\text{TPI}}$	I	**TP Receive Data.** The inverse of TPI.

Functional Description

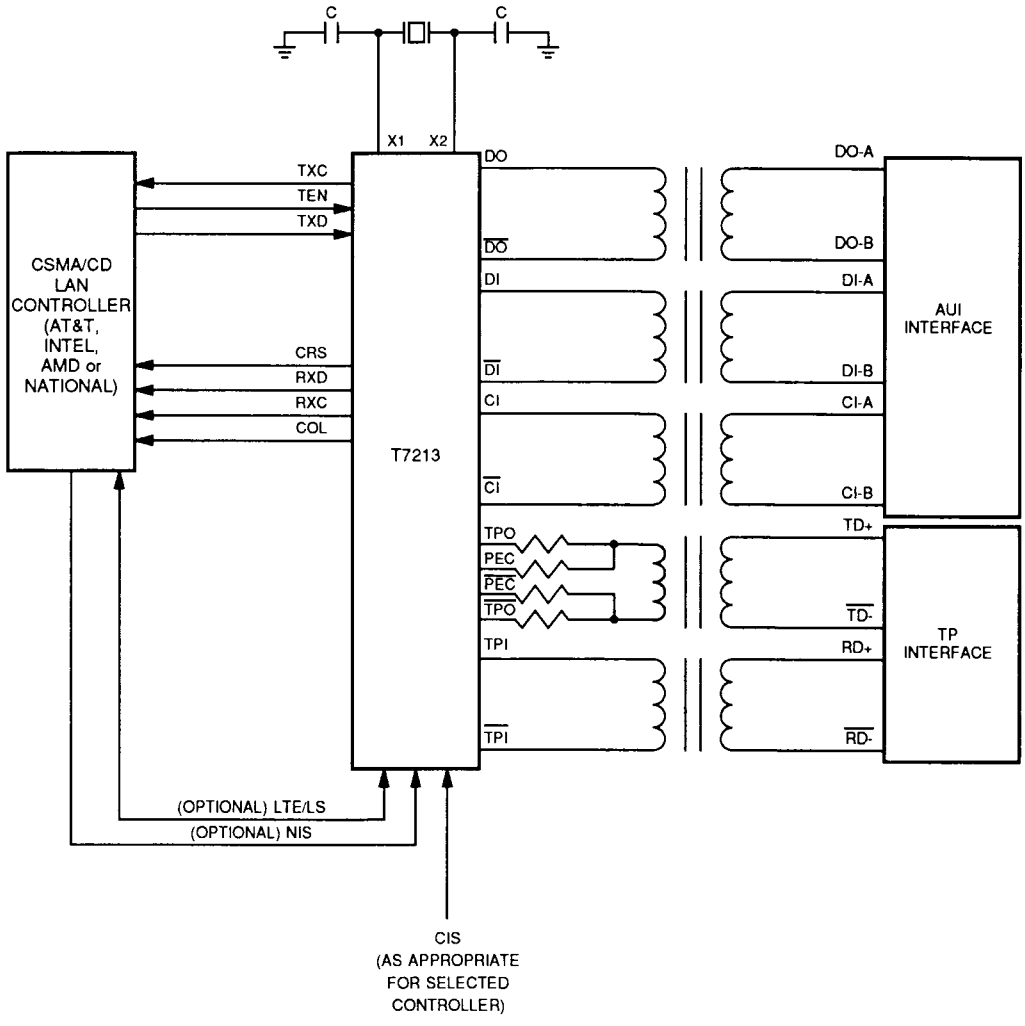


Figure 3. Typical Interface Application Diagram

Manchester Encoder

The Manchester Encoder provides the appropriate data, IDL pulse, and idle level to the selected network drivers (TP or AUI).

First, on the appropriate edge of TXC, the T7213 latches in the CSMA/CD controller's TEN and TXD outputs. If CIS is high (AT&T/Intel interface is selected), the T7213 disregards the first two NRZ bits transmitted in order to accommodate start-of-packet coding errors which may be present from the CSMA/CD controller.

Once encoding has started, the encoder translates TXD's NRZ format data to Manchester code for transmission on the selected network. Do not put Manchester data on TXD. The CSMA/CD controller is responsible for supplying valid preamble.

TEN must be deasserted at the end of the packet, after the last valid data bit, which is the last bit transmitted onto the selected media. The encoder will supply a valid IDL, and the T7213 must not see TEN again for at least 96 bit times (BT) (the interpacket gap [IPG]). This is to allow the AUI drivers to slowly decrease the current through the inductive load of the isolation transformer. The AUI drivers can be forced to turn on sooner than 96 BT, but the powerdown sequence will be interrupted.

The CSMA/CD controller is responsible for resolving any collisions which result on the network. The only time the T7213 will interrupt the transmission of a packet is when the watchdog timer expires (see TP Transceivers section); otherwise, the T7213 will transmit as long as TEN is asserted.

Functional Description (continued)

Manchester Decoder

The Manchester decoder uses a DPLL to extract the clock and NRZ data from the received Manchester data. The Manchester decoder also looks for IDL and Manchester code violations and reports them to the CSMA/CD controller. The Manchester code violation circuit uses the recovered clock to determine whether data with a missing mid-bit transition has been received. If this is true, the event is reported to the CSMA/CD controller similar to a collision. COL and CRS are then maintained until all receive activity stops. Because an inverted IDL pulse is a Manchester code violation, this feature can be used to determine reversed input pairs on TPI/$\overline{\text{TPI}}$.

Crystal Oscillator

The crystal oscillator is a 20 MHz ± 100 ppm circuit. The 20 MHz clock is used by the T7213 to create the TXC (10 MHz) clock which is used to strobe data out of the CSMA/CD controller. The 20 MHz clock is used to transmit data, derive pre-equalization timing, and drive internal counters. The 20 MHz clock is also used as the reference clock for the DPLL. At least 100 ms must elapse after initial powerup for all the internal circuits to stabilize and for this frequency to be correct. In order to ensure proper operation, the recommended crystal and bypass capacitors must be closely mounted to the T7213.

Table 2. Crystal Specifications

Parameter	Requirement
Type	Quartz Fundamental Mode
Frequency	20 MHz
Stability	25 °C ± 20 ppm 0 °C to 70 °C ± 25 ppm
Shunt Capacitance	<7 pF
Load Capacitance	50 pF
Series Resistance	<25 Ω

The following crystal meets the above requirements:

MTRON #465-160
MTRON Industries, Inc.
100 Douglas Ave.
Yankton, SD 57078-0630
(605) 665-9321

A 100 ppm accurate reference will result if the circuit of Figure 11 is realized.

Controller Interface Select (CIS) Circuit

The CIS circuit ensures that the proper controller signals are exchanged between the T7213 and the CSMA/CD controller, and it ensures that correct polarities are maintained during transmission, reception, and idle periods.

The T7213 provides two modes of operation: AT&T/Intel and National/AMD. A three-level input-sensing circuit is connected to the CIS input pin. When this pin is forced to V_{DD}, AT&T/Intel mode is selected. When it is allowed to float to mid-supply through included biasing circuitry, National/AMD mode is selected. The CIS input should not be switched while power is applied since erratic behavior can result. The forced GND condition is reserved for future use.

Network Interface Select (NIS) Circuit

The NIS circuit determines which network (AUI, TP, or LLB) is requested by the CSMA/CD controller. Through subsequent logic, data is directed from the transmit circuitry to the selected network and from the selected network to the data decoder. Only one network transceiver can be selected at a time; therefore, only one will be addressed by the T7213. Any activity on the deselected network will be disregarded. The NIS input pad is connected to a three-level sensing circuit, as is CIS.

Internal biasing allows a floating NIS pin to come to mid-supply in order to self-bias in LLB mode. To stay mid-supply, there must be <5 μA of leakage to any supply (this corresponds to >500 kΩ impedance to any supply). Because of the high impedance of the self-biasing circuit, eliminate the possibility of capacitive coupling of noisy surrounding circuitry overriding the node by connecting a .01 μF capacitor from NIS to ground. The remaining levels are high and low. These are achieved by overdriving the self-biasing circuit. To do this, the forcing circuit must sink/source >200 μA (this is equivalent to a <10 kΩ impedance to ground or V_{DD}.) Whenever the selected network is deselected and a new network is selected, NIS supplies an approximately 200 ms reset to the appropriate internal T7213 circuitry to ensure a smooth transition.

When NIS is high, TP mode is selected and the TP drivers are controlled by the transmit encoder. When deselected, all the TP output drivers are set to the idle state (all low). Also, when TP mode is selected, all the TP receiver signals are directed to the decoder. When TP is not selected, all TP inputs and the link integrity function are disregarded.

Functional Description (continued)

When NIS is low, AUI mode is selected and the AUI drivers are controlled by the transmit encoder. When deselected, all output drivers are set to the idle state (all off). Also, when AUI mode is selected, all the AUI receiver signals are directed to the decoder and the CI inputs are processed and directed to the appropriate interface circuit. When AUI is deselected, all AUI inputs are disregarded.

When NIS is floating, LLB mode is selected. LLB mode uses the same circuitry as TP mode, except the transmit data is looped back and not transmitted on the TP media output pins. As in TP mode, an SQE test signal is supplied at the end of each transmit packet. As a result of using the same TP circuitry, when in LLB mode, a watchdog timer is invoked. The data is Manchester encoded and then decoded through the T7213's DPLL. While in LLB mode, all input activity is disregarded. The LLB path is shown in Figure 1.

AUI Transceivers

The AUI transceivers include the DO drivers, DI receivers, and CI receivers.

The AUI driver will differentially drive a current onto the load connected between the DO and $\overline{DO}$ pins. At the end of a packet, 300 ns after the rising IDL transition, the output driver begins to reduce its output current drive in order to gradually reduce the current stored in the inductive load without violating IEEE Std 802.3, Figures 7—12.

For testing purposes, the AUI test load must be connected, as shown in Figure 11, for proper termination. If this is done, an output voltage between ±0.6 V and ±1.2 V is measured differentially between the two DO/$\overline{DO}$ pins. The output current is rated at ±21.5 mA ± 3.5 mA at V_{DD} = 5.0 V ± 10% at 25 °C.

The AUI receiver accepts data from the medium attachment unit (MAU) through the DI and $\overline{DI}$ pins. The input must be transformer coupled to the AUI circuit. DC biasing should be provided externally to the chip, with the common mode voltage set to nominal 2.5 V. The differential dc input impedance of the DI and $\overline{DI}$ pins is 20 kΩ ± 20%. Included in this block is a squelch circuit to prevent noise from indicating a packet is being received. This circuit is used to reject spurious noise on DI and $\overline{DI}$ to prevent unintentional start-up. The squelch remains on if the differential input signal is less than 160 mV peak or exceeds this magnitude for less than 20 ns. All signals on DI and $\overline{DI}$ are ignored while the squelch is on. The squelch is turned off if the differential input exceeds 300 mV peak for more than 75 ns, and it remains off until an IDL pulse is detected or the input signal does not exceed the detection threshold for 500 ns ± 100 ns. The receiver is able to resolve differential signals as small as 300 mV peak.

The T7213's CI and $\overline{CI}$ pins must be connected to the AUI's CI and $\overline{CI}$ terminals in a fashion similar to the DI and $\overline{DI}$ terminals. Internally, the CI squelch and receive circuitry is similar to the DI circuitry. However, the CI/$\overline{CI}$ squelch is turned off if the differential input exceeds 300 mV peak for more than 45 ns, to accommodate the 10 MHz CI/$\overline{CI}$ signal. The T7213 will assert and deassert COL asynchronously to any output. In AMD and National controller mode, the collision state machine is essentially independent of the receive data path; that is, CRS is not asserted during CI/$\overline{CI}$ activity unless its assertion is motivated by DI/$\overline{DI}$ activity. Also, the collision state machine cannot differentiate the CS1 from the CS0 signal.

TP Transceivers

The TP transceivers include the TP drivers and receivers. The TP drivers output CMOS logic levels with a source resistance less than 10 Ω and a maximum current rating of 25 mAdc. All TP output driver pins drive low 300 ns after the rising edge of IDL. Do not transmit again for the duration of the IPG (96 BT) to allow the internal SQE/SQE test circuit to perform.

The receiver is able to resolve differential signals as small as 350 mV peak. To do this, the common-mode voltage of the input is required to be a nominal 2.5 V. The DISC can also be configured to achieve long line length operation. To do this, reduce the input common-mode voltage to 2.15 V. If this is done, the squelch threshold is reduced a nominal 50 mV and extended line length operation results. The differential dc input impedance of the TPI/$\overline{TPI}$ pins is 20 kΩ ± 20%. The T7213 squelch function is divided into two parts. The first is amplitude based, where the differential input signal must exceed certain amplitude requirements. The second is time based, where the signals that do exceed the required amplitude must occur with certain polarities and at certain time intervals for the squelch function to be turned off. Once the squelch function has been turned off, all signals present on TPI/$\overline{TPI}$ are received. The squelch is turned back on when an IDL is detected, or there is no input activity for 5 BT ± 1 BT.

Functional Description (continued)

Also included in the TP transceivers is the logic needed to maintain the link-integrity function. LTE/LS is the link-integrity select/link-integrity status pad that alternates between being forced low (to light an external LED to show the link is up) and being forced into a high-impedance state (to determine whether the user wants link integrity enabled or to show the link is down by shutting off the LED). This pin is sampled for 800 ns every 26 ms in order to determine whether the user desires to maintain or cancel the link-integrity function. If LTE is not selected, no link-integrity pulses are transmitted, and incoming LTE pulses are ignored. Recommended applications are shown in Figure 13.

Inside the TP transceiver circuit block is a jabber watchdog timer. The jabber watchdog timer is a counter which starts to increment when transmission on the TP is started. If the CSMA/CD controller attempts to transmit more than 50 ms ± 5 ms, the timer expires and transmission on the TP media is inhibited. The timer is only enabled when the T7213 is configured for TP mode or LLB is invoked, not when configured in the AUI mode.

If the watchdog timer expires, the T7213 stops transmitting on the TP media and asserts COL to the CSMA/CD controller. COL will stay asserted for 500 ms ± 250 ms beyond the deassertion of TEN by the CSMA/CD controller. If the CSMA/CD controller attempts to transmit again while it is jabbed off in this manner, the 500 ms timeout is reset and COL remains asserted. The timer starts incrementing again when TEN is deasserted.

If a packet is received on the TP media while the CSMA/CD controller is jabbed off, COL remains asserted and the T7213 will send CRS to the CSMD/CD controller. If the CSMD/CD controller is still attempting to transmit by the end of this packet, or if the jabber timeout has not elapsed, the T7213 will remain in the jab state previously described.

An internal heartbeat circuit is included in order to simulate the heartbeat (SQE test) signal encountered from a MAU in a conventional 802.3 AUI environment. Analogous to this, the heartbeat is only applied to the CSMD/CD controller at the end of a successful transmission: no collision occurred, no jab occurred, and no link failure condition exists. The SQE test signal will appear to the CSMA/CD controller as COL is asserted (without CRS) 10 BT after IDL is transmitted—COL is held asserted for 11 BT.

To emulate an AUI MAU, when in LLB mode or in TP transmit mode, the encoded data the CSMD/CD controller is attempting to transmit is internally directed back to the timing recovery circuit. When in TP transmit mode, if a packet is received, COL is asserted and CRS is maintained until all activity (transmit and receive) stops; LLB mode cannot be interrupted by incoming data.

Absolute Maximum Ratings

Stresses in excess of the Absolute Maximum Ratings can cause permanent damage to the device. These are absolute stress ratings only. Functional operation of the device is not implied at these or any other conditions in excess of those indicated in the operational sections of this data sheet. Exposure to Absolute Maximum Ratings conditions for extended periods can adversely affect device reliability.

Parameter	Symbol	Min	Max	Unit
Ambient Operating Temperature	T_A	0	70	°C
Storage Temperature	T_{stg}	−65	150	°C
Analog Power Supply Voltage	V_{DDA}	—	5.5	V
Digital Power Supply Voltage	V_{DDD}	—	5.5	V
Voltage on Any Pin with Respect to Ground	—	−0.5	V_{DD} + 0.5	V

Handling Precautions

Although protection circuitry has been designed into this device, proper precautions should be taken to avoid exposure to electrostatic discharge (ESD) during handling and mounting. AT&T employs a human-body model (HBM) and a charged-device model (CDM) for ESD-susceptibility testing and protection design evaluation. ESD voltage thresholds are dependent on the circuit parameters used to define the model. No industry-wide standard has been adopted for the CDM. However, a standard HBM (resistance = 1500 Ω, capacitance = 100 pF) is widely used and therefore can be used for comparison purposes. The HBM ESD threshold presented here was obtained by using these circuit parameters.

Table 3. HBM ESD Threshold Voltage

Device	Voltage
T7213	≤4000 V

Electrical Characteristics

dc Characteristics

Table 4. Digital Interface

Parameter	Symbol	Test Conditions	Min	Max	Unit
Controller Interface Input Low	V_{IL}	—	—	0.8	V
Controller Interface Input High	V_{IH}	—	2.0	—	—
Controller Interface Rise/Fall Time: Input Output	T_R, T_F	 0.8 V and 2 V 0.6 V and 2.4 V, <20 pF load	 — —	 10 5	 ns ns
Controller Interface Output Low	V_{OL}	—	—	0.6	V
Controller Interface Output High	V_{OH}	—	2.4	—	V
Input Leakage Currents	I_{IH}, I_{LL}	Except CIS and NIS	—	10	μA
Max/Min Signal Applied to Pins	V_M	—	GND − 0.3	V_{DD} + 0.3	Vdc

Table 5. Power Dissipation

Parameter	Symbol	Min	Max	Unit
Positive Supply Voltage	V_{DDD}	4.5	5.5	Vdc
Positive Supply Voltage	V_{DDA}	4.5	5.5	Vdc
Positive Supply Current: No Traffic With Traffic	I_{DD}	 — —	 150 200	 mAdc mAdc
Power Dissipation: No Traffic With Traffic	P_D	 — —	 500 775	 mW mW

Table 6. Media Interface

Parameter	Symbol	Min	Max	Unit
AUI Input Voltage	V_{AIDF}	0.3	1.3	Vdiff
TP Input Voltage	V_{DIFF}	0.35	2.0	Vdiff
Oscillator Frequency Error (from 20 MHz)	E_{OSC}	—	100	ppm

Timing Characteristics

Table 7. Generic Timing for TP Applications (See Figure 4.)

Symbol	Parameter	Min	Max	Unit
tTPVCSH	TP Activity to CRS Assertion.	40	900	ns
tTPVRCH	TP Activity to RXC Valid.	1600	2300	ns
tTPHCSL	IDL to CRS Deassertion.	200	550	ns
tTPZCSL	Dead-signal to CRS Deassertion.	400	1000	ns
tTNHPOX	TEN Asserted to Transmit Pair Activity.	50	700	ns
tTNHCSH	TEN Asserted to CRS Asserted Due to Internal Loopback.	5	1900	ns
tTNHRCV	TEN Asserted to RXC Valid Due to Internal Loopback.	1000	1700	ns
tTNLPOH	TEN Deasserted to IDL Transmission.	50	300	ns
tPOHPOL	IDL Pulse-width.	250	350	ns
tTPVCLH	Time to Assert COL. T7213 is Transmitting; Receive Activity Starts.	40	900	ns
tTPHCLL	Time to Deassert COL. T7213 is Transmitting; Receive Activity Ceases.	300	900	ns
tTNHCLH	Time to Assert COL. T7213 is Receiving; Transmit Activity Starts.	5	900	ns
tTNLCLL	Time to Deassert COL. T7213 is Receiving; Transmit Activity Ceases.	5	900	ns
tCLHCLL	COL Pulse-width.	100	—	ns

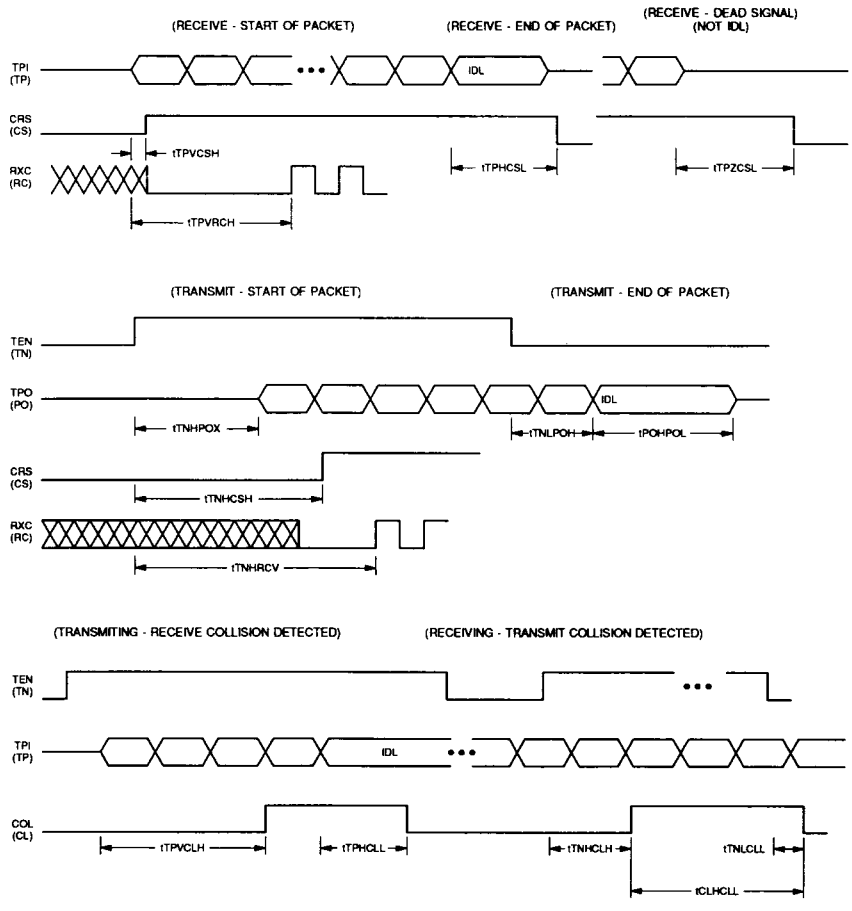


Figure 4. Generic Timing for TP Applications

Timing Characteristics (continued)

Table 8. Generic Timing for AUI Applications (See Figure 5.)

Symbol	Parameter	Min	Max	Unit
tDIVCSH	AUI Activity to CRS Assertion	25	300	ns
tDIVRCH	AUI Activity to RXC Valid	1300	2000	ns
tDIHCSL	IDL to CRS Deassertion	200	500	ns
tDIZCSL	Dead-signal to CRS Deassertion	400	1000	ns
tCLHCLL	COL Pulse-width	1400	—	ns
tTNHDOX	TEN Asserted to Transmit Pair Activity	150	600	ns
tTNLDOH	TEN Deasserted to IDL Transmission	50	300	ns
tDOHDOL	IDL Pulse-width	250	350	ns
tDOHDOZ	Time to Shut AUI Current Off after IDL Starts	7500	8500	ns
tCIVCLH	Time to Assert COL from Beginning of CI Activity	25	300	ns
tCIHCLL	Time to Deassert COL from Beginning of CI IDL	100	400	ns
tCIZCLL	Time to Deassert COL when CI Activity Ends with Dead-signal	100	800	ns

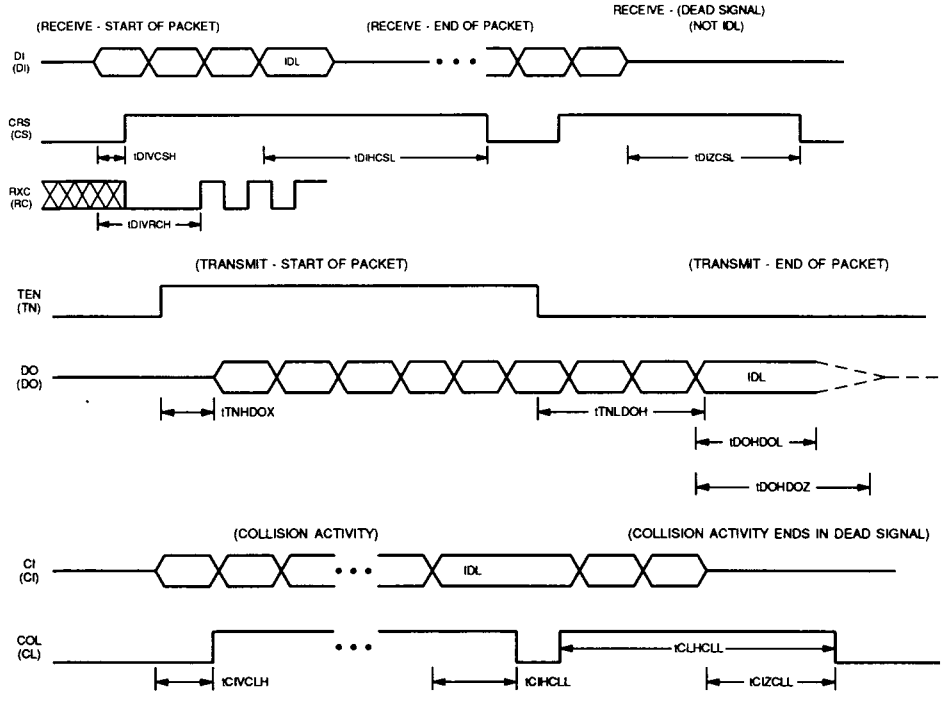


Figure 5. Generic Timing for AUI Applications

Timing Characteristics (continued)

Table 9. Generic Timing for LLB Applications (See Figure 6.)

Symbol	Parameter	Min	Max	Unit
tTNHCSH	Time from TEN Assertion to CRS Assertion when in LLB Mode	5	100	ns
tTNHRCV	Time from TEN Assertion to RXC is Valid when in LLB Mode	1000	1700	ns

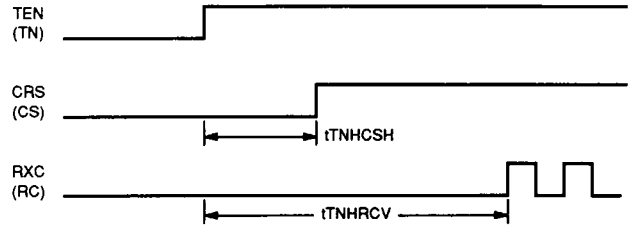


Figure 6. Generic Timing for LLB Applications

Table 10. Specific Timing for AT&T/Intel Controller Interfaces (See Figure 7.)

Symbol	Parameter	Min	Max	Unit
tRCLCSL	RXC Low to CRS Assertion	0	70	ns
tRDVRCL	RXD Setup Before RXC Falling Edge	30	—	ns
tRCLRDH	RXD Held Past RXC Falling Edge	30	—	ns
tRCHCSH	RXC High to CRS Deassertion	3	19	ns
tTNVTCL	TEN Setup Before TXC Falling Edge	50	—	ns
tTCLTNH	TEN Held Past TXC Falling Edge	0	—	ns
tTDVTCL	TXD Setup Before TXC Falling Edge	50	—	ns
tTCLTDH	TXD Held Past TXC Falling Edge	0	—	ns

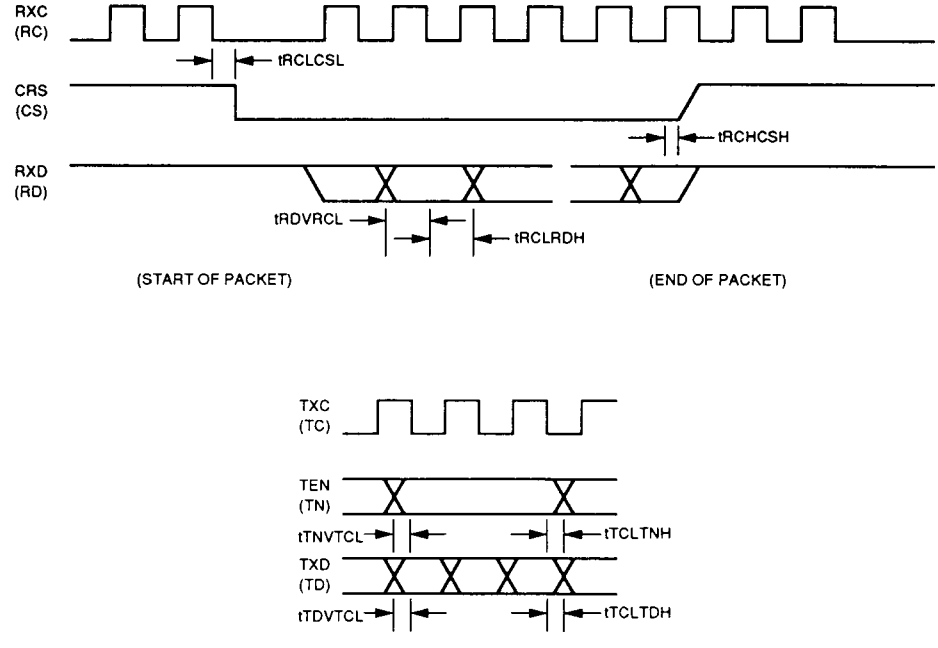


Figure 7. Specific Timing for AT&T/Intel Controller Interfaces

Timing Characteristics (continued)

Table 11. Specific Timing for National/AMD Controller Interfaces (See Figure 8.)

Symbol	Parameter	Min	Max	Unit
tRDVRCH	RXD Setup Before RXC Rising Edge	40	—	ns
tRCHRDH	RXD Held Past RXC Rising Edge	30	—	ns
tRCLCSL	RXC Low to CRS Deassertion	0	100	ns
tTNVTCH	TEN Setup Before TXC Rising Edge	30	—	ns
tTCHTNH	TEN Held Past TXC Rising Edge	0	—	ns
tTDVTCH	TXD Setup Before TXC Rising Edge	30	—	ns
tTCHTDH	TXD Held Past TXC Rising Edge	0	—	ns

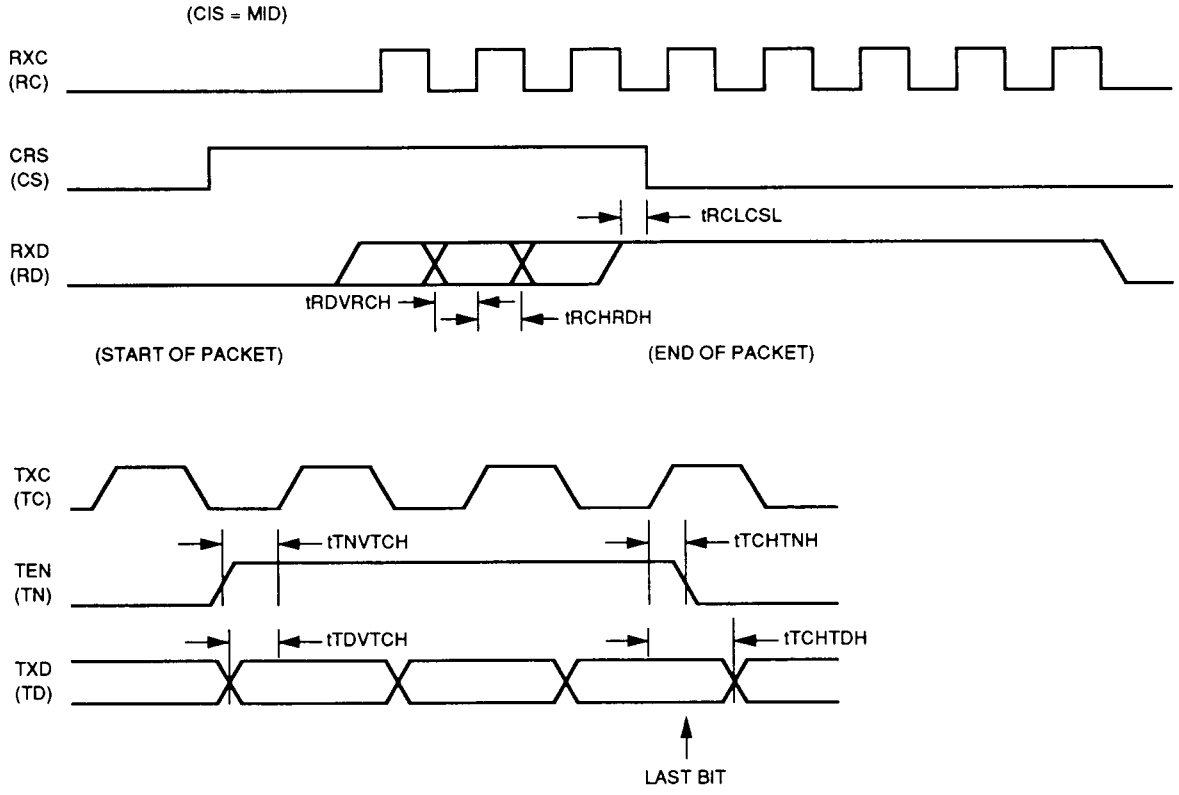


Figure 8. Specific Timing for National/AMD Controller Interfaces

Timing Characteristics (continued)

Table 12. Specific Timing for RXC and TXC (See Figure 9.)

Symbol	Parameter	Min	Max	Unit
tRCLRCH	RXC Low Pulse-width	45	55	ns
tRCHRCL	RXC High Pulse-width	45	55	ns
tTCLTCH	TXC Low Pulse-width	45	55	ns
tTCHTCL	TXC High Pulse-width	45	55	ns

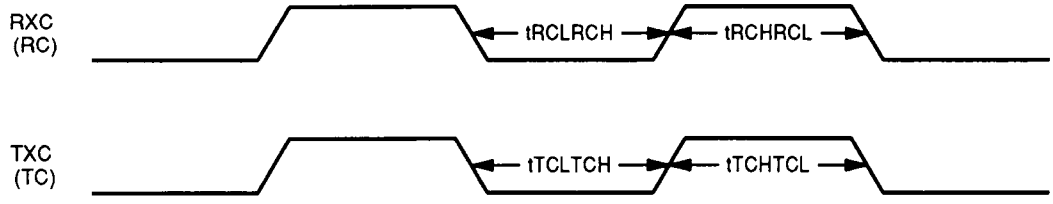


Figure 9. Specific Timing for RXC and TXC

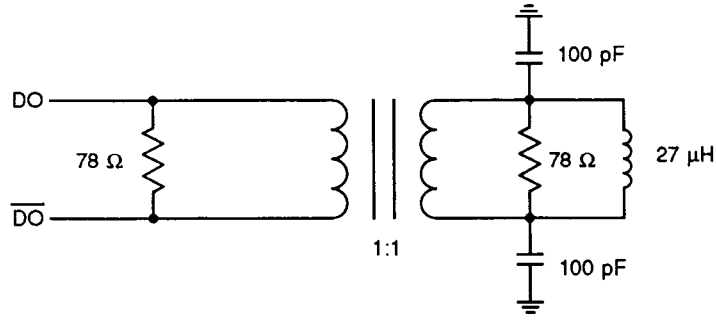
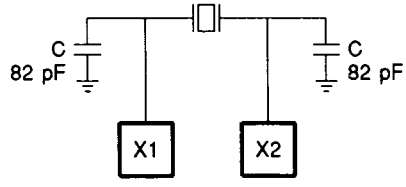


Figure 10. AUI Test Load



Notes:
C = ±5% accuracy.
Leads should be as short as possible.

Figure 11. Crystal Oscillator Recommended Circuit

Timing Characteristics (continued)

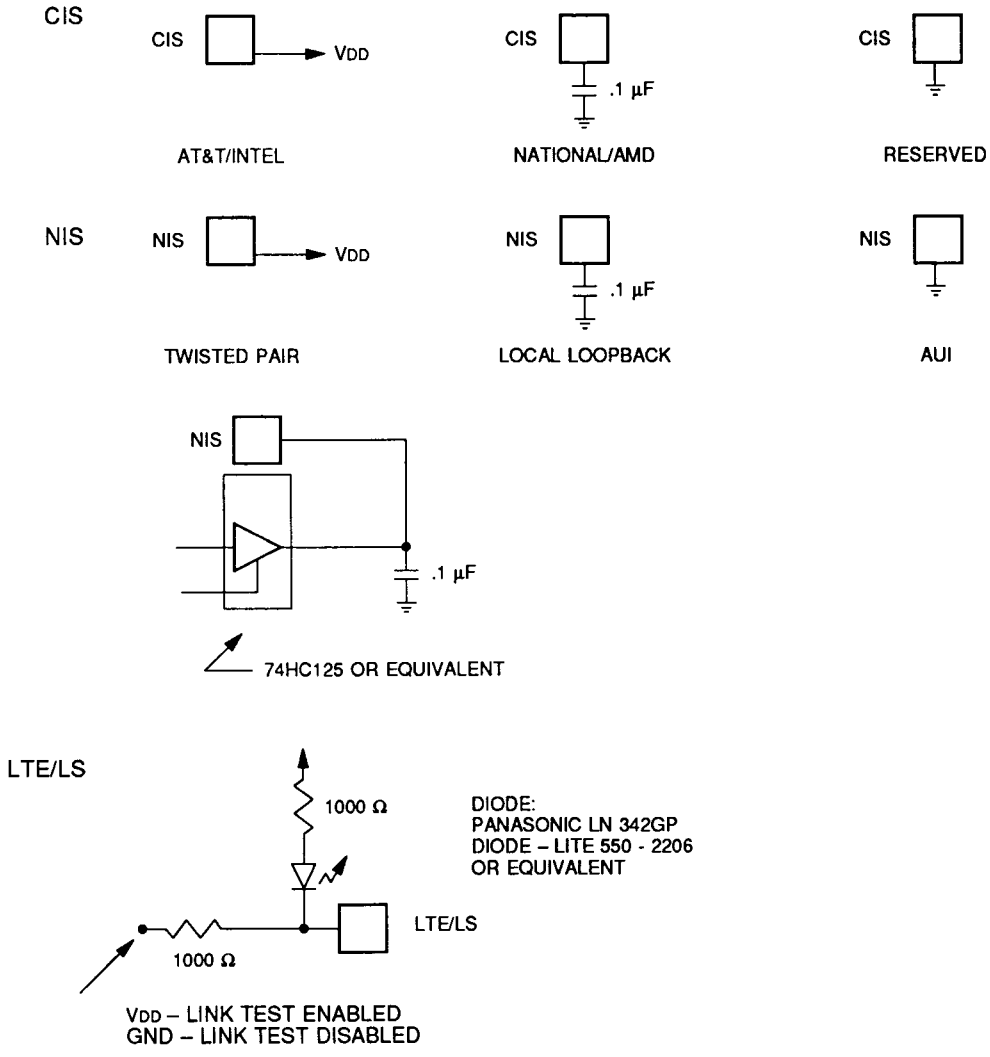
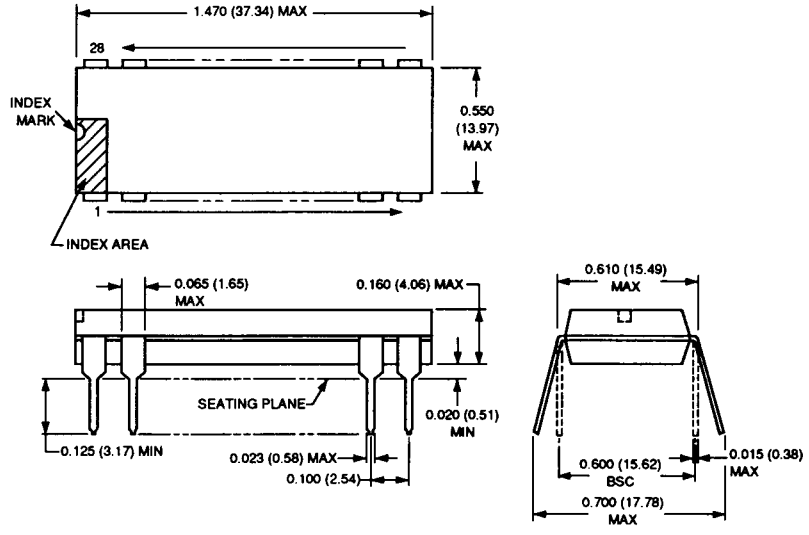


Figure 12. Strapping Options

Outline Diagrams

28-Pin, Plastic DIP

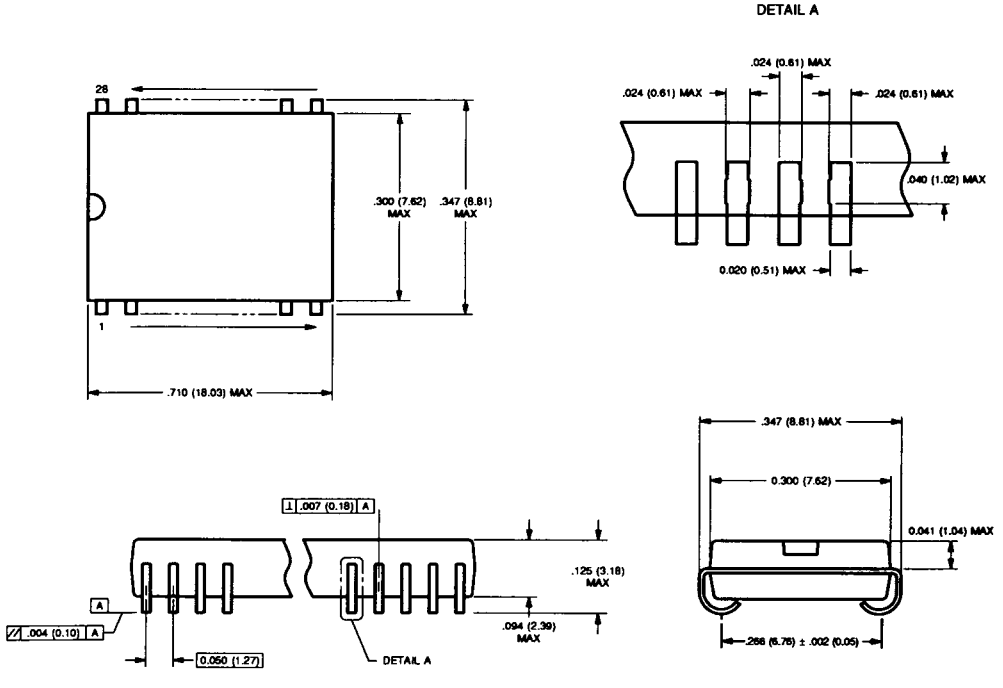
Dimensions are in inches and (millimeters).



Notes:
Meets JEDEC standards.
Index mark may be a semicircular notch or circular dimple located in the index area.

28-Pin, Plastic SOJ

Dimensions are in inches and (millimeters).



Note: Index mark may be a notch, dimple, or bevel located in the zone identified on the outline.

Ordering Information

Device Code	Package	Temperature
T7213-PC	28-Pin, Plastic DIP	0 °C to 70 °C
T7213-EC	28-Pin, Plastic SOJ	0 °C to 70 °C

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