Advance Data Sheet

ATT7C174

High-Speed CMOS SRAM 64 Kbit (8K x 8) Cache-Tag

Features

- 8K by 8-bit static RAM with 8-bit tag comparison logic
- Automatic powerdown during long cycles
- Advanced CMOS technology
- High-speed address-to-MATCH — to 12 ns
- High-speed flash clear
- High-speed read-access time
- Plug-compatible with IDT7174 and MK48H74
- Low-power operation
  - — Active: 320 mW typical at 35 ns
  - — Standby: 500 µW typical
- Data retention at 2 V for battery backup operation
- Package styles available:
  - — 28-pin, plastic DIP
  - — 28-pin, plastic SOJ (J-lead)

Description

The ATT7C174 device is a high-performance, low-power, CMOS static RAM organized as 8192 words by 8 bits per word and includes an 8-bit data comparator with MATCH output. The device is optimized for use as the address tag comparator in high-speed cache memory systems. The 8-bit data is input/output on shared I/O pins, and comparison is performed between 8-bit incoming data and accessed memory locations. One ATT7C174 can map 8K cache lines into a 1 Mbyte address space by comparing 20 address bits organized as 13-line address bits and 7-page address bits.

The ATT7C174 device is available in four speeds with maximum access times from 12 ns to 25 ns. Operation is from a single 5 V power supply. Power consumption is 320 mW (typical) at 35 ns. Dissipation drops to 75 mW (typical) when the memory is deselected (enable is high).

Two standby modes are available. Automatic powerdown during long cycles reduces power consumption during read or write accesses that are longer than the minimum access time, or when memory is deselected. In addition, data can be retained in inactive storage with a supply voltage as low as 2 V. The ATT7C174 consumes only 30 µW at 3 V (typical), thereby allowing effective battery backup operation.

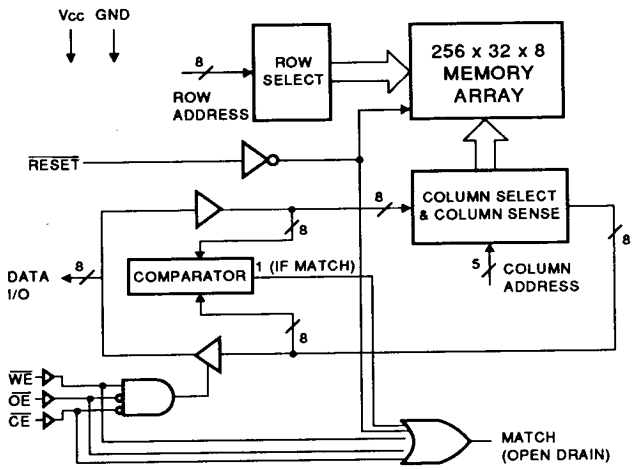

Figure 1. Block Diagram

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Pin Information

Table 1. Pin Descriptions

Pin	Name/Function
A0—A12	Address
I/O0—I/O7	Data Input/Output
$\overline{\text{CLEAR}}$	Clear Address Tag
MATCH	Data Comparison
$\overline{\text{CE}}$	Chip Enable
$\overline{\text{OE}}$	Output Enable
$\overline{\text{WE}}$	Write Enable
GND	Ground
Vcc	Power

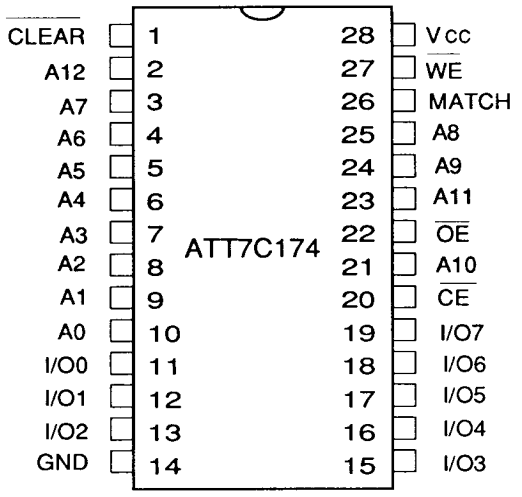

Figure 2. Pin Diagram

Table 2. Truth Table

X = don't care; L = V_{IL}; H = V_{IH}

$\overline{\text{WE}}$	$\overline{\text{CE}}$	$\overline{\text{OE}}$	$\overline{\text{CLEAR}}$	MATCH	I/O	Function
X	X	X	L	H	—	Reset All Bits to Low
X	H	X	H	H	High-Z	Deselect Chip
H	L	H	H	L	D_{IN}	No MATCH
H	L	H	H	H	D_{IN}	MATCH
H	L	L	H	H	D_{OUT}	Memory Read
L	L	X	H	H	D_{IN}	Memory Write

Functional Description

The ATT7C174 device provides asynchronous (unclocked) operation with matching access and cycle times. The active-low chip enable and output enable along with a 3-state I/O bus simplify the connection of several chips for increased storage capacity. Wide tag addresses are easily accommodated by paralleling devices and wire-ORing the MATCH outputs. Memory locations are specified on address pins A0 through A12 with the functions as defined in Table 2.

In addition, a high-speed $\overline{\text{CLEAR}}$ control clears all memory locations to 0 when activated. This allows all address-tag bits to be cleared when the cache is being powered on or flushed. During $\overline{\text{CLEAR}}$, the state of the I/O pins is completely defined by the $\overline{\text{WE}}$, $\overline{\text{CE}}$, and $\overline{\text{OE}}$ control inputs. Data-in has the same polarity as data-out.

Latchup and static discharge protection are provided on-chip. The ATT7C174 can withstand an injection of up to 200 mA on any pin without damage.

Absolute Maximum Ratings

Stresses exceeding the values listed under Absolute Maximum Ratings can cause permanent damage to the device. This is an absolute stress rating only. Functional operation of the device at these or any other conditions in excess of those indicated in the operational sections of this data sheet is not implied. Exposure to Absolute Maximum Ratings conditions for extended periods of time can adversely affect device reliability.

Parameter	Symbol	Min	Max	Unit
Storage Temperature	T_{stg}	−65	150	°C
Operating Ambient Temperature	T_A	−55	125	°C
Supply Voltage with Respect to Ground	V_{CC}	−0.5	7.0	V
Input Signal with Respect to Ground	—	−3.0	7.0	V
Signal Applied to High-impedance Output	—	−3.0	7.0	V
Output Current into Low Outputs	—	—	25	mA
Latchup Current	—	> 200	—	mA

Recommended Operating Conditions

Mode	Temperature Range (Ambient)	Supply Voltage
Active Operation	0 °C to 70 °C	4.5 V ≤ V_{CC} ≤ 5.5 V
Data Retention	0 °C to 70 °C	2.0 V ≤ V_{CC} ≤ 5.5 V

Electrical Characteristics

Over all Recommended Operating Conditions

Table 3. General Electrical Characteristics

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Output Voltage:						
High	V_{OH}	I_{OH} = –4.0 mA, V_{CC} = 4.5 V (except MATCH pin)	2.4	—	—	V
Low	V_{OL}	I_{OL} = 8.0 mA (all except MATCH pin)	—	—	0.4	V
		I_{OL} = 10.0 mA (all except MATCH pin)	—	—	0.5	V
		I_{OL} = 18.0 mA (MATCH pin)	—	—	0.4	V
		I_{OL} = 22.0 mA (MATCH pin)	—	—	0.5	V
Input Voltage:						
High	V_{IH}	—	2.2	—	V_{CC} + 0.3	V
Low	V_{IL}	See note 1.	–3.0	—	0.8	V
Input Current	I_{IX}	Ground ≤ V_I ≤ V_{CC}	–10	—	10	µA
Output Leakage Current	I_{OZ}	Ground ≤ V_O ≤ V_{CC}, $\overline{CE}$ = V_{CC}	–10	—	10	µA
Output Short Current	I_{OS}	V_O = Ground, V_{CC} = Max (See note 2.)	—	—	–350	mA
V_{CC} Current:						
Inactive	I_{CC2}	See note 3.	—	15	30	mA
Standby	I_{CC3}	See note 4.	—	100	500	µA
DR Mode	I_{CC4}	V_{CC} = 3.0 V (See note 5.)	—	10	250	µA
Capacitance:						
Input	C_I	T_A= 25 °C, V_{CC} = 5.0 V	—	—	5	pF
Output	C_O	Test frequency = 1 MHz (See note 6.)	—	—	7	pF

1. This device provides hard clamping of transient undershoot. Input levels below ground are clamped beginning at –0.6 V. A current in excess of 100 mA is required to reach –2 V. The device can withstand indefinite operation with inputs as low as –3 V, subject only to power dissipation and bond-wire fusing constraints.
2. Duration of the output short-circuit should not exceed 30 s.
3. Tested with outputs open and all address and data inputs stable. The device is continuously disabled, i.e., $\overline{CE}$ = V_{CC}. Input levels are within 0.2 V of V_{CC} or ground.
4. Data retention operation requires that V_{CC} never drops below 2.0 V. $\overline{CE}$ must be ≥ V_{CC} – 0.2 V. For all other inputs, V_{IN} ≥ V_{CC} – 0.2 V or V_{IN} < 0.2 V is required to ensure full powerdown.
5. This parameter is not 100% tested.

Table 4. Electrical Characteristics by Speed

Parameter	Symbol	Test Conditions	Speed				Unit
			25	20	15	12	
V_{CC} Current, Active	I_{CC1}	*	150	185	240	275	mA

* Tested with outputs open and all address and data inputs changing at the maximum write-cycle rate. The device is continuously enabled for writing, i.e., $\overline{CE}$, $\overline{OE}$, and $\overline{WE}$ ≤ V_{IL} Input pulse levels are 0 V to 3.0 V.

Timing Characteristics

Table 5. Read Cycle (See notes 1, 2, 3, and 4.)

Over all Recommended Operating Conditions; all measurements in ns. Test conditions assume input transition times of <3 ns, reference levels of 1.5 V, input pulse levels of 0 V to 3.0 V (see Figure 11), and output loading for specified I_{OL} and I_{OH} + 30 pF (see Figures 10A and 10C).

Symbol	Parameter	Speed							
		25		20		15		12	
		Min	Max	Min	Max	Min	Max	Min	Max
tADXADX, tCELCEH	Read-cycle Time	25	—	20	—	15	—	12	—
tADXDOV	Address Change to Output Valid (See notes 5 and 6.)	—	25	—	20	—	15	—	12
tADXDOX	Address Change to Output Change	3	—	3	—	3	—	3	—
tCELDOV	Chip Enable Low to Output Valid (See notes 5 and 7.)	—	25	—	20	—	15	—	12
tCELDOZ	Chip Enable Low to Output Low-Z (See notes 8 and 9.)	3	—	3	—	3	—	3	—
tCEHDOZ	Chip Enable High to Output High-Z (See notes 8 and 9.)	—	10	—	8	—	8	—	5
tOELDOV	Output Enable Low to Output Valid	—	12	—	10	—	8	—	6
tOELDOZ	Output Enable Low to Output Low-Z (See notes 8 and 9.)	0	—	0	—	0	—	0	—
tOEHDOZ	Output Enable High to Output High-Z (See notes 8 and 9.)	—	10	—	8	—	5	—	5
tCELICH, tADXICH	Chip Enable Low or Address Change to Powerup (See notes 10 and 11.)	0	—	0	—	0	—	0	—
tICHICL	Powerup to Powerdown (See notes 10 and 11.)	—	25	—	20	—	20	—	20

1. Each parameter is shown as a minimum or maximum value. Input requirements are specified from the point of view of the external system driving the chip. For example, tADXWEH is specified as a minimum since the external system must supply at least that much time to meet the worst-case requirements of all parts. Responses from the internal circuitry are specified from the point of view of the device. Access time, for example, is specified as a maximum since worst-case operation of any device always provides data within that time.
2. All address timings are referenced from the last valid address line to the first transitioning address line.
3. $\overline{CE}$ or $\overline{WE}$ must be high during address transitions.
4. This product is a very high-speed device, and care must be taken during testing in order to realize valid test information. Inadequate attention to setups and procedures can cause a good part to be rejected as faulty. Long high-inductance leads that cause supply bounce must be avoided by bringing the Vcc and ground planes directly up to the contactor fingers. A 0.01 µF high-frequency capacitor is also required between Vcc and ground. To avoid signal reflections, proper terminations must be used.
5. $\overline{WE}$ is high for the read cycle.
6. During this state, the chip is continuously selected ($\overline{CE}$ low).
7. All address lines are valid prior to or coincident with the $\overline{CE}$ transition to active.
8. At any given temperature and voltage condition, output-disable time is less than output-enable time for any given device.
9. Transition is measured ±200 mV from steady-state voltage with specified loading in Figure 10B. This parameter is sampled and not 100% tested.
10. This parameter is not 100% tested.
11. Powerup from I_{CC2} to I_{CC1} occurs as a result of any of the following conditions: (1) falling edge of $\overline{CE}$, (2) falling edge of $\overline{WE}$ ($\overline{CE}$ active), (3) transition on any address line ($\overline{CE}$ active), (4) transition on any data line ($\overline{CE}$ and $\overline{WE}$ active), or (5) falling edge of $\overline{CLEAR}$. The device automatically powers down from I_{CC1} to I_{CC2} after tICHICL has elapsed from any of the powerup triggers. The exception is $\overline{CLEAR}$, where the device remains powered up for the duration of the clear cycle. Power dissipation is dependent only on cycle rate, not on chip-select pulse width.

Timing Characteristics (continued)

Table 6. Write Cycle (See notes 1, 2, 3, and 4.)

Over all Recommended Operating Conditions; all measurements in ns. Test conditions assume input transition times of <3 ns, reference levels of 1.5 V, input pulse levels of 0 V to 3.0 V (see Figure 11), and output loading for specified I_{OL} and I_{OH} + 30 pF (see Figures 10A and 10C).

Symbol	Parameter	Speed							
		25		20		15		12	
		Min	Max	Min	Max	Min	Max	Min	Max
tADXADX	Write-cycle Time	20		20	—	15	—	12	—
tCELWEH	Chip Enable Low to End of Write Cycle	15	—	15	—	12	—	10	—
tADXWEX, tADXWEL	Address Change to Beginning of Write Cycle	0	—	0	—	0	—	0	—
tADXWEH	Address Change to End of Write Cycle	15	—	15	—	12	—	10	—
tWEHADX	End of Write Cycle to Address Change	0	—	0	—	0	—	0	—
tWELWEH	Write Enable Low to End of Write Cycle	15	—	15	—	12	—	10	—
tDIVWEH, tDIXCEH	Data Valid to End of Write Cycle	10	—	10	—	7	—	6	—
tWEHDIV, tWEHDIX	End of Write Cycle to Data Change	0	—	0	—	0	—	0	—
tWEHDOZ	Write Enable High to Output Low-Z (See notes 5 and 6.)	0	—	0	—	0	—	0	—
tWELDOZ	Write Enable Low to Output High-Z (See notes 5 and 6.)	—	7	—	7	—	5	—	4
tCELICH	Chip Enable Low to Powerup (See notes 7 and 8.)	0	—	0	—	0	—	0	—
tWELICH	Write Enable Low to Powerup (See notes 7 and 8.)	0	—	0	—	0	—	0	—
tCEHVCL	Chip Enable High to Data Retention (See note 7.)	0	—	0	—	0	—	0	—

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5. At any given temperature and voltage condition, output-disable time is less than output-enable time for any given device.
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8. Powerup from I_{CC2} to I_{CC1} occurs as a result of any of the following conditions: (1) falling edge of $\overline{CE}$, (2) falling edge of $\overline{WE}$ ($\overline{CE}$ active), (3) transition on any address line ($\overline{CE}$ active), (4) transition on any data line ($\overline{CE}$ and $\overline{WE}$ active), or (5) falling edge of $\overline{CLEAR}$. The device automatically powers down from I_{CC1} to I_{CC2} after tICHICL has elapsed from any of the powerup triggers. The exception is $\overline{CLEAR}$, where the device remains powered up for the duration of the clear cycle. Power dissipation is dependent only on cycle rate, not on chip-select pulse width.

Timing Characteristics (continued)

Table 7. MATCH and $\overline{\text{CLEAR}}$ Cycles

Over all Recommended Operating Conditions; all measurements in ns. Test conditions assume input transition times of <3 ns, reference levels of 1.5 V, input pulse levels of 0 V to 3.0 V (see Figure 11), and output loading for specified I_{OL} and I_{OH} + 30 pF (see Figures 10A and 10C).

Symbol	Parameter	Speed							
		25		20		15		12	
		Min	Max	Min	Max	Min	Max	Min	Max
tADXADX	MATCH-cycle Time	25	—	20	—	15	—	12	—
tADXMV	Address Change to MATCH Valid	—	22	—	20	—	15	—	12
tADXMX	Address Change to MATCH Change	3	—	3	—	3	—	3	—
tCELMV	Chip Enable Low to MATCH Valid	—	15	—	10	—	10	—	8
tCEHMH	Chip Enable High to MATCH High	—	15	—	10	—	10	—	8
tOEHMV	Output Enable High to MATCH Valid	—	15	—	15	—	13	—	10
tOELMH	Output Enable Low to MATCH High	—	20	—	15	—	12	—	10
tWEHMV	Write Enable High to MATCH Valid	—	15	—	15	—	13	—	10
tWELMH	Write Enable Low to MATCH High	—	20	—	15	—	12	—	10
tCLMH	$\overline{\text{CLEAR}}$ Low to MATCH High	0	20	0	15	0	12	0	10
tDVMV	Data Valid to MATCH Valid	—	15	—	15	—	13	—	10
tDXMX	Data Change to MATCH Change	0	—	0	—	0	—	0	—
tCLICL	Clear Cycle Time	55	—	45	—	35	—	30	—
tCLCH	$\overline{\text{CLEAR}}$ Pulse Width	15	—	15	—	12	—	12	—
tCLOEWEX	$\overline{\text{CLEAR}}$ Low to Inputs Don't Care	0	—	0	—	0	—	0	—
tCLICL	$\overline{\text{CLEAR}}$ Low to Powerdown	—	55	—	45	—	35	—	30
tCLICH	$\overline{\text{CLEAR}}$ Low to Powerup	0	—	0	—	0	—	0	—

1. Each parameter is shown as a minimum or maximum value. Input requirements are specified from the point of view of the external system driving the chip. For example, tADXWEH is specified as a minimum since the external system must supply at least that much time to meet the worst-case requirements of all parts. Responses from the internal circuitry are specified from the point of view of the device. Access time, for example, is specified as a maximum since worst-case operation of any device always provides data within that time.
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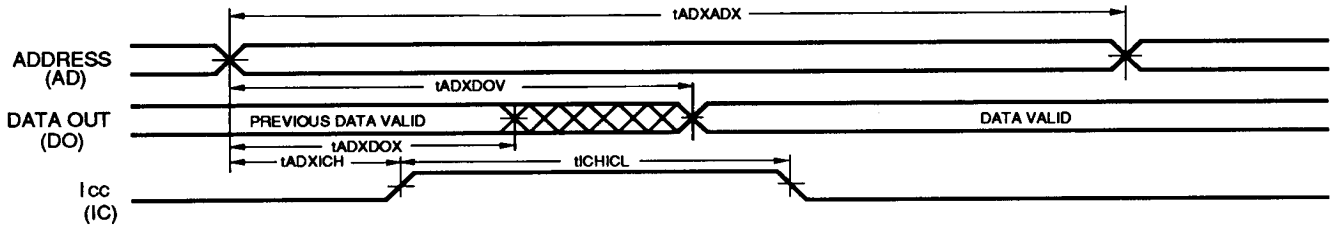
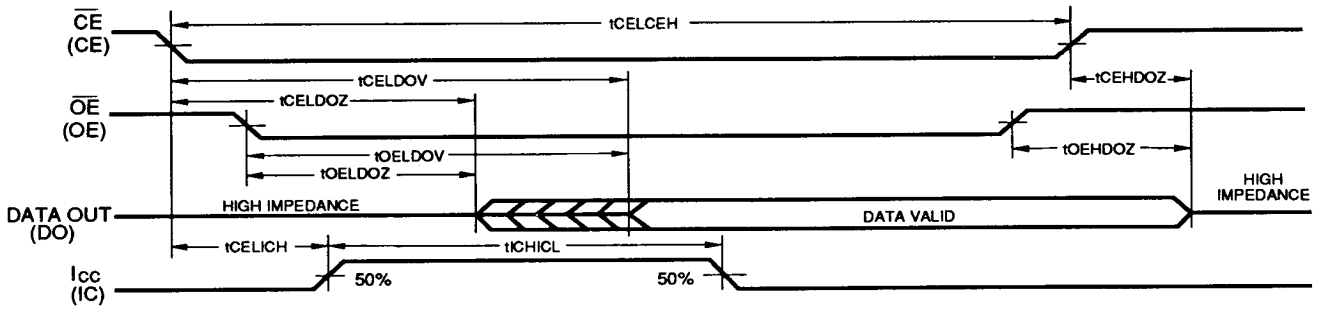
Timing Characteristics (continued)

Timing Diagrams



Notes:
$\overline{WE}$ is high for the read cycle.
The chip is continuously selected ($\overline{CE}$ low).

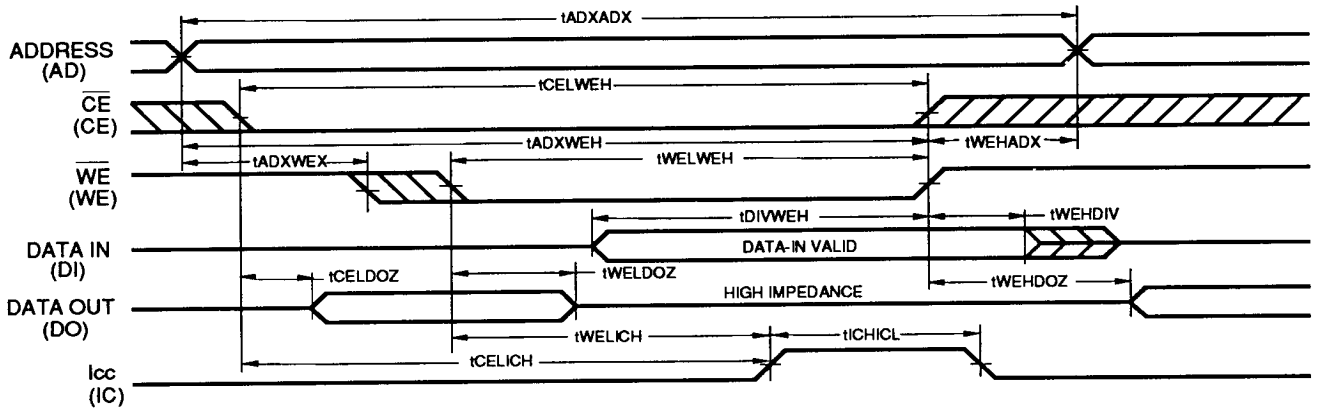
Figure 3. Read Cycle — Address-Controlled



Notes:
$\overline{WE}$ is high for the read cycle.
All address lines are valid prior to or coincident with the $\overline{CE}$ transition to low.

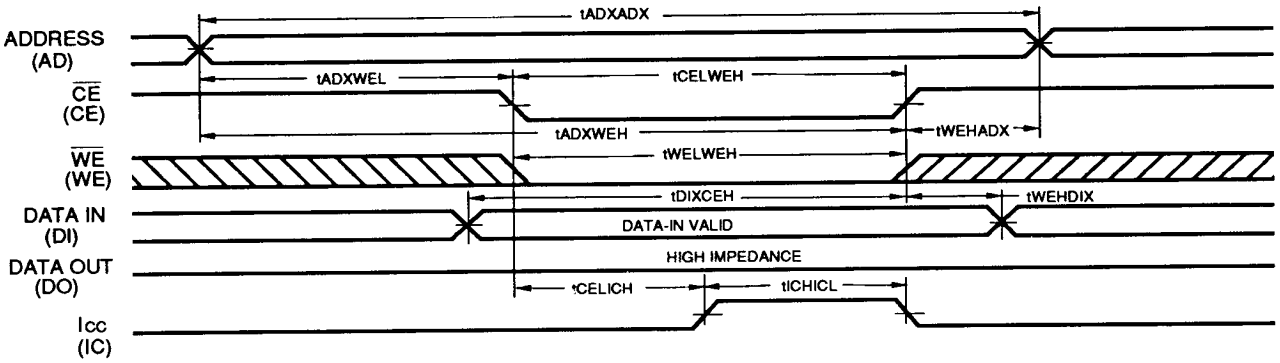
Figure 4. Read Cycle — $\overline{CE}$ / $\overline{OE}$ -Controlled

Timing Characteristics (continued)



1. The internal write cycle of the memory is defined by the overlap of $\overline{CE}$ low and $\overline{WE}$ low. Both signals must be low to initiate a write. Either signal can terminate a write by going high. The address, data, and control input setup and hold times should be referred to the signal that falls last or rises first.
2. If $\overline{WE}$ goes low before or concurrent with $\overline{CE}$ going low, the output remains in a high-impedance state.
3. If $\overline{CE}$ goes high before or concurrent with $\overline{WE}$ going high, the output remains in a high-impedance state.
4. Powerup from I_{CC2} to I_{CC1} occurs as a result of any of the following conditions: (1) falling edge of $\overline{CE}$, (2) falling edge of $\overline{WE}$ ($\overline{CE}$ active), (3) transition on any address line ($\overline{CE}$ active), (4) transition on any data line ($\overline{CE}$ and $\overline{WE}$ active), or (5) falling edge of $\overline{CLEAR}$. The device automatically powers down from I_{CC1} to I_{CC2} after tICHICL has elapsed from any of the powerup triggers. The exception is $\overline{CLEAR}$, where the device remains powered up for the duration of the clear cycle. Power dissipation is dependent only on cycle rate, not on chip-select pulse width.

Figure 5. Write Cycle — $\overline{WE}$-Controlled



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2. If $\overline{WE}$ goes low before or concurrent with $\overline{CE}$ going low, the output remains in a high-impedance state.
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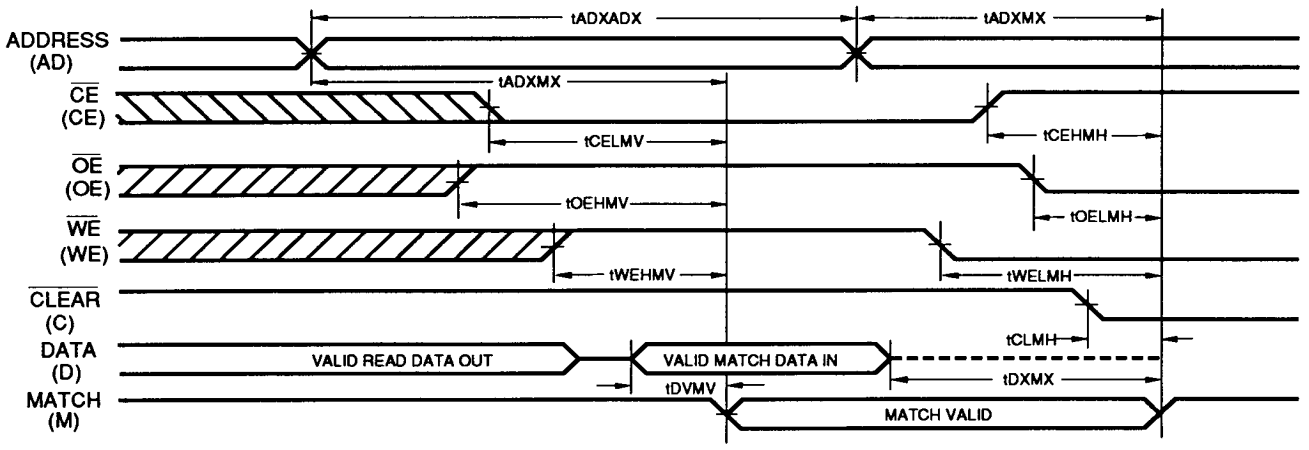
4. Powerup from I_{CC2} to I_{CC1} occurs as a result of any of the following conditions: (1) falling edge of $\overline{CE}$, (2) falling edge of $\overline{WE}$ ($\overline{CE}$ active), (3) transition on any address line ($\overline{CE}$ active), (4) transition on any data line ($\overline{CE}$ and $\overline{WE}$ active), or (5) falling edge of $\overline{CLEAR}$. The device automatically powers down from I_{CC1} to I_{CC2} after tICHICL has elapsed from any of the powerup triggers. The exception is $\overline{CLEAR}$, where the device remains powered up for the duration of the clear cycle. Power dissipation is dependent only on cycle rate, not on chip-select pulse width.

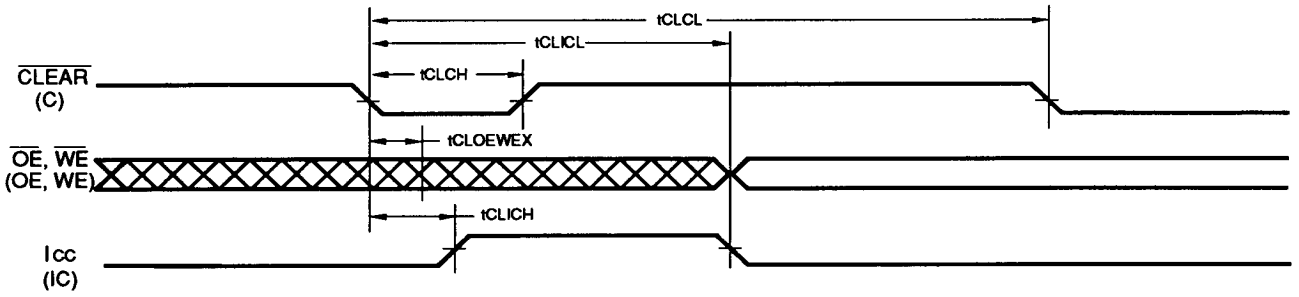
Figure 6. Write Cycle — $\overline{CE}$-Controlled

Timing Characteristics (continued)



Note:
Powerup from I_{CC2} to I_{CC1} occurs as a result of any of the following conditions: (1) falling edge of $\overline{CE}$, (2) falling edge of $\overline{WE}$ ($\overline{CE}$ active), (3) transition on any address line ($\overline{CE}$ active), (4) transition on any data line ($\overline{CE}$ and $\overline{WE}$ active), or (5) falling edge of $\overline{CLEAR}$. The device automatically powers down from I_{CC1} to I_{CC2} after tICHICL has elapsed from any of the powerup triggers. The exception is $\overline{CLEAR}$, where the device remains powered up for the duration of the clear cycle. Power dissipation is dependent only on cycle rate, not on chip-select pulse width.

Figure 7. MATCH Timing



Note:
Powerup from I_{CC2} to I_{CC1} occurs as a result of any of the following conditions: (1) falling edge of $\overline{CE}$, (2) falling edge of $\overline{WE}$ ($\overline{CE}$ active), (3) transition on any address line ($\overline{CE}$ active), (4) transition on any data line ($\overline{CE}$ and $\overline{WE}$ active), or (5) falling edge of $\overline{CLEAR}$. The device automatically powers down from I_{CC1} to I_{CC2} after tICHICL has elapsed from any of the powerup triggers. The exception is $\overline{CLEAR}$, where the device remains powered up for the duration of the clear cycle. Power dissipation is dependent only on cycle rate, not on chip-select pulse width.

Figure 8. $\overline{CLEAR}$ Timing

Timing Characteristics (continued)

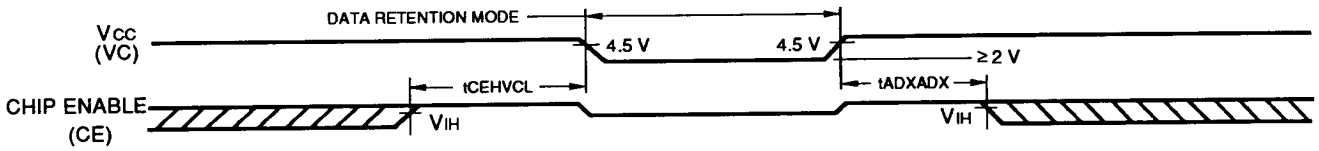
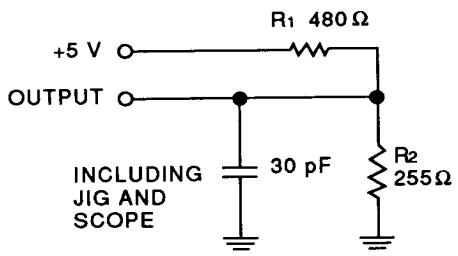
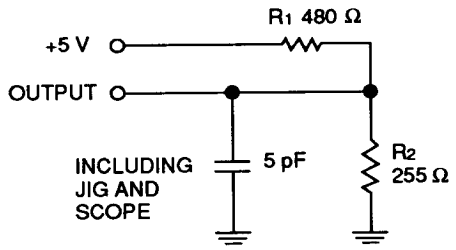


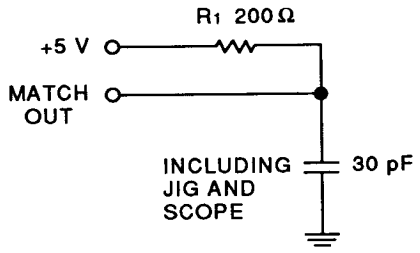
Figure 9. Data Retention



A.



B.



C.

Figure 10. Test Loads

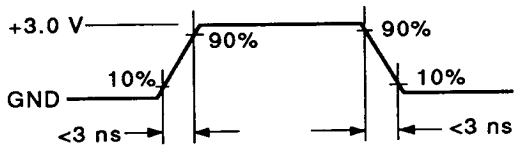
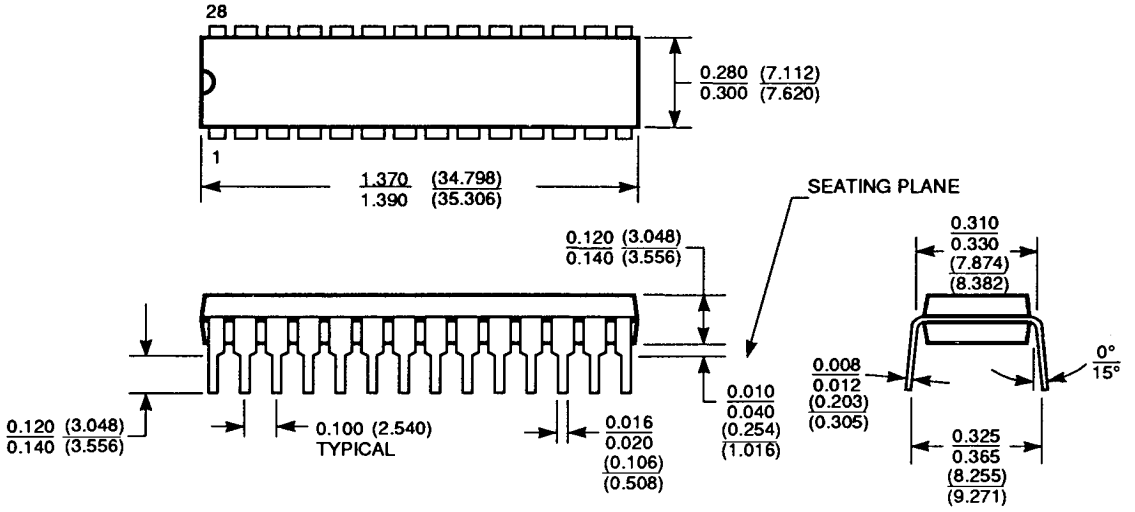


Figure 11. Transition Times

Outline Diagrams

28-Pin, Plastic DIP

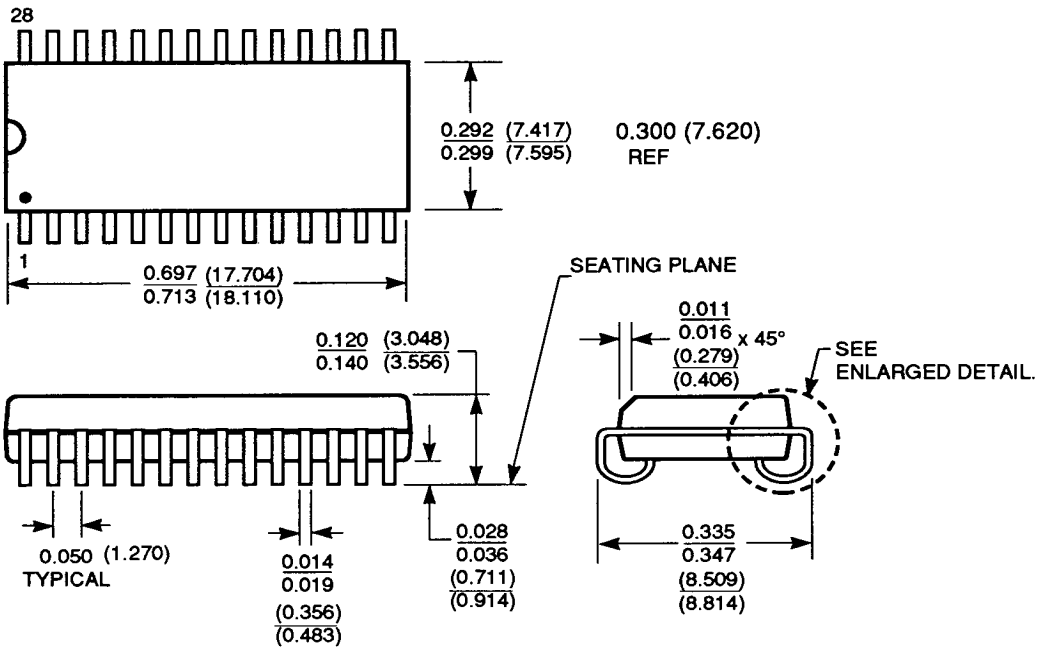
Dimensions are in inches and (millimeters).

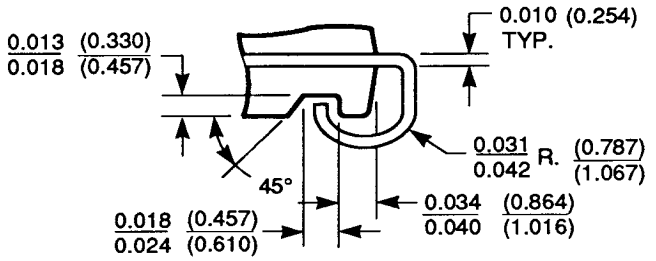


Outline Diagrams (continued)

28-Pin, Plastic SOJ

Dimensions are in inches and (millimeters).





ENLARGED DETAIL

Ordering Information

Operating Range 0 °C to 70 °C

Package Style	Performance Speed			
	25 ns	20 ns	15 ns	12 ns
28-Pin, Plastic DIP	ATT7C174P–25	ATT7C174P–20	ATT7C174P–15	ATT7C174P–12
28-Pin, Plastic SOJ	ATT7C174J–25	ATT7C174J–20	ATT7C174J–15	ATT7C174J–12

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EUROPE: AT&T Microelectronics, AT&T Deutschland GmbH, Bahnhofstr. 27A, D-8043 Unterfoehring, West Germany
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