AP-581

APPLICATION NOTE

Mobile Pentium® Processor with MMX™ Technology: Power Supply Design Considerations for Mobile Systems

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CONTENTS

1.0. INTRODUCTION

The performance level in the mobile market segment has increased and presents new challenges to the system designer. Performance on par with a desktop with new features like MMX™ technology create a need for more power to the CPU. The average and peak power of real applications as well as the maximum current consumption have risen. Thermal, power supply design, and power management issues are impacted as a result.

This document is mainly concerned with power supply design considerations. The amount, size, and type of bulk and high frequency decoupling capacitors placed at the CPU are important to support the tolerance specifications for the supply voltages. This document makes general recommendations based on a selected test system.

The new mobile processor family continues to support voltage reduction technology which allows the CPU core to operate at a lower voltage level than the I/O ring. For the P55C, the core voltage (V_{CC2}) operates at 2.45V while the I/O ring (V_{CC3}) operates at 3.3V, allowing compatibility with existing I/O designs. Two power supply solutions are required to provide the voltage and current to the split core and I/O power planes.

This document targets the designer who has developed systems for Pentium® processors with voltage reduction technology in the past and is familiar with the application notes listed in the reference section. This document recommends decoupling capacitance at the CPU level and makes no attempt to clarify power supply design issues. There is no intention to recommend any one power supply solution or vendor.

Section 2 of this document includes a discussion of mobile power supply options. High frequency and bulk decoupling capacitor solutions are discussed in Section 3. Section 4 describes the testing methodology and platform used for data collection are described. Section 5 presents the data while Section 6 offers a conclusion and summary.

The data presented in this application note reflects studies on a selected system. Measurements should be made on individual systems to ensure a robust design.

2.0. POWER SUPPLY OVERVIEW

The system designer must consider the two power requirements for the processor. The core requires 2.45V while the I/O requires 3.3V. V_{CC2} draws a significant amount of the total current and, as a result, presents the greatest challenge in meeting tolerance (± 165 mV).

These voltage levels must be maintained when the CPU cycles between the Active and StopClock states. The power consumption of each state differs so the power supply and CPU decoupling must be able to handle the associated load current changes. Table 1 indicates the current requirements of each state.

Along with the Active and StopClock states, the processor also enters a state known as StopGrant. In the Active state, the processor behaves normally and has a current draw dependent upon the activity of the CPU. In the StopClock state, the CPU clock is halted and the processor performs minimal activities. The StopGrant state occurs during the transition from Active to StopClock. It allows the current bus cycle to complete and then executes a StopGrant cycle which prepares the CPU and warns external devices of the upcoming StopClock state. The current consumed by the processor in StopGrant is slightly higher than that of StopClock.

During a state transition, the current draw of the CPU changes dramatically (from high to low draw, or vice-versa). The power supply responds to such a load change and either increases or decreases the power output as needed. Capacitors at the CPU sustain the voltage levels and act as a current sink, drawing excess current away from the CPU or from the power supply.

Regulator choice for the power supply plays a critical role in handling the transients mentioned above. A linear regulator handles the transients but is grossly inefficient for the mobile environment. A switching regulator does not handle transients as quickly, but its efficiency produces a longer battery life.

The following sections discuss the trade-offs in more detail and introduce a methodology to design a power supply solution using a switching regulator.

Table 1. Pentium® Processor Maximum Active and StopClock Power Supply Currents[1]

	P55CLM 150 MHz	P55CLM 166 MHz
I_{CC2} Max / I_{CC2} Min	3.7 A / ~20 mA	4.1 A / ~20 mA
I_{CC3} Max / I_{CC3} Min	370 mA / ~10 mA	400 mA / ~10 mA

NOTE:

1. StopClock numbers are not a specification.

2.1. Regulator Options

There are two fundamental choices for power supply implementation. The linear regulator utilizes a voltage divider to bring the supply voltage down to a proper level for the CPU. There are variations on this theme, but the end result is largely the same: inefficiency. For example, supplying a 2.5V linear regulator which has a 5.5V input, has an efficiency of 45 percent:

$$Efficiency = \frac{Pout}{Pin} = \frac{Vout \cdot Iout}{Vin \cdot Iin}$$

Since the load current always passes through the regulator, the power efficiency is equal to:

$$Efficiency = \frac{Vout}{Vin} = \frac{2.5}{5.5} = .45$$

In other words, the best utilization of input voltage the linear regulator can achieve is 45 percent. The remaining 55 percent is dissipated as heat and this causes thermal issues and shorter battery life. From the efficiency equation, if the input supply voltage is 12V, even larger penalties are introduced. While this type of regulation has its place in the desktop environment, it is not well-suited for the mobile platform.

The major benefit of a linear regulator, however, is its transient response. When reacting to a load change the regulator is able to respond quickly to compensate for the higher or lower current draw while maintaining a constant voltage output. The output power, then, is well-regulated.

A switching regulator, on the other hand, is extremely efficient (90 to 95 percent) but is slower to respond to load changes. Switching regulators control the current supplied by sensing the delivered current at a set frequency. It adjusts the supply current either by turning on or turning off the current output. This process normalizes the output voltage on the load.

2.2. The Switching Regulator

The basic layout of a switching regulator is detailed in Figure 1. This is a simplified schematic and shows only the critical components. This section will briefly describe the operation of the switching regulator and discuss some design trade-offs. A detailed discussion is beyond the scope of this document.

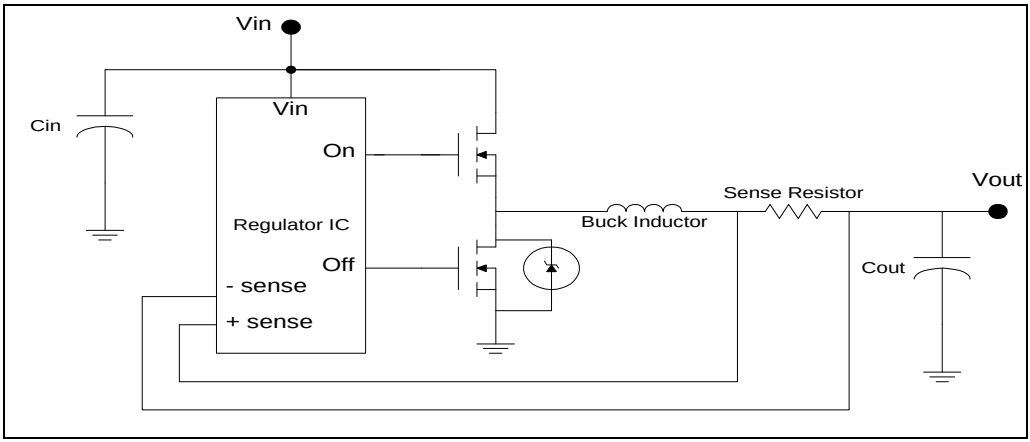

Figure 1. Basic Switching Regulator Layout

The switching regulator acts as a current-sense component, monitoring the output current at all times. The regulator derives its name from the fact that it is able to turn the output on or off, depending on the load demand. If the load demand is greater than the supplied power, the regulator turns on the top MOSFET in Table 1, allowing current to be driven through the buck inductor and to the load. In time, the output will exceed demand and the regulator turns off the top MOSFET and activates the bottom MOSFET providing a current path to ground. The output capacitor sustains the required voltage level. In order to obtain high efficiencies, the regulator supplies current about 90 percent of the time.

The current changes are detected via the sense resistor. When the voltage drop across the resistor is higher or lower than expected (relative to required output voltage), the actions described previously are performed. This voltage is sampled at the sense resistor at a pre-defined rate, known as the operating frequency (typically 150 to 400 KHz).

The transient response is proportional to the operating frequency of the switching regulator. The higher the sampling rate, the faster the part can respond to dramatic load or current changes. "A higher frequency generally results in lower efficiency because of MOSFET gate charge losses." [4] So there is an inherent trade-off between transient response and losses in efficiency. It is up to the system designer to make this decision. This document compares switching regulators operating at both 150 KHz (slower) and 250 KHz (faster). Tuned properly, these regulators typically achieve 90 percent to 95 percent efficiency.

Another concern for switching regulators is that of board space. The component count for more efficient regulators may number in the neighborhood of 20 to 25 (well above that for their linear counterparts). The added value in terms of battery life, less noise, and thermal issues, however, makes this type of regulator desirable in the mobile environment.

2.3. Critical System Parameters

This section is intended to be a reference for critical system parameters which should be considered in power supply design. These parameters will be used later in Section 4 where theoretical equations are presented which aid in bulk and high-frequency capacitor selection.

V_{CC} Tolerance	The maximum undershoot and overshoot allowed in the input voltage line.
Regulator Vin	The input voltage to the regulator - from the battery.
Regulator Vout	The output voltage of the regulator.
Regulator Efficiency	The percentage of input power converted to output power - a measure of energy efficiency.
Regulator Frequency	The frequency which the regulator samples the load current.
Regulator Tolerance	The variation on the output voltage.
Buck Inductance	The value of the inductor which supplies current to the load and controls regulator response time.
Max I_{CC}	The maximum specified load current of the CPU.
Minimum I_{CC}	The specified load current of the CPU while in StopGrant mode.
Current Slew	The maximum current change (mA/ns) at the CPU input pins.
HF Noise	The high-frequency noise in the power supply lines.

3.0. DECOUPLING CAPACITANCE

Decoupling capacitors near the CPU are necessary to handle rapid load current changes. At a time where the load demand decreases, the power supplied will be in excess for some short time. The supplied voltage level will increase until the switching regulator has a chance to lower the supplied power. Conversely, when the load demand increases, the voltage supplied will decrease for a short time. Figure 2 is an example of an increased load demand (the ESR and ESL effects are discussed later).

The reaction time governs how long it takes for the regulator to sense a change in load current. During the reaction time, depending on the CPU load, a current deficit or surplus can exist. The voltage level seen by the CPU is dependent on the size of the load and the current going through it. These changes in current require the switching regulator to either increase or decrease the supplied current to the CPU. While the regulator is 'blind,' however (during an off period of the switcher), the CPU must minimize the voltage increase or decrease. This can be done with adequate decoupling. During this time, the decoupling capacitors act as a temporary reservoir of current while the power supply is catching up with demanded current or ramping down while the demand drops.

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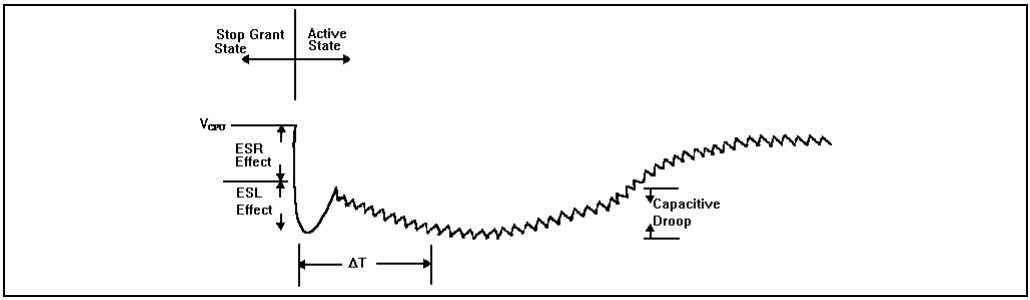

Figure 2. Power Supply Undershoot

The figure demonstrates two components of undershoot: the ESR effect and the ESL effect. Both of these effects impact bulk capacitor selection and are detailed in Section 5.2. The high frequency fluctuations are affected by the choice of high-frequency decoupling capacitors. This is discussed in the next section

3.1. High Frequency Bypass Capacitors

If significant enough, high frequency noise can violate the V_{CC} tolerance specification. This noise is caused by small variations in current over very short amounts of time. It is desirable to minimize high frequency noise with a low-pass filter at the CPU. This filter typically consists of low ESR capacitors with values of 0.1 µF and 0.01 µF. Ceramic capacitors work just fine in this regard.

Figure 3 shows a power supply with high frequency decoupling. A typical user application is running while the V_{CC2} line is sampled. The high frequency noise is minimal at 58 mV. The amount of noise should be kept as low as possible to allow greater freedom in dealing with the larger voltage fluctuations as a result of processor load changes.

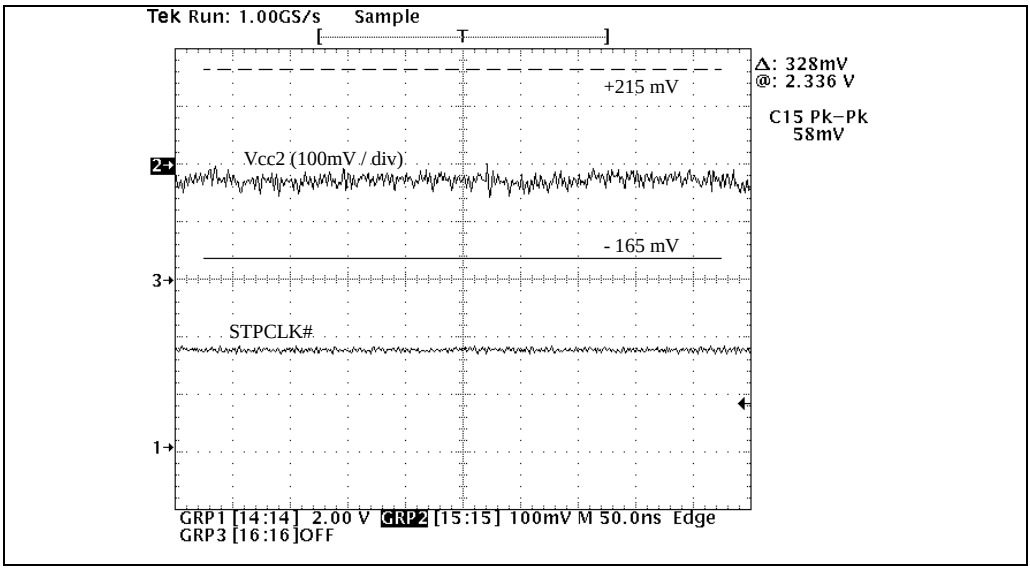

Figure 3. High Frequency V_{CC2} Noise Minimized With 8x0.1 µF and 8x0.01 µF Bypass Capacitors

3.2. Bulk Decoupling Capacitors

Bulk decoupling capacitors are needed to minimize V_{CC} transients due to large current changes during short amounts of time. In the case of a transition between the active and StopGrant states, a current change (in the case of V_{CC2}) on the order of three decades can occur. Essentially, the CPU transitions between acting as a full load to a 'no load' or vice-versa, causing a deficit, or surplus, of current relative to that in the previous state.

The power supply plays a role in reacting to such current swings. One parameter of the power supply, as described in Section 2.3, is reaction time, typically on the order of 5 to 30 µS. This parameter is determined by, among other factors, the buck inductor, switching frequency, and the design of the IC itself.

3.2.1. BULK CAPACITOR FUNCTIONALITY

The transients mentioned previously arise from large current changes over a short amount of time. The worst-case scenario, seen in Table 1, indicates a current change of approximately 3.5A in a short period of time. This, of course, is during an application which consumes maximum power. A low inductance path from V_{CC} to the capacitor material and from the capacitor material to ground is required in such power systems. This minimizes the transients associated with load changes. Low ESR (effective series resistance) and low ESL (effective series inductance) capacitors provide such a path and minimize transient effects.

In Figure 2, a hypothetical example shows a transition between 'no load' (StopGrant) and full load (active). Here the current demand by the CPU exceeds the instantaneous supply of current delivered by the power supply. As a result, the net supply voltage decreases. The bulk capacitors must 'filter' the voltage drop so it is minimized. Without such capacitors, the capacitive droop will exceed tolerance. Therefore it is critical that the system designer be assured that the bulk capacitance placed at the CPU is adequate to handle such current changes.

Two other effects are shown in Figure 2 as well: the ESR effect and the ESL effect. These are two parameters that the system designer should control to reduce the effects of the capacitive droop. No capacitor is ideal, of course, and each capacitor has some resistive effects. The larger the ESR of the capacitor, the larger the capacitive droop. Ideally ESR should not play a role as it decreases the margin for error in voltage tolerance levels.

The ESL effect also demonstrates the non-ideal nature of the capacitor and is caused by the parasitic inductance of the capacitor. An inductor has a voltage level governed by the following equation:

$$V = L\frac{dI}{dt}$$

The larger the change in current, the more pronounced the effect on capacitive droop. The system designer should select low ESL capacitors which minimize these effects. The ESL effect, the ESR effect, and the capacitive droop are overcome once the power supply reacts and begins to supply the required current.

3.2.2. RELEVANT THEORY

It is possible to work through a back of the envelope calculation with regard to the bulk and high frequency decoupling capacitors required. This should not act as a substitute for real laboratory data.

The first important notion is that of regulator response time. This has two components: the detection time and the reaction time. The regulator operates in a switching mode, sampling the current output at a fixed frequency. There exists a lag between the time the current output is in surplus or deficit and the time that the regulator senses this condition. This is known as the **detection time**. After the regulator senses a current change and attempts to compensate, the correction time is limited by the buck inductor and the magnitude of the current change in the state transition. This is the **reaction time**. The relevant equations are shown below:

Detection Time:

$$V = L\frac{dI}{dt}$$

$$t_r = L_B\frac{\Delta I}{\Delta V}$$

L_B is the value of the buck inductor, delta I is the current change associated with a state change, and delta V is the Vin minus the Vout of the power supply. This detection time, it should be noted, is regulator-dependent, and this equation for **reaction time** may not necessarily apply. For confidence, consult with the vendor for the value of the reaction and detection time of the regulator in the specific circuit.

For some configurations, the reaction time can be found as follows:

Reaction Time:

$$t_d = \frac{1 - \frac{V_{OUT}}{E_R V_{IN}}}{f_R}$$

Where E_R is the efficiency of the regulator and f_R is the operating frequency of the regulator.

The total response time of the regulator can be found by adding detection time and reaction time together. The response time plays a large role in determining the amount of bulk capacitance required.

The next step in the scratch-pad calculation of bulk capacitance required is in budgeting values for in-series resistance voltage drop and the drop associated with parasitic inductance, referred to as *voltage droop*. These values give a percentage of the operating margin to which the ESR and ESL values may contribute to voltage swings. The budget values are determined by allocating a part of the tolerance margin minus the system noise (also add an allowance for the tolerance of the regulator) to each component, usually a 60/40 ratio.

The total budget is found as follows:

$$budget = V_{CCtol} - V_{in} T_r - \frac{N_{pp}}{2}$$

Here, N_{pp} is the peak-to-peak noise inherent in the system. This typically falls in the range of 40 to 50 mV. T_r is the regulator tolerance, how inclined the regulator is to maintain the output voltage under normal conditions. The V_{CC}tol is the published specification for V_{CC} tolerance.

Once the calculation has been made the cushion for error in the voltage levels is known. Assign approximately 60 percent of this value to the in-series resistance budget (to allow for ESR in the capacitors) and 40 percent for ESL. The **maximum ESR**, the **capacitance needed**, and the **maximum ESL** can be determined from these values. They are calculated as follows:

$$ESR_{\max} = \frac{V_{ESR}}{\Delta I}$$

$$C = \frac{\Delta I\left(t_r\right)}{V_{CAP}}$$

$$L = V_{CAP}\left(\frac{dI}{dt}\right)^{-1}$$

Here, the maximum ESR is found using Ohm's law with the budgeted value for in-series resistance voltage drop. This value, when found, refers to the capacitor array as a whole. When using multiple capacitors the ESR rating of each individual capacitor should be determined. This value should be less than or equal to the value found above.

The capacitors' value is a function of the regulator response time (t_r), the current change associated with a state change, and the budget for capacitance droop (or parasitic inductance). This capacitance refers to the entire array, so treat multiple capacitors as capacitors in parallel – their values add. The inductance is found by multiplying the budgeted value for capacitor droop by the maximum current slew at the input pins of the processor (maximum current change per unit time).

These values should be used to provide a ballpark figure for decoupling requirements. They do not offer a substitute for actual laboratory data.

3.3. Recommended Materials

The type of capacitor used in both high frequency and bulk decoupling is critical. In the case of high-frequency capacitors, the ESR and ESL effects do not weigh as heavy due to the relatively small fluctuations in voltage levels. With this in mind, ceramic capacitors are recommended. This allows for a small form factor with adequate functionality. These capacitors should be placed as close as possible to the CPU with a wide trace to reduce any trace resistance or inductance. This document assumes the reader is familiar with such layout issues.

The capacitors used in decoupling for the core voltage should have low ESR and ESL values. The ESR values should be readily available in datasheets, but the values for ESL are not as attainable. Tantalum capacitors were used for the research of this document. These offer both low ESR and ESL and have no known wear out mechanisms. This translates into long life and no depreciation in performance as seen in older electrolyte capacitors. Appendix B lists vendors who manufacture low ESR / ESL capacitors.

Both ceramic and tantalum capacitors retain their low ESR at high frequencies without degradation. The ESR and ESL values determine how well the capacitor can source current. Surface mount packages should be utilized to minimize lead inductance. Design permitting, OSCON capacitors are also good choices for bulk capacitors. Their height, however, may limit usage.

4.0. TESTING METHODOLOGY AND PROCEDURE

This section documents the experimental platform used to verify the theoretical bulk and high-frequency capacitance recommendations. It is not intended to be used as a reference design nor does it imply any vendor-specific recommendations.

The testing procedure has been designed to isolate the CPU as much as possible from external performance factors. In doing so, measurements taken more closely reflect the effects of the CPU itself and not of the power supply or the system board. It is important to keep in mind that these factors may come into play on individual designs.

4.1. Reference Platform

Throughout data collection, the goal was to simulate the mobile environment as much as was practical and to place maximum demands on the CPU. An internal testing platform was used with a TCP (Tape Carrier Package) to SPGA (Staggered Pin Grid Array) interposer card. The interposer card held the TCP CPU and provided access to the STPCLK#, V_{CC2}, and V_{CC3} signals. Two switching-regulator power supplies were placed near the CPU and were connected by thin, two-inch wires to the power supply inputs. This setup essentially turns the power supply into a ‘black box.’ The longer wires introduce extra noise and minimize the effects of the output capacitance of the power supply with respect to the CPU. This, in turn, adds to the demands on the CPU decoupling. In a system design, a wide, short path from the power supply to the CPU is needed to minimize the IR drop. Figure 4 shows this setup.

The bench power supply was tuned to supply 5.5V to each switching regulator. The regulators used are based on the LTC1435 from Linear Technology. The DC094 demonstration board is a typical switching regulator implementation available from Linear Technology. Although the mobile Pentium processor with MMX technology nominal voltage is 2.45V, the regulators supplied 2.45 V and 3.3 V to the V_{CC2} and V_{CC3} via jumpers on the interposer card. The TCP part was then connected to the motherboard via the interposer card to the SPGA interface.

150 MHz CPU’s were used operating in a typical range on a 82430MX system equipped with 8 MB of RAM and no L2 cache. A Tektronix TLS 216 logic scope was used for data collection. The scope probes were connected to capacitor pads directly under the processor with minimal ground loop.

Table 2 summarizes the platform configuration.

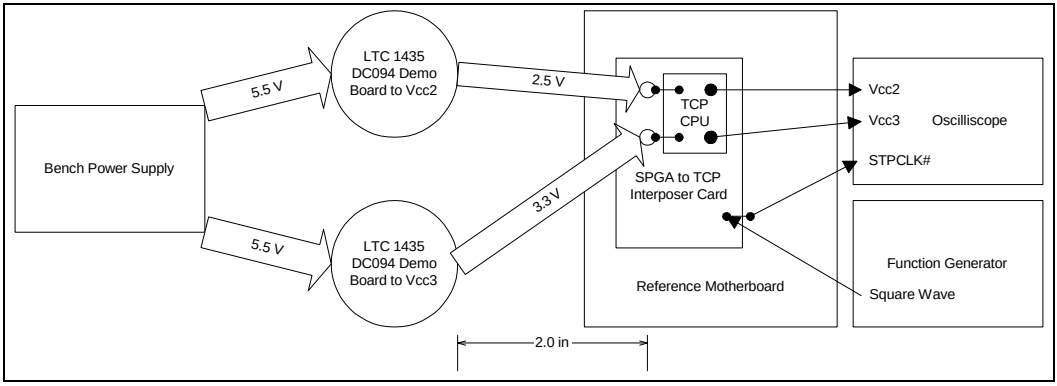

Figure 4. System Configuration

Table 2. Experimental Platform

Component	Description
Processor	P55CLM
Speed	150 MHz
Platform	Testing platform with TCP to SPGA interposer card
Chipset	82430MX
Memory	8 MB, no L2 cache
Measuring Device	Tektronix TLS 216 Logic Scope
Switching Regulator	LTC1435 @ 250, 150 KHz

4.2. Data Collection

To fully validate the amount of bulk and high-frequency bypass capacitance used, V_{CC2} and V_{CC3} must be measured during a transition between a large load and a small load. This can be accomplished in a number of ways. The procedure utilized in this report follows.

The placement of the oscilloscope probes is critical for accurate data collection. The probes must be placed as close as possible to the CPU power pins as possible to avoid introducing error into the measurements if the path to the probes is too long. This error may be in the form of trace inductance or resistance. Ideally, the probes should be soldered to a wide trace devoid of right-angle turns. In addition, the ground loop should be as small as possible.

In order to force the processor to draw a large amount of current in the active mode, a high power application code was loaded and executed. This code (hi_pwr2.exe) is known to draw a large amount of power. A brief description can be found in Appendix D. Any code or program that is known to consume higher than normal power may be used (such as MS-DOS* Edit). While the processor is in this state, a function generator manually toggled the STPCLK# pin at a frequency of 5000 Hz, forcing state transitions to and from StopGrant. It may also be useful to collect data while the system runs a typical user application. Some benchmarking utilities simulate this type of environment.

Toggling the STPCLK# pin forces the processor in and out of the StopGrant state. Trigging on a high-to-low transition shows the transient related to entering StopGrant. In this case, the CPU enters StopGrant after the currently executing bus cycle. As the CPU requires significantly less current in this state, the V_{CC} levels can be expected to rise as the power supply is fully capable of supplying the required voltage under a 'no-load' condition.

Triggering on a low-to-high transition shows the transient related to exiting StopGrant. Here, the processor enters the active state and begins executing the high power code once again. Essentially, the processor transitions between 'no-load' and 'full-load.' The voltage levels are expected to dip somewhat as the power supply compensates for the increased current demand.

The critical measurements must be taken directly at either transition (a rising or falling edge of STPCLK#). Any spikes in the V_{CC} line or significant over or undershoot are likely to occur a short amount of time after the transition. Readings, therefore, should be taken at a very high sampling rate. For this document, most readings were taken at one giga-sample per second. This allowed for a 250 ns window to examine the transient just after the transition. To view a larger picture which shows the full state transition, switch to a lower sampling rate which allows a full period of the STPCLK# signal to be seen. This gives the assurance that voltage levels on a larger scale do not exceed tolerance.

5.0. PRESENTATION OF DATA

This section details the data collected under the methodology described in Section 4. The first section details data collected with a 250 KHz switching regulator. The second section presents data collected with 150 KHz regulators. Both were measured with adequate bulk and high frequency bypass capacitance. The third section briefly documents data taken with inadequate capacitance. In all figures, C15 refers to V_{CC2} and C16 refers to V_{CC3}. GRP2 refers to V_{CC2} and GRP3 refers to V_{CC3}. By examining the measurements to the right and bottom of the display with the above assignments in mind, the minimum, maximum and scale of the wave forms can be determined.

5.1. 250 KHz Switching Regulator

Data in this section was collected with the following bypass capacitance (manufacturers and product codes may be found in Section 6):

V_{CC2} Bulk:	4 x 100 µF
V_{CC3} Bulk:	1 x 33 µF
V_{CC2} High Frequency:	7 x 0.1 µF, 8 x 0.01 µF
V_{CC3} High Frequency:	4 x 0.1 µF, 4 x 0.01 µF

Figure 5 demonstrates that V_{CC3} remains well within tolerance of the minimum value of V_{CC3}, 80mV below 3.3V. The specification, of course, is for a +215mV/-165mV deviation.

In Figures 5 and 6, the V_{CC2} and V_{CC3} wave forms lie within tolerance. These wave forms were collected while executing the high power code and represent a worst-case scenario. Such deviations may or may not be seen in typical user applications. These wave forms, however, should offer confidence in the recommended values for decoupling capacitance.

The maximum deviation from tolerance in Figure 7 is 88 mV and 24 mV for V_{CC2} and V_{CC3}, respectively. The figures indicate that the processor voltage requirements are met in general during both state transitions.

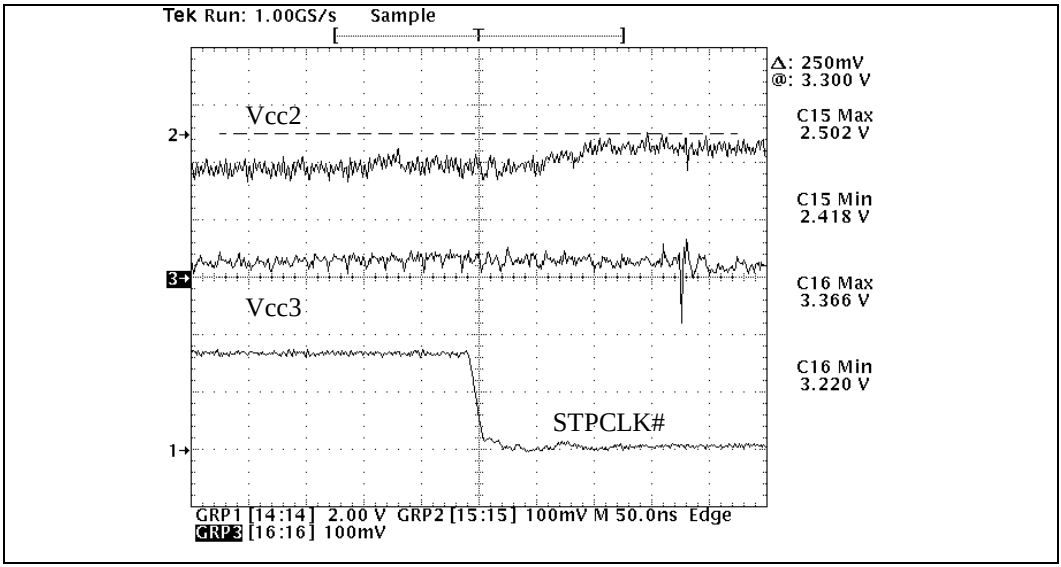

Figure 5. 250 KHz Regulator Entering StopGrant

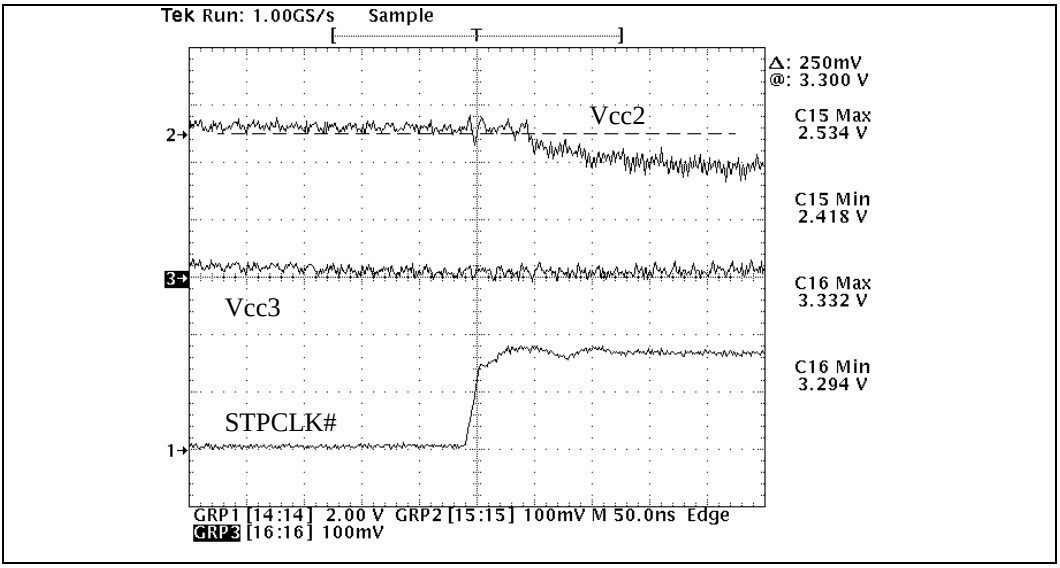

Figure 6. 250 KHz Regulator Exiting StopGrant

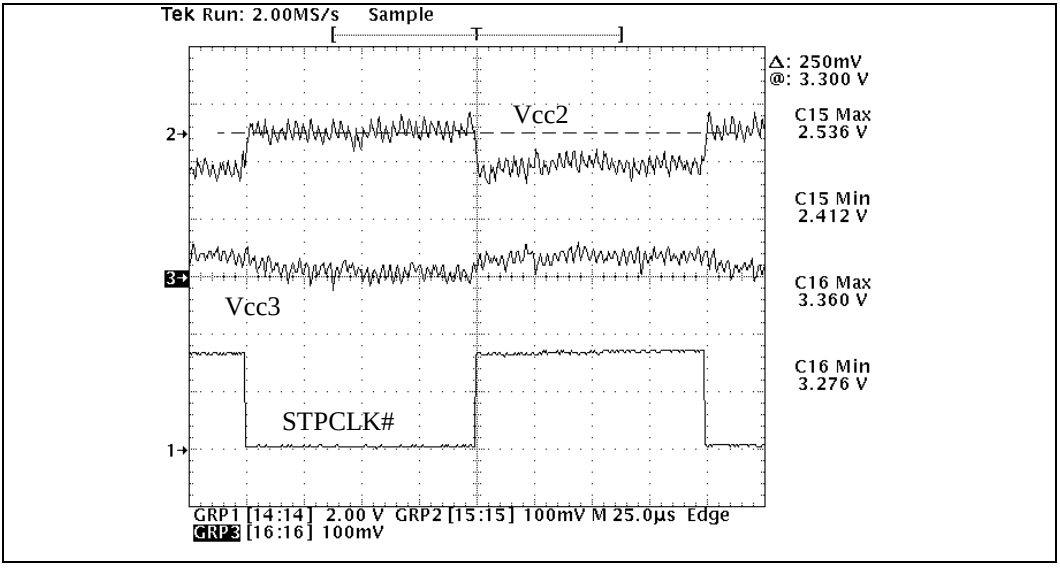

Figure 7. 250 KHz Regulator Toggling States

5.2. 150 KHz Switching Regulator

The data in this section was taken with the same capacitor array as in Section 5.1, but with a 150 KHz regulator. As the speed of the switching regulator decreases, slower response times are expected. This translates into larger voltage droops and slower settling times. The data in this section supports such an expectation.

In this data the tolerance specifications are also met. Consider the processor entering StopGrant at a small time scale. Figure 8 shows, at a 50 ns/division range, the spike seen approximately 180 ns after the transition of STPCLK# to the active level. The spike is of the same order of magnitude as seen in Figure 5. It is within tolerance, however, as is probably associated more with the testing platform than the processor itself.

Other than the above abnormality, the data is quite acceptable. Both V_{CC2} and V_{CC3} lie within tolerance in all cases. This data, then, can be considered as a base case upon which to build individualized decoupling solutions. It is important to realize that the data in these two sections do not necessarily reflect a normal system. It is platform specific and merely serves as a starting point for OEM designs.

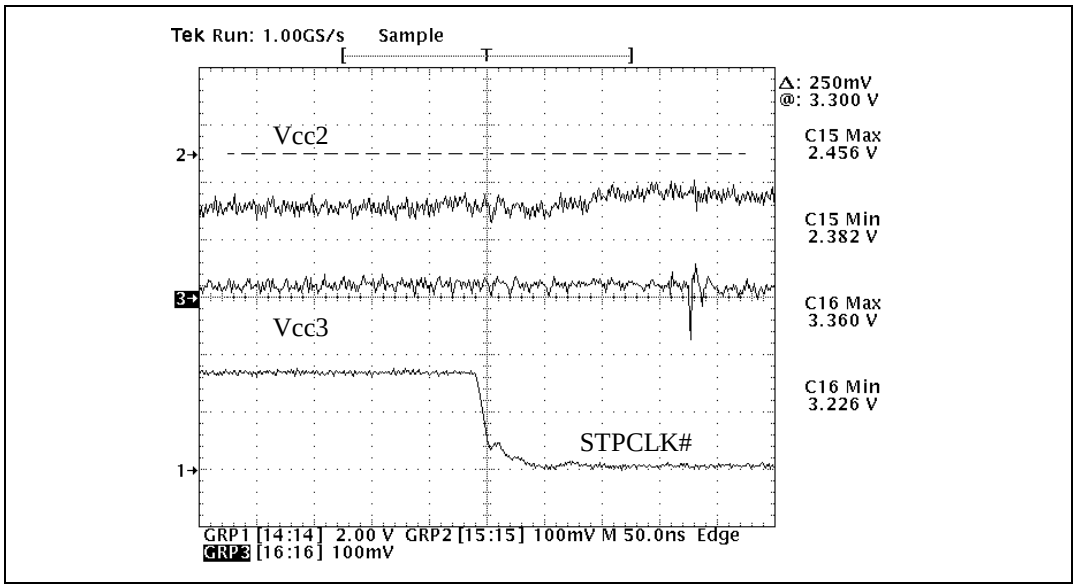

Figure 8. 150 KHz Regulator Entering StopGrant

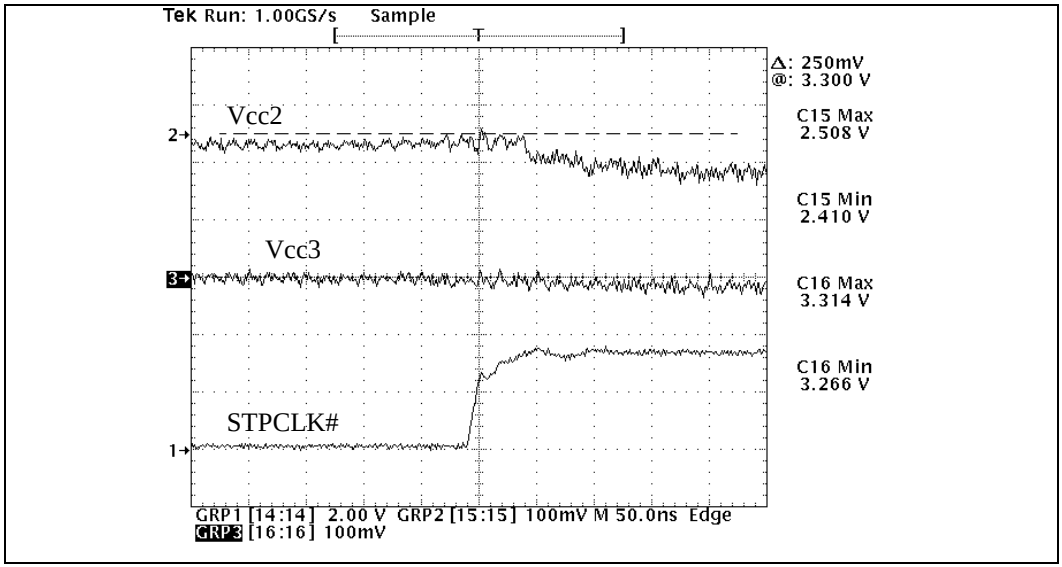

Figure 9. 150 KHz Regulator Exiting StopGrant

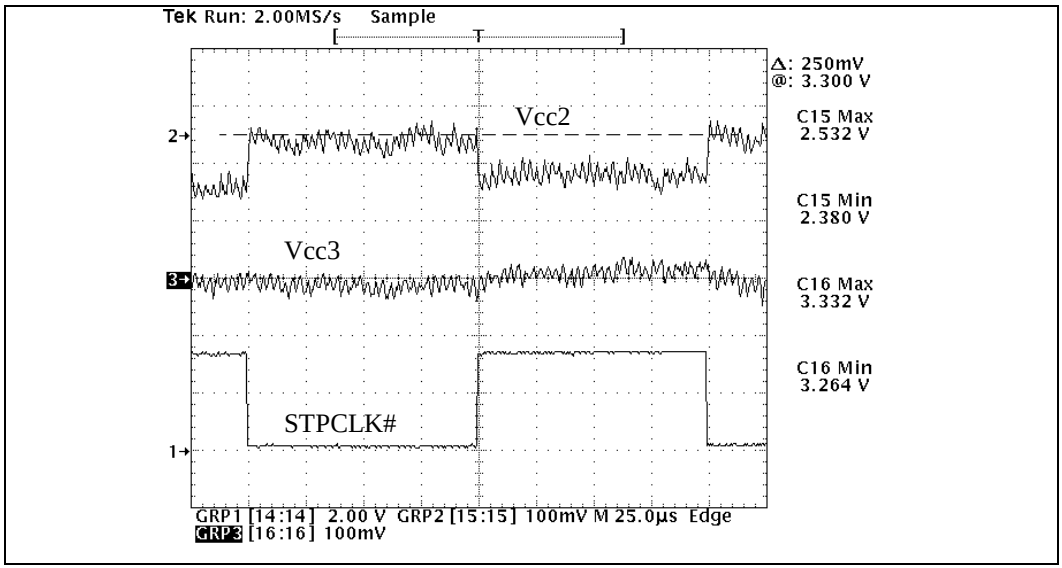

Figure 10. 150 KHz Regulator Toggling States

5.3. Other Data

This section is intended to provide a reference worse than the case detailed above. The levels of bulk capacitance are decreased as are the number of high frequency capacitors in order to demonstrate the effects of minimal decoupling. In the first scenario, the bulk decoupling on V_{CC2} is decreased by one-half and the high-frequency decoupling on V_{CC3} is decreased by the same amount. In the second scenario, all bulk decoupling capacitors are removed.

5.3.1. 250 KHZ REGULATOR MINIMAL DECOUPLING CAPACITORS

In this scenario, the values for the decoupling capacitors are as follows:

V_{CC2} Bulk:	2 x 100 µF
V_{CC3} Bulk:	1 x 33 µF
V_{CC2} HF:	7 x 0.1 µF, 8 x 0.01 µF
V_{CC3} HF:	2 x 0.1 µF, 2 x 0.01 µF

Figure 11 shows the processor entering StopGrant while Figure 12 shows the processor exiting StopGrant. Figure 13 shows both state transitions.

Given that this is a representative system and a typical processor, the data indicates that the values for bulk decoupling on V_{CC2} are very close to exceeding specifications. Figure 13 shows an undershoot of 140 mV and an overshoot of 112 mV. Initially, it may seem as though system board space may be saved by incorporating this particular capacitor array. However, system variations may lead to scenarios where the tolerance specification cannot be met. As a result, it is not recommended that this configuration be used.

The changes in high frequency bypass capacitance in V_{CC3} do not cause the tolerance specifications to be exceeded. The data does indicate that the trend is toward more dramatic fluctuations in voltage (as seen in Figure 13). If the system designer wishes to lower the high frequency bypass capacitance, this should be analyzed with reference to individual designs.

One important observation to make regarding V_{CC3} is applicable to leakage currents. System noise is a function of the voltage difference between V_{CC2} and V_{CC3}. The data in the previous sections suggest that the high-frequency component of V_{CC3} can be tightly coupled. As a result, the level of V_{CC3} may be reduced such that the tolerance specification is met but V_{CC3} is targeted at slightly below 3.3V. If the high frequency decoupling capacitance is reduced significantly, this may no longer be an option.

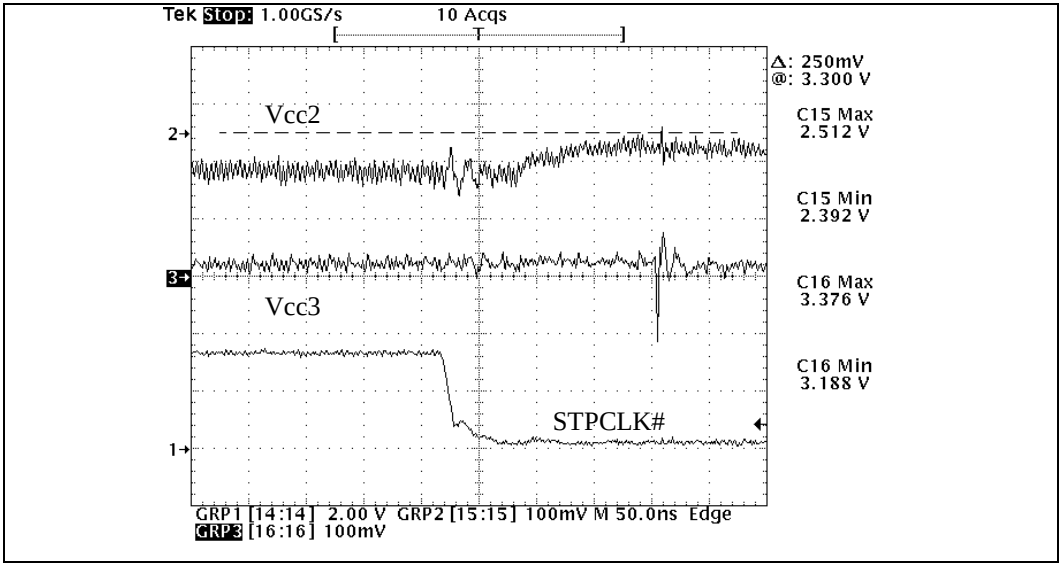

Figure 11. 250 KHz Data Entering StopGrant With Decreased Bulk, High Frequency Bypass Capacitance

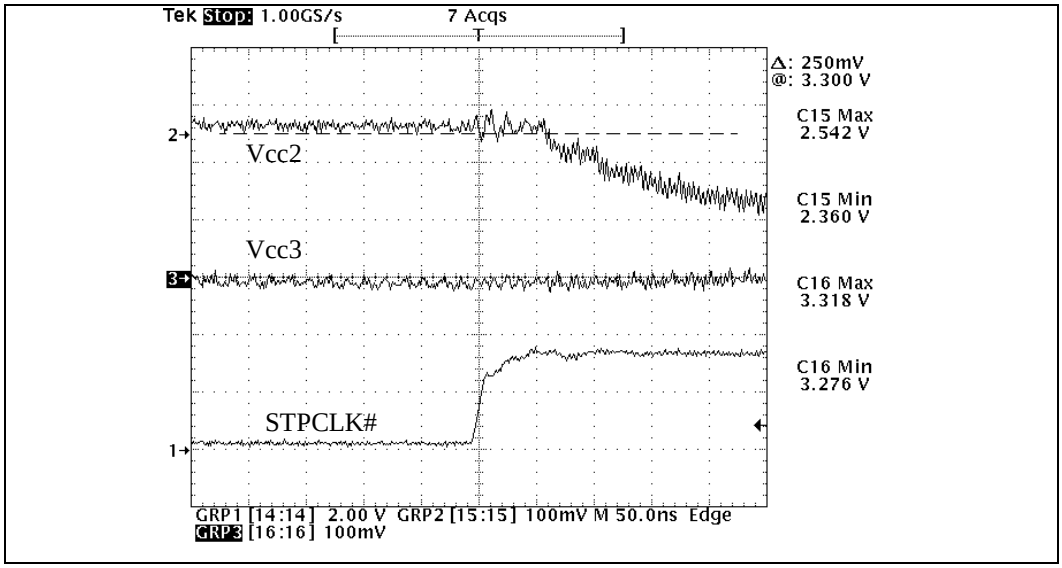

Figure 12. 250 KHz Data Exiting StopGrant With Decreased Bulk, High Frequency Bypass Capacitance

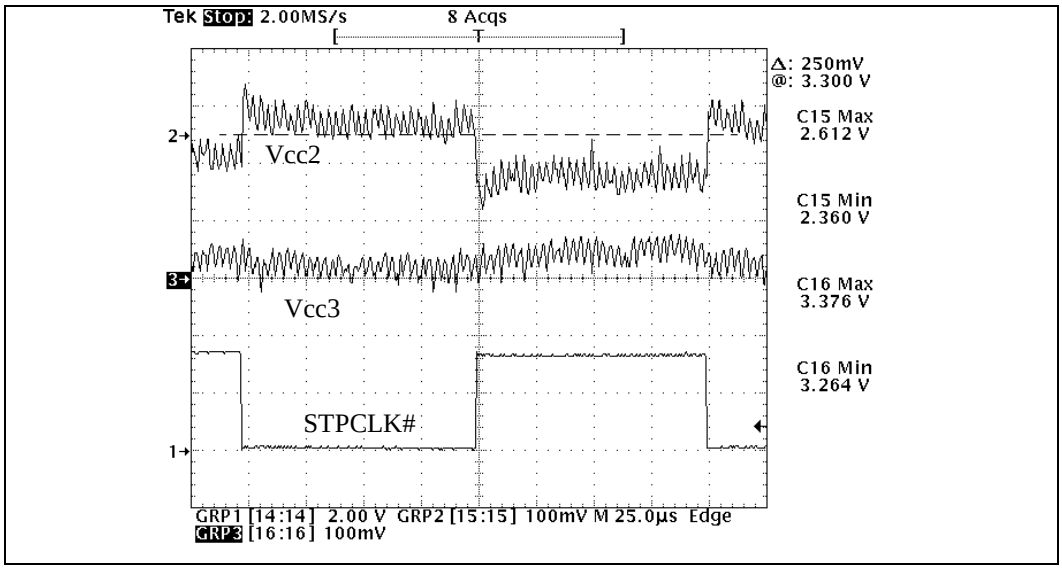

Figure 13. 250 KHz Data Toggling States With Decreased Bulk, High Frequency Bypass Capacitance

5.3.2. 250 KHZ WITHOUT DECOUPLING CAPACITORS

In this section, data is presented which has been collected without the use of any bulk decoupling capacitors. The effect is quite dramatic and serves to show the overall importance of such capacitors. It also shows the independence of the CPU decoupling from the output capacitance of the power supply. The data shows the processor entering and exiting StopGrant and shows the voltage levels on both V_{CC2} and V_{CC3} exceeding tolerance by a significant margin.

The high frequency capacitors remain the same and play no significant role in keeping the voltage levels at tolerance. Primarily, this data serves to demonstrate that the output capacitance at the power supply does not play a large role in keeping the processor's voltage within tolerance. Instead, it is intended to sustain the power supply output during the times at which the regulator is switched off.

In Figure 14, V_{CC2} rises to 3.26 volts, which is 595 mV above the maximum voltage allowed in tolerance. In Figure 15, V_{CC2} is as low as 1.812 volts. This is 523 mV under the minimum allowed voltage. With this data, it becomes clear that V_{CC2} requires careful consideration in terms of decoupling.

V_{CC3}, on the other hand, does not demonstrate fluctuations as severe as V_{CC2}. It is important to remember that V_{CC3} consumes only 10 percent of steady-state power in the CPU itself and will not be as affected by state transitions as V_{CC2} is. Operating without bulk decoupling capacitors is **not recommended**.

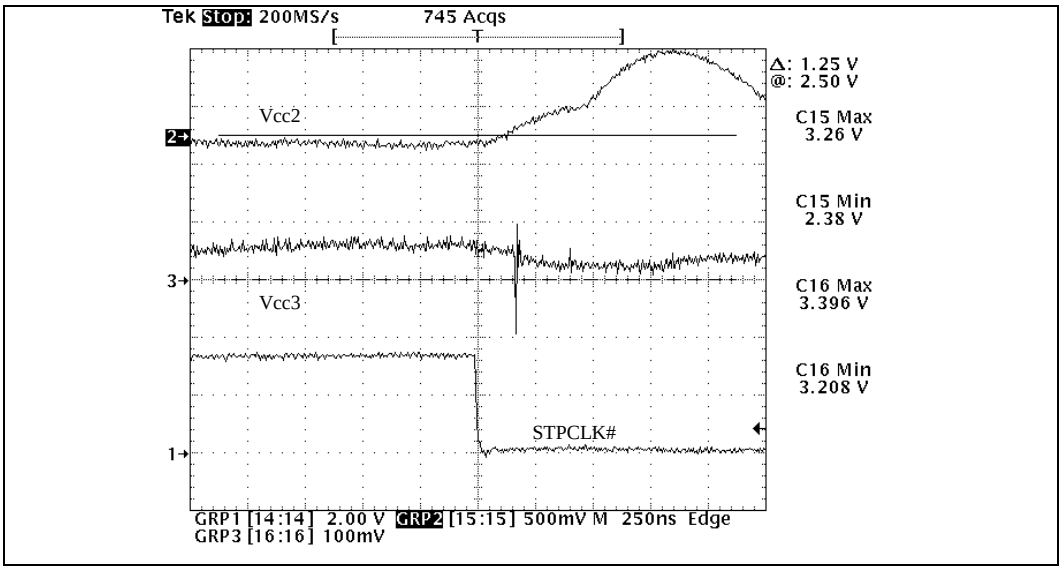

Figure 14. Entering StopGrant Without Bulk Decoupling Capacitors

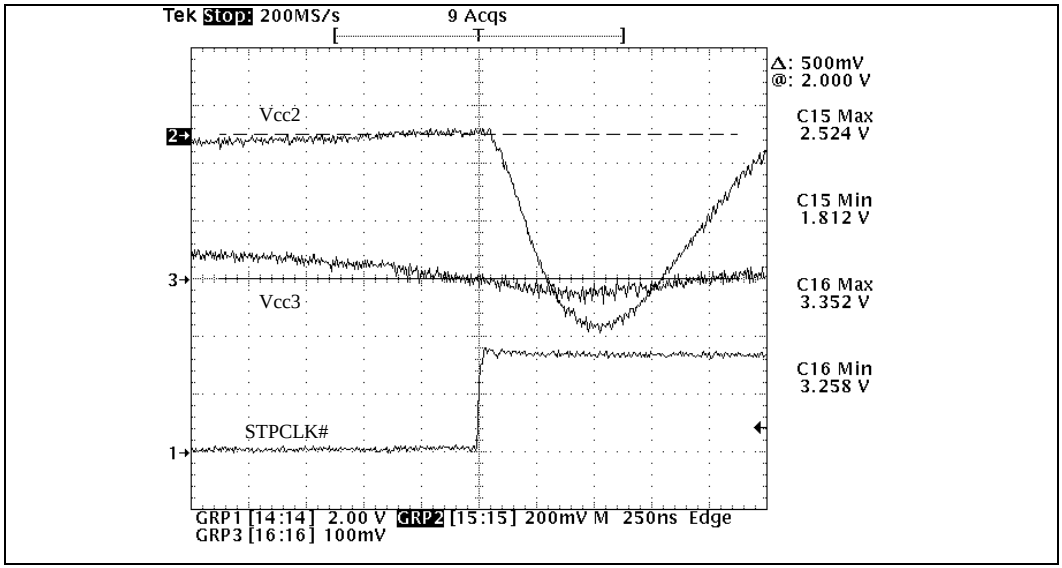

Figure 15. Exiting StopGrant Without Bulk Decoupling Capacitance

6.0. SUMMARY AND CONCLUSIONS

It is possible to meet the V_{CC2} and V_{CC3} tolerance specifications following the steps outlined in this application note. The recommended values are small enough to consume minimal board space but offer confidence with a wide margin for error. The scenarios illustrated in this document show the importance for careful consideration of the values for bulk and high frequency decoupling and support the notion that they are system-dependent in many ways.

For the P55C-150MHz, the bulk decoupling capacitors recommended for V_{CC2} are four 100 µF tantalum capacitors. They offer low in-series resistance and parasitic inductance. For V_{CC3}, one 33 µF tantalum capacitor is recommended. On the other hand, high frequency decoupling is very system-specific. An array of 0.1 and 0.01 µF ceramic capacitors is recommended. For V_{CC2}, 7 x 0.1 µF and 8 x 0.01 µF capacitors were used. For V_{CC3}, 4 x 0.1 µF and 4 x 0.01 µF capacitors were used. For the P55C-166MHz, our analysis indicates that five 100 µF bulk capacitors should suffice. These recommendations are summarized in Table 3. The exact manufacturers and product codes used are shown in Appendix C.

When a capacitor array is chosen, it is important to test under a variety of conditions. These tests focused on the worst-case scenario: a transition between full-load and no-load in terms of the CPU. The capacitors should also be tested in typical user applications: boot-up, shut-down, etc. It is also important to keep in mind that the amount of decoupling capacitance is largely determined by the switching regulator used. Some regulators operate at a higher frequency than others or are inherently more efficient. Be sure to check with your power supply vendor for any specific instructions.

Table 3. Recommended Decoupling Capacitor Values

Component	0.01 µF Capacitors	0.1 µF Capacitors	Bulk Capacitors
150 MHz V_{CC2}	8	8	4 x 100 µF
150 MHz V_{CC3}	4	4	1 x 33 µF
166 MHz V_{CC2}	8	8	5 x 100 µF
166 MHz V_{CC3}	4	4	1 x 33 µF

Appendix A - Bibliography

- *Pentium® Processor With Voltage Reduction Technology: Power Supply Design Considerations for Mobile Systems*, Application Note AP-519, Order Number 242558-001, May 1995.
- *Pentium® Processor (610\75) Power Supply Considerations for Mobile Systems*, Application Note, Order Number 242415, October 1994.
- *Pentium® Processor (610\75) Design Considerations for Mobile Systems*, Application Note AP-518, Order Number 242417-001, October 1994.
- *Linear Technology, LTC 1435 High Efficiency Low Noise Synchronous Step-Down Switching Regulator*, Datasheet, April 1996.
- *Linear Technology, Demo Manual DC094 Design Ready Switcher: LTC1435 Constant Frequency Synchronous DC/DC Converter*, Manual.
- *Basic Tantalum Capacitor Technology*, Gill, John, AVX Ltd., Tantalum Division, Paignton, England.

Appendix B
Vendors Providing Voltage Regulators and Capacitors

The list below is meant to be representative only, and does not include all vendors of a particular type. Intel has not tested all of the components listed below and cannot guarantee that these components will meet every PC manufacturers specific requirements.

Voltage Regulators:

Linear Technology Corporation
1630 McCarthy Blvd.
Milpitas, CA 95035-7487
Tel. (408) 432-1900
Maxim Integrated Products
120 San Gabriel Drive
Sunnyvale, CA 94086
Tel. (408) 737-7600

Siliconix, Inc.
2201 Laurelwood Road
Santa Clara, CA 95054-1595
Tel. (800) 554-5565

Decoupling Capacitors:

AVX Corporation TPSE Series
Myrtle Beach, South Carolina 29577 USA

Digi-Key Corporation
701 Brooks Avenue South
Thief River Falls, MN 56701-0677
Tel. (218) 681-6674

KEMET Electronics Corporation T Series
P.O.Box 5928
Greenville, South Carolina 29606 USA
Tel. (803) 963-6348

Nichicon (American) Corporation PL Series
927 East State Parkway,
Schaumburg, Illinois 60173 USA

Sanyo Video Components OS-CON Series
2001 Sanyo Ave.
San Diego, California 92073 USA
Tel. (619) 661-6835

Appendix C
Bulk and High Frequency Capacitors Utilized in Experimentation

Type	Material	Vendor	Product Code	Package	Capacitance	Volts	ESR
Bulk	Tantalum	AVX	107	D	100 µF	10 V	0.9 ohm
Bulk	Tantalum	AVX	336	D	33 µF	16 V	0.9 ohm
HF	Ceramic	Digikey	---	SMT_805	0.01 µF	---	---
HF	Ceramic	Digikey	---	SMT_805	0.1 µF	---	---

Appendix D
High Power Application Code (hi_pwr2.exe) Operating Instructions and Details

Operating Instructions:

The hi_pwr2.exe contains a short loop of Intel Architecture intensive code. This code uses the most power of any stable, MS-DOS executable program that Intel has tested on Pentium processors with MMX technology.

This code has been optimized for use only with Pentium processors with MMX technology. Any power testing on a Pentium processor should be done with the old hi_pwr.exe (STR4Y) code.

To use this code for V_{CC} transient analysis:

1. Execute the code
2. While the code is executing, toggle the STPCLK# signal (i.e. with a frequency generator since the code itself will not toggle STPCLK#)
3. Measure the noise transients as described in this document.

Since this program runs in an infinite loop and disables all interrupts, a hard reboot of the system is necessary to exit out of the code.

If you have any questions, please contact your local Intel representative.