IBM 486DX2 - V MICROPROCESSORS
486DX2 Style CPUs with 8K Write-Back Cache, On-Chip FPU, Advanced Power Management, and 3 Volt Technology

IBM Microelectronics

Addendum to BL486DX/DX2 Data Book

1. OVERVIEW

This addendum to the IBM 486DX2 Data Book documents product improvements for the IBM 486DX2 series of IBM CPUs. Specifications in this addendum are valid for the clock-doubled IBM 486DX2-V devices only. Major product features include:

- Core speeds up to 80 MHz
- 3 Volt process technology
- 5 Volt tolerant I/O
- 8 KByte write-back cache
- Burst write capability
- IBM system management mode with programmable SMM pin interface
- Low-power suspend mode
- 168-pin PGA, 208-pin QFP packages
-
-

2. Electrical Specifications

The electrical specifications listed in this addendum replace the electrical specifications presented in the IBM 486DX2 Data Book for the IBM 486DX2-V and reference the same notes and drawings.

2.1 Absolute Maximum Ratings

The following table lists absolute maximum ratings for the IBM 486DX2-V microprocessors. Stresses beyond those listed under Table 2-1 limits may cause permanent damage to the device. These are stress ratings only and do not imply that operation under any conditions other than those listed under Table 2-2 ,"Recommended Operating Conditions" is possible. Exposure to conditions beyond Table 2-1 may (1) reduce device reliability and (2) result in premature failure even when there is no immediately apparent sign of failure.

Table 2-1. IBM 486DX2-V Absolute Maximum Ratings

PARAMETER	MIN	MAX	UNITS	NOTES
Case Temperature	-65˚	+91 (PGA)˚	C	Power Applied
	-65˚	+87 (QFP)˚	C	Power Applied
Storage Temperature	-65˚	+150˚	C	No Bias
Supply Voltage, V_{CC}	-0.5	4.5	V	With Respect to V_{SS}
Voltage On Any Pin	-0.5	6.0*	V	With Respect to V_{SS}
Input Clamp Current, I_{1K}		10	mA	Power Applied
Output Clamp Current, I_{OK}		25	mA	Power Applied

*Note: The maximum "Voltage On Any Pin" for IBM 486DX2-V devices with a stepping ID below 10h is Vcc+0.5volts; for devices with stepping IDs greater than 10h, the maximum voltage is 6.0 volts, as shown. (The stepping ID for a IBM 486DX2-V CPU can be found by reading the DIR1 configuration register.)

2.2 Recommended Operating Conditions

Table 2-2 presents the recommended operating conditions for the IBM 486DX2-V device.

Table 2-2. IBM 486DX2-V Recommended Operating Conditions

PARAMETER	PGA (-GP)		QFP (-QP)		UNITS	NOTES
	MIN	MAX	MIN	MAX		
T_C Case Temperature	0˚	+85˚	0˚	+85˚	C	Power Applied
V_{CC} Supply Voltage						
50 MHz (3.3V)	3.00	3.60	3.00	3.60	V	With Respect to V_{ss}
66 MHz (3.3V)	3.15	3.45	3.15	3.45	V	With Respect to V_{ss}
66 MHz (3.45V)	3.30	3.60	3.30	3.60	V	With Respect to V_{ss}
66 MHz (3.6V)	3.45	3.75	3.45	3.75	V	With Respect to V_{ss}
80 MHz (4.0V)	3.80	4.20	-	-	V	With Respect to V_{ss}
V_{IH} High Level Input	2.0	5.5	2.0	5.5	V	*Note
V_{IL} Low Level Input	-0.3	0.6	-0.3	0.6	V	
I_{OH} Output Current (High)		-1.0		-1.0	mA	$V_{OH}=V_{OH(MIN)}$
I_{OL} Output Current (Low)		3.0		3.0	mA	$V_{OL}=V_{OL(MAX\}}$

*Note: V_{IH} specification shown for the IBM 486DX2-V applies to devices with stepping IDs of 10h and greater (DIR1 configuration register). IBM 486DX2-V devices with a stepping ID of less than 10h require a $V_{IH}(max) = V_{CC}+0.3$ volts.

2.3 DC Characteristics

Table 2-3. IBM 486DX2-V DC Characteristics
(at Recommended Operating Conditions)

PARAMETER	PGA (-GP)		QFP (-QP)		UNITS	NOTES
	MIN	MAX	MIN	MAX		
V_{OL} Output Low Voltage I_{OL} = 3 mA		0.45		0.45	V	
V_{OH} Output High Voltage I_{OH} = -1 mA	2.4		2.4		V	
I_{LI} Input Leakage Current For all pins except those listed in Table 4-1.		15		15	µA	$0 < V_{IN} < V_{CC}$
I_{IH} Input Leakage Current For all pins with internal pull-downs.		200		200	µA	V_{IH} = 2.4 V See Table 4-1.
I_{IL} Input Leakage Current For all pins with internal pull-ups.		-400		-400	µA	V_{IL} = 0.45 V See Table 4-1.
I_{CC} Active I_{CC}	Typical:		Typical:			Note 1,5
50 MHz (3.3V)	325	555	325	555	mA	
66 MHz (3.3V)	350	650	350	650		
66 MHz (3.45V)	375	665	375	665		
66 MHz (3.6V)	400	675	400	675		
80 MHz (4.0V)	570	885	-	-		
I_{CCSM} Suspend Mode I_{CC}	Typical:		Typical:			Note 1, 3
50 MHz (3.3V)	12	26	12	26	mA	
66 MHz (3.3V)	13	30	13	30		
66 MHz (3.45V)	13	30	13	30		
66 MHz (3.6V)	14	30	14	30		
80 MHz (4.0V)	16	34	-	-		
I_{CCSS} Standby I_{CC} (Suspend/CLK Stop)	Typical:		Typical:			
0 MHz (3.3V)	2.0	6.0	2.0	6.0	mA	Note 4
0 MHz (3.45V)	2.0	6.0	2.0	6.0		
0 MHz (3.6 V)	2.0	6.0	2.0	6.0		
0 MHz (4.0 V)	2.0	10.0	2.0	10.0		
C_{IN} Input Capacitance		20		20	pF	f_c = 1 MHz (Note 2)
C_{OUT} Output or I/O Capacitance		20		20	pF	f_c = 1 MHz (Note 2)
C_{CLK} CLK Capacitance		20		20	pF	f_c = 1 MHz (Note 2)

Notes:
1. MHz ratings refer to internal clock frequency.
2. Not 100% tested.
3. All inputs at 0.4 or V_{CC} - 0.4 (CMOS levels). All inputs held static except clock and all outputs unloaded (static I_{OUT} = 0 mA) Specification also valid for UP# = 0.
4. All inputs at 0.4 or V_{CC} - 0.4 (CMOS levels). All inputs held static and all outputs unloaded (static I_{OUT} = 0 mA).
5. Typical I_{CC} for PGA, 50 MHz, measured at 3.3 V.
   Typical I_{CC} for PGA, 66 and 80 MHz, measured at 4.0 V.
   Typical I_{CC} for QFP, 50 and 66 MHz, measured at 3.3 V.

2.4 AC Characteristics

Tables 2-5 through 2-7 list the AC characteristics including output delays, input setup requirements, input hold requirements and output float delays. These measurements are based on the measurement points identified in Figure 4-1 (Page 4-6) and Figure 4-2 (Page 4-6) of the IBM 486DX2 Data Book. The rising clock edge reference level V_{REF} and other reference levels are shown in Table 2-4 below for the IBM 486DX2-V. Input or output signals must cross these levels during testing.

Table 2-4. Drive Level and Measurement Points for Switching Characteristics

SYMBOL	IBM 486DX2-V	UNITS
V_{REF}	1.5	V
V_{IHD}	2.3	V
V_{ILD}	0	V

Note: Refer to Figure 4-1 of the IBM 486DX2 Data Book

Table 2-5. AC Characteristics for IBM 486DX2-V50
T_{CASE} = 0˚ to 85˚ C, C_L = 50pF
External CLK = 25 MHz (Max.)

SYMBOL	PARAMETERS	MIN (ns)	MAX (ns)	FIGURE	NOTES
T1	CLK Period	40		4-2	
T2	CLK High Time	14		4-2	At 2 V
T3	CLK Low Time	14		4-2	$V_{IL(MAX)}$
T4	CLK Fall Time		4	4-2	2 V to $V_{IL(MAX)}$
T5	CLK Rise Time		4	4-2	$V_{IL(MAX)}$ to 2 V
T6	A31-A2, ADS#, BE3#-BE0#, BREQ, D/C#, HLDA, FERR#, LOCK#, M/IO#, PCD, PWT, W/R# Valid Delay	3	19	4-6	
T6a	SMADS#, SMI# Valid Delay	3	19	4-6	
T7	A31-A2, ADS#, BE3#-BE0#, BREQ, D/C#, HLDA, LOCK#, M/IO#, PCD, PWT, W/R# Float Delay		28	4-7	Note 1
T7a	SMADS#, SMI# Float Delay		28	4-7	Note 1
T8	PCHK# Valid Delay	3	24	4-5	
T8a	BLAST#, PLOCK# Valid Delay	3	24	4-6	
T8b	HITM#, RPLSET(1-0), RPLVAL#, SUSPA# Valid Delay	3	24	4-6	
T9	BLAST#, PLOCK# Float Delay		28	4-7	Note 1
T9a	RPLSET(1-0), RPLVAL# Float Delay		28	4-7	Note 1
T10	D31-D0, DP3-DP0 Write Data Valid Delay	3	20	4-6	
T11	D31-D0, DP3-DP0 Write Data Float Delay		28	4-7	Note 1

Table 2-5. AC Characteristics for IBM 486DX2-V50
T_{CASE} = 0˚ to 85˚ C, C_L = 50pF
External CLK = 25 MHz (Max.)

SYMBOL	PARAMETERS	MIN (ns)	MAX (ns)	FIGURE	NOTES
T12	EADS# Setup Time	8		4-3	
T12a	INVAL Setup Time	8		4-3	
T13	EADS# Hold Time	3		4-3	
T13a	INVAL Hold Time	3		4-3	
T14	BS16#, BS8#, KEN# Setup Time	8		4-3	
T15	BS16#, BS8#, KEN# Hold Time	3		4-3	
T16	BRDY#, RDY# Setup Time	8		4-4	
T17	BRDY#, RDY# Hold Time	3		4-4	
T18	AHOLD, HOLD Setup Time	10		4-3	
T18a	BOFF# Setup Time	10		4-3	
T19	AHOLD, BOFF#, HOLD Hold Time	3		4-3	
T20	A20M#, FLUSH#, IGNNE#, INTR, NMI, RESET Setup Time	10		4-3	
T20a	SMI#, SUSP#, WM_RST Setup Time	10		4-3	
T21	A20M#, FLUSH#, INTR, IGNNE#, NMI, RESET Hold Time	3		4-3	
T21a	SMI#, SUSP#, WM_RST Hold Time	3		4-3	
T22	A31-A4, D31-D0, DP3-DP0 Read Setup Time	6		4-3, 4-4	
T23	A31-A4, D31-D0, DP3-DP0 Read Hold Time	3		4-3, 4-4	

Note 1: Not 100% tested.

Table 2-6. AC Characteristics for IBM 486DX2-V66
T_{CASE} = 0˚ to 85˚ C, C_L = 50pF
External CLK = 33 MHz (Max.)

SYMBOL	PARAMETERS	MIN (ns)	MAX (ns)	FIGURE	NOTES
T1	CLK Period	30		4-2	
T2	CLK High Time	11		4-2	At 2 V
T3	CLK Low Time	11		4-2	$V_{IL(MAX)}$
T4	CLK Fall Time		3	4-2	2 V to $V_{IL(MAX)}$
T5	CLK Rise Time		3	4-2	$V_{IL(MAX)}$ to 2 V
T6	A31-A2, ADS#, BE3#-BE0#, BREQ, D/C#, FERR#, HLDA, LOCK#, M/IO#, PCD, PWT, W/R# Valid Delay	3	16	4-6	
T6a	SMADS#, SMI# Valid Delay	3	16	4-6	
T7	A31-A2, ADS#, BE3#-BE0#, BREQ, D/C#, HLDA, LOCK#, M/IO#, PCD, PWT, W/R# Float Delay		20	4-7	Note 1
T7a	SMADS#, SMI# Float Delay		20	4-7	Note 1

Table 2-6. AC Characteristics for IBM 486DX2-V66
T_{CASE} = 0˚ to 85˚ C, C_L = 50pF
External CLK = 33 MHz (Max.)

SYMBOL	PARAMETERS	MIN (ns)	MAX (ns)	FIGURE	NOTES
T8	PCHK# Valid Delay	3	22	4-5	
T8a	BLAST#, PLOCK# Valid Delay	3	20	4-6	
T8b	HITM#, RPLSET(1-0), RPLVAL#, SUSPA# Valid Delay	3	20	4-6	
T9	BLAST#, PLOCK# Float Delay		20	4-7	Note 1
T9a	RPLSET(1-0), RPLVAL# Float Delay		20	4-7	Note 1
T10	D31-D0, DP3-DP0 Write Data Valid Delay	3	19	4-6	
T11	D31-D0, DP3-DP0 Write Data Float Delay		20	4-7	Note 1
T12	EADS# Setup Time	6		4-3	
T12a	INVAL Setup Time	6		4-3	
T13	EADS# Hold Time	3		4-3	
T13a	INVAL Hold Time	3		4-3	
T14	BS16#, BS8#, KEN# Setup Time	6		4-3	
T15	BS16#, BS8#, KEN# Hold Time	3		4-3	
T16	BRDY#, RDY# Setup Time	6		4-4	
T17	BRDY#, RDY# Hold Time	3		4-4	
T18	AHOLD, HOLD Setup Time	6		4-3	
T18a	BOFF# Setup Time	9		4-3	
T19	AHOLD, BOFF#, HOLD Hold Time	3		4-3	
T20	A20M#, FLUSH#, IGNNE#, INTR, NMI, RESET Setup Time	6		4-3	
T20a	SMI#, SUSP#, WM_RST Setup Time	6		4-3	
T21	A20M#, FLUSH#, IGNNE#, INTR, NMI, RESET Hold Time	3		4-3	
T21a	SMI#, SUSP#, WM_RST Hold Time	3		4-3	
T22	A31-A4, D31-D0, DP3-DP0 Read Setup Time	6		4-3, 4-4	
T23	A31-A4, D31-D0, DP3-DP0 Read Hold Time	3		4-3, 4-4	

Note 1: Not 100% tested.

Table 2-7. AC Characteristics for IBM 486DX2-V80
T_{CASE} = 0˚ to 85˚ C, C_L = 50pF
External CLK = 40 MHz (Max.)

SYMBOL	PARAMETERS	MIN (ns)	MAX (ns)	FIGURE	NOTES
T1	CLK Period	25		4-2	
T2	CLK High Time	9		4-2	At 2 V
T3	CLK Low Time	9		4-2	$V_{IL(MAX)}$
T4	CLK Fall Time		3	4-2	2 V to $V_{IL(MAX)}$

Table 2-7. AC Characteristics for IBM 486DX2-V80
T_{CASE} = 0˚ to 85˚ C, C_L = 50pF
External CLK = 40 MHz (Max.)

SYMBOL	PARAMETERS	MIN (ns)	MAX (ns)	FIGURE	NOTES
T5	CLK Rise Time		3	4-2	$V_{IL(MAX)}$ to 2 V
T6	A31-A2, ADS#, BE3#-BE0#, BREQ, D/C#, FERR#, HLDA, LOCK#, M/IO#, PCD, PWT, W/R# Valid Delay	3	14	4-6	
T6a	SMADS#, SMI# Valid Delay	3	14	4-6	
T7	A31-A2, ADS#, BE3#-BE0#, BREQ, D/C#, HLDA, LOCK#, M/IO#, PCD, PWT, W/R# Float Delay		19	4-7	Note 1
T7a	SMADS#, SMI# Float Delay		19	4-7	Note 1
T8	PCHK# Valid Delay	3	18	4-5	
T8a	BLAST#, PLOCK# Valid Delay	3	16	4-6	
T8b	HITM#, RPLSET(1-0), RPLVAL#, SUSPA# Valid Delay	3	16	4-6	
T9	BLAST#, PLOCK# Float Delay		16	4-7	Note 1
T9a	RPLSET(1-0), RPLVAL# Float Delay		16	4-7	Note 1
T10	D31-D0, DP3-DP0 Write Data Valid Delay	3	17	4-6	
T11	D31-D0, DP3-DP0 Write Data Float Delay		19	4-7	Note 1
T12	EADS# Setup Time	6		4-3	
T12a	INVAL Setup Time	6		4-3	
T13	EADS# Hold Time	3		4-3	
T13a	INVAL Hold Time	3		4-3	
T14	BS16#, BS8#, KEN# Setup Time	6		4-3	
T15	BS16#, BS8#, KEN# Hold Time	3		4-3	
T16	BRDY#, RDY# Setup Time	6		4-4	
T17	BRDY#, RDY# Hold Time	3		4-4	
T18	AHOLD, HOLD Setup Time	6		4-3	
T18a	BOFF# Setup Time	7		4-3	
T19	AHOLD, BOFF#, HOLD Hold Time	3		4-3	
T20	A20M#, FLUSH#, IGNNE#, INTR, NMI, RESET Setup Time	6		4-3	
T20a	SMI#, SUSP#, WM_RST Setup Time	6		4-3	
T21	A20M#, FLUSH#, IGNNE#, INTR, NMI, RESET Hold Time	3		4-3	
T21a	SMI#, SUSP#, WM_RST Hold Time	3		4-3	
T22	A31-A4, D31-D0, DP3-DP0 Read Setup Time	6		4-3, 4-4	
T23	A31-A4, D31-D0, DP3-DP0 Read Hold Time	3		4-3, 4-4	

Note 1: Not 100% tested.

3. Programmable SMM Pin Interface

Following power-up or RESET, the IBM 486DX2-V SMM interface pins are disabled. Once enabled, these two pins can either function as defined in the IBM 486DX2 data book (SMI# and SMADS#) or can be programmed to function with a signalling protocol compatible with the 486 SL-enhanced CPUs (SMI#, SMIACT#). This section describes the operation of the SMM interface pins when operating in the SL-compatible mode.

3.1 SMM Mode Control Bit

Configuration register CCR3 bit 3 (SMM_Mode) controls the SMM interface mode. 0=Cyrix mode, 1=SL-compatible mode, and the default state is 0. If the SMI_Lock bit=0, SMM_Mode may be modified. If the SMI_Lock bit is set, the SMM_Mode bit can no longer be modified. Once the SMI_Lock bit is set, the CPU must be reset (RESET pin) in order to modify SMI_Lock and SMM_Mode.

3.2 Pin Definitions and Timing

The two pins that change function in SL-compatible mode are SMI# and SMADS#. Table 3-1 lists the pin definitions for these two pins. Figure 3-1 illustrates the required timing for the SMI# and SMIACT# signals.

Table 3-1. SMM Pin Definitions

IBM MODE	SL-COMPATIBLE MODE
SMI#: Bidirectional System Management Interrupt pin. Asserted by the system logic to request an SMI interrupt. Sampled by the CPU on each rising clock edge. Causes I/O trap to occur if sampled asserted at least two clocks prior to ready sampled asserted for an I/O cycle. Asserted by the CPU during execution of an SMI service routine or in response to SMINT if SMAC is set.	SMI#: System Management Interrupt input pin. Asserted by the system logic to request an SMI interrupt. Sampled by the CPU on each rising clock edge. SMI# is falling edge sensitive and causes an I/O trap to occur if sampled asserted at least three clocks prior to RDY#/BRDY# sampled asserted for any I/O cycle.
SMADS#: SMI Address Strobe output used to indicate that the current bus cycle is an SMM memory access.	SMIACT#: SMI Active output asserted by the CPU during execution of an SMI service routine.

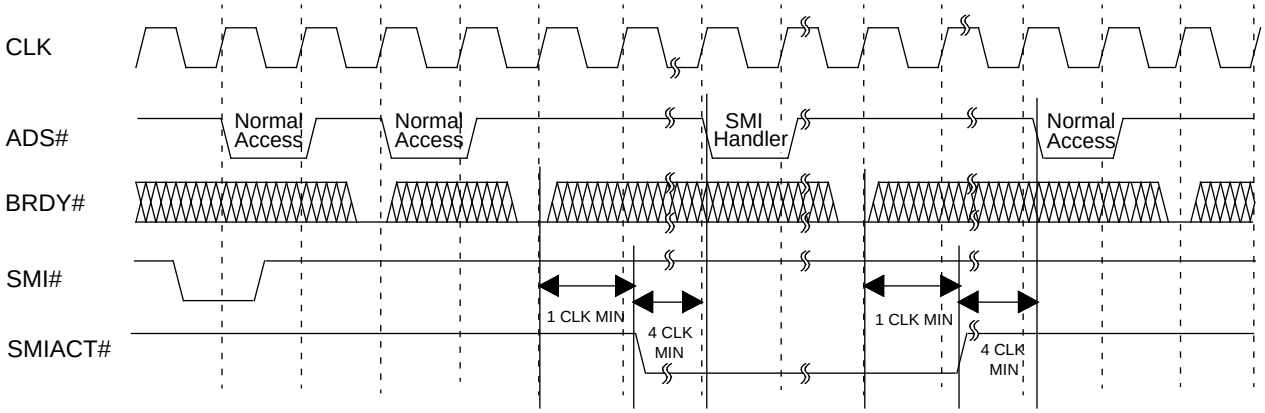


Figure 3-1. SMIACT# Timing

Note 1. SMIACT# is asserted a minimum of one clock after completion of the last normal access.
SMIACT# is asserted a minimum of four clocks prior to asserting ADS# to start the SMM state save.
Note 2. SMIACT# is negated a minimum of one clock after completion of the last SMM access of the state restore.
SMIACT# is negated a minimum of four clocks prior to asserting ADS# for the first normal access following the SMM state restore.

3.3 Nested SMI

In IBM compatible SMI mode, nested SMI's cannot occur due to the fact that the SMI# pin becomes an output during SMI servicing. In SL-compatible mode, if an SMI occurs during an SMI service routine, one and only one SMI# is latched. The latched SMI# is then serviced *immediately* following execution of a RSM instruction (used to exit the original SMI service routine).

3.4 IBM SMM Features Not Used with SL-Compatible Interface

The SMAC and MMAC functions are disabled when in SL-compatible mode. Additionally, SMIACT# remains asserted while executing an SMI service routine regardless of the address being accessed. In other words, if the SMI service routine accesses memory outside the defined SMM memory space, SMIACT# remains asserted. Also, the SMINT instruction should not be used in SL-compatible mode.

3.5 Write-Back Caching and SMM

486 SL-enhanced CPUs allow SMM memory accesses to be cached. This may cause coherency problems in systems where SMM memory space and normal memory space overlap. Therefore, Intel recommends one of two options: (1) flush the cache when entering and exiting an SMI service routine, or (2) flush the cache when entering an SMI service routine and then make all SMM accesses non-cacheable using the KEN# pin. In both cases, Intel recommends asserting the FLUSH# input when SMIACT# is asserted. This is acceptable for a CPU with a write-through cache because the flush invalidates the cache in a single clock.

However, on a CPU with a write-back cache, a FLUSH# requires writing all dirty data to external memory prior to invalidating the cache contents. Bus cycles that are intended for normal memory that is overlapped with the SMM memory space may occur. These bus cycles are intended for normal memory and should not be issued while SMIACT# is asserted.

Therefore, while in SL-compatible mode, the IBM CPU automatically writes all dirty data to memory and then invalidates the cache prior to asserting SMIACT#. This guarantees that no dirty data exists in the CPU at the time that SMIACT# is asserted.

Since SMM accesses are always non-cacheable on IBM CPUs and the cache is flushed prior to entering the SMI service routine, a bus snoop that occurs while SMIACT# is asserted can never hit on a dirty line that is in SMM space or the overlapped normal memory space. Therefore, bus snoops that occur while SMIACT# is asserted, never result in a memory incoherency.

4.0 Mechanical Specifications

4.1 168-Pin PGA Package

The pin assignments for the IBM 486DX2 168-pin PGA package are shown in Figure 5-1. Specifically, the J1 pin has changed from V_{CC} to NC. The pins are listed by signal name and pin number in Table 5-1 and Table 5-2. Please pay particular attention to the pins that are labelled in the tables, as there are have been several corrections to these tables.

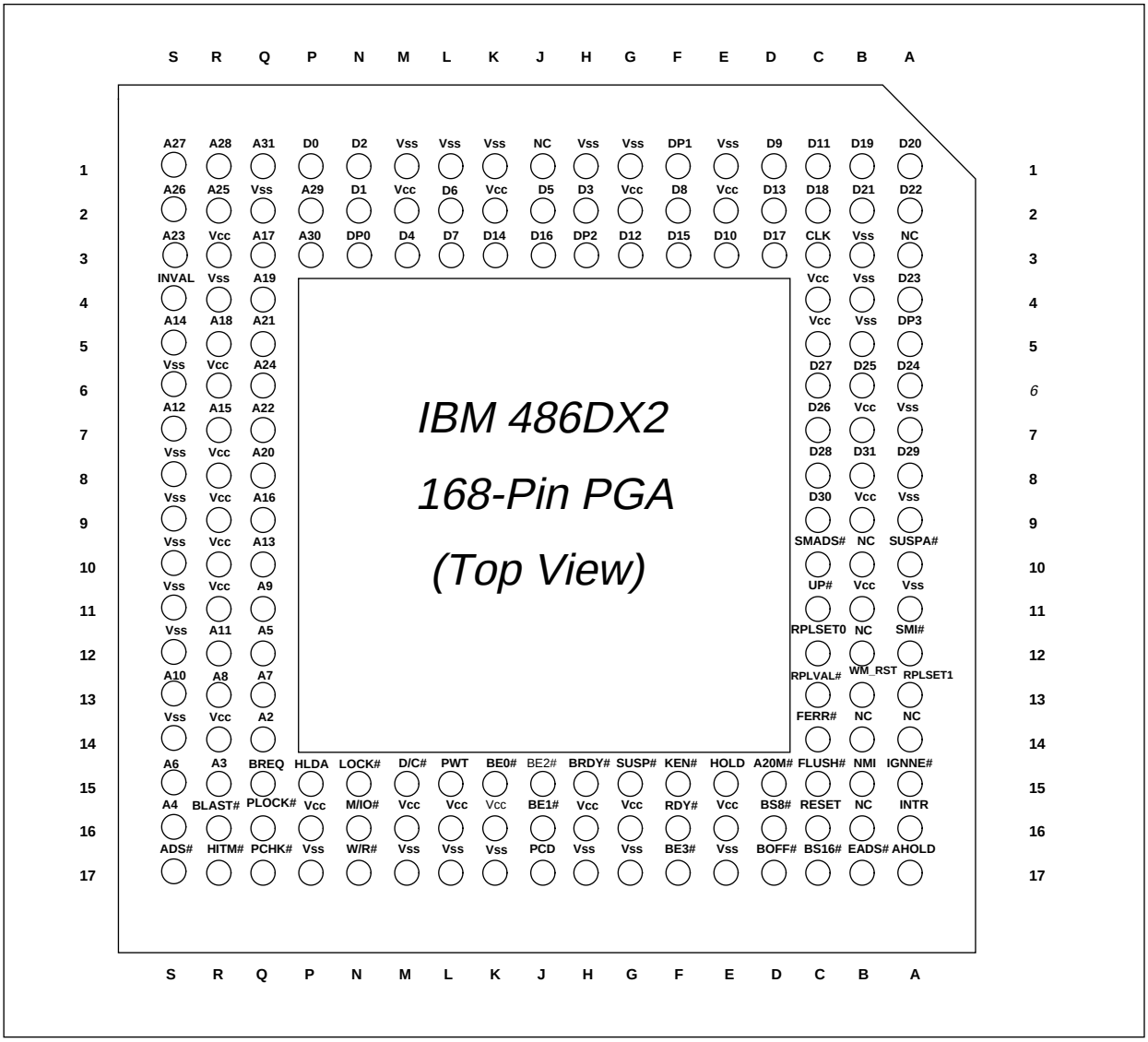


Figure 4-1. 168-Pin PGA Package Pin Assignments

Table 4-1. 168-Pin PGA Package Pin Numbers Sorted by Signal Name

Signal Name	Pin No.	Signal Name	Pin No.	Signal Name	Pin No.	Signal Name	Pin No.	Signal Name	Pin No.	Signal Name	Pin No.
A2	Q14	A29	P2	D11	C1	HITM#	R17	SUSP#	G15	VSS	A11
A3	R15	A30	P3	D12	G3	HLDA	P15	SUSPA#	A10	VSS	B3
A4	S16	A31	Q1	D13	D2	HOLD	E15	UP#	C11	VSS	B4
A5	Q12	ADS#	S17	D14	K3	IGNNE#	A15	VCC	B7	VSS	B5
A6	S15	AHOLD	A17	D15	F3	INTR	A16	VCC	B9	VSS	E1
A7	Q13	BE0#	K15	D16	J3	INVAL	S4	VCC	B11	VSS	E17
A8	R13	BE1#	J16	D17	D3	KEN#	F15	VCC	C4	VSS	G1
A9	Q11	BE2#	J15	D18	C2	LOCK#	N15	VCC	C5	VSS	G17
A10	S13	BE3#	F17	D19	B1	M/IO#	N16	VCC	E2	VSS	H1
A11	R12	BLAST#	R16	D20	A1	NC	A3	VCC	E16	VSS	H17
A12	S7	BOFF#	D17	D21	B2	NC	A14	VCC	G2	VSS	K1
A13	Q10	BRDY#	H15	D22	A2	NC	B10	VCC	G16	VSS	K17
A14	S5	BREQ	Q15	D23	A4	NC	B12	VCC	H16	VSS	L1
A15	R7	BS8#	D16	D24	A6	NC	B14	VCC	K2	VSS	L17
A16	Q9	BS16#	C17	D25	B6	NC	B16	VCC	K16	VSS	M1
A17	Q3	CLK	C3	D26	C7	NC	J1	VCC	L16	VSS	M17
A18	R5	D/C#	M15	D27	C6	NMI	B15	VCC	M2	VSS	P17
A19	Q4	D0	P1	D28	C8	PCD	J17	VCC	M16	VSS	Q2
A20	Q8	D1	N2	D29	A8	PCHK#	Q17	VCC	P16	VSS	R4
A20M#	D15	D2	N1	D30	C9	PLOCK#	Q16	VCC	R3	VSS	S6
A21	Q5	D3	H2	D31	B8	PWT	L15	VCC	R6	VSS	S8
A22	Q7	D4	M3	DP0	N3	RDY#	F16	VCC	R8	VSS	S9
A23	S3	D5	J2	DP1	F1	RESET	C16	VCC	R9	VSS	S10
A24	Q6	D6	L2	DP2	H3	RPLSET0	C12	VCC	R10	VSS	S11
A25	R2	D7	L3	DP3	A5	RPLSET1	A13	VCC	R11	VSS	S12
A26	S2	D8	F2	EADS#	B17	RPLVAL#	C13	VCC	R14	VSS	S14
A27	S1	D9	D1	FERR#	C14	SMADS#	C10	VSS	A7	W/R#	N17
A28	R1	D10	E3	FLUSH#	C15	SMI#	A12	VSS	A9	WM_RST	B13

Table 4-2. 168-Pin PGA Package Signal Numbers Sorted by Pin Number

Pin No.	Signal Name	Pin No.	Signal Name	Pin No.	Signal Name	Pin No.	Signal Name	Pin No.	Signal Name	Pin No.	Signal Name
A1	D20	B12	NC	D17	BOFF#	J15	BE#2	P2	A29	R7	A15
A2	D22	B13	WM_RST	E1	VSS	J16	BE#1	P3	A30	R8	VCC
A3	NC	B14	NC	E2	VCC	J17	PCD	P15	HLDA	R9	VCC
A4	D23	B15	NMI	E3	D10	K1	VSS	P16	VCC	R10	VCC
A5	DP3	B16	NC	E15	HOLD	K2	VCC	P17	VSS	R11	VCC
A6	D24	B17	EADS#	E16	VCC	K3	D14	Q1	A31	R12	A11
A7	VSS	C1	D11	E17	VSS	K15	BE0#	Q2	VSS	R13	A8
A8	D29	C2	D18	F1	DP1	K16	VCC	Q3	A17	R14	VCC
A9	VSS	C3	CLK	F2	D8	K17	VSS	Q4	A19	R15	A3
A10	SUSPA#	C4	VCC	F3	D15	L1	VSS	Q5	A21	R16	BLAST#
A11	VSS	C5	VCC	F15	KEN#	L2	D6	Q6	A24	R17	HITM#
A12	SMI#	C6	D27	F16	RDY#	L3	D7	Q7	A22	S1	A27
A13	RPLSET1	C7	D26	F17	BE3#	L15	PWT	Q8	A20	S2	A26
A14	NC	C8	D28	G1	VSS	L16	VCC	Q9	A16	S3	A23
A15	IGNNE#	C9	D30	G2	VCC	L17	VSS	Q10	A13	S4	INVAL
A16	INTR	C10	SMADS#	G3	D12	M1	VSS	Q11	A9	S5	A14
A17	AHOLD	C11	UP#	G15	SUSP#	M2	VCC	Q12	A5	S6	VSS
B1	D19	C12	RPLSET0	G16	VCC	M3	D4	Q13	A7	S7	A12
B2	D21	C13	RPLVAL#	G17	VSS	M15	D/C#	Q14	A2	S8	VSS
B3	VSS	C14	FERR#	H1	VSS	M16	VCC	Q15	BREQ	S9	VSS
B4	VSS	C15	FLUSH#	H2	D3	M17	VSS	Q16	PLOCK#	S10	VSS
B5	VSS	C16	RESET	H3	DP2	N1	D2	Q17	PCHK#	S11	VSS
B6	D25	C17	BS16#	H15	BRDY#	N2	D1	R1	A28	S12	VSS
B7	VCC	D1	D9	H16	VCC	N3	DP0	R2	A25	S13	A10
B8	D31	D2	D13	H17	VSS	N15	LOCK#	R3	VCC	S14	VSS
B9	VCC	D3	D17	J1	NC	N16	M/IO#	R4	VSS	S15	A6
B10	NC	D15	A20M#	J2	D5	N17	W/R#	R5	A18	S16	A4
B11	VCC	D16	BS8#	J3	D16	P1	D0	R6	VCC	S17	ADS#

4.3 Thermal Characteristics

PGA Package

Table 4-3 and table 4-4 list the maximum ambient temperatures permitted for various clock frequencies and airflows for the PGA Package for Vcc equal to 3.3, 3.45, 3.6, and 4.0 volts respectively.

Table 4-3. PGA Package Maximum Ambient Temperature (T_A) with V_{cc} = 3.3 Volts

CPU Internal Clock Frequency	Heatsink	Supply Current	AIRFLOW				
			0 (ft/min)	50 (ft/min)	100 (ft/min)	200 (ft/min)	400 (ft/min)
50 MHz	NO	.555 A	57 ^{o}C	58 ^{o}C	59 ^{o}C	61 ^{o}C	67 ^{o}C
66 MHz	NO	.640 A	54 ^{o}C	55 ^{o}C	56 ^{o}C	58.5 ^{o}C	65 ^{o}C

Table 4-4. PGA Package Maximum Ambient Temperature (T_A) with V_{cc} = 3.45 Volts

CPU Internal Clock Frequency	Heatsink	Supply Current	AIRFLOW				
			0 (ft/min)	50 (ft/min)	100 (ft/min)	200 (ft/min)	400 (ft/min)
66 MHz	NO	.645 A	52.5 ^{o}C	54 ^{o}C	55 ^{o}C	57 ^{o}C	64 ^{o}C

Table 4-4. PGA Package Maximum Ambient Temperature (T_A) with V_{cc} = 3.6 Volts

CPU Internal Clock Frequency	Heatsink	Supply Current	AIRFLOW				
			0 (ft/min)	50 (ft/min)	100 (ft/min)	200 (ft/min)	400 (ft/min)
66 MHz	NO	.675 A	49.5 °C	51 °C	52 °C	54.5 °C	62 °C

Table 4-4. PGA Package Maximum Ambient Temperature (T_A) with V_{cc} = 4.0 Volts

CPU Internal Clock Frequency	Heatsink	Supply Current	AIRFLOW				
			0 (ft/min)	50 (ft/min)	100 (ft/min)	200 (ft/min)	400 (ft/min)
80 MHz	NO	.875 A	33.5 °C	35 °C	37 °C	41 °C	52 °C

CQFP Package

Table 4-5 and table 4-6 list the maximum ambient temperatures permitted for various clock frequencies and airflows for the CQFP Package for Vcc equal to 3.3, 3.45, 3.6, and 4.0 volts respectively.

Table 4-5. CQFP Package Maximum Ambient Temperature (T_A) with V_{cc} = 3.3 Volts

CPU Internal Clock Frequency	Heatsink	Supply Current	AIRFLOW				
			0 (ft/min)	50 (ft/min)	100 (ft/min)	200 (ft/min)	400 (ft/min)
66 MHz	NO	.640 A	28 ^{o}C	36 ^{o}C	42 ^{o}C	48 ^{o}C	53.5 ^{o}C

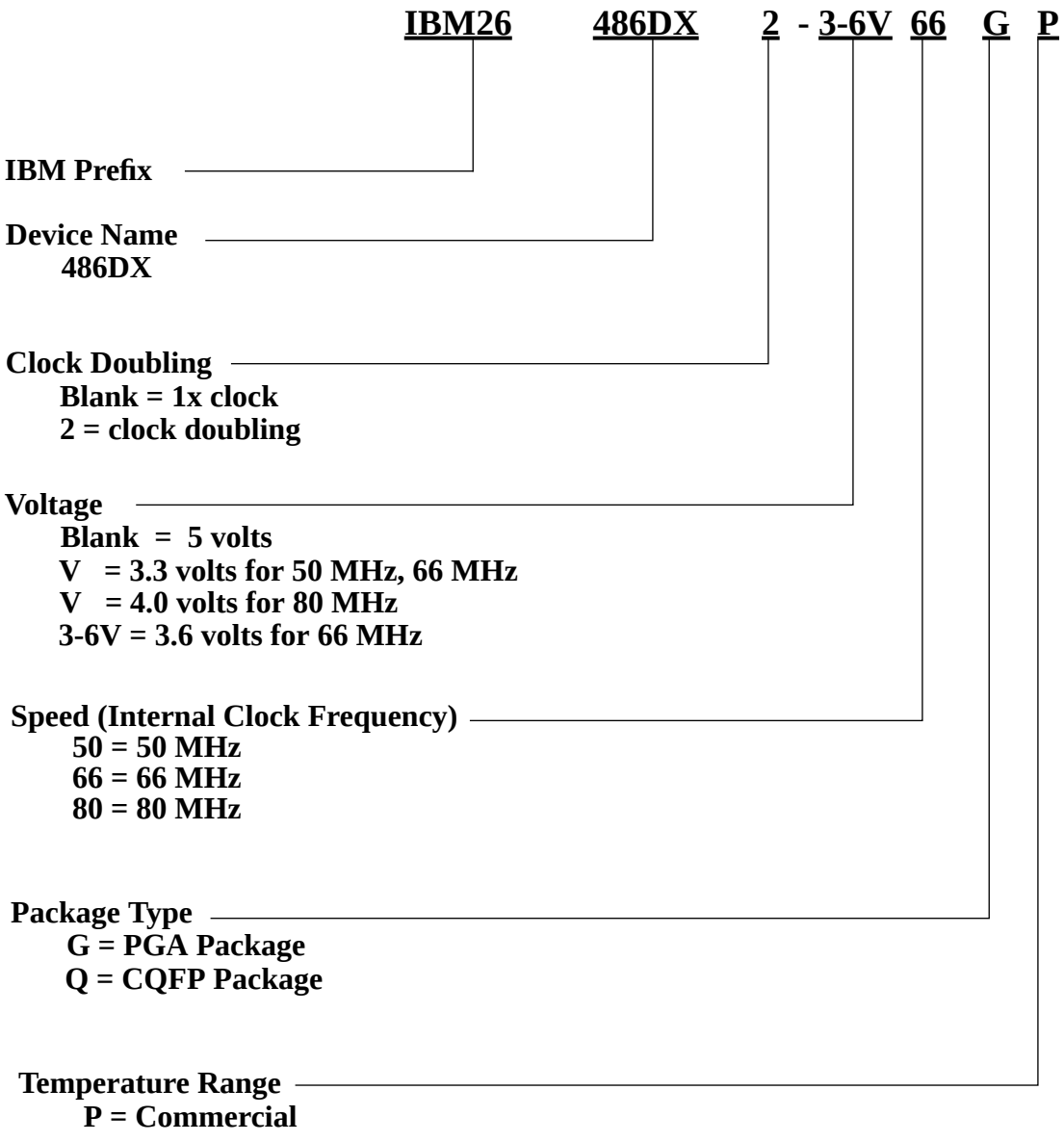
Table 4-6. CQFP Package Maximum Ambient Temperature (T_A) with V_{cc} = 3.45 Volts

CPU Internal Clock Frequency	Heatsink	Supply Current	AIRFLOW				
			0 (ft/min)	50 (ft/min)	100 (ft/min)	200 (ft/min)	400 (ft/min)
66 MHz	NO	.640 A	25 ^{o}C	33.5 ^{o}C	40 ^{o}C	46.5 ^{o}C	52 ^{o}C

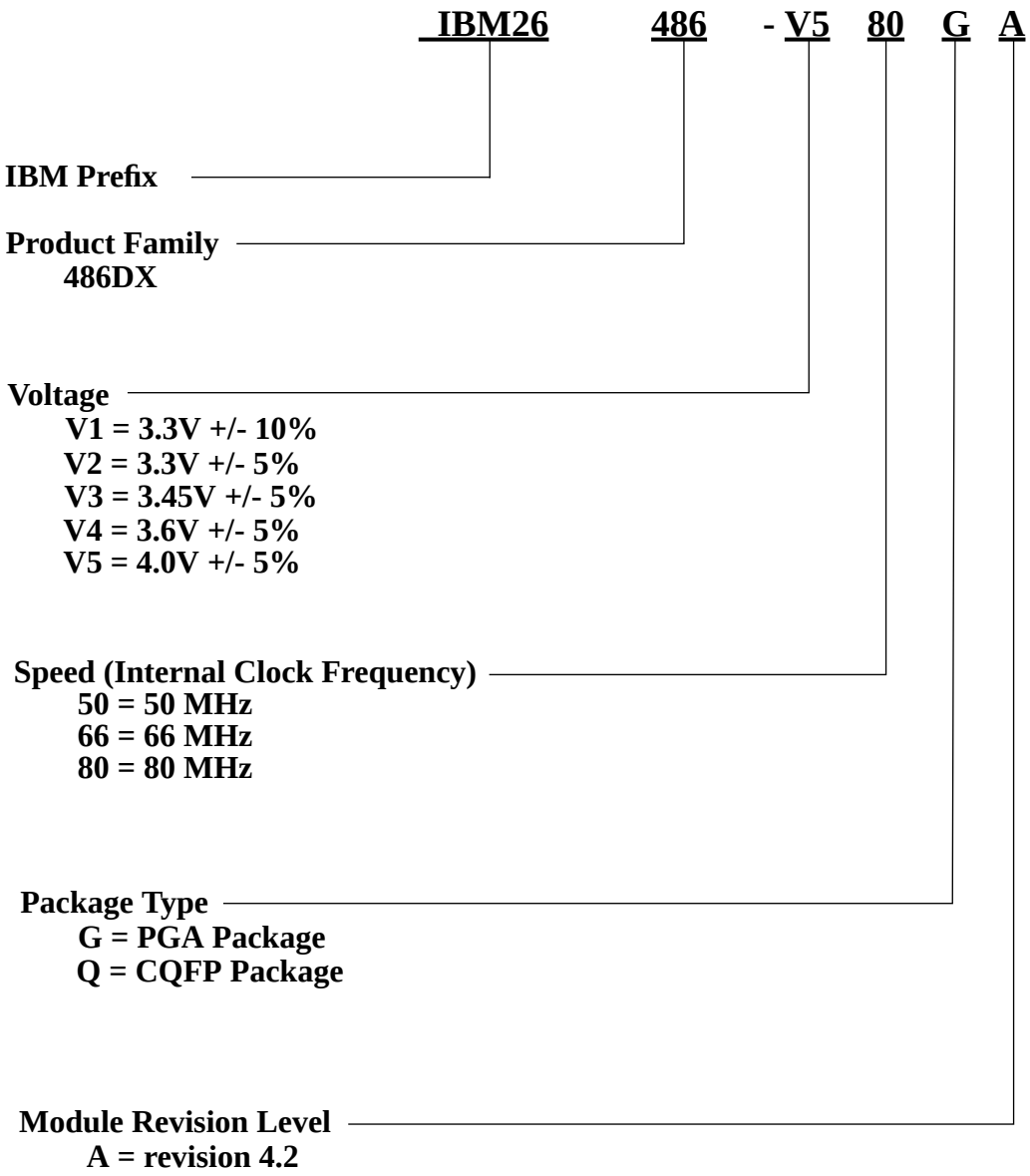
Table 4-6. CQFP Package Maximum Ambient Temperature (T_A) with V_{cc} = 3.6 Volts

CPU Internal Clock Frequency	Heatsink	Supply Current	AIRFLOW				
			0 (ft/min)	50 (ft/min)	100 (ft/min)	200 (ft/min)	400 (ft/min)
66 MHz	NO	.675 A	19.5 ^{o}C	28.5 ^{o}C	35.5 ^{o}C	42.5 ^{o}C	49 ^{o}C

Ordering Information for Rev Levels 1.8, 1.9, 1.91, 4.0 & 4.1



Ordering Information for Rev Levels 4.2 and above



The IBM 486DX2 part numbers for revisions below 4.2 are listed below:

Table B-1. IBM 486DX2 Part Numbers for Rev 1.8, 1.9, 1.91, 4.0, and 4.1

Part Number	V_{cc} (V)	Frequency (MHz)		Package		AC Specification
		Bus	Internal	CQFP	PGA	
IBM26486DX2-V50GP	3.3	25	50		X	Table 2-5 (addendum)
IBM26486DX2-V66GP	3.3	33	66		X	Table 2-6 (addendum)
IBM26486DX2-V66QP	3.3	33	66	X		Table 2-6 (addendum)
IBM26486DX2-3-6V66GP	3.6	33	66		X	Table 2-6 (addendum)
IBM26486DX2-3-6V66QP	3.6	33	66	X		Table 2-6 (addendum)
IBM26486DX2-V80GP	4.0	40	80		X	Table 2-7 (addendum)
IBM26486DX2-50GP	5.0	25	50		X	Table 4-7 (databook)
IBM26486DX2-66GP	5.0	33	66		X	Table 4-8 (databook)

The IBM 486DX2 part numbers for revisions 4.2 and above are listed below:

Table B-2. IBM 486DX2 Part Numbers for Rev 4.2 and above.

Part Number	V_{cc} (V)	Frequency (MHz)		Package		AC Specification
		Bus	Internal	CQFP	PGA	
IBM26486-V150GA	3.3	25	50		X	Table 2-5 (addendum)
IBM26486-V266GA	3.3	33	66		X	Table 2-6 (addendum)
IBM26486-V266QA	3.3	33	66	X		Table 2-6 (addendum)
IBM26486-V466GA	3.6	33	66		X	Table 2-6 (addendum)
IBM26486-V466QA	3.6	33	66	X		Table 2-6 (addendum)
IBM26486-V666GA	3.45/3.6	33	66		X	Table 2-6 (addendum)
IBM26486-V666QA	3.45/3.6	33	66	X		Table 2-6 (addendum)
IBM26486-V580GA	4.0	40	80		X	Table 2-7 (addendum)

IBM Microelectronics [redacted]

This document may contain preliminary information and is subject to change by IBM without notice. IBM assumes no responsibility of liability for any use of the information contained herein. Nothing in this document shall operate as an express or implied license or indemnity under the intellectual property rights of IBM or third parties. The products described in this document are not intended for use in implantation or any other direct life support applications where malfunction may result in physical harm or injury to persons.

NO WARRANTIES OF ANY KIND, INCLUDING BUT NOT LIMITED TO, THE IMPLIED WARRANTIES OF MERCHANTABILITY OR FITNESS FOR A PARTICULAR PURPOSE ARE OFFERED IN THIS DOCUMENT.