TLC34077
Video Interface Palette

Data Manual

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TEXAS INSTRUMENTS

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This device includes circuits that are patented and circuit designs that have patents pending.

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1 Introduction

The TLC34077 Video Interface Palette (VIP) is designed to provide lower system cost with a higher level of integration by incorporating all the high-speed timing, synchronizing, and multiplexing logic usually associated with graphics systems into one device, thus greatly reducing chip count. Since all high-speed signals (excluding the clock source) are contained on-chip, RF noise considerations are simplified. Maximum flexibility is provided through the pixel multiplexing scheme, which allows for 32-, 16-, and 8-bit pixel buses to be accommodated without any circuit modification. The TLC34077 is software compatible with the IMSG176/8 and Brooktree BT476/8 color palettes.

The TLC34077 VIP is pin-for-pin compatible with the TLC34076 VIP, but with a reduced feature set optimized for cost sensitive, high-performance PC graphics applications. The TLC34077 is compatible with a variety of graphics processors, including the ATI 68800 *mach 32* series of graphics accelerators.

The TLC34077 features a separate VGA bus that allows data from the feature connector of most VGA-supported personal computers to be fed directly into the palette without the need for external data multiplexing. This allows a replacement graphics board to remain downward compatible by utilizing the existing graphics circuitry often located on the motherboard.

The 24- and 16-bit true-color modes that are provided allow bits of color information to be transferred directly from the pixel port to the DACs.

The TLC34077 has a 256-by-24 color lookup table with triple 8-bit video D/A converters capable of directly driving a doubly terminated 75-Ω line. Sync generation is incorporated on the green output channel.

Clocking is provided through one of two TTL-compatible inputs and is software selectable. The video clock output provides a software-selected divide ratio of the chosen clock input.

1.1 Features

- Versatile multiplexing interface allows lower pixel bus rate
- High level of integration to provide lower system cost and complexity
- Direct VGA pass-through capability
- True-color (direct-addressing) modes support various 24- and 16-bit formats
- 5-6-5 XGA format compatible
- 5-5-5 TARGA format compatible
- Directly interfaces to most graphics processors
- Triple 8-bit D/A converters
- 110- and 135-MHz versions
- 256-word color palette RAM
- On-chip voltage reference
- RS-343A-compatible outputs
- TTL-compatible inputs
- Standard MPU interface
- Pixel word mask
- On-chip clock selection
- Software downward compatible with INMOS IMSG176/8 and Brooktree BT476/8 color palettes
- TIGA™-software-standard compatible
- LinEPIC™ 1-µm CMOS process

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1.2 Functional Block Diagram

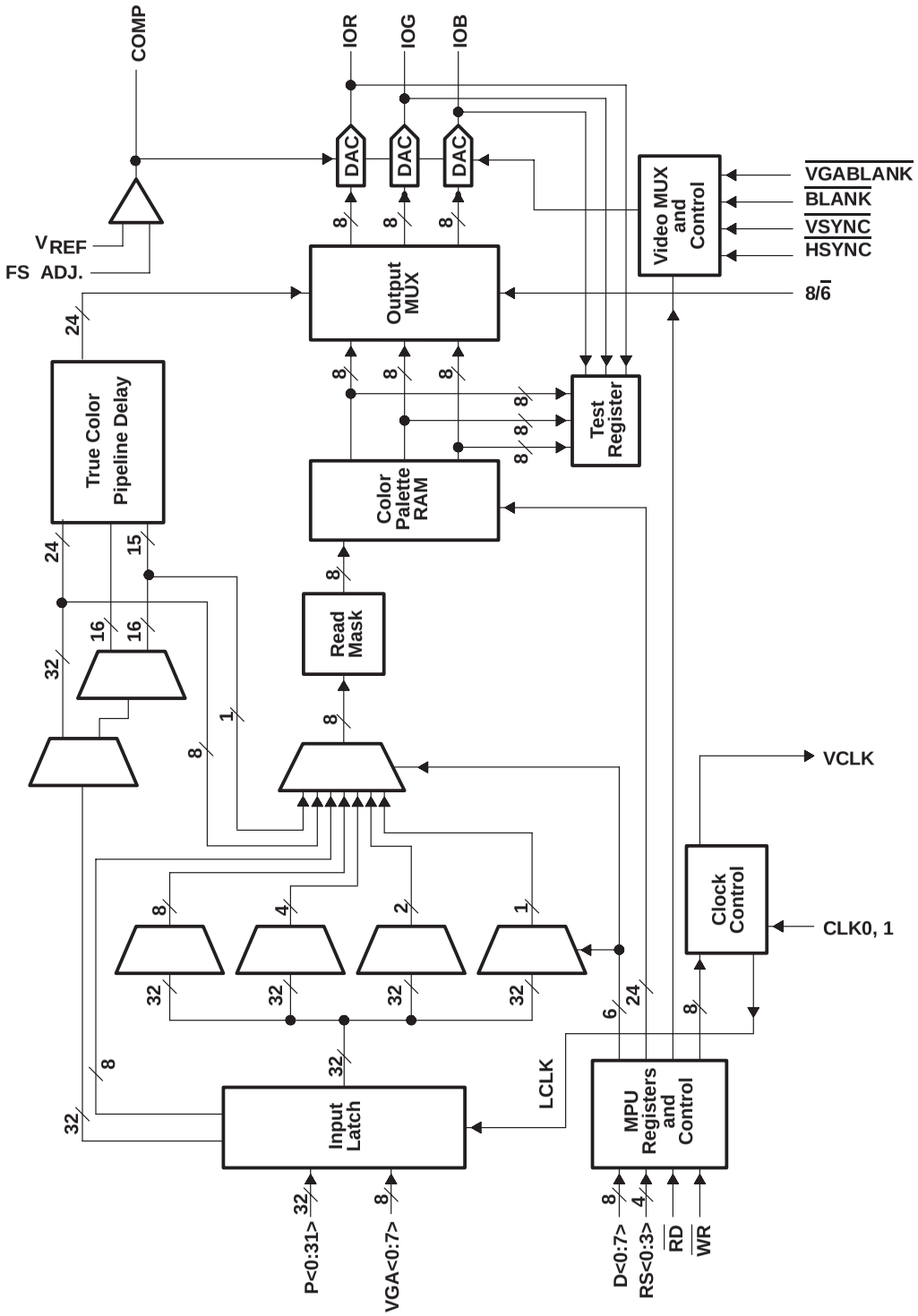
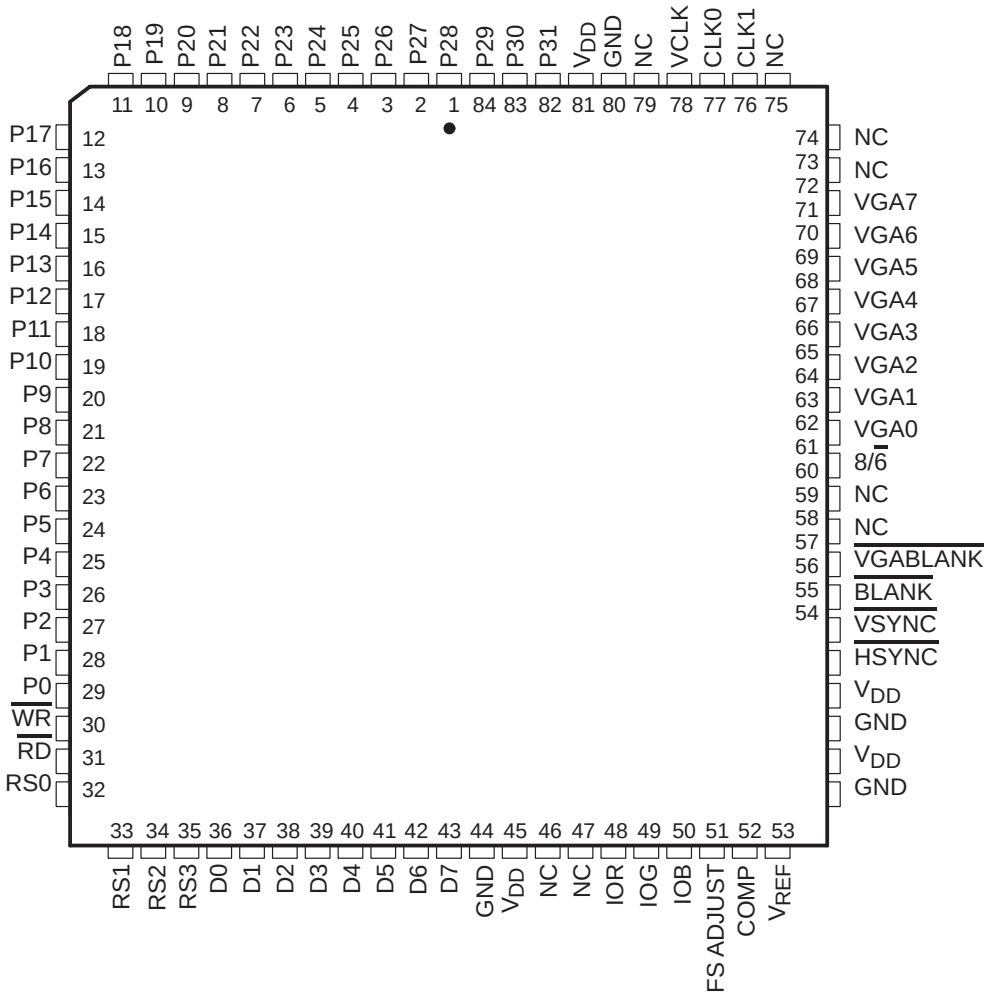


Figure 1–1. Functional Block Diagram

1.3 Terminal Assignments



NC – No internal connection

Figure 1–2. Terminal Assignments

1.4 Ordering Information

TLC34077 – (X)XX FN

Pixel clock frequency indicator
MUST CONTAIN TWO OR THREE CHARACTERS:
- –110: 110-MHz pixel clock
- –135: 135-MHz pixel clock

Package
MUST CONTAIN TWO LETTERS:
- FN: plastic, square, leaded chip carrier (formed leads)

1.5 Terminal Functions

PIN NAME	PIN NO.	I/O	DESCRIPTION
$\overline{\text{BLANK}}$, $\overline{\text{VGABLANK}}$	60, 61	I	Blanking inputs. Two blanking inputs are provided in order to remove any external multiplexing of the signals that may cause data and blank to skew. When the $\overline{\text{VGA}}$ pass-through mode is set in the mux control register, the $\overline{\text{VGABLANK}}$ input is used for blanking; otherwise, $\overline{\text{BLANK}}$ is used.
CLK<0:1>	77, 76	I	Dot clock inputs. Any of the three clocks can be used to drive the dot clock at frequencies up to 135 MHz. When VGA pass-through mode is active, CLK0 is used by default.
COMP	52	I	Compensation input. This terminal provides compensation for the internal reference amplifier. A resistor (optional) and ceramic capacitor are required between this terminal and V_{DD}. The resistor and capacitor must be as close to the device as possible to avoid noise pickup. Refer to Appendix B for more details.
D<0:7>	36 – 43	I/O	MPU interface data bus. Used to transfer data in and out of the register map and palette/overlay RAM.
FS ADJUST	51	I	Full-scale adjustment pin. A resistor connected between this pin and ground controls the full-scale range of the DACs.
GND	44, 54, 56, 80		Ground. All GND pins must be connected. The analog and digital GND pins are connected internally.
$\overline{\text{HSYNC}}$, $\overline{\text{VSYNC}}$	58, 59	I	Horizontal and vertical sync inputs. These signals are used to generate the sync level on the green current output. They are active-low inputs for the normal modes and are passed through a true/complement gate. For the VGA pass-through mode, they are passed through to HSYNCOUT and VSYNCOUT without polarity change as specified by the control register (see Section 2.8).
IOR, IOG, IOB	48, 49, 50	O	Analog current outputs. These outputs can drive a 37.5-Ω load directly (doubly terminated 75-Ω line), thus eliminating the need for any external buffering.
NC	46, 47, 62, 63, 73, 74, 75, 79		No internal connection
P<0:31>	29 – 1, 84 – 82	I	Pixel input port. This port can be used in various modes as shown in the MUX control register. It is recommended that unused pins be tied to ground. It also supports Little/Big Endian data formats. All the unused pins must be tied to GND.
$\overline{\text{RD}}$	31	I	Read strobe input. A low logic level on this pin initiates a read from the TLC34077 register map. Reads are performed asynchronously and are initiated on the falling edge of $\overline{\text{RD}}$ (see Figure 3 – 1).
RS<0:3>	32–35	I	Register select inputs. These pins specify the location in the register map that is to be accessed, as shown in Table 2–1.
VCLK	78	O	Video clock output. User-programmable output for synchronization of the TLC34077 to a graphics processor.
V_{DD}	45, 55, 57, 81		Power. All V_{DD} pins must be connected. The analog and digital V_{DD} pins are connected internally.

PIN NAME	PIN NO.	I/O	DESCRIPTION
VGA<0:7>	65–72	I	VGA pass-through bus. This bus can be selected as the pixel bus for VGA pass-through mode. It does not allow for any multiplexing.
V_{REF}	53		Voltage reference for DACs. (An internal voltage reference of nominally 1.235 V is supplied in.) A 0.1-µF ceramic capacitor between this terminal and GND is recommended for noise filtering using either the internal or an external reference voltage. The internal reference voltage can be overridden by an externally supplied voltage. The typical connection is shown in Appendix B.
$\overline{WR}$	30	I	Write strobe input. A low logic level on this pin initiates a write to the TLC34077 register map. Write transfers are asynchronous. The data written to the register map is latched on the rising edge of $\overline{WR}$ (see Figure 3–1).
8/$\overline{6}$	64	I	DAC resolution selection. This pin is used to select the data bus width (8 or 6 bits) for the DACs and is provided to maintain compatibility with the INMOS IMSG176/8 color palette. When this pin is at a high logic level, 8-bit bus transfers are used, with D<7> being the MSB and D<0> the LSB. For 6-bit bus operation, while the color palette still has the 8-bit information, D<5> shifts to the bit 7 position, D<0> shifts to the bit 2 position, and the two LSBs are filled with zeros at the output MUX to the DAC. When read in the 6-bit mode, the palette-holding register zeroes out the two MSBs.

NOTES: 1. Although leaving unused pins floating will not adversely affect device operation, tying unused pins to ground lowers power consumption and, thus, is recommended.
2. All digital inputs and outputs are TTL compatible, unless otherwise noted.

2 Detailed Description

2.1 MPU Interface

The processor interface is controlled via read and write strobes ($\overline{RD}$, $\overline{WR}$), four register select pins (RS<0:3>), and the 8/$\overline{6}$ select pin. The 8/$\overline{6}$ select pin is used to select between 8- and 6-bit operation and is provided in order to maintain compatibillity with the IMSG176/8 color palette. This operation is carried out in order to utilize the maximum range of the DACs.

The internal register map is shown in Table 2–1. The MPU interface operates asynchronously with data transfers being synchronized by internal logic. All the register locations support read and write operations.

Table 2–1. Internal Register Map

RS3	RS2	RS1	RS0	REGISTER ADDRESSED BY MPU
L	L	L	L	Palette address register – write mode
L	L	L	H	Color palette holding register
L	L	H	L	Pixel read mask
L	L	H	H	Palette address register – read mode
L	H	L	L	Reserved
L	H	L	H	Reserved
L	H	H	L	Reserved
L	H	H	H	Reserved
H	L	L	L	General control register
H	L	L	H	Input clock selection register
H	L	H	L	Output clock selection register
H	L	H	H	MUX control register
H	H	L	H	Reserved
H	H	H	H	Reset state

2.2 Color Palette RAM

The color palette RAM is addressed by two internal 8-bit registers, one for reading from the RAM and one for writing to the RAM. These registers are automatically incremented following a RAM transfer, allowing the entire palette to be read/written with only one access of the address register. When the address register increments beyond the last location in RAM, it is reset to the first location (address 0). Although all read and write accesses to the RAM are asynchronous to LCLK, VCLK, and the dot clock, they are performed within one dot clock and so do not cause any noticeable disturbance on the display.

The color palette RAM is 24 bits wide for each location (8 bits each for red, green, and blue). If 6-bit mode is chosen (8/$\overline{6}$ = low), the two MSBs are still written to the color palette RAM. However, if they are read back in the 6-bit mode, the two MSBs are set to 0 to maintain compatibility with the IMSG176/8 and BT476/8 color palettes. The output MUX shifts the six LSBs to the six MSB positions, fills the two LSBs with 0s, then feeds the eight bits to the DAC. With the 8/$\overline{6}$ pin held low, data on the lowest six bits of the data bus ae internally shifted up by two bits to occupy the upper six bits at the output MUX, and the bottom two bits are then zeroed. The test register and the ones accumulation register both take data before the output MUX to give the user the maximum flexibility.

The color palette RAM access methodology is described in the following two sections and is fully compatible with the IMSG176/8 and BT476/8 color palettes.

2.2.1 Writing to the Color Palete RAM

To load the color palette RAM, the MPU must first write to the address register (write mode) with the address where the modification is to start. This action is followed by three successive wwrites to the palette-holding register with eight bits each of red, gree, and blue data. After the blue data write cycle, the three bytes of color are concatenated into a 24-bit word and written to the color palette RAM location specified by the address register. The address register then increments to point to the next color palette RAM location, which the MPU may modify by simply wariting another sequence of red, green, and blue data bytes. A block of color values in consecutive locations may be written to by writing the start address and performing continuous red, green, and blue write cycles until the entire block has been written.

2.2.2 Reading From the Color Palette RAM

Reading from the color palette RAM is performed by writing the location to be read to the address register. This action initiates a transfer from the color palette RAM into the holding rgister followed by an increment of the address register. Three successive MPU reads from the holding register produce red, green, and blue color data (six or eight bits, depending on the 8/$\overline{6}$ mode) for the specified location. Following the blue read cycle, the contents of the color palette RAM at the address specified by the address register are copied into the holding register and the address register is again incremented. As with writing to the color palette RAM, a block of color values in consecutive locations may be read by writing the start address and performing continuous red, green, and blue read cycles until the entire block has been read.

2.3 Input/Output Clock Selection and Generation

The TLC34077 provides two clock inputs. The TTL inputs can be used for video rates up to 135 MHz. The clock source used at power up is CLK0; an alternative source can be selected by software during normal operation. This chosen clock input is used unmodified as the dot clock (representing the pixel rate to the monitor). The device does, however, allow for user programming of LCLK and the VCLK output (latch and video clocks) via the output clock selection register. The input/output clock selection registers are shown in Tables 2–2, 2–3, and 2–4.

VCLK is designed to work with video control signals like BLANK and SYNC's. LCLK is the latch clock for loading data into the pixel port. It is an internal signal that must be programmed in the output clock selection register. Even though LCLK and VCLK can be selected independently, there is still a relationship between the two as discussed below. Many system considerations have been carefully covered in the design, leaving maximum freedom to the user.

Internally, both LCLK and VCLK are generated from a common clock counter that increments on the rising edge of the DOTCLK. Therefore, when VCLK is enabled, it is in phase with LCLK (see Figure 2–1).

The internal clock counter is initialized to value 0 any time the output clock-selection register (bits 5, 4, 2, 1) are all set to 1's. This provides a simple mechanism to synchronize multiple video interface palettes by providing a known phase relationship for the various system clocks. One can write directly to the output clock selection register to cause this to occur, or any of the various resets (POR, hardware, software – see section 1.5) will also cause the appropriate bits to be written and the counters to reset. It is up to the user to provide some means of disabling the dot-clock input to the part while this reset is occurring, if multiple parts are to be synchronized.

Appendix A discusses the LCLK/VCLK relationship specific to the TMS340x0 GSP.

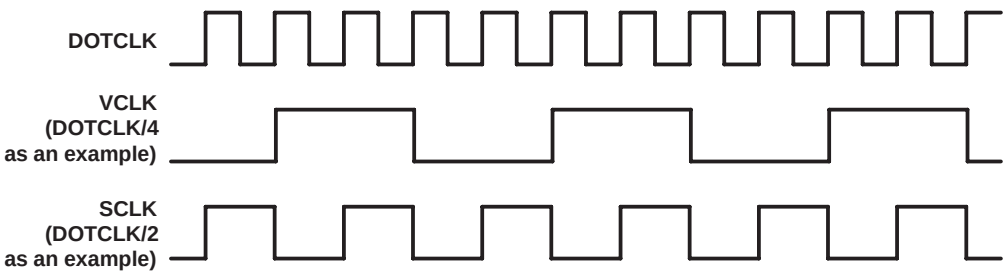


Figure 2–1. DOTCLK/VCLK/LCLK Relationship

Table 2–2. Input Clock Selection Register Format

BITS†				FUNCTION‡
3	2	1	0	
0	0	0	0	Select CLK0 as clock source§
0	0	0	1	Select CLK1 as clock source

† Register bits 4, 5, 6, and 7 are *don't care* bits.
‡ When the clock selection is altered, a minimum 30-ns delay is incurred before the new clocks are stabilized and running.
§ CLK0 is chosen at power up to support the VGA pass-through mode.

Table 2–3. Output Clock Selection Register Format

BITS†						FUNCTION‡
5	4	3	2	1	0	
0	0	0	X	X	X	VCLK frequency = DOTCLK frequency
0	0	1	X	X	X	VCLK frequency = DOTCLK frequency/2
1	1	X	X	X	X	VCLK output held at logic high level (default condition)§
X	X	X	0	0	0	LCLK frequency = DOTCLK frequency
X	X	X	0	0	1	LCLK frequency = DOTCLK frequency/2
X	X	X	1	1	X	LCLK output held at logic level low (default condition)§

† Register bits 6 and 7 are *don't care* bits.
‡ When the clock selection is altered, a minimum 30-ns delay is incurred before the new clocks are stabilized and running.
§ These lines indicate the power-up conditions required to support the VGA pass-through mode.

Table 2–4. VCLK/LCLK Divide Ratio Selection (Output Clock Selection Register Value in Hex)

LCLK / VCLK	BITS 2. . . 0¶	000	001
BITS 5. . .3¶	divide DOTCLK by	1	2
000	1	00	01
001	2	08	09

¶ Output clock selection register bits

2.3.1 LCLK

Data is latched inside the device on the rising edge of LCLK, which is an internal programmable signal. Therefore, LCLK must be set as a function of the pixel bus width and the number of bit planes. LCLK can be selected as divisions of 1 or 2 of the dot clock. If LCLK is not used, the output can be switched off and held low.

The trailing edge of VCLK is used internally by the TLC34077 to sample and latch the $\overline{\text{BLANK}}$ input. The TLC34077 video blanking circuitry is designed with sufficient pipeline delay to allow the internal sampled $\overline{\text{BLANK}}$ signal to align with the pipelined RGB data to the video DACs. The logic described above works in situations where the LCLK period is shorter than, equal to, or longer than the VCLK period.

The default divide ratio for LCLK is 1:1, as used in Mode 0.

Depending on the frequency relationship between LCLK and VCLK, their phase relationship could be critical. Please refer to Appendix C for a more detailed discussion.

2.3.2 VCLK

The VCLK frequency can be selected to be 1/1 or 1/2 of that of the dot clock, or it can be held at a high logic level. The default condition is for VCLK to be held at a high logic level. VCLK is not used in VGA pass-through mode.

VCLK is used by a GSP or custom-designed control logic to generate control signals ($\overline{\text{BLANK}}$, $\overline{\text{HSYNC}}$, and $\overline{\text{VSYNC}}$). As can be seen from Figure 2–2, since the control signals are sampled by VCLK, it is obvious that VCLK has to be enabled.

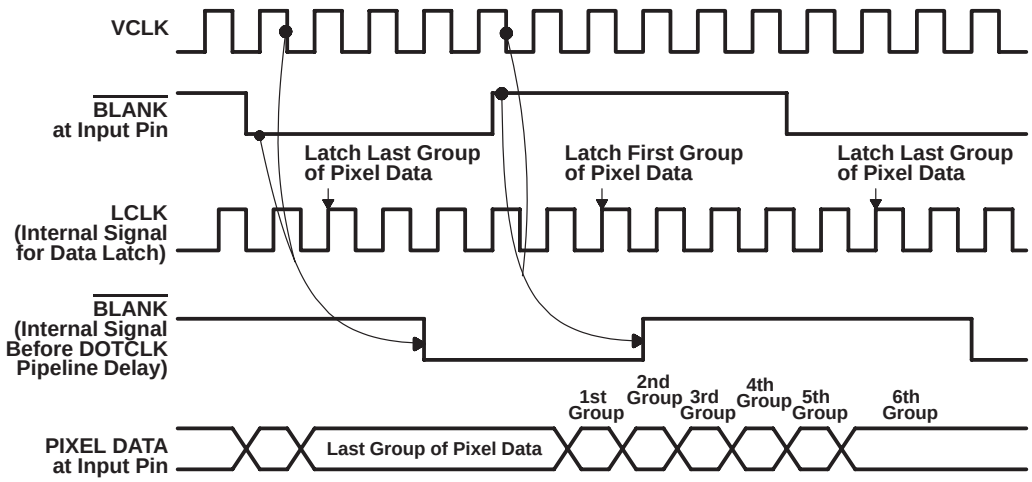


Figure 2–2. LCLK/VCLK Control Timing

2.4 Multiplexing Scheme

The TLC34077 offers a highly versatile multiplexing scheme as illustrated in Table 2–5. The on-chip multiplexing allows the system to be reconfigured to different dilsplay modes without hardware modification.

2.4.1 VGA Pass-Through Mode

Mode 0, the VGA pass-through mode, is used to emulate the VGA modes of most personal computers. The advantage of this mode is that the TLC34077 can take data presented on the feature connectors of most VGA-compatible PC systems into the device on a separate bus, thus requiring no external multiplexing. This feature is particularly useful for systems in which the existing graphics circuitry is on the motherboard. In this instance, it enables implementation of a drop-in graphics card that maintains compatibility with all existing software by using the on-board VGA circuitry but routing the emerging bit-plane data through the TLC34077. This is the default mode at power up. When the VGA pass-through mode is selected after the device is powered up, the clock selection register, the general control register, and the pixel read mask register are set to their default states automatically.

Since this mode is designed with the feature connector philosophy, all the timing is referenced to CLK0, which is used by default for VGA pass-through mode. For all the other modes, CLK <0:1> are the oscillator sources for DOTCLK, VCLK, and LCLK.

2.4.2 Multiplexing Modes

In addition to the VGA pass-through mode, there are three other modes available. Modes 1 and 2 use 8 bit planes to address the color palette. These modes allow dot-clock-to-LCLK ratios of 1:1 (8-bit bus), or 2:1 (16-bit bus).

2.4.3 True-Color Modes

Mode 3 is the true-color mode in which 24, 16, or 15 bits of data are transferred from the pixel port directly to the DACs, but with the same amount of pipeline delay as the control signals ($\overline{\text{BLANK}}$ and SYNCs). For proper true color operation, all overlay bits defined for a given mode should be set to logic ‘0’ or the read mask must be set to 00h.

Mode 3a is the TARGA compatible (5-5-5) true-color mode. In this 16-bit mode, there are 5 bits of RED, 5 bits of GREEN, 5 bits of BLUE. Refer to Table 2–7 for the exact bit definitions.

Mode 3b is the XGA compatible (5-6-5) true-color mode. This 16-bit mode has 5 bits of RED, 6 bits of GREEN, and 5 bits of BLUE data. Refer to Table 2–7 for the exact bit definitions.

Mode 3c is a multiplexed version of mode 3a, that allows two 16-bit TARGA-compatible words to be latched into the TLC34077 pixel port with one LCLK. In this mode, the 16-bit word latched on pixel port inputs P0–P15 is executed first, while the word latched on P16–P31 is executed last. The user should program the LCLK divide ratio in the output-clock selection register to /2. Refer to Table 2–7 for the exact bit definitions.

Mode 3d is a multiplexed version of mode 3b, that allows two 16-bit XGA-compatible words to be latched into the TLC34077 pixel port with one LCLK. In this mode, the 16-bit word latched on pixel port inputs P0–P15 is executed first, while the word latched on P16–P31 is executed last. The user should program the LCLK divide ratio in the output-clock selection register to /2. Refer to Table 2–7 for the exact bit definitions.

Mode 3e is a 24-bit true-color mode that features 8 bits of data for each color. The order in which the color fields appear in the 32-bit word are the reverse of mode 3f. Refer to Table 2–7 for the exact bit definitions.

Mode 3f is the 24-bit true-color mode used on the TLC34077. It also features 8 bits of data for each color. Refer to Table 2–7 for the exact bit definitions.

Since only 5 bits (6 bits for GREEN in Mode 3b and 3d) are provided for each color in the 16-bit true-color modes (3a – 3d), the color data will be internally shifted by the TLC34077 to the 5 MSB positions (6 MSB positions for GREEN in Mode 3b and 3d) before being presented to the three color DACs. The remaining lower 3 bits (lower 2 bits for GREEN in Modes 3b and 3d) are then set to logic 0.

When in true-color modes 3e or 3f, the data input only works in the 8-bit mode. In other words, if only 6 bits are to be used, the 2 LSB inputs for each color must be tied to GND. However, the palette, which is used

by the overlay input, is still governed by 8/6-input pin and the output MUX will select 8-bits data or 6-bits data accordingly. The 8/6-input pin is also valid in the other 16-bit modes as well.

2.4.4 Multiplex Control Register

The multiplexer is controlled via the 8-bit multiplex control register. The bit fields of the register are in Table 2–5 and Table 2–6.

As an example of how to use Table 2–5, suppose that the design goals specify a system with eight data bits per pixel and the lowest possible LCLK rate. Table 2–5 shows that, for non-VGA-pass-through operation, Modes 1 and 2 support an 8-bit pixel depth. The lowest-possible LCLK rate within mode 1 is 1:2. This set of conditions is selected by writing the value 10h to the mux control register. The pixel latching sequence column shows that, in this mode, P<7:0> should be connected to the earliest-displayed pixel plane, followed by P<15:8>, as the last displayed pixel plane. Assuming that VCLK is programmed as DOTCLK/2, Table 2–4 shows that the 1:2 LCLK ratio is selected by writing the value 09h to the output clock selection register.

When the mux control register is loaded with 2Dh, the TLC34077 enters the VGA pass-through mode (the same condition as the default power-up mode). Please refer to Section 2.5.4 for more details.

Table 2–5. Mode and Bus Width Selection

MODE	MUX CONTROL REGISTER BITS†						DATA BITS PER PIXEL‡	PIXEL BUS WIDTH	LCLK DIVIDE RATIO§	PIXEL LATCHING SEQUENCE¶
	5	4	3	2	1	0				
0#	1	0	1	1	0	1	8	8	1	1) VGA<7:0>
1	0	1	1	1	0	0	8	8	1	1) P<7:0>
2	0	1	1	1	0	1	8	16	2	1) P<7:0> 2) P<15:8>
3	See Table 2–6 and Table 2–7									

† Bits 6 and 7 are *don't care* bits.

‡ This is the number of bits of pixel port (or VGA port in mode 1) information used as color data for each displayed pixel, often referred to as the number of bit planes. This may be color palette address data (Modes 0–2) or DAC data (mode 3).

§ The LCLK divide ratio is the number used for the output clock selection register. It indicates the number of pixels per bus load or the number of pixels associated with each LCLK pulse. For example, with a 16-bit pixel bus width and 8 bit planes, 2 pixels comprise each bus load. The LCLK divide ratio is not automatically set by mode selection, but must be written to the output clock selection register.

¶ For each operating mode, the pixel latching sequence indicates the sequence in which pixel port or VGA port data are latched into the device. The latching sequence is initiated by a rising edge on LCLK. For modes in which multiple groups of data are latched, the LCLK rising edge latches all the groups, and the pixel clock shifts them out starting with the low-numbered group.

Mode 0 is VGA pass-through mode.

|| For proper true color operation, all overlay bits defined for a given true color mode must be set to logic 0 or the read mask must be cleared by setting it to 00h. See Table 2–7.

NOTE: Although leaving unused pins floating will not adversely affect device operation, tying unused pins to ground lowers power consumption and, thus, is recommended.

Table 2–6. True-Color Mode

MODE	MUX CONTROL REGISTER BITS†						DATA BITS PER PIXEL‡	PIXEL BUS WIDTH	LCLK DIVIDE RATIO§	OVERLAY BITS PER PIXEL (4)	PIXEL LATCHING SEQUENCE¶
	5	4	3	2	1	0					
3											
3a	0	0	1	0	0	0	15	16	1	1	1) P<15:0>
3b	0	0	1	0	0	1	16	16	1	N/A	1) P<15:0>
3c	0	0	1	0	1	0	15	32	2	1	1) P<15:0> 2) P<31:16>
3d	0	0	1	0	1	1	16	32	2	N/A	1) P<15:0> 2) P<31:16>
3e	0	0	1	1	1	0	24	32	1	8	1) P<31:0>
3f	0	0	1	1	0	1	24	32	1	8	1) P<31:0>

† Bits 6 and 7 are *don't care* bits.

‡ This is the number of bits of pixel port (or VGA port in mode 1) information used as color data for each displayed pixel, often referred to as the number of bit planes. This may be color palette address data (Modes 0–2) or DAC data (Mode 3).

§ The LCLK divide ratio is the number used for the output clock selection register. It indicates the number of pixels per bus load or the number of pixels associated with each LCLK pulse. For example, with a 16-bit pixel bus width and 8 bit planes, 2 pixels comprise each bus load. The LCLK divide ratio is not automatically set by mode selection, but must be written to the output clock selection register.

¶ For each operating mode, the pixel latching sequence indicates the sequence in which pixel port or VGA port data are latched into the device. The latching sequence is initiated by a rising edge on LCLK. For modes in which multiple groups of data are latched, the LCLK rising edge latches all the groups, and the pixel clock shifts them out starting with the low-numbered group. For example, in mode 6d with a 32-bit pixel bus width, the rising edge of LCLK latches all the data groups, and the pixel clock shifts them out in the order P<15:0>, P<31:16>.

‖ For proper true color operation, all overlay bits defined for a given true color mode must be set to logic 0 or the read mask must be cleared by setting it to 00h. See Table 2–7.

NOTE: Although leaving unused pins floating will not adversely affect device operation, tying unused pins to ground lowers power consumption and, thus, is recommended.

Table 2–7. True-Color Bit Definitions

Little Endian

Pixel Bus	P31	P30	P29	P28	P27	P26	P25	P24	P23	P22	P21	P20	P19	P18	P17	P16
Data Bus	D31	D30	D29	D28	D27	D26	D25	D24	D23	D22	D21	D20	D19	D18	D17	D16
a																
b																
c	O	R4	R3	R2	R1	R0	G4	G3	G2	G1	G0	B4	B3	B2	B1	B0
d	R4	R3	R2	R1	R0	G5	G4	G3	G2	G1	G0	B4	B3	B2	B1	B0
e	O7	O6	O5	O4	O3	O2	O1	O0	R7	R6	R5	R4	R3	R2	R1	R0
f	B7	B6	B5	B4	B3	B2	B1	B0	G7	G6	G5	G4	G3	G2	G1	G0

Pixel Bus	P15	P14	P13	P12	P11	P10	P9	P8	P7	P6	P5	P4	P3	P2	P1	P0
Data Bus	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
a	O	R4	R3	R2	R1	R0	G4	G3	G2	G1	G0	B4	B3	B2	B1	B0
b	R4	R3	R2	R1	R0	G5	G4	G3	G2	G1	G0	B4	B3	B2	B1	B0
c	O	R4	R3	R2	R1	R0	G4	G3	G2	G1	G0	B4	B3	B2	B1	B0
d	R4	R3	R2	R1	R0	G5	G4	G3	G2	G1	G0	B4	B3	B2	B1	B0

e	G7	G6	G5	G4	G3	G2	G1	G0	B7	B6	B5	B4	B3	B2	B1	B0
f	R7	R6	R5	R4	R3	R2	R1	R0	O7	O6	O5	O4	O3	O2	O1	O0

2.4.5 Read Masking

The read mask register is used to enable or disable a pixel address bit from addressing the color palette RAM. Each palette address bit is logically ANDed with the corresponding bit from the read mask register before addressing the palette. This function is performed after the addition of the page register bits and, therefore, a zeroing of the read mask results in one unique palette location (location 0) and is not affected by the palette page register contents.

Note also that the Read Mask can be used to zero the overlay data in the True Color modes.

2.5 Reset

There are three ways to reset the TLC34077:

1. Power-on reset
2. Hardware reset
3. Software reset

2.5.1 Power-On Reset

There is a POR (power-on reset) circuit built into the TLC34077. This POR words at power on only. Even though this circuitry is provided, it is still recommended for the user to design a hardware reset circuit to ensure the reset condition after power up as described in section 2.5.2.

Once the voltage is stabilized, the default condition for all registers is VGA mode. Note also that, when the TLC34077 is reset, the LCLK and VCLK counters are reset as well. See 2.3 and 2.5.4.

2.5.2 Hardware Reset

The TLC34077 resets whenever RS<3:0> = HHHH and a rising edge occurs on the $\overline{\text{WR}}$ input. The more rising $\overline{\text{WR}}$ edges occur, the more reliable the TLC34077 is reset. This scheme (bursting $\overline{\text{WR}}$ strobes until the power supply voltage stabilizes) is suggested at power up if a hardware reset approach is used.

The default reset condition is VGA mode, and the values for each register are shown in Section 2.5.4. Note also that, when the TLC34077 is reset, the LCLK and VCLK counters are reset. See Section 2.3.

2.5.3 Software Reset

Whenever the mux control register is set for VGA pass-through mode after power up, all registers are initialized accordingly. Since VGA pass-through mode is the default condition at power up and hardware reset, the act of selecting the VGA pass-through mode through programming the mux control register is viewed as a software reset. Therefore, whenever mux control register bits <5:0> are set to 2Dh, the TLC34077 initiates a software reset. This also resets the LCLK and VCLK counters (see 2.3). This is referred to as a software reset, since it is typically initiated by software, unlike POR or hardware resets.

2.5.4 VGA Pass-Through Mode Default Conditions

The value contained in each register after hardware or software reset is shown below:

Mux control register:	2Dh
Input clock selection register:	00h
Output clock selection register:	3Fh
General control register:	03h
Pixel read mask register:	FFh
Palette address register:	xxh
Palette holding register:	xxh

2.6 Frame Buffer Interface

The TLC34077 provides two clock signals for controlling the frame buffer interface: LCLK and VCLK. VCLK is used to clock and synchronize control inputs like $\overline{\text{HSYNC}}$, $\overline{\text{VSYNC}}$, and $\overline{\text{BLANK}}$.

The pixel data presented at the inputs is latched at the rising edge of LCLK in normal mode or the rising edge of CLK0 in VGA pass-through mode. Control inputs HSYNC, VSYNC, and BLANK are sampled and latched at the falling edge of VCLK in normal mode, while HSYNC, VSYNC, and VGABLANK are latched at the rising edge of CLK0 in VGA pass-through mode. Both data and control signals are lined up at the DAC outputs to the monitor through the internal pipeline delay, so external glue logic is not required. The outputs of the DACs are capable of directly driving a 37.5-Ω load, as in the case of a doubly terminated 75-Ω cable. See Figures 2–4 and 2–5 for nominal output levels.

2.7 Analog Output Specifications

The DAC outputs are controlled by current sources (three for IOG and two each for IOR and IOB) as shown in Figure 2–3. In the normal case, there is a 7.5-IRE difference between blank and black levels, which is shown in Figure 2–4. If a 0-IRE pedestal is desired, it can be selected by resetting bit 4 of the general control register (see Section 2.9.1). The video output for a 0-IRE pedestal is shown in Figure 2–5.

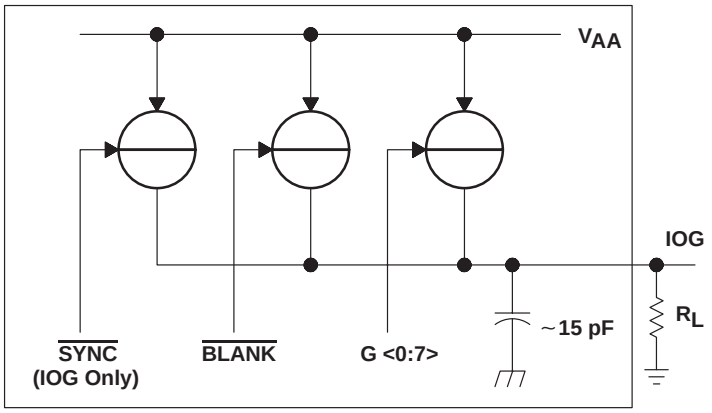


Figure 2–3. Equivalent Circuit of the IOG Current Output

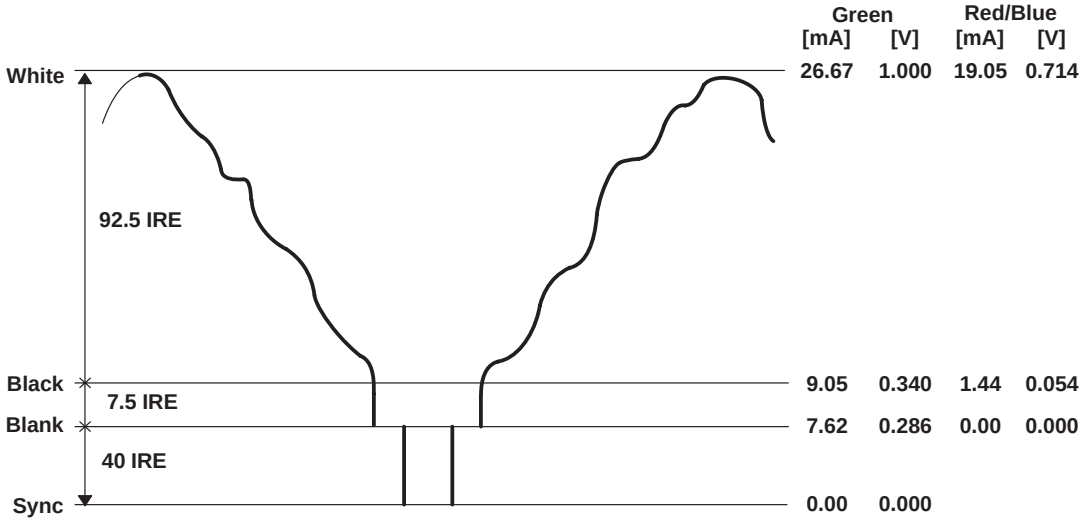


Figure 2–4. 7.5-IRE, 8-Bit Composite Video Output

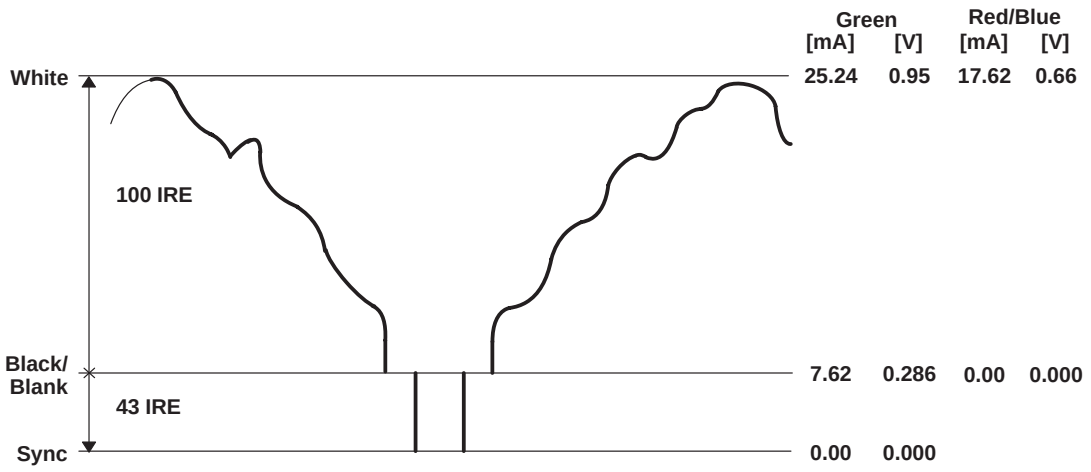


Figure 2–5. 0-IRE, 8-Bit Composite Video Output

NOTE: 75-Ω doubly terminated load. V_{REF} = 1.235 V, R_{SET} = 523 Ω. RS-343A levels and tolerances are assumed.

A resistor (R_{SET}) is needed to connect the FS ADJUST pin to GND to control the magnitude of the full-scale video signal. The IRE relationships in Figures 2–4 and 2–5 are maintained regardless of the full-scale output current.

The relationship between R_{SET} and the full-scale output current IOG is:

$$R_{SET}\ (\Omega) = K1 \times V_{REF}\ (V) / IOG\ (mA)$$

The full-scale output current on IOR and IOB for a given R_{SET} is:

$$IOR, IOB\ (mA) = K2 \times V_{REF}\ (V) / R_{SET}\ (\Omega)$$

where K1 and K2 are defined as:

	IOG		IOR, IOB	
	8-BIT OUTPUT	**6-BIT OUTPUT**	**8-BIT OUTPUT**	**6-BIT OUTPUT**
7.5-IRE	K1 = 11,294	K1 = 11,206	K2 = 8,067	K2 = 7,979
0-IRE	K1 = 10,684	K1 = 10,600	K2 = 7,462	K2 = 7,374

2.8 $\overline{\text{HSYNC}}$, $\overline{\text{VSYNC}}$, and $\overline{\text{BLANK}}$

For the normal modes, $\overline{\text{HSYNC}}$ and $\overline{\text{VSYNC}}$ are active-low pulses. As described in Section 2.3 and Figure 2–2, the $\overline{\text{BLANK}}$, $\overline{\text{HSYNC}}$, and $\overline{\text{VSYNC}}$ inputs are sampled and latched on the falling edge of VCLK in the normal modes, and they are latched on the rising edge of the CLK0 input in the VGA pass-through mode. Refer to Figure 3–2 for the detailed timing.

The $\overline{\text{HSYNC}}$ and $\overline{\text{VSYNC}}$ inputs are used for both the VGA pass-through and normal modes. If the application uses both VGA pass-through and normal modes, an external multiplexer is needed to select $\overline{\text{HSYNC}}$ and $\overline{\text{VSYNC}}$ between VGA pass-through mode and normal mode.

The $\overline{\text{HSYNC}}$, $\overline{\text{VSYNC}}$, and $\overline{\text{BLANK}}$ signals have internal pipeline delays to align with the data at the DAC outputs. The relationship between VCLK and LCLK and the internal VCLK sample and latch delay need to be carefully reviewed and programmed. See Section 2.3 and Figure 2–2 for more details.

As shown in Figure 2–3 for the IOG DAC output, active $\overline{\text{HSYNC}}$ and $\overline{\text{VSYNC}}$ signals turn off the sync current source (after the pipeline delay) independent of the $\overline{\text{BLANK}}$ signal level. In real applications, $\overline{\text{HSYNC}}$ and $\overline{\text{VSYNC}}$ should only be active (low) when $\overline{\text{BLANK}}$ is active (low).

2.9 General Control Register

The general control register is used for sync and pedestal control. Only bits 4 and 5 should be altered. All other bits should be left to their default state. The default is 03h (hex).

Table 2–10. General Control Register Bit Functions

GENERAL CONTROL REGISTER BIT								FUNCTION
7	6	5	4	3	2	1	0	
0	0	X	0	0	0	1	1	0-IRE pedestal (default)
0	0	X	1	0	0	1	1	7.5-IRE pedestal
0	0	0	X	0	0	1	1	Disable sync (default)
0	0	1	X	0	0	1	1	Enable sync

2.9.1 Pedestal Enable Control (Bit 4)

This bit specifies whether a 0- or 7.5-IRE blanking pedestal is to be generated on the video outputs. Having a 0-IRE blanking pedestal means that the black and blank levels are the same.

0: 0-IRE pedestal (default)
1: 7.5-IRE pedestal

2.9.2 Sync Enable Control (Bit 5)

This bit specifies whether or not SYNC information is to be output onto IOG.

0: Disable sync (default)
1: Enable sync

3 Electrical Specifications

3.1 Absolute Maximum Ratings Over Operating Free-Air Temperature Range (Unless Otherwise Noted)†

Supply voltage, V_{DD} (see Note 1) . . . . . 7 V
Input voltage range, V_I . . . . . –0.5 V to V_{DD} + 0.5 V
Analog output short-circuit duration to any power supply or common . . . . . unlimited
Operating free-air temperature range, T_A . . . . . 0°C to 70°C
Storage temperature range . . . . . –65°C to 150°C
Junction temperature . . . . . 175°C
Case temperature for 10 seconds: FN package . . . . . 260°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds . . . . . 260°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values are with respect to the GND terminal.

3.2 Recommended Operating Conditions

		MIN	NOM	MAX	UNIT
V_{DD}	Supply voltage	4.75	5	5.25	V
V_{REF}	Reference voltage	1.15	1.235	1.26	V
V_{IH}	High-level input voltage	2.4		V_{DD} + 0.5	V
V_{IL}	Low-level input voltge			0.8	V
R_L	Output load resistance		37.5		Ω
R_{SET}	FS ADJUST resistor		523		Ω
T_A	Operating free-air temperature	0		70	°C

3.3 Electrical Characteristics

PARAMETER			TEST CONDITIONS	MIN	TYP†	MAX	UNIT
V_{OH}	High-level output voltage		I_{OH} = –800 µA	2.4			V
V_{OL}	Low-level output voltage	D<0:7>, VCLK	I_{OL} = 3.2 mA			0.4	V
I_{IH}	High-level input current		V_I = 2.4 V			1	µA
I_{IL}	Low-level input current		V_I = 0.8 V			–1	µA
I_{DD}	Supply current, pseudo-color mode	TLC34077-110	V_{DD} = 5 V, See Note 2			475	mA
		TLC34077-135				535	
I_{DD}	Supply current, true color mode	TLC34077-110				475	
		TLC34077-135				475	
I_{OZ}	High-impedance-state output currrent					10	µA
C_i	Input capacitance		f = 1 MHz, V_I = 2.4 V		4		pF

† All typical values are at V_{DD} = 5 V, T_A = 25°C.

NOTE 2: I_{DD} is measured with DOTCLK running at the maximum specified frequency, LCLK frequency = DOTCLK frequency/4, and the palette RAM loaded with full-range toggling patterns (00h/00h/FFh/FFh/00h/00h/FFh/FFh/ . . .). Pseudo-color mode is also known as color indexing mode.

3.4 Operating Characteristics

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
	Resolution (each DAC)	8/$\overline{6}$ high		8		bits
		8/$\overline{6}$ low		6		
E_L	End-point linearity error (each DAC)	8/$\overline{6}$ high			1	LSB
		8/$\overline{6}$ low			1/4	
E_D	Differential linearity error (each DAC)	8/$\overline{6}$ high			1	LSB
		8/$\overline{6}$ low			1/4	
	Gray scale error				5%	
	Output current, See Note 4	White level relative to blank	17.69	19.05	20.4	mA
		White level relative to black (7.5 IRE only)	16.74	17.62	18.5	
		Black level relative to blank (7.5 IRE only)	0.95	1.44	1.9	
		Blank level on IOR, IOB	0	5	50	µA
		Blank level on IOG (with SYNC enabled)	6.29	7.6	8.96	mA
		Sync level on IOG (with SYNC enabled)	0	5	50	µA
		One LSB (8/$\overline{6}$ high)		69.1		µA
		One LSB (8/$\overline{6}$ low)		276.4		
	DAC-to-DAC matching			2%	5%	
	DAC-to-DAC crosstalk			–20		dB
V_{OC}	Output compliance		–1		1.2	V
V_{ref}	Voltage reference output voltage		1.15	1.235	1.26	V
	Output impedance			50		kΩ
	Output capacitance	f = 1 MHz, I_{OUT} = 0		13		pF
	Clock and data feedthrough			–20		dB
	Glitch impulse (see Note 3)			50		pV-s
	Pipeline delay	Normal mode	1 LCLK + 9 DOTCLK			periods
		VGA pass-through mode	7.5 DOTCLK			

NOTES: 3. Glitch impulse does not include clock and data feedthrough. The –3-dB test bandwidth is twice the clock rate.

4. Test conditions for RS343-A video signals (unless otherwise specified): “Recommended Operating Conditions”, using external voltge reference VREF = 1.235 V, RSET = 523 Ω. When using the internal voltage reference, RSET may need to be adjusted in order to meet these limits.

3.5 Timing Requirements

PARAMETER		TLC34077-110		TLC34077-135		UNIT
		MIN	MAX	MIN	MAX	
	DOTCLK frequency		110		135	MHz
	CLK0 frequency for VGA pass-through mode		85		85	MHz
t_{cyc}	Clock cycle time	9.1		7.4		ns
t_{su1}	Setup time, RS<0:3> valid before $\overline{RD}$ or $\overline{WR}$ ↓	10		10		ns
t_{h1}	Hold time, RS<0:3> valid after $\overline{RD}$ or $\overline{WR}$ ↓	10		10		ns
t_{su2}	Setup time, D<0:7> valid before $\overline{WR}$ ↑	35		35		ns
t_{h2}	Hold time, D<0:7> valid after $\overline{WR}$ ↑	0		0		ns
t_{su3}	Setup time, VGA<0:7> and $\overline{HSYNC}$, $\overline{VSYNC}$, and $\overline{VGABLANK}$ valid before CLK0 ↑	2		2		ns
t_{h3}	Hold time, VGA<0:7> and $\overline{HSYNC}$, $\overline{VSYNC}$, and $\overline{VGABLANK}$ valid after CLK0 ↑	2		2		ns
t_{su4}	Setup time, P<0:31> valid before LCLK ↑	2		0		ns
t_{h4}	Hold time, P<0:31> valid after LCLK ↑	5		5		ns
t_{su5}	Setup time, $\overline{HSYNC}$, $\overline{VSYNC}$, and $\overline{BLANK}$ valid before VCLK ↓	5		5		ns
t_{h5}	Hold time, $\overline{HSYNC}$, $\overline{VSYNC}$, and $\overline{BLANK}$ valid after VCLK ↓	2		2		ns
t_{w1}	Pulse duration, $\overline{RD}$ or $\overline{WR}$ low	50		50		ns
t_{w2}	Pulse duration, $\overline{RD}$ or $\overline{WR}$ high	30		30		ns
t_{w3}	Pulse duration, clock high	3.5		3		ns
t_{w4}	Pulse duration, clock low	3.5		3		ns

NOTE 5: TTL input signals are 0 to 3 V with less than 3 ns rise/fall time between the 10% and 90% levels unless otherwise specified. For input and output signals, timing reference points are at the 10% and 90% signal levels. Analog output loads are less than 10 pF. D<0:7> output loads are less than 50 pF. All other output loads are less than 50 pF, unless otherwise specified.

3.6 Switching Characteristics

TL34077-110, TLC34077-135

PARAMETER		TLC34077-110			TLC34077-135			UNIT
		MIN	TYP	MAX	MIN	TYP	MAX	
	LCLK frequency			85			85	MHz
	VCLK frequency			85			85	MHz
t_{en1}	Enable time, $\overline{RD}$ low to D<0:7> valid			40			40	ns
t_{dis1}	Disable time, $\overline{RD}$ high to D<0:7> disabled			17			17	ns
t_{v1}	Valid time, D<0:7> valid after $\overline{RD}$ high	5			5			ns
t_{d1}	Delay time, $\overline{RD}$ low to D<0:7> starting to turn on	5			5			ns
t_{d2}	Delay time, selected input clock high/low to DOTCLK (internal signal) high/low		7			7		ns
t_{d3}	Delay time, DOTCLK high/low to VCLK high/low		6			6		ns
t_{d4}	Delay time, VCLK high/low to LCLK high/low (see Note 6)	0		5	0		5	ns
t_{d5}	Delay time, DOTCLK high/low to LCLK high/low		8			8		ns
t_{d6}	Delay time, DOTCLK high to IOR/IOG/IOB active (analog output delay time) (see Note 7)		20			20		ns
t_{d7}	Analog output settling time (see Note 8)			6			6	ns
t_r	Analog output rise time (see Note 9)		2			2		ns
	Analog output skew	0		2	0		2	ns

NOTES: 6. VCLK frequency = SCLK frequency.
7. Measured from the 90% point of the rising edge of DOTCLK to 50% of the full-scale transition.
8. Measured from the 50% point of the full-scale transition to the point at which the output has settled, within ± 1 LSB (settling time does not include clock and data feedthrough).
9. Measured between 10% and 90% of the full-scale transition.

3.7 Timing Diagrams

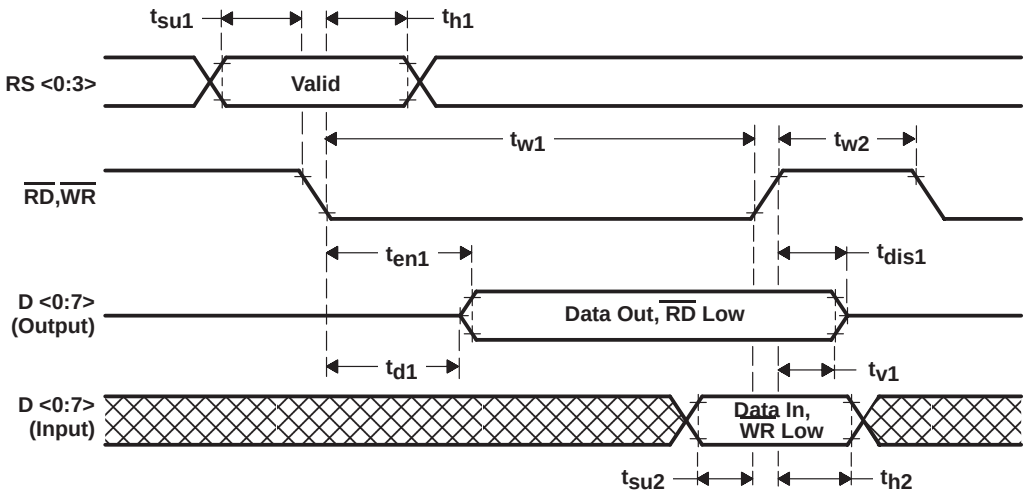


Figure 3–1. MPU Interface Timing

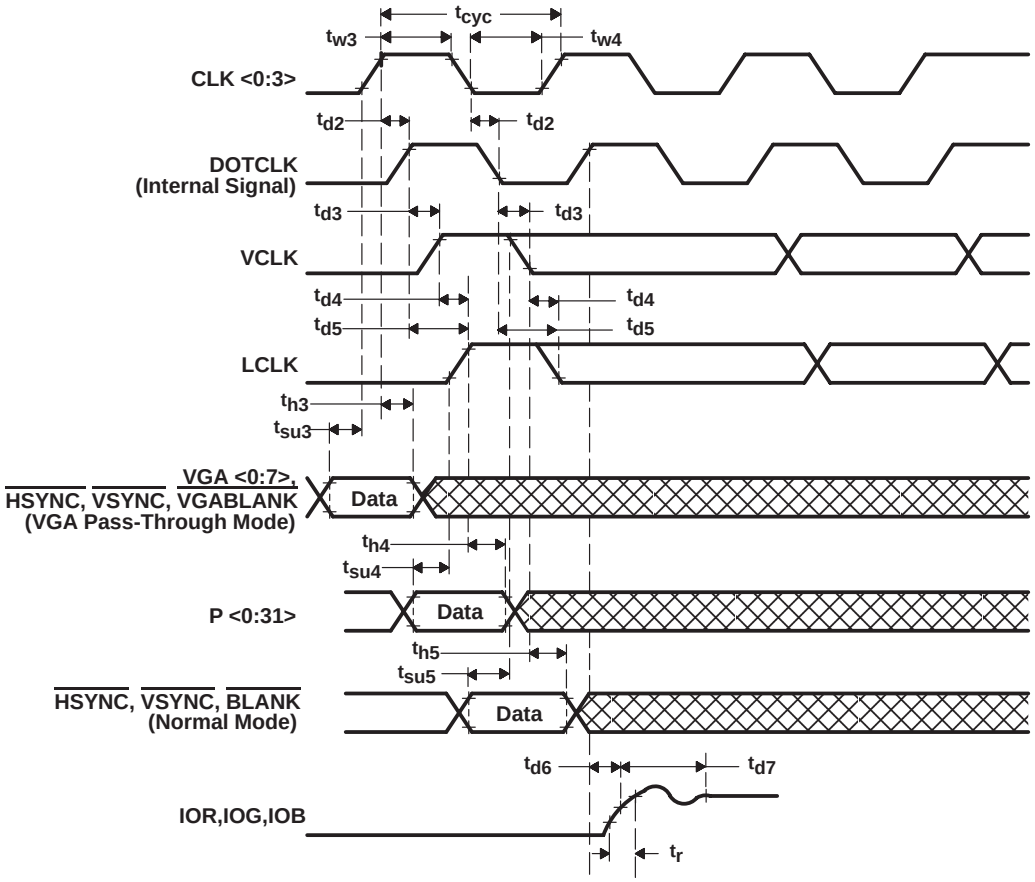


Figure 3–2. Video Input/Output

Appendix A
VCLK and the TMS340x0

While the TLC34077 VCLK output is designed for compatibility with all graphics systems, it is also tightly coupled with the TMS340x0 graphics system processors. All the timing requirements of the TMS340x0 have been considered. However, there are a few points that need to be explained with regard to applications.

VCLK

All the video control signals in the TMS340x0 (i.e., $\overline{\text{BLANK}}$, $\overline{\text{HSYNC}}$, and $\overline{\text{VSYNC}}$) are triggered and generated from the falling edge of VCLK. The fact that the TLC34076 uses the falling edge to sample and latch the $\overline{\text{BLANK}}$ input gives users maximum freedom to choose the frequency of VCLK and interconnect the TLC34077 with the TMS340x0 GSP without glue logic. Needless to say, the VCLK frequency needs to be selected to be compatible with the minimum VCLK period required by the TMS340x0.

Appendix B
PC Board Layout Considerations

PC Board Considerations

A four-layer PC board should be used with the TLC34077: one layer each for 5-V power and GND and two layers for signals. The layout should be optimized for the lowest-possible noise on the TLC34077 power and ground lines by shielding the digital inputs and providing good decoupling. The lead length between groups of V_{DD} and GND pins should be minimized so as to reduce inductive ringing. The terminal assignments for the TLC34077 P<0:31> inputs were selected for minimum interconnect lengths between these inputs and the VRAM pixel data outputs. The TLC34077 should be located as close to the output connectors as possible to minimize noise pickup and reflections due to impedance mismatching.

Ground Plane

A single ground plane is recommended for both the TLC34077 and the rest of the logic. Separate digital and analog ground planes are not needed.

Power Plane

Split power planes are recommended for the TLC34077 and the rest of the logic. The TLC34077 and its associated analog circuitry should have their own power plane (referred to as A_{VCC} in Figure B–1). The two power planes should be connected at a single point through a ferrite bead as shown in Figures B–1, B–2, and B–3. This bead should be located within three inches of the TLC34077.

Supply Decoupling

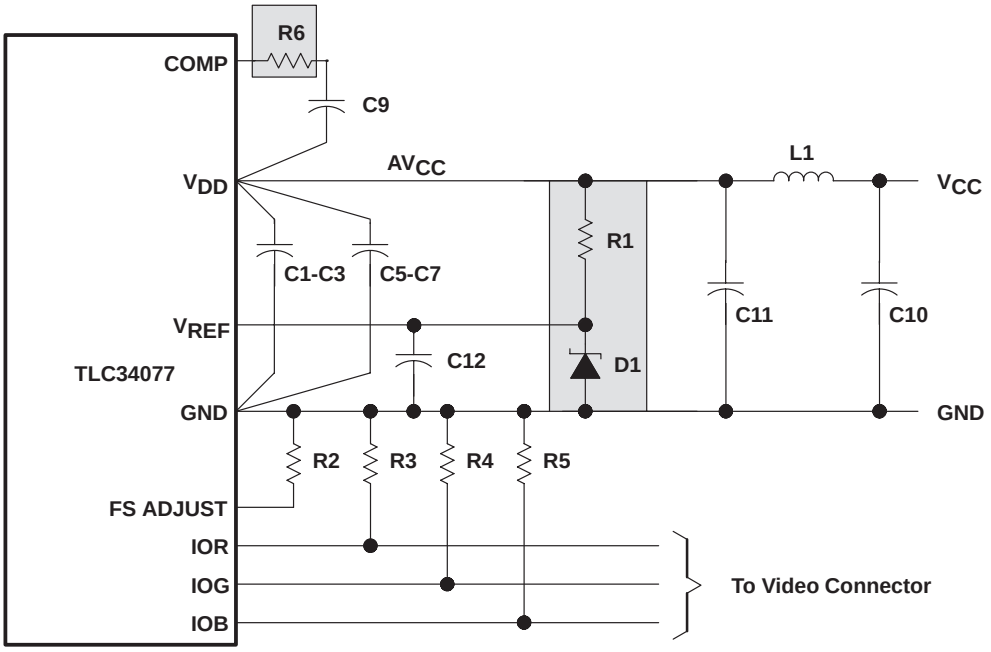
Bypass capacitors should be installed using the shortest leads possible, consistent with reliable operation, to reduce the lead inductance.

For the best performance, a 0.1-μF ceramic capacitor in parallel with a 0.01-μF chip capacitor should be used to decouple each of the three groups of power pins to GND. These capacitors should be placed as close as possible to the device as shown in Figure B–2.

If a switching power supply is used, the designer should pay close attention to reducing power supply noise and should consider using a three-terminal voltage regulator for supplying power to A_{VCC}.

COMP and V_{REF} Terminals

A 100-Ω resistor (optional) and 0.1-μF ceramic capacitor (approximate values) should be connected in series between the device's COMP and V_{DD} terminals in order to avoid noise and color-smearing problems. Also, whether an internal or external voltage reference is used, a 0.1-μF capacitor should be connected between the device's V_{REF} and GND terminals to further stabilize the video image. These resistor and capacitor values may vary depending on the board layout; experimentation may be required in order to determine optimum values.



LOCATION	DESCRIPTION
C1-C3, C9-C10, C12	0.1-μF ceramic capacitor
C5-C7	0.01-μF ceramic chip capacitor
C11	33-μF tantalum capacitor
L1	ferrite bead
R1	1000-Ω 1% metal-film resistor
R2	523-Ω 1% metal-film resistor
R3, R4, R5	75-Ω 1% metal-film resistor
R6	100-Ω 5% resistor
D1	1.2-V voltage reference

Figure B–1. Typical Connection Diagram and Components (Shaded Area is Optional)

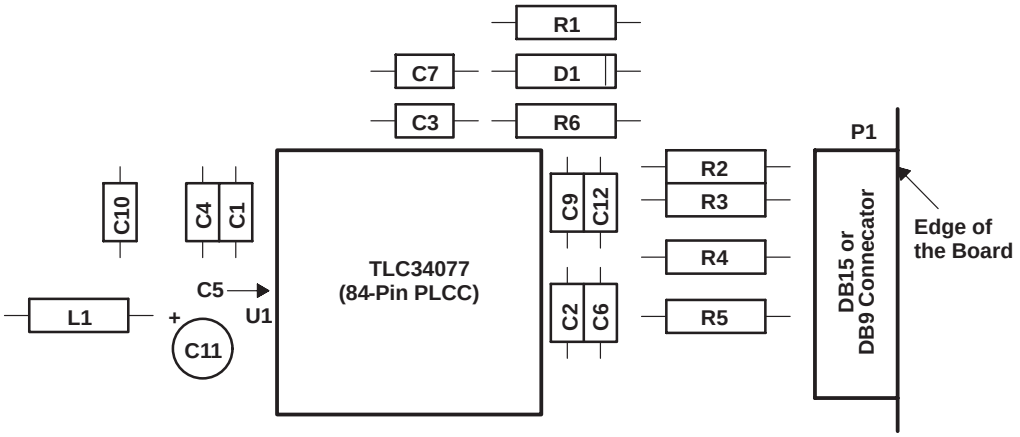


Figure B–2. Typical Component Placement (Component Side)

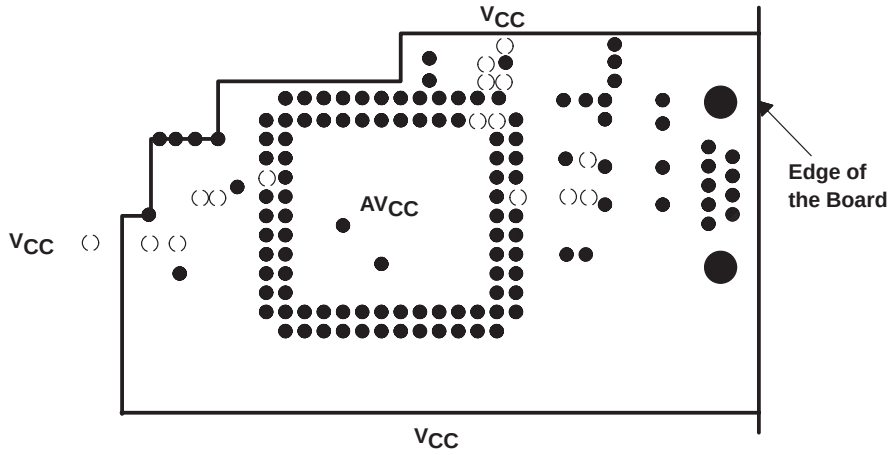
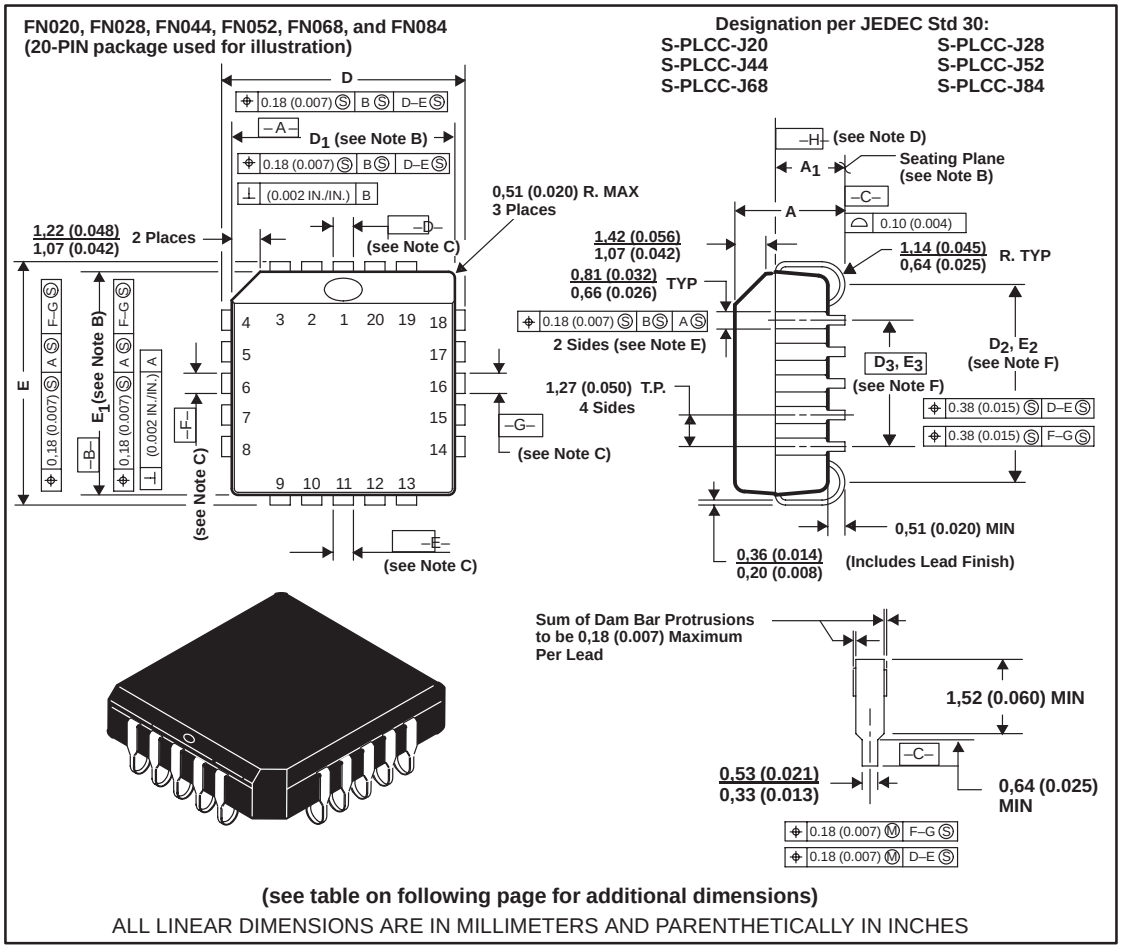


Figure B–3. Typical Split Power Plane (Solder Side)

Appendix C
Mechanical Data

FN020, FN028, FN044, FN052, FN068, and FN084 plastic J-leaded chip carrier

Each of these chip carrier packages consists of a circuit mounted on a lead frame and enncapsulated within an electrically nonconductive plastic compound. The compound withstands soldering temperatures with no deformation, and circuit performance characteristics remain stable when the devices are operated in high-humidity conditions. The package is intended for surface mounting on 1,27 (0.050) centers. Leads require no additional cleaning or processing when used in soldered assembly.



(see table on following page for additional dimensions)

ALL LINEAR DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES

Mechanical Data

FN020, FN028, FN044, FN052, FN068, and FN084 plastic J-leaded chip carrier (continued)

JEDEC	NO. OF	A		A_1		D, E		D_1, E_1		D_2, E_2		D_3, E_3
OUTLINE	PINS	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	BASIC
MO-047AA	20	4,19 (0.165)	4,57 (0.180)	2,29 (0.090)	3,05 (0.120)	9,78 (0.385)	10,03 (0.395)	8,89 (0.350)	9,04 (0.356)	7,37 (0.290)	8,38 (0.330)	5,08 (0.200)
MO-047AB	28	4,19 (0.165)	4,57 (0.180)	2,29 (0.090)	3,05 (0.120)	12,32 (0.485)	12,57 (0.495)	11,43 (0.450)	11,58 (0.456)	9,91 (0.390)	10,92 (0.430)	7,62 (0.300)
MO-047AC	44	4,19 (0.165)	4,57 (0.180)	2,29 (0.090)	3,05 (0.120)	17,40 (0.685)	17,65 (0.695)	16,51 (0.650)	16,66 (0.656)	14,99 (0.590)	16,00 (0.630)	12,70 (0.500)
MO-047AD	52	4,19 (0.165)	5,08 (0.200)	2,29 (0.090)	3,30 (0.130)	19,94 (0.785)	20,19 (0.795)	19,05 (0.750)	19,20 (0.756)	17,53 (0.690)	18,54 (0.730)	15,24 (0.600)
MO-047AE	68	4,19 (0.165)	5,08 (0.200)	2,29 (0.090)	3,30 (0.130)	25,02 (0.985)	25,27 (0.995)	24,13 (0.950)	24,33 (0.958)	22,61 (0.890)	23,62 (0.930)	20,32 (0.800)
MO-047AF	84	4,19 (0.165)	5,08 (0.200)	2,29 (0.090)	3,30 (0.130)	30,10 (1.185)	30,35 (1.195)	29,21 (1.150)	29,41 (1.141)	27,69 (1.090)	28,70 (1.130)	25,40 (1.000)

NOTES: A. All dimensions conform to JEDEC Specification MO-047AA/AF. Dimensions and tolerancing are per ANSI Y14.5M – 1982.

B. Dimensions D_1 and E_1 do not include mold flash protrusion. Protrusion shall not exceed 0,25 (0.010) on any side. Centerline of center pin each side is within 0,10 (0.004) of package centerline by dimension B. The lead contact points are planar within 0,10 (0.004).

C. Datums $\boxed{\text{D – E}}$ and $\boxed{\text{F – G}}$ for center leads are determined at datum $\boxed{\text{– H –}}$.

D. Datum $\boxed{\text{– H –}}$ is located at top of leads where they exit plastic body.

E. Location of datums $\boxed{\text{– A –}}$ and $\boxed{\text{– B –}}$ to be determined at datum $\boxed{\text{– H –}}$.

F. Determined at seating plane $\boxed{\text{– C –}}$.

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