Video Subsystem

The system video is generated by the IBM Video Graphics Array (VGA) and its associated circuitry. The associated circuitry consists of the video memory and a video digital to analog converter (DAC). The 256K bytes of video memory consists of four 64K by 8 memory maps. The red, green, and blue (RGB) outputs from the video DAC drive 31.5 kHz direct drive analog displays.

All video modes available on the IBM Monochrome Display Adapter, IBM Color/Graphics Monitor Adapter, and IBM Enhanced Graphics Adapter are supported, regardless of which analog display is connected. All video modes supported by the video subsystem are available on all of the supported analog displays. Colors will be displayed as shades of gray when the monochrome analog display is connected.

The new modes available are:

- 640 x 480 graphics in both 2 and 16 colors
- 720 x 400 alphanumeric in both 16-color and monochrome
- 360 x 400 16-color alphanumeric
- 320 x 200 graphics with 256 colors.

In addition, all 200 line modes are double scanned by the video subsystem and displayed as 400 lines on the display. This means that each one-pel-high horizontal scan line is displayed twice on the display.

The VGA does the interfacing between the system microprocessor and video memory. All data passes through the VGA when the system microprocessor writes to or reads from video memory. The VGA controls the arbitration for video memory between the system microprocessor and the cathode-ray tube (CRT) controller function contained within the VGA. Programs do not need to wait for horizontal retrace to update the display buffer. The system microprocessor will receive better performance when accessing the display buffer during non-active display times, because there is less interference from the CRT controller.

Video memory addressing is controlled by the VGA. The starting address of the video memory is programmable to three different starting addresses for compatibility with previous video adapters. BIOS will program the VGA appropriately during a video mode set.

In alphanumeric modes, the system microprocessor writes ASCII character code and attribute data to the video memory maps 0 and 1 respectively. The character generator is stored in video map 2 and is loaded by BIOS during an alphanumeric video mode set. BIOS downloads the character generator data (character generator = font = character set) from system ROM. Three fonts are contained in ROM. Two fonts contain dot patterns identical to those provided by the IBM Monochrome Display Adapter, the IBM Color/Graphics Monitor Adapter, and the IBM Enhanced Graphics Adapter. The third font is a new 8 x 16 character font. Up to eight 256-character fonts can be loaded into video memory map 2 at one time (the IBM Enhanced Graphics Adapter allows up to four fonts). A BIOS interface exists to load user-defined fonts. As on the IBM Enhanced Graphics Adapter, a register selects which font is actually used to form characters. Also, as on the IBM Enhanced Graphics Adapter, the intensity bit in the attribute byte may be redefined as a switch between two 256-character fonts. This allows 512 characters to be displayed on the screen at one time. See "Character Map Select Register," on page 4-68, and "Ram Loadable Character Generator" on page 4-112 for more information.

The VGA formats the information stored in video memory into an 8-bit digital value that is sent to the video DAC. This 8-bit value allows access to a maximum of 256 registers inside the video DAC. For example, in the 2-color graphics modes, only two different 8-bit values would be presented to the video DAC. In the 256-color graphics mode, 256 different 8-bit values would be presented to the video DAC. Each register inside the video DAC contains a color value that is selected from a choice of 256K colors.

The video DAC outputs three analog color signals (red, green, and blue) that are sent to the 15-pin display connector. The monochrome analog display uses only the green analog output. This output is used to determine the shade of gray that will be displayed.

The video subsystem supports attachment of only 31.5 kHz direct drive analog displays. Other IBM displays are *not* supported because

they have digital interfaces, or have a different horizontal sweep frequency.

A BIOS call exists to enable or disable the VGA. Disable means that the VGA will not respond to video memory or I/O reads or writes. The contents of registers and video memory are preserved with the values present when the disable is invoked. Because of this, the VGA continues to generate valid video output if it is doing so before it is disabled.

Compatibility with other hardware is best achieved by using the BIOS interface whenever possible. If an application is forced to write directly to the VGA, the following rules should be followed.

- When programming address registers, all currently reserved bits should be set to 0 to maximize compatibility with other hardware.
- When programming data registers, all currently reserved bits should be read out and written back unmodified to maximize compatibility with other hardware.

Previous video adapters required that the video mode used correspond to the display attached. For example, the IBM Enhanced Graphics Adapter required that the Enhanced Color Display be attached to run mode hex (3*), and required that the monochrome display be attached to run mode hex 7. All the modes supported by the VGA are supported by the IBM 31.5 kHz direct drive analog displays. Colors are displayed as shades of gray when the monochrome analog display is connected. Circuitry exists on the system board to detect which type of analog display is connected (color or monochrome). BIOS maps (sums) the colors into shades of gray.

The Auxiliary Video connector is a 20-pin connector located in line with one of the channel connectors on the system board. This connector allows passing of video data from the VGA to an adapter plugged into a channel connector. Also, the system board video buffers can be turned off and video from the adapter can drive the video DAC and the 15-pin connector that drives the analog display. The full channel is available for use by the adapter. For more information on the Auxiliary Video Connector see "Auxiliary Video Connector" on page 4-119.

The following is a block diagram of the video subsystem, which is part of the system board.

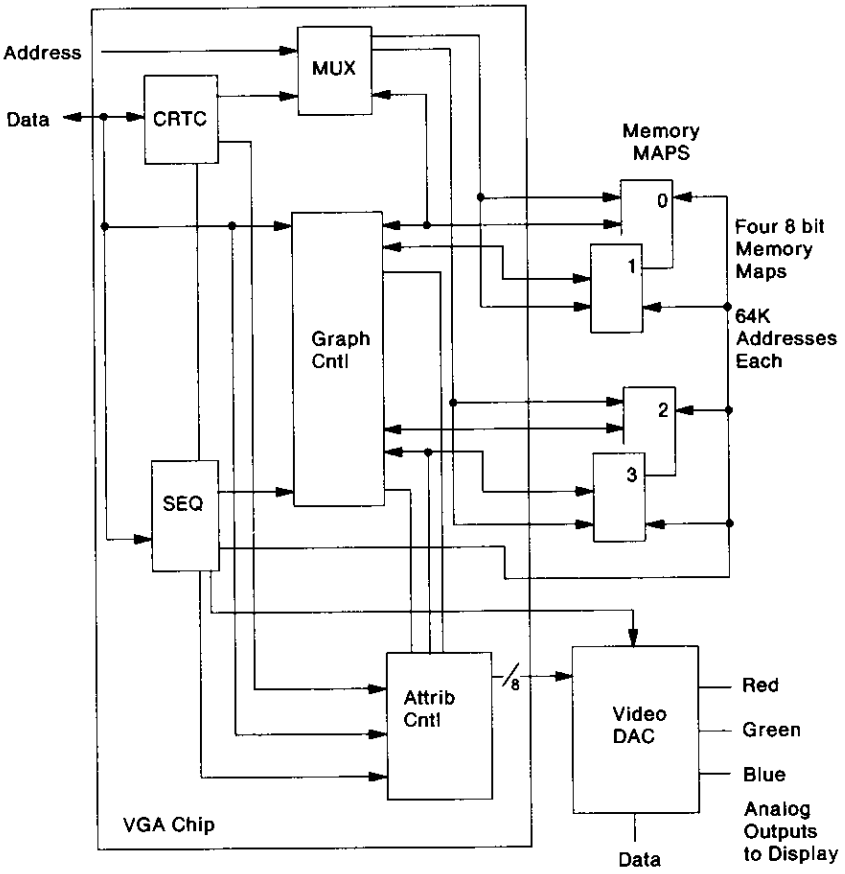

Figure 4-11. Video Subsystem Block Diagram

Major Components

Most of the logic for the VGA is contained in one module. This module contains all the circuits necessary to generate the timing for the video memory, and generates the video information that goes to the video digital-to-analog converter (DAC).

BIOS ROM

Software support is provided by video BIOS. Video BIOS is part of the system BIOS. BIOS is contained in a read-only memory (ROM) on the system board. This ROM BIOS contains the character generators and the control code to run the video subsystem.

Support Logic

Two clock sources (25.175 MHz and 28.322 MHz) provide the dot rate. The clock source is selected by setting a bit in a sequencer register. This is done by BIOS when a mode set is done.

The digital video output is sent to the digital-to-analog converter (DAC), which contains a color look-up table. Three analog signals (red, green, blue) are output from the DAC and are then sent to the display. Also see the attribute controller block diagram on page 4-26 and the auxiliary video connector block diagram on page 4-120. The 'sync' signals to the monitor are TTL levels. The analog video signals are 0 to 0.7 volts.

The maximum number of colors displayed is 16 out of 256K[1], except mode hex 13, which can display 256 out of 256K. The maximum number of shades of gray is 16 out of 64, except mode hex 13, which can display 64 out of 64 shades of gray.

Video Graphics Array Components

The Video Graphics Array has four major components. They are: the CRT Controller, the Sequencer, the Graphics Controller, and the Attribute Controller.

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1 K = 1024

CRT Controller

The Cathode Ray Tube Controller (CRTC) generates horizontal and vertical synchronous timings, addressing for the regenerative buffer, cursor and underline timings, and refresh addressing for the dynamic RAMs.

Sequencer

The Sequencer generates basic memory timings for the dynamic RAMs and the character clock for controlling regenerative memory fetches. It allows the system microprocessor to access memory during active display intervals by inserting dedicated system microprocessor memory cycles periodically between the display memory cycles. Map mask registers are available to protect entire memory maps from being changed.

Graphics Controller

The graphics controller is the interface between video memory and both the attribute controller during active display times and the system microprocessor during video memory reads or writes. During display times, memory data is latched and sent to the attribute controller. In All Points Addressable (APA) modes, the parallel memory data is converted to serial bit-plane data before being sent; in alphanumeric (A/N) modes, the parallel attribute data is sent directly. During a system microprocessor write or read to video memory, the graphics controller can perform logical operations on the memory data before it reaches video memory or the system microprocessor data bus, respectively. These logical operations are composed of four logical write modes and two logical read modes. These features allow enhanced operations such as a color compare read mode, individual bit masking during write modes, 32-bit writes in a single memory cycle, and writing to the display buffer on non-byte boundaries.

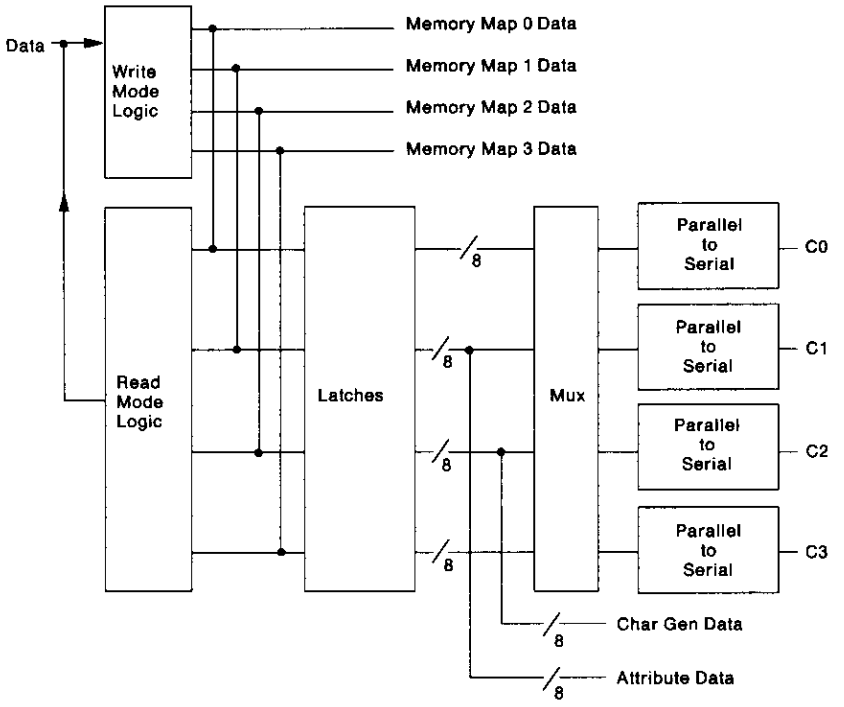


Figure 4-12. Graphics Controller Block Diagram

Attribute Controller

The attribute controller takes in data from video memory via the graphics controller and formats it for display on the display screen. Incoming attribute data in A/N mode, and serialized bit-plane data in APA mode, is converted to an 8-bit output digital color value. Each output color value is selected from an internal color palette of 64 possible colors (except in 256-color mode). The output color value is sent to the integrated DAC, where it is used as an address into an 18-bit color register whose value is in turn converted to three analog color signals that drive the display. Blinking, underlining, cursor insertion, and PEL panning are also controlled in the attribute controller.

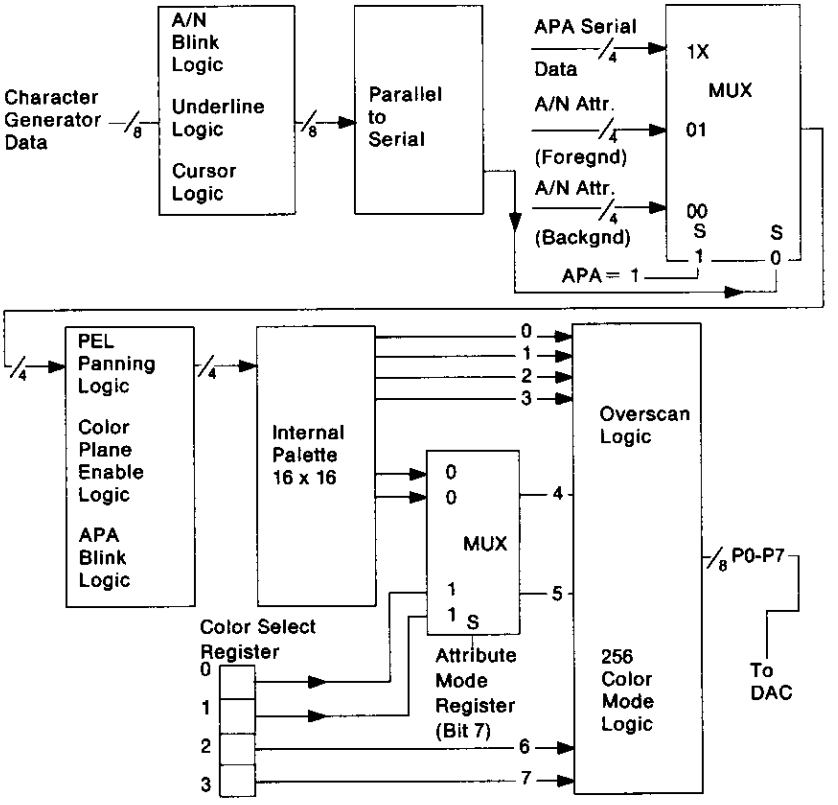


Figure 4-13. Attribute Controller Block Diagram

Modes of Operation

The following figure describes the modes supported by BIOS on IBM 31.5 kHz direct drive analog color and monochrome displays.

Mode (hex)	Type	Colors	Alpha Format	Buffer Start	Box Size	Max. Pgs.	Vert. Freq.	PELS
0, 1	A/N	16/256K	40 x 25	B8000	8 x 8	8	70 Hz	320 x 200
2, 3	A/N	16/256K	80 x 25	B8000	8 x 8	8	70 Hz	640 x 200
0*, 1*	A/N	16/256K	40 x 25	B8000	8 x 14	8	70 Hz	320 x 350
2*, 3*	A/N	16/256K	80 x 25	B8000	8 x 14	8	70 Hz	640 x 350
0+, 1+	A/N	16/256K	40 x 25	B8000	9 x 16	8	70 Hz	360 x 400
2+, 3+	A/N	16/256K	80 x 25	B8000	9 x 16	8	70 Hz	720 x 400
4, 5	APA	4/256K	40 x 25	B8000	8 x 8	1	70 Hz	320 x 200
6	APA	2/256K	80 x 25	B8000	8 x 8	1	70 Hz	640 x 200
7	A/N	-	80 x 25	B0000	9 x 14	8	70 Hz	720 x 350
7+	A/N	-	80 x 25	B0000	9 x 16	8	70 Hz	720 x 400
D	APA	16/256K	40 x 25	A0000	8 x 8	8	70 Hz	320 x 200
E	APA	16/256K	80 x 25	A0000	8 x 8	4	70 Hz	640 x 200
F	APA	-	80 x 25	A0000	8 x 14	2	70 Hz	640 x 350
10	APA	16/256K	80 x 25	A0000	8 x 14	2	70 Hz	640 x 350
11	APA	2/256K	80 x 30	A0000	8 x 16	1	60 Hz	640 x 480
12	APA	16/256K	80 x 30	A0000	8 x 16	1	60 Hz	640 x 480
13	APA	256/256K	40 x 25	A0000	8 x 8	1	70 Hz	320 x 200

* Enhanced modes from the IBM Enhanced Graphics Adapter.
\+ Enhanced modes

Figure 4-14. BIOS Video Modes

When the color display is used, each color is selected from a palette of 256K colors.

When the monochrome display is used, the colors are displayed as shades of gray. Each shade of gray is selected from a palette of 64.

Modes hex 0 through 6 emulate the support provided by the IBM Color/Graphics Monitor Adapter.

Modes hex 0, 2 and 4 are identical to modes hex 1,3 and 5 respectively. On the Color/Graphics Monitor Adapter there was a difference in these modes. On modes hex 0, 2, and 4, the color burst was turned off. Color burst is not provided by the video subsystem. Mode hex 3+ is the default mode with an analog color display attached to the system. Mode hex 7+ is the default mode with an analog monochrome display attached to the system.

Mode hex 7 emulates the support provided by the IBM Monochrome Display Adapter.

Modes hex 0*, 1*, 2*, 3*, D, E, F, and 10 emulate the support provided by the IBM Enhanced Graphics Adapter.

Double-scan means that each horizontal scan line is displayed twice, This is used for 200-line modes; they are displayed as 400 lines on the display. Border support is dependent on the BIOS mode selected. The following shows which BIOS modes support Double Scan and Border.

Mode (hex)	Double Scan	Border Support
0, 1	Yes	No
2, 3	Yes	Yes
0*, 1*	No	No
2*, 3*	No	Yes
0+, 1+	No	No
2+, 3+	No	Yes
4, 5	Yes	No
6	Yes	Yes
7	No	Yes
7+	No	Yes
D	Yes	No
E	Yes	Yes
F	No	Yes
10	No	Yes
11	No	Yes
12	No	Yes
13	Yes	Yes

* Enhanced modes from the IBM Enhanced Graphics Adapter.
\+ Enhanced modes

Figure 4-15. BIOS Double Scan and Border Support

Display Support

The video subsystem supports attachment of 31.5 kHz horizontal sweep frequency direct drive analog displays. These displays have a vertical sweep frequency capability of 50 to 70 cycles per second, providing extended color and sharpness and reduced flicker in most modes. Other IBM displays are *not* supported because they have digital interfaces, or have a different horizontal and vertical sweep frequency. The following figure summarizes the analog display characteristics.

Parameter	Color	Monochrome
Horizontal Scan Rate	31.5 kHz	31.5 kHz
Vertical Scan Rate	50 to 70 Hz	50 to 70 Hz
Video Bandwidth	28 MHz	28 MHz
Displayable Colors*	256/256K Maximum	64/64 Shades Gray
Maximum Horizontal Resolution	720 PELs	720 PELs
Maximum Vertical Resolution	480 PELs	480 PELs

* Controlled by Video Circuit

Figure 4-16. IBM 31.5 kHz Direct Drive Analog Displays

Since both color and monochrome displays run at the same sweep rate, all modes work on either type. The vertical gain of the display is controlled by the polarity of the vertical and horizontal sync pulses. This is done so that 350, 400, or 480 lines can be displayed without adjusting the display. See "15-Pin Display Connector Timing (Sync Signals)" on page 4-121 for more information.

Video Subsystem Programmable Option Select

The video subsystem supports Programmable Option Select (POS). When the POS sleep bit is set, the video subsystem does not respond to any memory or I/O reads or writes. Video is still generated if the video subsystem is programmed to do so. Programmable Option Select has to be enabled for video subsystem operation.

The implementation of Programmable Option Select (POS) for the video subsystem is described below:

- When in setup mode (I/O address hex 0094, bit 5 equals 0) the VGA responds to a single option select byte at I/O address hex 0102 and treats the LSB (bit 0) of that byte as the VGA sleep bit. When the LSB equals 0, the VGA does not respond to commands, addresses, or data, on the data bus. When the LSB equals 1 the VGA responds. If the VGA was set up and is generating video output when the LSB is set to 0, the output is still generated.
- The VGA responds only to address hex 0102 when in the setup mode. No other addresses are valid at that time. Conversely, the VGA ignores address hex 0102 when in the enabled mode (I/O address hex 0094, bit 5 equals 1), and decodes normal I/O and memory addresses.

Note: When VGA is disabled, accesses to the video DAC registers are disabled.

When the system is powered on, the power-on self-test (POST) initializes and enables the video subsystem.

For information on BIOS calls to enable or disable the VGA, see the *IBM Personal System/2 and Personal Computer BIOS Interface Technical Reference*.

Alphanumeric Modes

This section describes the alphanumeric modes supported by the video subsystem and BIOS. Note that the colors in this section are generated when the BIOS is used to set the mode. BIOS initializes the video subsystem and the video DAC palette to generate these colors. If the video DAC palette is changed, different colors are generated.

The alphanumeric modes are modes hex 0 - 3 and 7. The mode chart lists the variations of these modes. The data format for alphanumeric modes is the same as the data format on the IBM Color/Graphics Monitor Adapter, the IBM Monochrome Display Adapter, and the IBM Enhanced Graphics Adapter. As in the EGA, bit 3 of the attribute byte may be redefined by the Character Map Select register to act as a switch between character sets. This gives the programmer access to 512 characters at one time.

When an alphanumeric mode is selected, the BIOS transfers character patterns from the ROM to map 2. The system microprocessor stores the character data in map 0, and the attribute data in map 1. The programmer can view map 0 and 1 as a single buffer in alphanumeric modes. The CRTC generates sequential addresses, and fetches one character code byte and one attribute byte at a time. The character code and row scan count are combined to address map 2, which contains the character generators. The appropriate dot patterns are then sent to the palette in the attribute section, where color is assigned according to the attribute data.

Every display-character position in the alphanumeric mode is defined by two bytes in the display buffer. Both the color/graphics and the monochrome emulation modes use the following 2-byte character/attribute format.

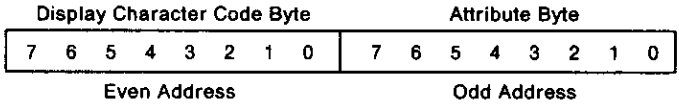


Figure 4-17. Character/Attribute Format

See Section 8, "Characters and Keystrokes" on page 8-1, for characters loaded during BIOS mode sets.

The functions of the attribute byte are defined in the following table:

Attribute Function	Attribute Byte							
	7	6	5	4	3	2	1	0
	B/I	R	G	B	I/CS	R	G	B
	Background				Foreground			
Normal (White on Black)	B/I	0	0	0	I/CS	1	1	1
Reverse (Black on White)	B/I	1	1	1	I/CS	0	0	0
Nondisplay (Black)	B/I	0	0	0	I/CS	0	0	0
Nondisplay (White)	B/I	1	1	1	I/CS	1	1	1
Mono = Underline / Color = Blue	B/I	0	0	0	I/CS	0	0	1

I = Highlighted
B = Blinking Foreground (Character)
CS = Character select

The BIOS defaults on a mode set are blink for bit 7 (B/I), and intensity for bit 3 (I/CS).

Figure 4-18. Attribute Byte Functions

The attribute byte definitions are:

Bit	Color	Function
7	B/I	Blinking/Background Intensity
6	R	Background Color
5	G	
4	B	
3	I/CS	Intensity/Character Select
2	R	Foreground Color
1	G	
0	B	

This figure shows the same information as the previous figure. It is included here for clarity.

Figure 4-19. Attribute Byte Definitions

For more information about the attribute byte, see "Character Map Select Register" on page 4-68 and "Attribute Mode Control Register" on page 4-102.

Any other code combination produces white-on-white in the monochrome emulation mode and the following colors in the color emulation mode:

I	R	G	B	Color
0	0	0	0	Black
0	0	0	1	Blue
0	0	1	0	Green
0	0	1	1	Cyan
0	1	0	0	Red
0	1	0	1	Magenta
0	1	1	0	Brown
0	1	1	1	White
1	0	0	0	Gray
1	0	0	1	Light Blue
1	0	1	0	Light Green
1	0	1	1	Light Cyan
1	1	0	0	Light Red
1	1	0	1	Light Magenta
1	1	1	0	Yellow
1	1	1	1	White (High Intensity)

Figure 4-20. Attribute Byte Colors

Both 40 column and 80 column alphanumeric modes are supported. The 40-column alphanumeric modes (all variations of modes hex 0 and 1) have the following features:

- Display up to 25 rows of 40 characters each
- Require 2,000 bytes of read/write memory per page
- One character and attribute for each character.

The 80-column alphanumeric modes (all variations of modes hex 2, 3, and 7) have the following features:

- Display up to 25 rows of 80 characters each
- Require 4,000 bytes of read/write memory per page
- One character and attribute for each character.

Graphics Modes

This section describes the graphics modes supported by the video subsystem and BIOS. Note that the colors in this section are generated when the BIOS is used to set the mode. BIOS initializes the video subsystem and the video DAC palette to generate these colors. If the video DAC palette is changed, different colors are generated.

320 x 200 Four-Color Graphics (Modes Hex 4 and 5)

Addressing, mapping and data format are the same as the 320 x 200 PEL mode of the IBM Color/Graphics Monitor Adapter. The display buffer is configured at hex B8000. Bit image data is stored in memory maps 0 and 1. The two bit planes (C0 and C1) are each formed from bits from both memory maps.

This mode has the following features:

- Contains a maximum of 200 rows of 320 PELs
- Selects one of four colors for each PEL
- Requires 16,000 bytes of read/write memory
- Uses memory-mapped graphics
- Double-scanned on display to 400 rows
- Formats four PELs-per-byte in the following manner:

Bit	Function
7	C1 - First Display PEL
6	C0 - First Display PEL
5	C1 - Second Display PEL
4	C0 - Second Display PEL
3	C1 - Third Display PEL
2	C0 - Third Display PEL
1	C1 - Fourth Display PEL
0	C0 - Fourth Display PEL

Figure 4-21. PEL Format, Modes hex 4 and 5

- Organizes graphics memory in two banks of 8,000 bytes, using the following format:

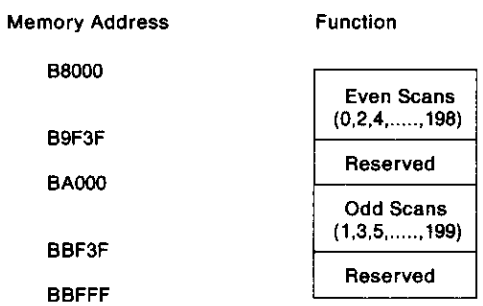


Figure 4-22. Video Memory Format

Address hex B8000 contains the PEL information for the upper-left corner of the display area.

- Color selection is determined by the following:

C1	C0	Color Selected	
0	0	Black	
0	1	Light Cyan	* Green
1	0	Light Magenta	* Red
1	1	Intensified White	* Brown

* Selectable by a video BIOS call

Figure 4-23. Color Selections, Modes Hex 4 and 5

640 x 200 Two Color Graphics (Mode Hex 6)

Addressing, mapping and data format are the same as the 640 x 200 PEL black and white mode of the IBM Color/Graphics Monitor Adapter. The display buffer is configured at hex B8000. Bit image data is stored in memory map 0 and comprises a single bit plane (C0).

This mode has the following features:

- Contains a maximum of 200 rows of 640 PELs.
- Supports two colors only.
- Requires 16,000 bytes of read/write memory.
- Addressing and mapping procedures are the same as 320 x 200 two- and four-color graphics, but the data format is different. In this mode, each bit in memory is mapped to a PEL on the screen.
- Double scanned on display to 400 rows.
- Formats eight PELs per byte in the following manner:

Bit	Function
7	First Display PEL
6	Second Display PEL
5	Third Display PEL
4	Fourth Display PEL
3	Fifth Display PEL
2	Sixth Display PEL
1	Seventh Display PEL
0	Eighth Display PEL

Figure 4-24. PEL Format, Mode hex 6

The bit definition for each PEL is (0 = Black) and (1 = Intensified White).

640 x 480 Two Color Graphics (Mode Hex 11)

This mode provides two color graphics with the same data format as mode 6. Addressing and mapping is shown under "Video Memory Organization" on page 4-40.

The bit image data is stored in map 0 and comprises a single bit plane (C0). A sequential buffer starting at address hex A0000 is provided. Location hex A0000 contains the byte with information for

the first eight PELs; location hex A0001 contains information for the second eight PELs, and so on. The bit definition for each PEL is (0 = Black) and (1 = Intensified White).

640 x 350 Graphics (Mode Hex F)

This mode emulates the EGA graphics on the IBM Monochrome Display with the following attributes: black, video, blinking video, and intensified video. Resolution of 640 x 350 requires 56K bytes to support four attributes. Maps 0 and 2 are used in this mode. Map 0 is the video bit plane, and map 2 is the intensity bit plane. Both planes reside at address hex A0000.

Two bits, one from each bit plane, define one picture element (PEL) on the screen. The bit definitions for the PELs are given in the following table. The video bit plane is denoted by C0 and the Intensity Bit Plane is denoted by C2.

C2	C0	PEL Color
0	0	Black
0	1	White
1	0	Blinking White
1	1	Intensified White

Figure 4-25. PEL Bit Definitions

The byte organization in memory is linear. The first eight PELs on the screen are defined by the contents of memory in location hex A0000, the second eight PELs by location hex A0001, and so on. The first PEL within any one byte is defined by bit 7 in the byte. The last PEL within the byte is defined by bit 0 in the byte.

Since both bit planes reside at address hex A0000, the user must select which plane or planes to update. This is accomplished by the Map Mask register of the sequencer. For more information, see "Video Memory Organization" on page 4-40.

16 Color Graphics Modes (Mode Hex 10, D, E, and 12)

These modes support graphics in 16 colors. The bit image data is stored in all four memory maps in these modes. Each memory map contains the data for one bit plane. Each bit plane represents a color as shown below. The bit planes are denoted as C0, C1, C2 and C3 respectively.

C0 = Blue PELs
C1 = Green PELs
C2 = Red PELs
C3 = Intensified PELs

Four bits (one from each plane) define one PEL on the screen. The color combinations are illustrated in the following figure:

C3	C2	C1	C0	Color
0	0	0	0	Black
0	0	0	1	Blue
0	0	1	0	Green
0	0	1	1	Cyan
0	1	0	0	Red
0	1	0	1	Magenta
0	1	1	0	Brown
0	1	1	1	White
1	0	0	0	Dark Gray
1	0	0	1	Light Blue
1	0	1	0	Light Green
1	0	1	1	Light Cyan
1	1	0	0	Light Red
1	1	0	1	Light Magenta
1	1	1	0	Yellow
1	1	1	1	Intensified White

Figure 4-26. Palette Colors

The display buffer resides at address hex A0000. The Map Mask register is used to select any or all of the maps to be updated when a memory write to the display buffer is executed by the system microprocessor.

256 Color Graphics Mode (Mode Hex 13)

This mode provides graphics with the capability to display 256 colors on the screen at one time.

The display buffer is linear, starting at address hex A0000, and 64,000 bytes long. The first location contains the 8-bit color for the upper left hand PEL. The second byte contains the second PEL and so on for 64,000 PELs (320 x 200). The bit image data is stored in all four memory maps and comprises four bit planes. The four bit planes are sampled twice to produce eight bit planes that address the video DAC.

The internal palette of the video subsystem is not used to select colors. It is set by BIOS and should not be changed. The external palette in the video DAC is programmed by the BIOS such that the first 16 locations contain colors that are compatible with colors of other modes. See Figure 4-27 on page 4-40. The second 16 registers contain 16 evenly spaced gray shades. The remaining 216 locations are loaded based on a hue-saturation-intensity model tuned to provide a usable, generic color set that covers a wide range of color values.

The following figure shows the colors that are compatible with colors of other modes.

Attribute Byte								Analog Output Color
C7	C6	C5	C4	C3	C2	C1	C0	
0	0	0	0	0	0	0	0	Black
0	0	0	0	0	0	0	1	Blue
0	0	0	0	0	0	1	0	Green
0	0	0	0	0	0	1	1	Cyan
0	0	0	0	0	1	0	0	Red
0	0	0	0	0	1	0	1	Magenta
0	0	0	0	0	1	1	0	Brown
0	0	0	0	0	1	1	1	White
0	0	0	0	1	0	0	0	Dark Gray
0	0	0	0	1	0	0	1	Light Blue
0	0	0	0	1	0	1	0	Light Green
0	0	0	0	1	0	1	1	Light Cyan
0	0	0	0	1	1	0	0	Light Red
0	0	0	0	1	1	0	1	Light Magenta
0	0	0	0	1	1	1	0	Yellow
0	0	0	0	1	1	1	1	Intensified White

Figure 4-27. Attribute Byte

The video DAC palette can be programmed with 256K different colors.

This mode has the following features:

- Contains a maximum of 200 rows of 320 PELs
- Double scanned on display to 400 rows
- Selects one of 256K colors for each PEL
- Requires 64,000 bytes of read/write memory
- Uses memory-mapped graphics
- Uses one byte of memory for each PEL.

Video Memory Organization

The video display buffer on the system board consists of 256K bytes of dynamic read/write memory configured as four 64K-byte video maps.

The address of the display buffer can be changed to remain compatible with other video adapters and application software. Four locations are provided. The buffer can be configured at segment address hex A0000 for a length of 128K bytes, at hex A0000 for a length of 64K bytes, at hex B0000 for a length of 32K bytes, or at hex B8000 for a length of 32K bytes.

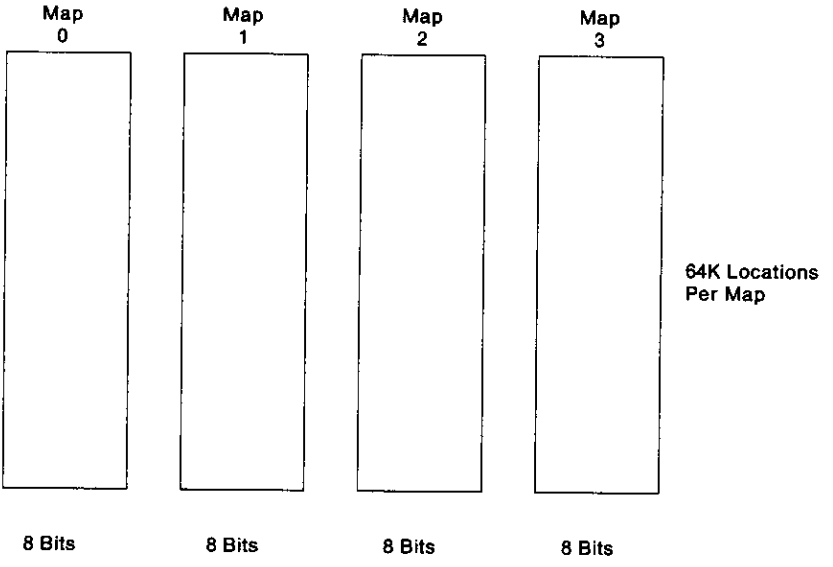


Figure 4-28. 256K Video Memory Map

Maps 0 through 3 usually form bit planes 0 through 3.

Map 0 = Bit Plane 0

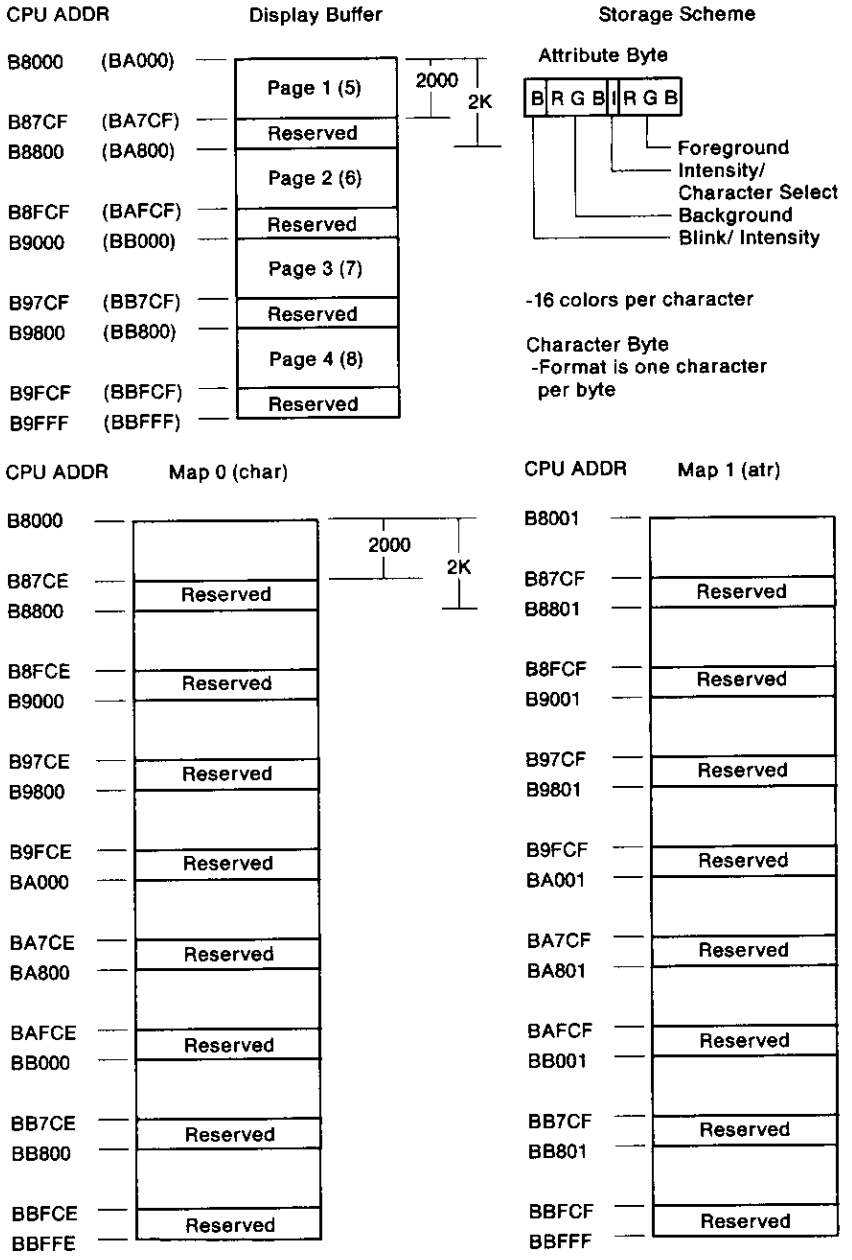
Map 1 = Bit Plane 1

Map 2 = Bit Plane 2

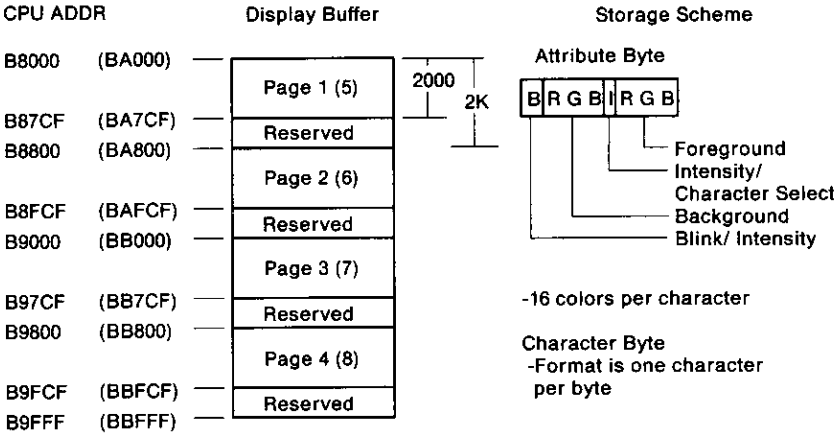
Map 3 = Bit Plane 3

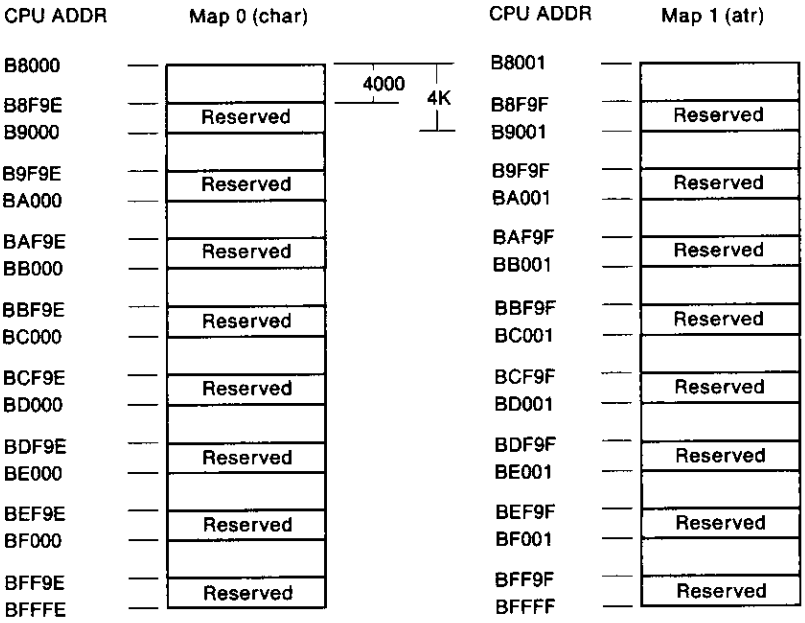
In mode hex 13, each of the four bit planes is formed with data from all four maps. The four bits are sampled twice internally to produce the eight bit values needed to select 256 colors.

Modes hex 0, 1 (All Variations of Modes Hex 0 and 1)

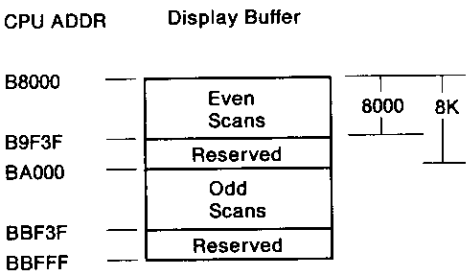


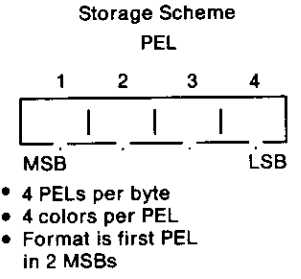
Modes hex 2, 3 (All Variations of Modes Hex 2 and 3)

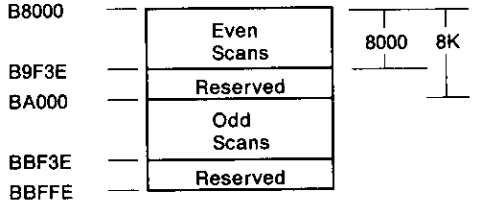


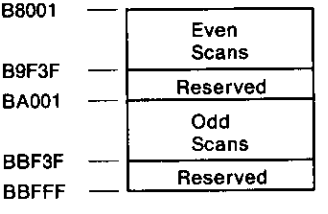


Modes hex 4, 5

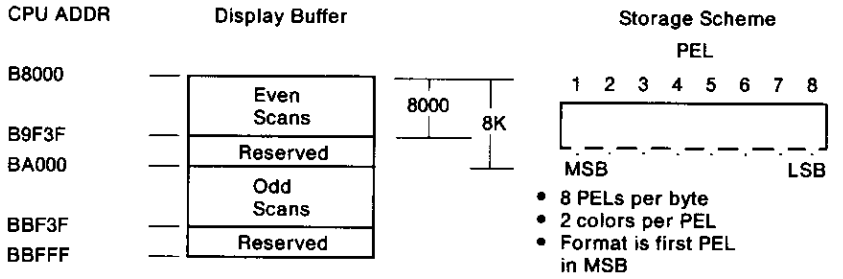

CPU ADDR
Display Buffer
B8000
B9F3F
BA000
BBF3F
BBFFF
Even Scans
Reserved
Odd Scans
Reserved
8000
8K

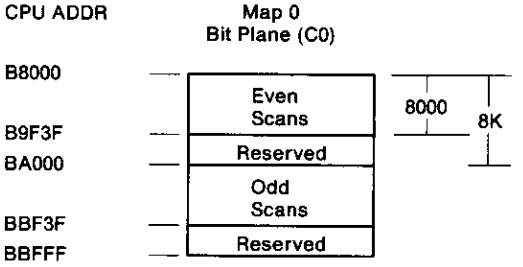

Storage Scheme
PEL
1
2
3
4
MSB
LSB
• 4 PELs per byte
• 4 colors per PEL
• Format is first PEL in 2 MSBs


CPU ADDR
Map 0
B8000
B9F3E
BA000
BBF3E
BBFFE
Even Scans
Reserved
Odd Scans
Reserved
8000
8K

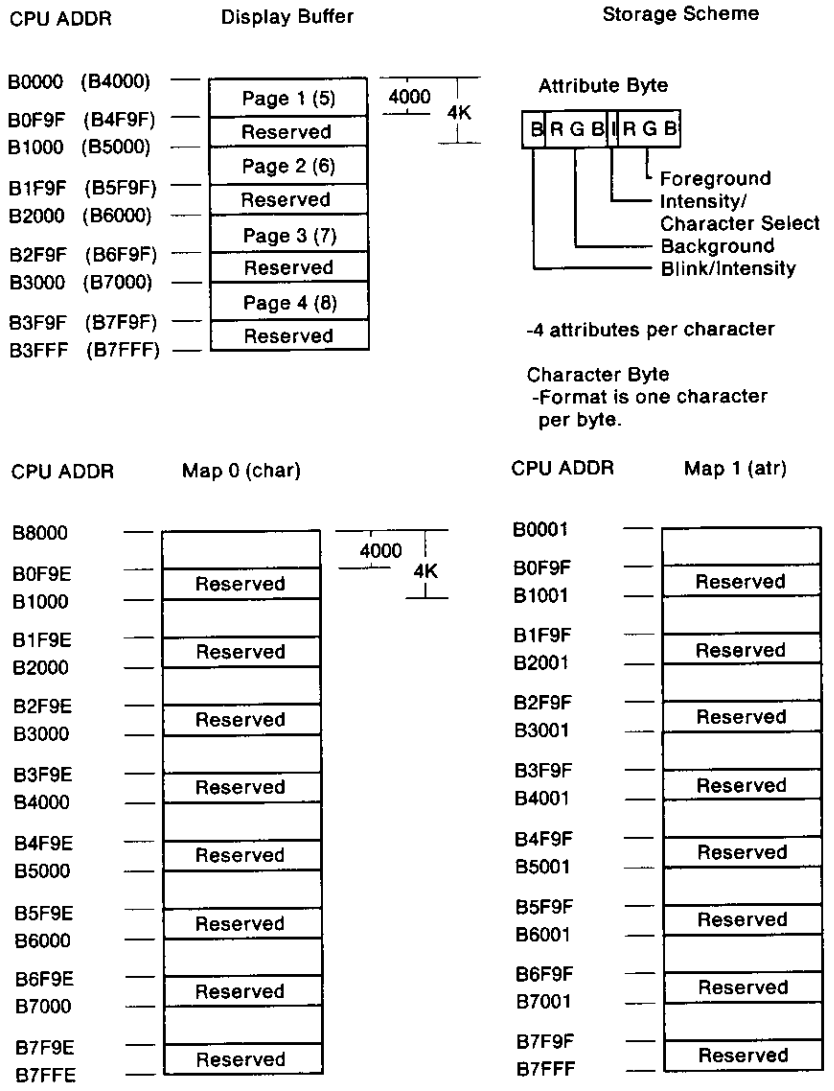

CPU ADDR
Map 1
B8001
B9F3F
BA001
BBF3F
BBFFF
Even Scans
Reserved
Odd Scans
Reserved

Mode Hex 6

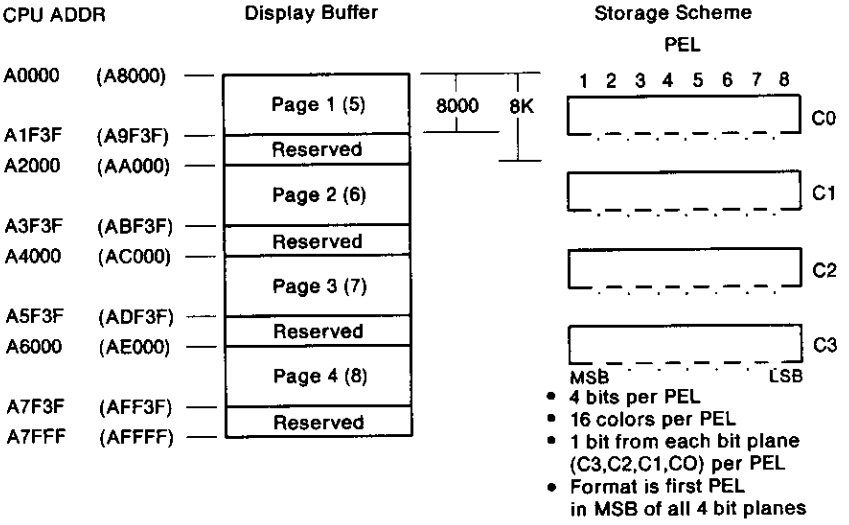

CPU ADDR
Display Buffer
Storage Scheme
PEL
B8000
B9F3F
BA000
BBF3F
BBFFF
Even Scans
Reserved
Odd Scans
Reserved
8000
8K
1 2 3 4 5 6 7 8
MSB
LSB
• 8 PELs per byte
• 2 colors per PEL
• Format is first PEL in MSB

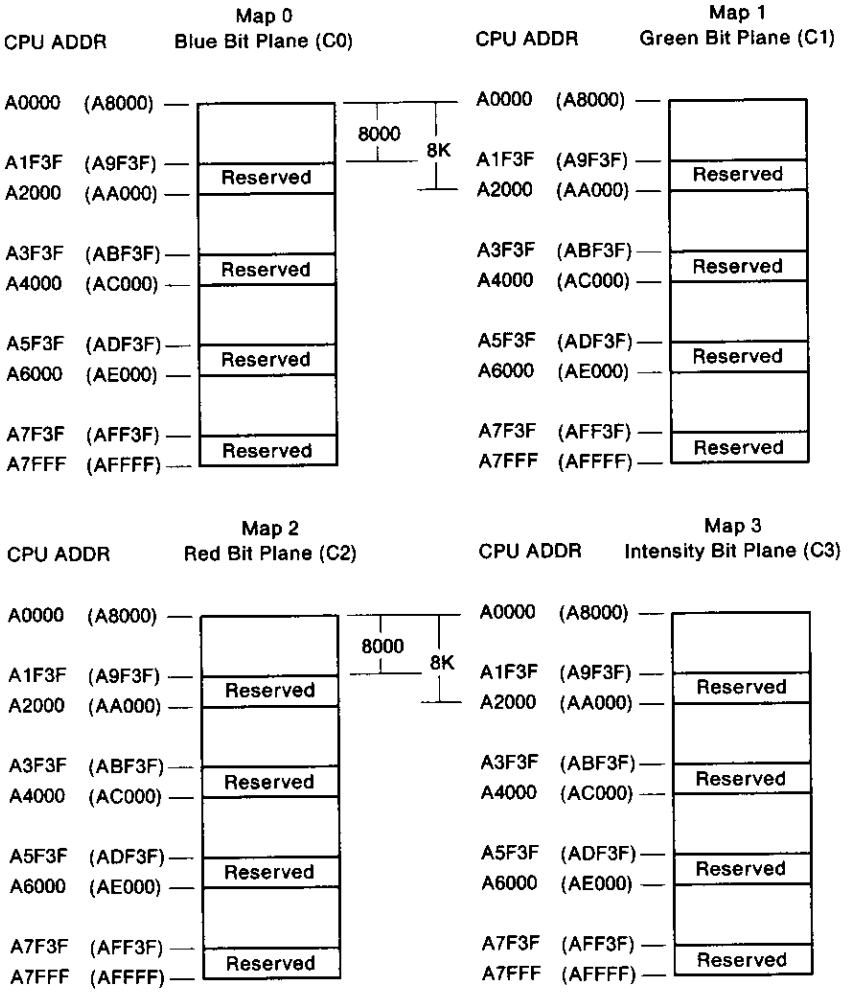

CPU ADDR
Map 0
Bit Plane (C0)
B8000
B9F3F
BA000
BBF3F
BBFFF
Even Scans
Reserved
Odd Scans
Reserved
8000
8K

Mode Hex 7 (All Variations of Mode Hex 7)

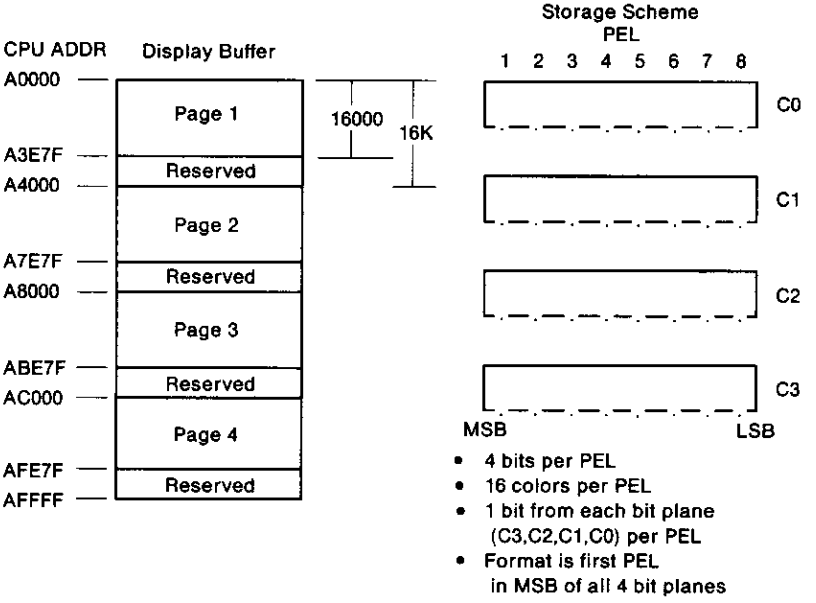


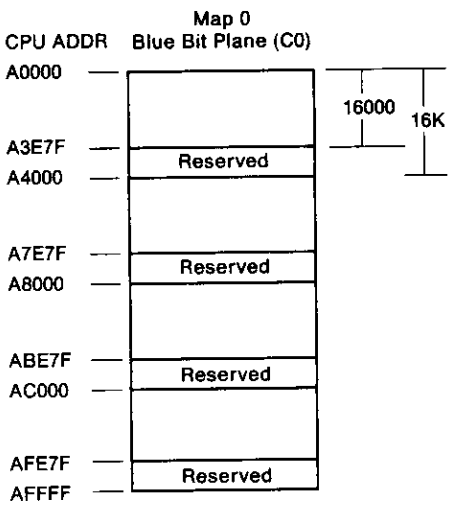
Mode Hex D

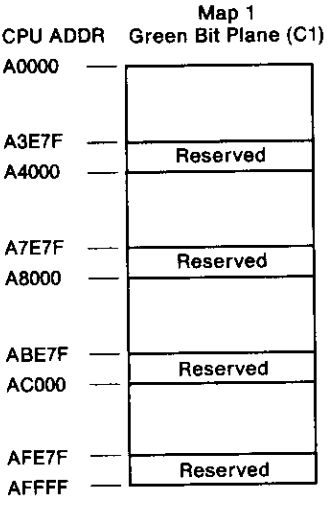

CPU ADDR
Display Buffer
Storage Scheme
PEL
A0000 (A8000)
A1F3F (A9F3F)
A2000 (AA000)
A3F3F (ABF3F)
A4000 (AC000)
A5F3F (ADF3F)
A6000 (AE000)
A7F3F (AFF3F)
A7FFF (AFFFF)
Page 1 (5)
Reserved
Page 2 (6)
Reserved
Page 3 (7)
Reserved
Page 4 (8)
Reserved
8000
8K
1 2 3 4 5 6 7 8
C0
C1
C2
C3
MSB
LSB
• 4 bits per PEL
• 16 colors per PEL
• 1 bit from each bit plane (C3,C2,C1,CO) per PEL
• Format is first PEL in MSB of all 4 bit planes

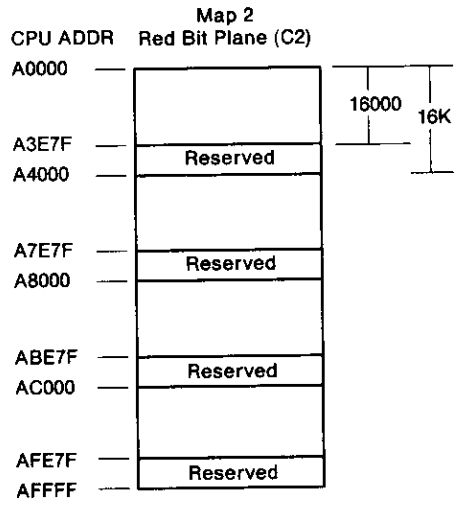

Map 0
CPU ADDR
Blue Bit Plane (C0)
A0000 (A8000)
A1F3F (A9F3F)
A2000 (AA000)
A3F3F (ABF3F)
A4000 (AC000)
A5F3F (ADF3F)
A6000 (AE000)
A7F3F (AFF3F)
A7FFF (AFFFF)
Reserved
Reserved
Reserved
Reserved
8000
8K
Map 1
CPU ADDR
Green Bit Plane (C1)
A0000 (A8000)
A1F3F (A9F3F)
A2000 (AA000)
A3F3F (ABF3F)
A4000 (AC000)
A5F3F (ADF3F)
A6000 (AE000)
A7F3F (AFF3F)
A7FFF (AFFFF)
Reserved
Reserved
Reserved
Reserved
Map 2
CPU ADDR
Red Bit Plane (C2)
A0000 (A8000)
A1F3F (A9F3F)
A2000 (AA000)
A3F3F (ABF3F)
A4000 (AC000)
A5F3F (ADF3F)
A6000 (AE000)
A7F3F (AFF3F)
A7FFF (AFFFF)
Reserved
Reserved
Reserved
Reserved
8000
8K
Map 3
CPU ADDR
Intensity Bit Plane (C3)
A0000 (A8000)
A1F3F (A9F3F)
A2000 (AA000)
A3F3F (ABF3F)
A4000 (AC000)
A5F3F (ADF3F)
A6000 (AE000)
A7F3F (AFF3F)
A7FFF (AFFFF)
Reserved
Reserved
Reserved
Reserved

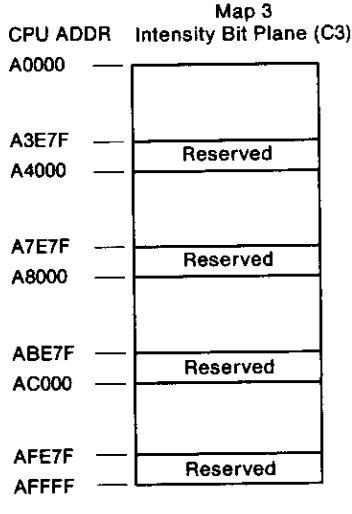
Mode Hex E


CPU ADDR
Display Buffer
A0000
Page 1
A3E7F
Reserved
A4000
Page 2
A7E7F
Reserved
A8000
Page 3
ABE7F
Reserved
AC000
Page 4
AFE7F
Reserved
AFFFF
16000
16K
Storage Scheme
PEL
1 2 3 4 5 6 7 8
C0
C1
C2
C3
MSB
LSB
• 4 bits per PEL
• 16 colors per PEL
• 1 bit from each bit plane (C3,C2,C1,C0) per PEL
• Format is first PEL in MSB of all 4 bit planes

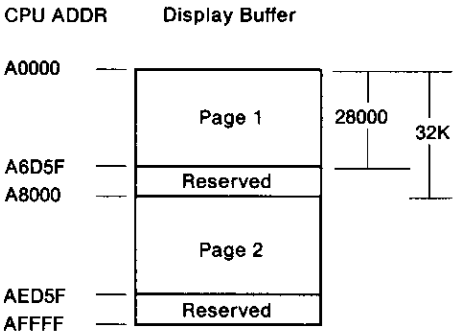

Map 0
CPU ADDR
Blue Bit Plane (C0)
A0000
A3E7F
A4000
A7E7F
A8000
ABE7F
AC000
AFE7F
AFFFF
Reserved
Reserved
Reserved
Reserved
16000
16K

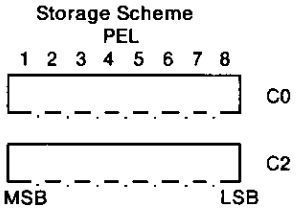

Map 1
CPU ADDR
Green Bit Plane (C1)
A0000
A3E7F
A4000
A7E7F
A8000
ABE7F
AC000
AFE7F
AFFFF
Reserved
Reserved
Reserved
Reserved


Map 2
CPU ADDR
Red Bit Plane (C2)
A0000
A3E7F
A4000
A7E7F
A8000
ABE7F
AC000
AFE7F
AFFFF
Reserved
Reserved
Reserved
Reserved
16000
16K

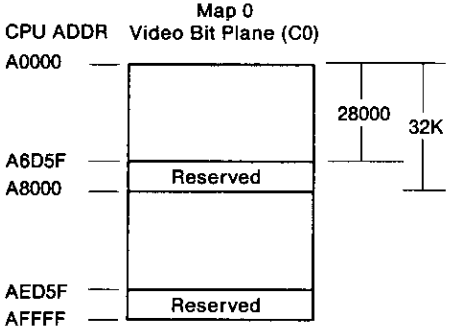

Map 3
CPU ADDR
Intensity Bit Plane (C3)
A0000
A3E7F
A4000
A7E7F
A8000
ABE7F
AC000
AFE7F
AFFFF
Reserved
Reserved
Reserved
Reserved

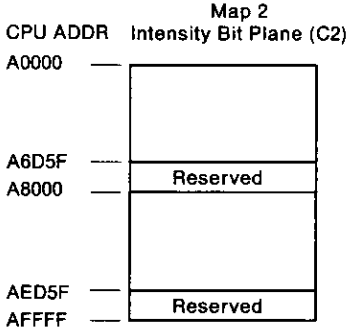
Mode Hex F



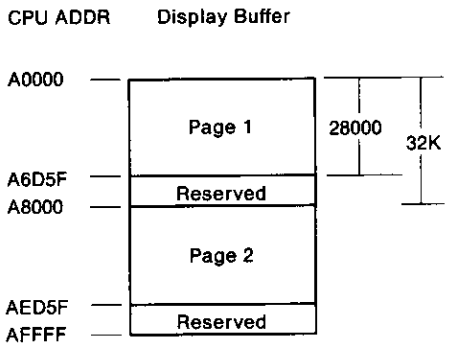


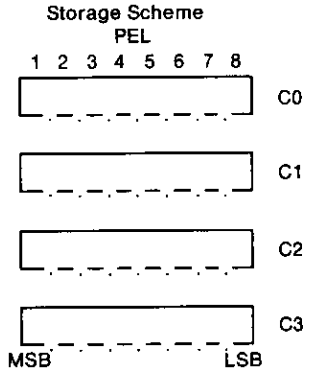
- 2 bits per PEL
- 4 attributes per PEL
- 1 bit from each bit plane (C2,C0)
- Format is first PEL is MSB of video and intensity bit planes



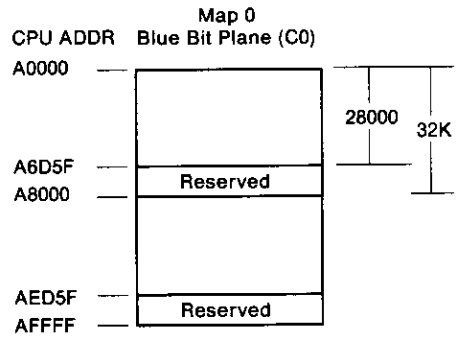


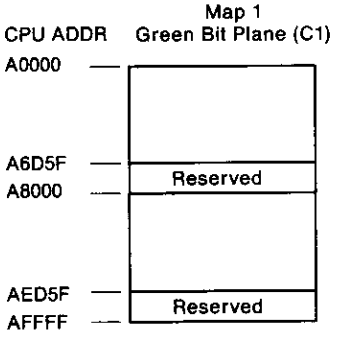
Mode Hex 10

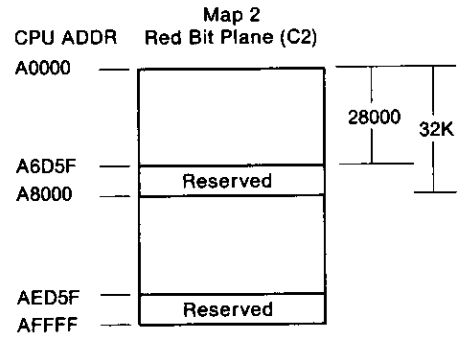


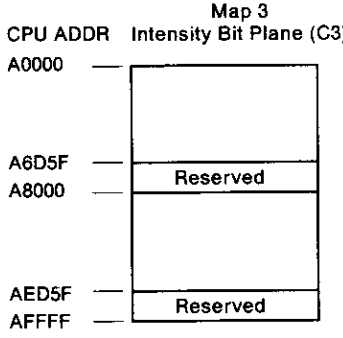


- 4 bits per PEL
- 16 colors per PEL
- 1 bit from each bit plane (C3,C2,C1,C0) per PEL
- Format is first PEL in MSB of all 4 bit planes

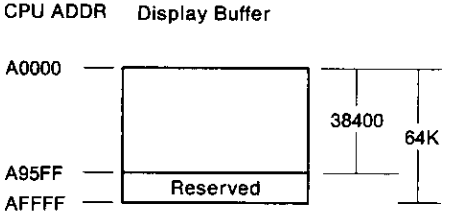


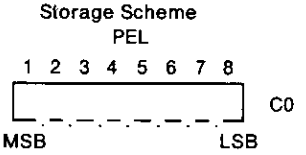




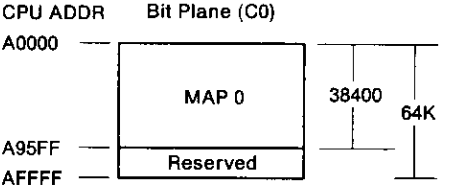


Mode Hex 11

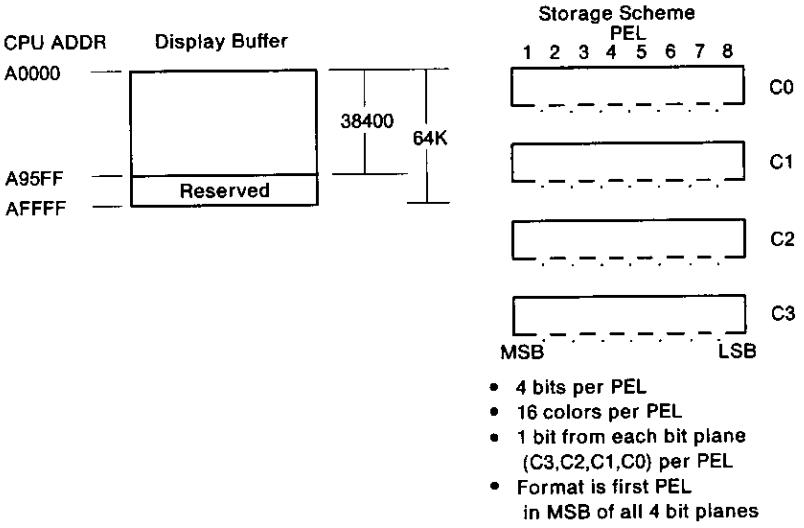




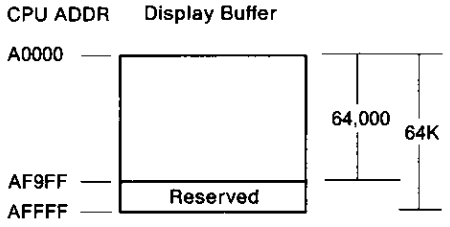
- 1 bit per PEL
- 2 attributes per PEL
- Format is first PEL in MSB position



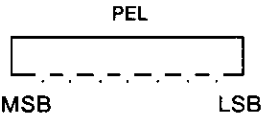
Mode Hex 12


CPU ADDR
Display Buffer
A0000
A95FF
AFFFF
Reserved
38400
64K
Storage Scheme
PEL
1 2 3 4 5 6 7 8
C0
C1
C2
C3
MSB
LSB
• 4 bits per PEL
• 16 colors per PEL
• 1 bit from each bit plane (C3,C2,C1,C0) per PEL
• Format is first PEL in MSB of all 4 bit planes
Map 0
CPU ADDR
Blue Bit Plane (C0)
A0000
A95FF
AFFFF
Reserved
38400
64K
Map 1
CPU ADDR
Green Bit Plane (C1)
A0000
A95FF
AFFFF
Reserved
Map 2
CPU ADDR
Red Bit Plane (C2)
A0000
A95FF
AFFFF
Reserved
38400
64K
Map 3
CPU ADDR
Intensity Plane (C3)
A0000
A95FF
AFFFF
Reserved

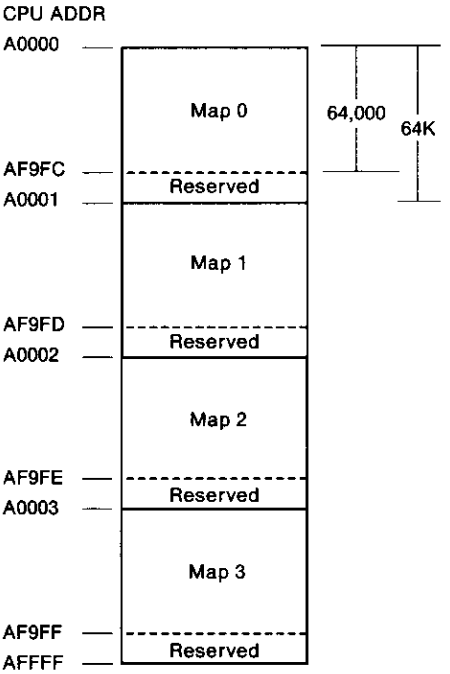
Mode Hex 13



Storage Scheme



- 8 bits per PEL
- 256 colors per PEL
- 1 PEL per byte
- Format is PEL 1 at address A0000



Video Memory Read/Write Operations

Video Memory Write Operations

During system microprocessor writes to the video memory, the maps are enabled by the logical decode of the memory address and, depending on the video mode, the Map Mask register. The data flow for a system microprocessor write operation is illustrated in the following figure.

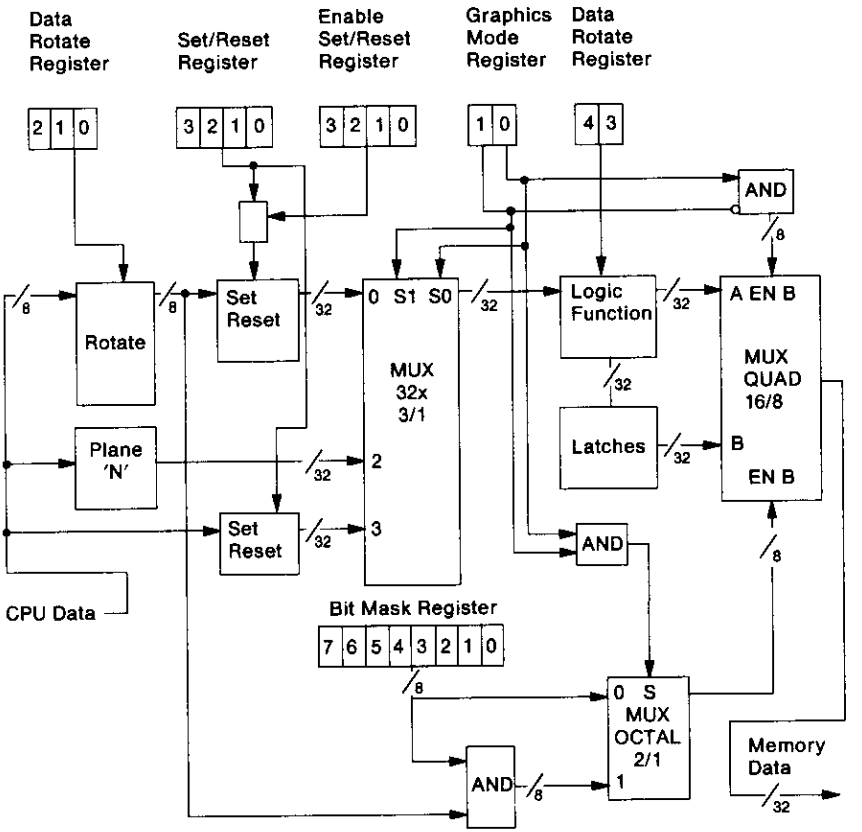


Figure 4-29. Data Flow for VGA Memory Write Operations

Note: Which maps are actually written with data is under control of the system microprocessor memory address, which depends on the mode selected and the Map Mask register.

Video Memory Read Operations

There are two ways to do video memory Reads. When Read type 0 is selected using the Graphics Mode register, the system microprocessor Reads to the video memory return the 8-bit value that is determined by the logical decode of the memory address, and the Read Map Select register if applicable. When Read type 1 is selected using the Graphics Mode register, the 8-bit value returned is the result of the color compare operation controlled by the Color Compare and Color Don't Care registers. The data flow for the color compare operations is illustrated in the following figure.

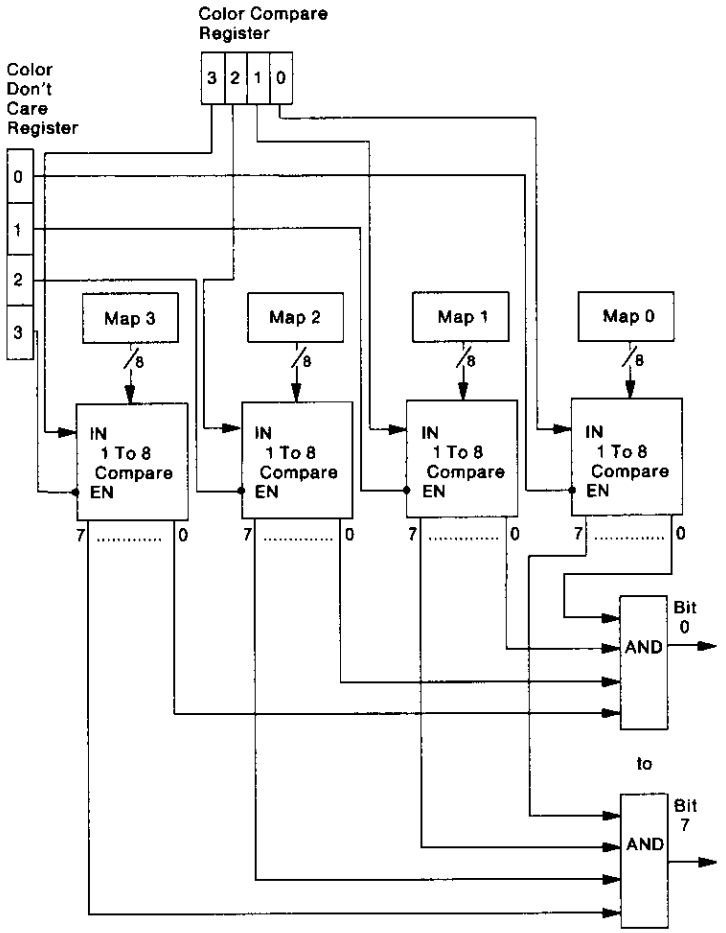


Figure 4-30. VGA Color Compare Operations

Registers

There are six sets of registers in the video subsystem. All but the system microprocessor data latches and the attribute address flip-flop are readable. The following figure lists the registers and the I/O address where they are located. The figure also lists whether or not they are read/write, read-only, or write-only.

	R/W	Monochrome Emulation	Color Emulation	Either
General Registers	**Addresses used 03BA or 03DA; 03C2; 03CA; and 03CC**			
Miscellaneous Output Reg	W			03C2
	R			03CC
Input Status Register 0	RO			03C2
Input Status Register 1	RO	03BA	03DA	
Feature Control Register	W	03BA	03DA	
	R			03CA
Video Subsystem Enable	RW			03C3
Attribute Registers	**Addresses used 03C0 - 03C1**			
Address Register	RW			03C0
Other Attribute Registers	W			03C0
(03C0 write, 03C1 read)	R			03C1
CRT Controller Registers	**Addresses used 03D4 to 03D5 or 03B4 to 03B5**			
Index Register	RW	03B4	03D4	
Other CRT Controller Regs.	RW	03B5	03D5	
Sequencer Registers	**Addresses used 03C4 to 03C5**			
Address Register	RW			03C4
Other Sequencer Registers	RW			03C5
Graphics Registers	**Addresses used 03CE to 03CF**			
Address Register	RW			03CE
Other Graphics Registers	RW			03CF

RO = Read Only, RW = Read / Write
Register addresses are in hex.

Figure 4-31. VGA Register Overview

The VGA also provides the system microprocessor interface for the video DAC. The DAC has one address register. It is written to address hex 03C7 or 03C8, and read from address hex 03C8.

PEL Address (Write Mode)	RW	03C8
PEL Address (Read Mode)	WO	03C7
DAC State Register	RO	03C7
PEL Data Register	RW	03C9
PEL Mask *	RW	03C6

RO = Read-Only, RW = Read/Write, WO = Write-Only.
Register addresses are in hex.

* This register must not be written to by application code or destruction of the color look-up table may occur. See also Video Digital-to-Analog Converter on page 4-115 for programming considerations.

Figure 4-32. DAC Register Usage

General Registers

This section contains descriptions of the following registers.

Name	Read Port	Write Port	Index
Miscellaneous Output Register	03CC	03C2	-
Input Status Register 0	03C2	-	-
Input Status Register 1	03?A	-	-
Feature Control Register	03CA	03?A	-
VGA Enable Register	03C3	03C3	-
DAC State Register	03C7	-	-

The (?) is controlled by Bit 0 of the Miscellaneous Output register.
? = B in Monochrome Emulation Modes and
? = D in Color Emulation Modes
Register addresses are in hex.

Figure 4-33. General Register Overview

Miscellaneous Output Register

This is a read/write register. A hardware reset causes all bits to reset to 0.

Read address = hex 03CC; Write address = hex 03C2.

Bit	Function
7	Vertical Sync Polarity
6	Horizontal Sync Polarity
5	Page Bit For Odd/Even (diagnostic use)
4	Reserved = 0
3	Clock Select 1
2	Clock Select 0
1	Enable RAM
0	I/O Address Select

Figure 4-34. Miscellaneous Output Register

Bit 7 Vertical Sync Polarity - A logical 0 selects positive vertical retrace; a logical 1 selects negative vertical retrace.

Bit 6 Horizontal Sync Polarity - A logical 0 selects positive horizontal retrace; a logical 1 selects negative horizontal retrace.

Note: Bits 7 and 6 are selected based on the vertical size as shown in the following figure.

Bit 7	Bit 6	Vertical Size
0	0	Reserved = 0
1	0	400 lines
0	1	350 lines
1	1	480 lines

Figure 4-35. Display, Vertical Size

Bit 5 Page Bit For Odd/Even - Selects between two 64K pages of memory when in the Odd/Even modes (0-5). A logical 0 selects the low page of memory; a logical 1 selects the high page of memory. This bit is provided for diagnostic use.

Bit 4 Reserved

Bits 3, 2 Clock Select - These two bits select the clock source according to the following table:

Bit 3	Bit 2	Function
0	0	Selects 25.175 MHz clock for 640 Horizontal PELs
0	1	Selects 28.322 MHz clock for 720 Horizontal PELs
1	0	Selects external clock input from the auxiliary video connector for the input clock. This input clock should be kept between 14.3 MHz and 28.4 MHz.
1	1	Reserved

Figure 4-36. Clock Select 3 and 2 Bit Definitions

Bit 1 Enable RAM - A logical 0 disables Video RAM address decode from the system microprocessor; a logical 1 enables Video RAM to the system microprocessor.

Bit 0 I/O Address Select - CRTC I/O address hex 03BX/03DX . This bit maps the CRTC I/O addresses for IBM Monochrome or Color/Graphics Monitor Adapter emulation. A logical 0 sets CRTC addresses to hex 03BX and Input Status register 1's address to hex 03BA for Monochrome emulation. A logical 1 sets CRTC addresses to hex 03DX and Input Status register 1's address to hex 03DA for IBM Color/Graphics Monitor Adapter emulation.

Input Status Register 0

This is a read-only register.

Read address = hex 03C2

Bit	Function
7	CRT Interrupt
6, 5	Reserved = 0
4	Switch Sense Bit
3 - 0	Reserved = 0

Figure 4-37. Input Status Register 0

Bit 7 CRT Interrupt - A logical 1 indicates a vertical retrace interrupt is pending; a logical 0 indicates the vertical retrace interrupt is cleared.

Bits 6, 5 Reserved

Bit 4 Switch Sense Bit - This bit allows the system microprocessor to read the switch sense line. This bit allows the power-on self-test to determine if a monochrome or color display is connected to the system.

Bits 3 - 0 Reserved

Input Status Register 1

This is a read-only register.

Read address = hex 03?A

Bit	Function
7, 6	Reserved = 0
5	Diagnostic 0
4	Diagnostic 1
3	Vertical Retrace
2, 1	Reserved = 0
0	Display Enable

Figure 4-38. Input Status Register 1

Bits 7, 6 Reserved

Bits 5, 4 Diagnostic Usage - These bits are selectively connected to two of the eight color outputs of the Attribute Controller. The Color Plane Enable register controls the multiplexer for the video wiring. The following figure illustrates the combinations available and the color output wiring.

Color Plane Register		Input Status Register 1	
Bit 5	Bit 4	Bit 5	Bit 4
0	0	P2	P0
0	1	P5	P4
1	0	P3	P1
1	1	P7	P6

Figure 4-39. Diagnostic Bits

Bit 3 Vertical Retrace - A logical 0 indicates that video information is being displayed; a logical 1 indicates a vertical retrace interval. This bit can be programmed to interrupt the system microprocessor on interrupt level 2 at the start of the vertical retrace. This is done through bits 5 and 4 of the Vertical Retrace End register.

Bit 2, 1 Reserved

Bit 0 Display Enable - Logical 1 indicates a horizontal or vertical retrace interval. This bit is the real-time status of the inverted display enable signal. To avoid glitches on the display, some programs use this status bit to restrict screen updates to inactive display intervals. The video subsystem has been designed to eliminate this software requirement, so display screen updates may be made at any time.

Feature Control Register

Write address = 03?A; Read address = 03CA.

All bits in this register are reserved, bit 3 must equal 0.

Video Subsystem Enable Register

Bit	Function
7 - 1	Reserved = 0
0	Video Subsystem Enable

Figure 4-40. Video Subsystem Enable Register, Address hex 03C3)

Bits 7 - 1 Reserved

Bit 0 When this bit is set to a 1, the video I/O and memory address decoding is enabled. A 0 disables the video I/O and memory address decoding.

Note: Accesses to the Video Subsystem Enable register are not affected by the VGA sleep bit (I/O port 102, bit 0), described in "Video Subsystem Programmable Option Select" on page 4-29.

Sequencer Registers

Name	Port (hex)	Index (hex)
Sequencer Address	03C4	-
Reset	03C5	00
Clocking Mode	03C5	01
Map Mask	03C5	02
Character Map Select	03C5	03
Memory Mode	03C5	04

Figure 4-41. Sequencer Register Overview

Sequencer Address Register

The Sequencer Address register is a pointer register located at address hex 03C4. This register is loaded with a binary value that points to the Sequencer Data register where data is to be written. This value is referred to as "Index" in the figure above.

Bit	Function
7 - 3	Reserved = 0
2 - 0	Sequencer Address

Figure 4-42. Sequencer Address Register

Bits 7 - 3 Reserved

Bits 2 - 0 Sequencer Address Bits - A binary value pointing to the register where data is to be written.

Reset Register

This is a read/write register pointed to when the value in the Address register is hex 00. The port address for this register is hex 03C5.

Bit	Function
7 - 2	Reserved = 0
1	Synchronous Reset
0	Asynchronous Reset

Figure 4-43. Reset Register, Index Hex 00

Bits 7 - 2 Reserved

Bit 1 Synchronous Reset - A logical 0 commands the sequencer to synchronously clear and halt. Bits 1 and 0 must both be 1 to allow the sequencer to operate. This bit must be set to 0 before changing either bit 3 or bit 0 of the Clocking Mode register, or bit 3 or bit 2 of the Miscellaneous Output register.

Bit 0 Asynchronous Reset - A logical 0 commands the sequencer to asynchronously clear and halt. A logical 1 commands the sequencer to run unless bit 1 is set to 0. Resetting the sequencer with this bit can cause data loss in the dynamic RAMs.

Clocking Mode Register

This is a read/write register pointed to when the value in the Address register is hex 01. The port address for this register is hex 03C5.

Bit	Function
7, 6	Reserved = 0
5	Screen Off
4	Shift 4
3	Dot Clock
2	Shift Load
1	Reserved = 0
0	8/9 Dot Clocks

Figure 4-44. Clocking Mode Register, Index Hex 01

Bits 7, 6 Reserved

Bit 5 Screen Off - A logical 1 turns off the video screen and assigns maximum memory bandwidth to the system microprocessor. A logical 0 selects normal screen operation. The screen is blanked when this bit is set, and the sync pulses are maintained. Use this bit for rapid full-screen updates.

Bit 4 Shift 4 - When set to 0, the video serializers are loaded every character clock; when set to 1, the serializers are loaded every fourth character clock. This mode is useful when 32 bits are fetched per cycle and chained together in the shift registers.

Bit 3 Dot Clock - A logical 0 selects normal dot clocks derived from the sequencer master clock input. When this bit is set to 1, the master clock will be divided by 2 to generate the dot clock. All the other timings are affected because they are derived from the dot clock. Dot clock divided by 2 is used for 320 and 360 horizontal PEL modes.

Bit 2 Shift Load - When set to 0, and Bit 4 is set to 0, the video serializers are reloaded every character clock; when set to 1, the video serializers are loaded every other character clock. This mode is useful when 16 bits are fetched per cycle and chained together in the shift registers.

Bit 1 Reserved

Bit 0 8/9 Dot Clocks - A logical 0 directs the sequencer to generate character clocks 9 dots wide; a logical 1 directs the sequencer to generate character clocks 8 dots wide. Alphanumeric modes hex 0+, 1+, 2+, 3+, 7 and 7+ are the only modes that use character clocks 9 dots wide. All other modes must use 8 dots per character clock. The 9 dot mode is for Alphanumeric modes only. The 9th dot equals the 8th dot for ASCII codes C0 through DF hex. See the attribute line graphics character bit in the Attribute Mode Control register (index hex 10) on page 4-102.

Map Mask Register

This is a read/write register pointed to when the value in the address register is hex 02. The port address for this register is hex 03C5.

Bit	Function
7 - 4	Reserved = 0
3	Map 3 Enable
2	Map 2 Enable
1	Map 1 Enable
0	Map 0 Enable

Figure 4-45. Map Mask Register, Index Hex 02

Bits 7 - 4 Reserved

Bits 3 - 0 Map Mask - A logical 1 enables the system microprocessor to write to the corresponding map. If this register is programmed with a value of 0FH, the system microprocessor can perform a 32-bit write operation with only one memory cycle. This substantially reduces the overhead on the system microprocessor during display update cycles in graphics modes. Data scrolling operations are also enhanced by setting this register to a value of 0FH and writing the display buffer address with the data stored in the system microprocessor data latches. This is a read-modify-write operation. When odd/even modes are selected, maps 0 and 1 and maps 2 and 3 should have the same map mask value. When chain 4 mode is selected, all maps should be enabled.

Character Map Select Register

This is a read/write register pointed to when the value in the Address register is hex 03. The port address for this register is hex 03C5.

Bit	Function
7, 6	Reserved = 0
5	Character Map Select High Bit A
4	Character Map Select High Bit B
3, 2	Character Map Select A
1, 0	Character Map Select B

Figure 4-46. Character Map Select Register, Index Hex 03

Bits 7, 6 Reserved

Bit 5 Character Map Select High Bit A

Bit 4 Character Map Select High Bit B

Bits 3, 2 Character Map Select A - Selects the portion of map 2 used to generate Alpha characters when attribute bit 3 is a 1, according to the following figure:

Bit 5 Value	Bit 3 Value	Bit 2 Value	Map Selected	Table Location
0	0	0	0	1st 8K of Map 2
0	0	1	1	3rd 8K of Map 2
0	1	0	2	5th 8K of Map 2
0	1	1	3	7th 8K of Map 2
1	0	0	4	2nd 8K of Map 2
1	0	1	5	4th 8K of Map 2
1	1	0	6	6th 8K of Map 2
1	1	1	7	8th 8K of Map 2

Figure 4-47. Character Map Select A

In alphanumeric modes, bit 3 of the attribute byte normally has the function of turning the foreground intensity on or off. This bit, however, may be redefined as a switch between character sets. For this feature to be enabled, the following must be true:

- Memory Mode register bit 1, must be equal to 1.
- The value of Character Map Select A does not equal the value of Character Map Select B.

If either condition is not met, the first 16K of Map 2 is used.

Bits 1, 0 Character Map Select B - Selects the portion of map 2 used to generate Alpha characters when attribute bit 3 is a 0, according to the following table:

Bit 4 Value	Bit 1 Value	Bit 0 Value	Map Selected	Table Location
0	0	0	0	1st 8K of Map 2
0	0	1	1	3rd 8K of Map 2
0	1	0	2	5th 8K of Map 2
0	1	1	3	7th 8K of Map 2
1	0	0	4	2nd 8K of Map 2
1	0	1	5	4th 8K of Map 2
1	1	0	6	6th 8K of Map 2
1	1	1	7	8th 8K of Map 2

Figure 4-48. Character Map Select B

Memory Mode Register

This is a read/write register pointed to when the value in the Address register is hex 04. The system microprocessor output port address for this register is 03C5.

Bit	Function
7 - 4	Reserved = 0
3	Chain 4
2	Odd/Even
1	Extended Memory
0	Reserved = 0

Figure 4-49. Memory Mode Register, Index Hex 04

Bits 7 - 4 Reserved

Bit 3 Chain 4 - A logical 0 enables system microprocessor addresses to sequentially access data within a bit map by use of the Map Mask register. A logical 1 causes the two low-order bits to select the map that will be accessed as shown in following figure.

Note: This bit controls the map selected in the graphics subsection during system microprocessor reads.

A1	A0	Map Selected
0	0	0
0	1	1
1	0	2
1	1	3

Figure 4-50. Memory Mode, Chain 4

Bit 2 Odd/Even - A logical 0 directs even system microprocessor addresses to access maps 0 and 2, while odd system microprocessor addresses access maps 1 and 3. A logical 1 causes system microprocessor addresses to sequentially access data within a bit map. The maps are accessed according to the value in the Map Mask register.

Bit 1 Extended Memory - A logical 1 indicates that greater than 64K of video memory is present. This bit must be set to allow the VGA to use the 256K of video memory on the system board, and to enable the character map selection on the previous page.

Bit 0 Reserved

CRT Controller Registers

Name	Port (hex)	Index (hex)
CRT Controller Address Register	03?4	-
Horizontal Total	03?5	00
Horizontal Display Enable End	03?5	01
Start Horizontal Blanking	03?5	02
End Horizontal Blanking	03?5	03
Start Horizontal Retrace Pulse	03?5	04
End Horizontal Retrace	03?5	05
Vertical Total	03?5	06
Overflow	03?5	07
Preset Row Scan	03?5	08
Maximum Scan Line	03?5	09
Cursor Start	03?5	0A
Cursor End	03?5	0B
Start Address High	03?5	0C
Start Address Low	03?5	0D
Cursor Location High	03?5	0E
Cursor Location Low	03?5	0F
Vertical Retrace Start	03?5	10
Vertical Retrace End	03?5	11
Vertical Display Enable End	03?5	12
Offset	03?5	13
Underline Location	03?5	14
Start Vertical Blank	03?5	15
End Vertical Blank	03?5	16
CRTC Mode Control	03?5	17
Line Compare	03?5	18

? = B in Monochrome Emulation Modes and
? = D in Color Emulation Modes
This is controlled by Bit 0 of the Miscellaneous Output register

Figure 4-51. CRT Controller Register Overview

CRT Controller Address Register

The Address register is a pointer register located at hex 03B4 or hex 03D4. Which address is used depends on Bit 0 of the Miscellaneous Output register at address hex 03C2. The CRT Address register is loaded with a binary value that points to the CRT Controller Data register where data is to be written. This value is referred to as "Index" in the preceding table. All CRT controller registers are read/write registers.

Bit	Function
7	Reserved = 0
6	Reserved = 0
5	For test, must = 0
4	CRTC Address
3	CRTC Address
2	CRTC Address
1	CRTC Address
0	CRTC Address

Figure 4-52. CRT Controller Address Register

Bits 7, 6 Reserved

Bit 5 This is a test bit for chip testing and must remain 0.

Bits 4 - 0 CRT Controller Address Bits - A binary value pointing to the CRT Controller register where data is to be written.

Horizontal Total Register

This is a read/write register pointed to when the value in the CRT Controller Address register is hex 00. The system microprocessor output port address for this register is hex 03?5.

Bit	Function
7 - 0	Horizontal Total (-5)

Figure 4-53. Horizontal Total Register, Index Hex 00

This register defines the total number of characters in the horizontal scan interval including the retrace time. The value directly controls the period of the horizontal retrace output signal. An internal horizontal character counter counts character clock inputs to the CRT Controller, and all horizontal and vertical timings are based upon the Horizontal register. Comparators are used to compare register values with horizontal character values to provide horizontal timings.

Bits 7 - 0 Horizontal Total - The total number of characters less 5.

Horizontal Display Enable End Register

This is a read/write register pointed to when the value in the CRT Controller Address register is hex 01. The system microprocessor output port address for this register is hex 03?5.

Bit	Function
7 - 0	Horizontal Display Enable End (-1)

Figure 4-54. Horizontal Display Enable End Register, Index Hex 01

This register defines the length of the horizontal display enable signal. It determines the number of displayed character positions per horizontal line.

Bits 7 - 0 Horizontal Display Enable End - A value one less than the total number of displayed characters.

Start Horizontal Blanking Register

This is a read/write register pointed to when the value in the CRT Controller Address register is hex 02. The system microprocessor output port address for this register is hex 03?5.

Bit	Function
7 - 0	Start Horizontal Blanking

Figure 4-55. Start Horizontal Blanking Register, Index Hex 02

This register determines when the horizontal blanking output signal becomes active.

Bits 7 - 0 Start Horizontal Blanking - The horizontal blanking signal becomes active when the horizontal character counter reaches this value.

End Horizontal Blanking Register

This is a read/write register pointed to when the value in the CRT Controller Address register is hex 03. The system microprocessor output port address for this register is hex 03?5.

Bit	Function
7	Test, must be 1
6	Display Enable Skew Control
5	Display Enable Skew Control
4 - 0	End Blanking

Figure 4-56. End Horizontal Blanking Register, Index Hex 03

This register determines when the horizontal blanking output signal becomes inactive.

Bit 7 Test Bit - This bit is used for chip testing and must be set to logical 1.

Bits 6, 5 Display Enable Skew Control - These two bits determine the amount of display enable skew. Display enable skew control is required to provide sufficient time for the CRT Controller to access the display buffer to obtain a character and attribute code, access the character generator font, and then go through the Horizontal PEL Panning register in the Attribute Controller. Each access

requires the display enable signal to be skewed one character clock unit so that the video output is in synchronization with the horizontal and vertical retrace signals. The bit values and amount of skew are shown in the following table:

Bit 6	Bit 5	Skew
0	0	Zero character clock skew
0	1	One character clock skew
1	0	Two character clock skew
1	1	Three character clock skew

Figure 4-57. Bit Values and Amount of Skew

Bits 4 - 0 End Horizontal Blanking - A value equal to the six least-significant bits of the horizontal character counter value at which time the horizontal blanking signal becomes inactive (logical 0). To obtain a blanking signal of width W, the following algorithm is used: Value of Start Blanking register + width of blanking signal in character clock units = 6-bit result to be programmed into the End Horizontal Blanking register. Bit number 5 is located in the End Horizontal Retrace register (index hex 05).

Start Horizontal Retrace Pulse Register

This is a read/write register pointed to when the value in the CRT Controller Address register is hex 04. The system microprocessor output port address for this register is hex 03?5.

Bit	Function
7 - 0	Start Horizontal Retrace Pulse

Figure 4-58. Start Horizontal Retrace Pulse Register, Index Hex 04

This register is used to center the screen horizontally, and to specify the character position at which the Horizontal Retrace Pulse becomes active.

Bits 7 - 0 Start Horizontal Retrace Pulse - The value programmed is a binary count of the character position number at which the signal becomes active.

End Horizontal Retrace Register

This is a read/write register pointed to when the value in the CRT Controller Address register is hex 05. The system microprocessor output port address for this register is hex 03?5.

Bit	Function
7	End Horizontal Blanking, bit 5
6, 5	Horizontal Retrace Delay
4 - 0	End Horizontal Retrace

Figure 4-59. End Horizontal Retrace Register, Index Hex 05

This register specifies the character position at which the Horizontal Retrace Pulse becomes inactive (logical 0).

Bit 7 End Horizontal Blanking, Bit number 5. The first 4 bits are located in the End Horizontal Blanking register (index hex 03).

Bits 6, 5 Horizontal Retrace Delay - These bits control the skew of the horizontal retrace signal. Binary 00 equals no horizontal retrace delay. For some modes, it is necessary to provide a horizontal retrace signal that takes up the entire blanking interval. Some internal timings are generated by the falling edge of the horizontal retrace signal. To guarantee the signals are latched properly, the retrace signal is started before the end of the display enable signal, and then skewed several character clock times to provide the proper screen centering.

Bits 4 - 0 End Horizontal Retrace - A value equal to the five least-significant bits of the horizontal character counter value at which time the horizontal retrace signal becomes inactive (logical 0). To obtain a retrace signal of width W, the following algorithm is used: Value of Start Retrace register + width of horizontal retrace signal in character clock units = 5-bit result to be programmed into the End Horizontal Retrace register.

Vertical Total Register

This is a read/write register pointed to when the value in the CRT Controller Address register is hex 06. The system microprocessor output port address for this register is hex 03?5.

Bit	Function
7 - 0	Vertical Total (-2)

Figure 4-60. Vertical Total Register, Index Hex 06

Bits 7 - 0 Vertical Total - This is the low-order eight bits of a 10-bit register. The binary value represents the number of horizontal raster scans on the CRT screen, minus 2, including vertical retrace. The value in this register determines the period of the vertical retrace signal.

Bit 8 of this register is contained in the CRT Controller Overflow register hex 07 bit 0.

Bit 9 of this register is contained in the CRT Controller Overflow register hex 07 bit 5.

CRT Controller Overflow Register

This is a read/write register pointed to when the value in the CRT Controller Address register is hex 07. The system microprocessor output port address for this register is hex 03?5.

Bit	Function
7	Vertical Retrace Start Bit 9
6	Vertical Display Enable End Bit 9
5	Vertical Total Bit 9
4	Line Compare Bit 8
3	Start Vertical Blank Bit 8
2	Vertical Retrace Start Bit 8
1	Vertical Display Enable End Bit 8
0	Vertical Total Bit 8

Figure 4-61. CRTC Overflow Register, Index Hex 07

Bit 7 Vertical Retrace Start - Bit 9 of the Vertical Retrace Start register (index hex 10).

Bit 6 Vertical Display Enable End - Bit 9 of the Vertical Display Enable End register (index hex 12).

Bit 5 Vertical Total - Bit 9 of the Vertical Total register (index hex 06).

Bit 4 Line Compare - Bit 8 of the Line Compare register (index hex 18).

Bit 3 Start Vertical Blank - Bit 8 of the Start Vertical Blank register (index hex 15).

Bit 2 Vertical Retrace Start - Bit 8 of the Vertical Retrace Start register (index hex 10).

Bit 1 Vertical Display Enable End - Bit 8 of the Vertical Display Enable End register (index hex 12).

Bit 0 Vertical Total - Bit 8 of the Vertical Total register (index hex 06).

Preset Row Scan Register

This is a read/write register pointed to when the value in the CRT Controller Address register is hex 08. The system microprocessor output port address for this register is hex 03?5.

Bit	Function
7	Reserved = 0
6	Byte Panning Control
5	Byte Panning Control
4 - 0	Starting Row scan count after a Vertical Retrace

Figure 4-62. Preset Row Scan Register, Index Hex 08

This register is used for PEL scrolling.

Bit 7 Reserved

Bits 6, 5 Byte Panning Control - These two bits control byte panning in modes programmed as multiple shift modes. (Currently, no modes are programmed for multiple shift operation.) This is required for PEL-panning operations. The PEL Panning register in the attribute section provides panning of up to 7 or 8 individual PELs. In single byte shift modes, to pan to the next higher PEL (8 or 9), the CRT Controller start address is incremented and attribute panning is reset to 0. In multiple shift modes, the byte pan bits are used as extensions to the attribute PEL Panning register. This allows panning across the width of the video output shift. For example, in the 32-bit shift mode, the byte pan and PEL-panning bits provide up to 31 bits of panning capability. To pan from position 31 to 32, the CRT controller start address is incremented and PEL- and

byte-panning is reset to 0. These bits should normally be set to 0.

Bits 4 - 0 Preset Row Scan (PEL Scrolling) - This register specifies the starting row scan count after a vertical retrace. The row scan counter increments each horizontal retrace time until a maximum row scan occurs. At maximum row scan compare time, the row scan is cleared (not preset).

Maximum Scan Line Register

This is a read/write register pointed to when the value in the CRT Controller Address register is hex 09. The system microprocessor output port address for this register is hex 03?5.

Bit	Function
7	200 --> 400 Line Conversion
6	Line Compare Bit 9
5	Start Vertical Blank Bit 9
4 - 0	Maximum Scan Line

Figure 4-63. Maximum Scan Line Register, Index Hex 09

Bit 7 200 to 400 Line Conversion is done when this bit is set to 1. The clock in the row scan counter is divided by 2. This allows the older 200-line modes to be displayed as 400 lines on the display (this is line doubling; each line is displayed twice). When this bit is a 0, the clock to the row scan counter is equal to the horizontal scan rate. Line doubling is not enabled.

Bit 6 Line Compare - Bit 9 of the Line Compare register (index hex 18).

Bit 5 Start Vertical Blank - Bit 9 of the Start Vertical Blank register (index hex 15).

Bits 4 - 0 Maximum Scan Line - This register specifies the number of scan lines per character row. The number to be programmed is the maximum row scan number minus 1.

Cursor Start Register

This is a read/write register pointed to when the value in the CRT Controller Address register is hex 0A. The system microprocessor output port address for this register is hex 03?5.

Bit	Function
7, 6	Reserved = 0
5	Cursor Off
4 - 0	Row Scan Cursor Begins

Figure 4-64. Cursor Start Register, Index Hex 0A

Bits 7, 6 Reserved

Bit 5 Cursor Off - A logical 1 turns off the cursor, a logical 0 turns on the cursor.

Bits 4 - 0 Cursor Start - This register specifies the row scan of a character line where the cursor is to begin. The number programmed is one less than the starting cursor row scan.

When the Cursor Start register is programmed with a value greater than the Cursor End register, no cursor is generated.

Cursor End Register

This is a read/write register pointed to when the value in the CRT Controller Address register is hex 0B. The system microprocessor output port address for this register is hex 03?5.

Bit	Function
7	Reserved = 0
6, 5	Cursor Skew Control
4 - 0	Row Scan Cursor Ends

Figure 4-65. Cursor End Register, Index Hex 0B

Bit 7 Reserved

Bits 6, 5 Cursor Skew - These bits control the skew of the cursor signal. Cursor skew delays the cursor by the selected number of clocks. For example, a skew of 1 moves the cursor right one position on the screen.

Bit 6	Bit 5	Function
0	0	Zero-character clock skew
0	1	One-character clock skew
1	0	Two-character clock skew
1	1	Three-character clock skew

Figure 4-66. Cursor Skew

Bits 4 - 0 Cursor End - These bits specify the row scan of a character line where the cursor is to end.

Start Address High Register

This is a read/write register pointed to when the value in the CRT Controller Address register is hex 0C. The system microprocessor input/output port address for this register is hex 03?5.

Bit	Function
7 - 0	High Order Start Address

Figure 4-67. Start Address High Register, Index Hex 0C

Bits 7 - 0 Start Address High - These are the high-order 8 bits of the start address. The 16-bit value, from the high-order and low-order Start Address registers, is the first address after the vertical retrace on each screen refresh.

Start Address Low Register

This is a read/write register pointed to when the value in the CRT Controller Address register is hex 0D. The system microprocessor input/output port address for this register is hex 03?5.

Bit	Function
7 - 0	Low Order Start Address

Figure 4-68. Start Address Low Register, Index Hex 0D

Bits 7 - 0 Start Address Low - These are the low-order 8 bits of the start address.

Cursor Location High Register

This is a read/write register pointed to when the value in the CRT Controller Address register is hex 0E. The system microprocessor input/output port address for this register is hex 03?5.

Bit	Function
7 - 0	High Order Cursor Location

Figure 4-69. Cursor Location High Register, Index Hex 0E

Bits 7 - 0 Cursor Location High - These are the high-order 8 bits of the cursor location.

Cursor Location Low Register

This is a read/write register pointed to when the value in the CRT Controller Address register is hex 0F. The system microprocessor input/output port address for this register is hex 03?5.

Bit	Function
7 - 0	Low Order Cursor Location

Figure 4-70. Cursor Location Low Register, Index Hex 0F

Bits 7 - 0 Cursor Location Low - These are the low-order 8 bits of the cursor location.

Vertical Retrace Start Register

This is a read/write register pointed to when the value in the CRT Controller Address register is hex 10. The system microprocessor output port address for this register is hex 03?5.

Bit	Function
7 - 0	Low order Vertical Retrace Pulse

Figure 4-71. Vertical Retrace Start Register, Index Hex 10

Bits 7 - 0 Vertical Retrace Start - This is the low-order 8 bits of the vertical retrace pulse start position, programmed in horizontal scan lines. Bit 8 is in the CRTC Overflow register (index hex 07).

Vertical Retrace End Register

This is a read/write register pointed to when the value in the CRT Controller Address register is hex 11. The system microprocessor output port address for this register is hex 03?5.

Bit	Function
7	Protect R0-7
6	Select 5 Refresh Cycles
5	0=Enable Vertical Interrupt
4	0=Clear Vertical Interrupt
3 - 0	Vertical Retrace End

Figure 4-72. Vertical Retrace End Register, Index Hex 11

Bit 7 Protect R0-7 - A logical 1 disables writing to CRTC registers 0-7. A logical 0 enables writing to R0-7. The line compare bit 4 in register hex 07 is not protected.

Bit 6 Select 5 Refresh Cycles - A logical 1 generates five DRAM refresh cycles per horizontal line. A logical 0 selects three refresh cycles. Selecting five refresh cycles allows use of the VGA chip with slow sweep rate displays (15.75 kHz). This bit is set to 0 by BIOS during a mode set, a reset, or power on.

Bit 5 Enable Vertical Interrupt - A logical 0 enables a vertical retrace interrupt. The vertical retrace interrupt is on IRQ2. This interrupt level may be shared so the Input Status register 0, bit 7, should be checked to find out if the VGA

generated the interrupt. As with bit 4, do not change the value of the other bits in this register.

Bit 4 Clear Vertical Interrupt - A logical 0 clears a vertical retrace interrupt. At the end of the active vertical display time, a flip-flop is set in the VGA for vertical interrupt. The output of this flip-flop goes to the system board interrupt controller. An interrupt handler has to reset this flip-flop by writing a 0 to this bit, then setting the bit to 1 so that the flip-flop does not hold interrupts inactive. Do not change the other bits in this register. The register is readable, so a read can be done to determine what the other bits are before the flip-flop is reset.

Bits 3 - 0 Vertical Retrace End - These bits determine the horizontal scan count value when the vertical retrace output signal becomes inactive. The register is programmed in units of horizontal scan lines. To obtain a vertical retrace signal of width W, the following algorithm is used: Value of Start Vertical Retrace register + width of vertical retrace signal in horizontal scan units = 4-bit result to be programmed into the End Horizontal Retrace register.

Vertical Display Enable End Register

This is a read/write register pointed to when the value in the CRT Controller Address register is hex 12. The system microprocessor output port address for this register is hex 03?5.

Bit	Function
7 - 0	Low Order Vertical Display Enable End (-1)

Figure 4-73. Vertical Display Enable End Register, Index Hex 12

Bits 7 - 0 Vertical Display Enable End - These are the low-order 8 bits of a 10-bit register that defines the vertical display enable end position.

Bit 8 of this register is contained in the CRT Controller Overflow register hex 07, bit 1.

Bit 9 of this register is contained in the CRT Controller Overflow register hex 07, bit 6.

This register specifies which scan line ends the active video area of the screen. It is programmed with the total number of lines minus one.

Offset Register

This is a read/write register pointed to when the value in the CRT Controller Address register is hex 13. The system microprocessor output port address for this register is hex 03?5.

Bit	Function
7 - 0	Logical Line Width of the Screen

Figure 4-74. Offset Register, Index Hex 13

Bits 7 - 0 Offset - This register specifies the logical line width of the screen. The starting memory address for the next character row is larger than the current character row by two or four times this amount. The Offset register is programmed with a word address. Depending on the method of clocking the CRT Controller, this word address is either a word or doubleword address.

Underline Location Register

This is a read/write register pointed to when the value in the CRT Controller Address register is hex 14. The system microprocessor output port address for this register is hex 03?5.

Bit	Function
7	Reserved = 0
6	Doubleword Mode
5	Count By 4
4 - 0	Horizontal row scan where underline will occur

Figure 4-75. Underline Location Register, Index Hex 14

Bit 7 Reserved

Bit 6 Doubleword Mode - When this bit is a logical 1, memory addresses are doubleword addresses. See the description of the CRTC Mode Control register (index hex 17), bit 6, on page 4-87.

Bit 5 Count By 4 - When this bit is a logical 1, the memory address counter is clocked with the character clock divided by 4. This bit is used when doubleword addresses are used.

Bits 4 - 0 Underline Location - This register specifies the horizontal row scan of a character row on which an underline occurs. The value programmed is one less than the scan line number desired.

Start Vertical Blanking Register

This is a read/write register pointed to when the value in the CRT Controller Address register is hex 15. The system microprocessor output port address for this register is hex 03?5.

Bit	Function
7 - 0	Start Vertical Blanking (-1)

Figure 4-76. Start Vertical Blanking Register, Index Hex 15

Bits 7 - 0 Start Vertical Blank - These are the low 8 bits of a 10-bit register.

Bit 8 is in the CRTC Overflow register (index hex 07).

Bit 9 is in the Maximum Scan Line register (index hex 09).

The value of these 10 bits is one less than the horizontal scan line count at which the vertical blanking signal becomes active.

End Vertical Blanking Register

This is a read/write register pointed to when the value in the CRT Controller Address register is hex 16. The system microprocessor output port address for this register is hex 03?5.

Bit	Function
7 - 0	End Vertical Blanking

Figure 4-77. End Vertical Blanking Register, Index Hex 16

Bits 7 - 0 End Vertical Blank - This register specifies the horizontal scan count value when the vertical blank output signal becomes inactive. The register is programmed in units of horizontal scan lines.

To obtain a vertical blank signal of width W, the following algorithm is used: (Value of Start Vertical Blank register minus 1) + width of vertical blank signal in horizontal scan units = 8-bit result to be programmed into the End Vertical Blank register.

CRTC Mode Control Register

This is a read/write register pointed to when the value in the CRT Controller Address register is hex 17. The system microprocessor output port address for this register is hex 03?5.

Bit	Function
7	Hardware Reset
6	Word/Byte Mode
5	Address Wrap
4	Reserved = 0
3	Count By Two
2	Horizontal Retrace Select
1	Select Row Scan Counter
0	CMS 0

Figure 4-78. CRTC Mode Control Register, Index Hex 17

Bit 7 Hardware Reset - A logical 0 forces horizontal and vertical retrace to clear. A logical 1 forces horizontal and vertical retrace to be enabled. This bit does not reset any other registers or outputs.

Bit 6 Word Mode or Byte Mode - When this bit is a logical 0, the word mode shifts all memory address counter bits down one bit, and the most-significant bit of the counter appears on the least-significant bit of the memory address outputs. See Figure 4-79 on page 4-88 for address output details. A logical 1 selects the byte address mode.

Bit 6 of the End Vertical Blanking register in the CRT Controller also controls the addressing. When it is a 0,bit 6 above has control. When it is a 1, the addressing is forced to be shifted by two bits. See doubleword addressing in Figure 4-79 on page 4-88.

Memory Address	Byte Address Mode	Word Address Mode	Doubleword Address Mode
MA 0/RFA 0	MA 0	MA 15 or MA 13	MA 12
MA 1/RFA 1	MA 1	MA 0	MA 13
MA 2/RFA 2	MA 2	MA 1	MA 0
MA 3/RFA 3	MA 3	MA 2	MA 1
MA 4/RFA 4	MA 4	MA 3	MA 2
MA 5/RFA 5	MA 5	MA 4	MA 3
MA 6/RFA 6	MA 6	MA 5	MA 4
MA 7/RFA 7	MA 7	MA 6	MA 5
MA 8/RFA 8	MA 8	MA 7	MA 6
MA 9	MA 9	MA 8	MA 7
MA 10	MA 10	MA 9	MA 8
MA 11	MA 11	MA 10	MA 9
MA 12	MA 12	MA 11	MA 10
MA 13	MA 13	MA 12	MA 11
MA 14	MA 14	MA 13	MA 12
MA 15	MA 15	MA 14	MA 13

Figure 4-79. Internal Memory Address Counter Wiring to the Output Multiplexer

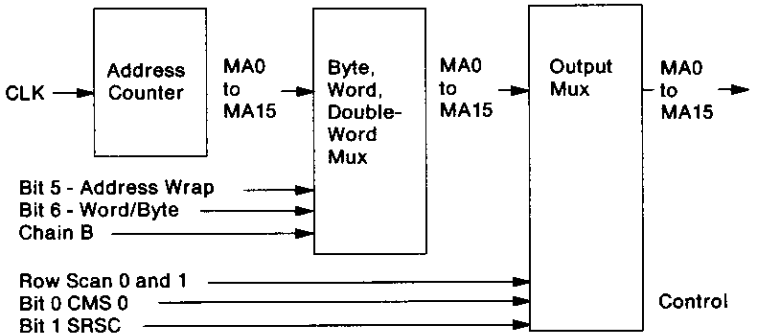


Figure 4-80. CRTC Memory Address Mapping

Bit 5 Address Wrap - This bit selects memory address counter bit MA 13 or bit MA 15, and it appears on the MA 0 output pin in the word address mode. If the VGA is not in the word address mode, MA 0 counter output appears on the MA 0 output pin. A logical 1 selects MA 15. In odd/even mode, bit MA 15 should be selected since 256K of video memory is installed on the system board. (Bit MA 13 is selected in applications where only 64K memory is

present. This function implements IBM Color/Graphics Monitor Adapter compatibility.)

Bit 4 Reserved

Bit 3 Count By Two - When this bit is set to 0, the memory address counter is clocked with the character clock input. A logical 1 clocks the memory address counter with the character clock input divided by 2. This bit is used to create either a byte or word refresh address for the display buffer.

Bit 2 Horizontal Retrace Select - This bit selects horizontal retrace or horizontal retrace divided by 2 as the clock that controls the vertical timing counter. This bit can be used to effectively double the vertical resolution capability of the CRT Controller. The vertical counter has a maximum resolution of 1024 scan lines due to the 10-bit wide Vertical Total register. If the vertical counter is clocked with the horizontal retrace divided by 2, then the vertical resolution is doubled to 2048 horizontal scan lines. A logical 0 selects HRTC and a logical 1 selects HRTC divided by 2.

Bit 1 Select Row Scan Counter - A logical 0 selects row scan counter bit 1 on the MA 14 output pin. A logical 1 selects the MA 14 counter bit on the MA 14 output pin.

Bit 0 Compatibility Mode Support - When this bit is a logical 0, row scan address bit 0 is substituted for memory address bit 13 during active display time. A logical 1 enables memory address bit 13 to appear on the memory address output bit 13 signal of the CRT Controller. The CRT Controller used on the IBM Color/Graphics Monitor Adapter is the 6845. The 6845 has 128 horizontal scan line address capability. To obtain 640-by-200 graphics resolution, the CRTC is programmed for 100 horizontal scan lines with 2 row scan addresses per character row. Row scan address bit 0 becomes the most-significant address bit to the display buffer. Successive scan lines of the display image are displaced in memory by 8K bytes. This bit allows compatibility with the 6845 and Color Graphics APA modes of operation.

Line Compare Register

This is a read/write register pointed to when the value in the CRT Controller Address register is hex 18. The system microprocessor output port address for this register is hex 03?5.

Bit	Function
7 - 0	Line Compare Target

Figure 4-81. Line Compare Register, Index Hex 18

Bits 7 - 0 Line Compare - This register is the low-order 8 bits of the compare target. When the vertical counter reaches this value, the internal start of the line counter is cleared. Because of this, an area of the screen is not affected by scrolling. Bit 8 of this register is in the Overflow register hex 07. Bit 9 is in the maximum scan line register hex 09.

Graphics Controller Registers

Name	Port (hex)	Index (hex)
Graphics Address	03CE	-
Set/Reset	03CF	00
Enable Set/Reset	03CF	01
Color Compare	03CF	02
Data Rotate	03CF	03
Read Map Select	03CF	04
Graphics Mode Register	03CF	05
Miscellaneous	03CF	06
Color Don't Care	03CF	07
Bit Mask	03CF	08

Figure 4-82. Graphics Controller Register Overview

Graphics Address Register

This is a read/write register and the system microprocessor output port address for this register is hex 03CE.

Bit	Function
7 - 4	Reserved = 0
3 - 0	Graphics Address

Figure 4-83. Graphics Address Register

Bits 7 - 4 Reserved

Bits 3 - 0 Graphics Address Bits - These bits point to the other registers in the graphics section.

Set/Reset Register

This is a read/write register pointed to by the value in the Graphics Address register. This value must be hex 00 before writing can take place. The system microprocessor output port address for this register is hex 03CF.

Bit	Function
7 - 4	Reserved = 0
3	Set/Reset Map 3
2	Set/Reset Map 2
1	Set/Reset Map 1
0	Set/Reset Map 0

Figure 4-84. Set/Reset Register, Index Hex 00

Bits 7 - 4 Reserved

Bits 3 - 0 Set/Reset - These bits represent the value written to all 8 bits of the respective memory map when the system microprocessor does a memory write with write mode 0 selected and Set/Reset mode is enabled. Set/Reset can be enabled on a map-by-map basis with separate Out commands to the Enable Set/Reset register.

Enable Set/Reset Register

This is a read/write register and is pointed to by the value in the Graphics Address register. This value must be hex 01 before writing can take place. The system microprocessor output port for this register is hex 03CF.

Bit	Function
7 - 4	Reserved = 0
3	Enable Set/Reset Map 3
2	Enable Set/Reset Map 2
1	Enable Set/Reset Map 1
0	Enable Set/Reset Map 0

Figure 4-85. Enable Set/Reset Register, Index Hex 01

Bits 7 - 4 Reserved

Bits 3 - 0 Enable Set/Reset - These bits enable the set/reset function. When enabled (bit = 1) the respective memory map is written with the value of the Set/Reset register provided the write mode is 0. When write mode is 0 and Set/Reset is not enabled (bit equals 0) on a map, that map is written with the value of the system microprocessor data.

Color Compare Register

This is a read/write register pointed to by the value in the Graphics Address register. This value must be hex 02 before writing can take place. The system microprocessor output port address for this register is hex 03CF.

Bit	Function
7 - 4	Reserved = 0
3	Color Compare Map 3
2	Color Compare Map 2
1	Color Compare Map 1
0	Color Compare Map 0

Figure 4-86. Color Compare Register, Index Hex 02

Bits 7 - 4 Reserved

Bits 3 - 0 Color Compare - These bits represent a 4-bit color value to be compared. If the system microprocessor sets read mode 1 in the graphics section and does a memory read, the data returned from the memory cycle will be a 1 in each bit position where the 4 maps equal the Color Compare register.

The color compare bit is the value that all bits of the corresponding map's byte are compared with. Each of the 8 bit positions of the selected byte are then compared across the four maps and a 1 is returned in each bit position where the bits of all four maps equal their respective color compare values.

Data Rotate Register

This is a read/write register pointed to by the value in the Graphics Address register. This value must be hex 03 before writing can take place. The system microprocessor output port address for this register is hex 03CF.

Bit	Function
7 - 5	Reserved = 0
4	Function Select
3	Function Select
2	Rotate Count 2
1	Rotate Count 1
0	Rotate Count 0

Figure 4-87. Data Rotate Register, Index Hex 03

Bits 7 - 5 Reserved

Bits 4, 3 Function Select - Data written to memory can operate logically with data already in the system microprocessor latches.

Data can be any of the choices selected by the Write Mode register except system microprocessor latches, which may not be modified. If rotated data is selected, the rotate applies before the logical function. The bit functions are defined in the following.

Bit 4	Bit 3	Function
0	0	Data unmodified
0	1	Data ANDed with latched data.
1	0	Data ORed with latched data.
1	1	Data XORed with latched data.

Figure 4-88. Function Select Bit Definitions

Bits 2 - 0 Rotate Count - These bits represent a binary encoded value of the number of positions to right-rotate the system microprocessor data bus during system microprocessor memory writes. This operation is done when the write mode is 0. To write non-rotated data the system microprocessor must select a count of 0.

Read Map Select Register

This is a read/write register pointed to by the value in the Graphics Address register. This value must be hex 04 before writing can take place. The system microprocessor output port address for this register is hex 03CF.

Bit	Function
7 - 2	Reserved = 0
1	Map Select 1
0	Map Select 0

Figure 4-89. Read Map Select Register, Index Hex 04

Bits 7 - 2 Reserved

Bits 1, 0 Map Select - These bits represent a binary encoded value of the memory map number from which the system microprocessor reads data. This register has no effect on the color compare read mode. In odd/even modes the value may be 00 or 01 (10 or 11) for chained maps 0, 1 (2, 3).

Graphics Mode Register

This is a read/write register pointed to by the value in the Graphics Address register. This value must be hex 05 before writing can take place. The system microprocessor output port address for this register is 03CF.

Bit	Function
7	Reserved = 0
6	256 color mode
5	Shift Register Mode
4	Odd/Even
3	Read Type
2	Reserved = 0
1, 0	Write Mode

Figure 4-90. Graphics Mode Register, Index Hex 05

Bit 7 Reserved

Bit 6 256 Color Mode - A logical 0 allows bit 5 to control the loading of the Shift registers. A logical 1 causes the Shift registers to be loaded in a manner that supports the 256-color mode.

Bit 5 Shift register - A logical 1 directs the Shift registers in the graphics section to format the serial data stream with even-numbered bits from both maps on the even-numbered maps and odd-numbered bits from both maps on the odd maps. This bit is used for modes 4 and 5.

Bit 4 Odd/Even - A logical 1 selects the odd/even addressing mode, which is useful for emulation of the IBM Color/Graphics Monitor Adapter compatible modes. Normally the value here follows the value of the Memory Mode register bit 2 of the Sequencer.

Bit 3 Read Type - When this bit is a logical 0, the system microprocessor reads data from the memory map selected by the Read Map Select register, unless bit 3 of the Sequencer Memory Mode register equals 1. In this case the Read Map Select register has no effect. When this bit is a logical 1, the system microprocessor reads the results of the comparison of the four memory maps and the Color Compare register.

Bit 2 Reserved

Bits 1, 0 Write Mode

The bit functions are defined as follows:

Bit 1	Bit 0	Function
0	0	Each memory map is written with the system microprocessor data rotated by the number of counts in the Rotate register, unless Set/Reset is enabled for the map. Maps for which Set/Reset is enabled are written with 8 bits of the value contained in the Set/Reset register for that map.
0	1	Each memory map is written with the contents of the system microprocessor latches. These latches are loaded by a system microprocessor Read operation.
1	0	Memory map *n* (0 through 3) is filled with 8 bits of the value of data bit *n*.
1	1	Each map is written with 8 bits of the value contained in the Set/Reset register for that map (the Enable Set/Reset register has no effect). Rotated system microprocessor data is ANDed with the Bit Mask register data to form an 8-bit value that performs the same function as the Bit Mask register does in write modes 0 and 2 (see also Bit Mask register on page 4-99).

Figure 4-91. Write Mode Bit Definitions

The logic function specified by the Function Select register is applied to data being written to memory following modes 0, 2, and 3 above.

Miscellaneous Register

This is a read/write register pointed to by the value in the Graphics Address register. This value must be hex 06 before writing can take place. The system microprocessor output port for this register is hex 03CF.

Bit	Function
7 - 4	Reserved = 0
3	Memory Map 1
2	Memory Map 0
1	Odd/Even
0	Graphics Mode

Figure 4-92. Miscellaneous Register, Index Hex 06

Bits 7 - 4 Reserved

Bits 3, 2 Memory Map - These bits control the mapping of the regenerative buffer into the system microprocessor address space. The bit functions are defined below:

Bit 3	Bit 2	Function
0	0	Hex A0000 for 128K bytes
0	1	Hex A0000 for 64K bytes
1	0	Hex B0000 for 32K bytes
1	1	Hex B8000 for 32K bytes

Figure 4-93. Miscellaneous Register, Bits 3 and 2

Bit 1 Odd/Even - When set to 1, this bit directs the system microprocessor address bit 0 to be replaced by a higher-order bit and odd/even maps to be selected with odd/even values of the system microprocessor A0 bit, respectively.

Bit 0 Graphics Mode - This bit controls alphanumeric mode addressing. A logical 1 selects graphics mode. When set to graphics mode, the character generator address latches are disabled.

Color Don't Care Register

This is a read/write register and is pointed to by the value in the Graphics Address register. This value must be hex 07 before writing can take place. The system microprocessor output port for this register is hex 03CF.

Bit	Function
7 - 4	Reserved = 0
3	Map 3 = Don't Care
2	Map 2 = Don't Care
1	Map 1 = Don't Care
0	Map 0 = Don't Care

Figure 4-94. Color Don't Care Register, Index Hex 07

Bits 7 - 4 Reserved

Bit 3 Map 3:

1 - Participate in the color compare cycle.
0 - Don't participate in the color compare cycle.

Bit 2 Map 2:

1 - Participate in the color compare cycle.
0 - Don't participate in the color compare cycle.

Bit 1 Map 1:

1 - Participate in the color compare cycle.
0 - Don't participate in the color compare cycle.

Bit 0 Map 0:

1 - Participate in the color compare cycle.
0 - Don't participate in the color compare cycle.

Bit Mask Register

This is a read/write register and is pointed to by the value in the Graphics Address register. This value must be hex 08 before writing can take place. The system microprocessor output port for this register is hex 03CF.

Bit	Function
7 - 0	0-Immune to Change, 1-Unimpeded Writes

Figure 4-95. Bit Mask Register, Index Hex 08

Bits 7 - 0 Bit Mask - Any bit programmed to 0 causes the corresponding bit **n** in each map to be immune to change, provided that the location being written was the last location read by the system microprocessor. Bits programmed to a 1 allow unimpeded writes to the corresponding bits in the maps.

The bit mask applies to write modes 0 and 2. To preserve bits using the bit mask, data must be latched internally by reading the location. When data is written to preserve the bits, the most current data in the latches is written in those positions. The bit mask applies to all maps simultaneously.

Attribute Controller Registers

Name	Port (hex)	Index (hex)
Address Register	03C0	-
Palette Registers	03C0	00-0F
Attribute Mode Control Register	03C0	10
Overscan Color Register	03C0	11
Color Plane Enable Register	03C0	12
Horizontal PEL Panning Register	03C0	13
Color Select Register	03C0	14

Figure 4-96. Attribute Controller Register Overview

Each attribute data register is written at 03C0 as described below. Data is read from them at address 03C1.

Attribute Address Register

This is a read/write register. The system microprocessor output port is hex 03C0.

Bit	Function
7, 6	Reserved = 0
5	Palette Address Source
4 - 0	Attribute Address

Figure 4-97. Attribute Address Register

Bits 7, 6 Reserved

Bit 5 Palette Address Source - When loading the Color Palette registers, bit 5 must be cleared to 0.

For normal operation of the attribute controller, bit 5 must be set to 1. This enables the video memory data to access the palette registers.

Bits 4 - 0 Attribute Address Bits - The Attribute Address register is a pointer register located at hex 03C0. This register is loaded with a binary value that points to the Attribute Data register where data is to be written.

The Attribute Controller register does not have an address bit input to control selection of the Address and Data registers. An internal address flip-flop controls selection

of either the Address or Data registers. To initialize the flip-flop, an IOR instruction is issued to the Attribute Controller at address 03BA or 03DA. This clears the flip-flop, and selects the Address register. After the Address register has been loaded with an out to 03C0, the next Out instruction to 03C0 loads the Data register. The flip-flop toggles each time an Out instruction is issued to the Attribute Controller. It does not toggle on In instructions for Read to 03C1. Also see "Video Graphics Array Programming Considerations" on page 4-107.

Palette Registers Hex 00 through Hex 0F

This is a read/write register. Write at address hex 03C0; Read at address hex 03C1.

Bit	Function
7, 6	Reserved = 0
5	P5
4	P4
3	P3
2	P2
1	P1
0	P0

Figure 4-98. Palette Registers Hex 00 through Hex 0F, Index Hex 00-0F

Bits 7, 6 Reserved

Bits 5 - 0 Palette - These 6-bit registers allow a dynamic mapping between the text attribute or graphic color input value and the display color on the CRT screen. A logical 1 selects the appropriate color. The Palette registers should be modified only during the vertical retrace interval to avoid problems with the displayed image. These internal Palette register values are sent off the chip to the video DAC, where they in turn serve as addresses into the DAC internal registers. Also see the Attribute Controller block diagram on page 4-26.

Attribute Mode Control Register

This is a read/write register pointed to by the value in the Attribute Address register. This value must be hex 10 before writing can take place. The system microprocessor output port address for this register is hex 03C0. The system microprocessor input port address for this register is hex 03C1.

Bit	Function
7	P5, P4 Select
6	PEL Width
5	PEL Panning Compatibility
4	Reserved = 0
3	Select Background Intensity or Enable Blink
2	Enable Line Graphics Character Code
1	Mono Emulation
0	Graphics/Alphanumeric Mode

Figure 4-99. Attribute Mode Control Register, Index Hex 10

Bit 7 P5, P4 Select - This bit selects the source for the P5 and P4 digital video bits that go off the chip. When this bit equals 0, P5, P4 are the outputs of the Palette registers. When this bit equals 1, P5, P4 are bits 1, 0 of the Color Select register. Also see the Attribute Controller block diagram on page 4-26, and "Video DAC Programming Considerations" on page 4-117.

Bit 6 PEL Width - When this bit equals 1, the video pipeline is sampled so that 8 bits are available to select a color in the 256-color mode (hex 13). This bit should equal 0 in all other modes.

Bit 5 PEL Panning Compatibility - When this bit equals 0, line compare has no effect on the output of the PEL Panning register. When this bit equals 1, a successful line compare in the CRT controller forces the output of the PEL Panning register to 0 until +VSYNC occurs, at which time the output returns to its programmed value. This bit allows a selected portion of a screen to be panned.

Bit 4 Reserved

Bit 3 Enable Blink/Select Background Intensity - A logical 0 selects the background intensity of the attribute input. This mode was available on the IBM Monochrome and Color/Graphics Monitor adapters. A logical 1 enables the

blink attribute in alphanumeric modes. This bit must also be set to 1 for blinking graphics modes.

Bit 2 Enable Line Graphics Character Codes - When this bit is set to 0, the ninth dot will be the same as the background. A logical 1 enables the special line graphics character codes for the IBM Monochrome emulation mode. This bit when enabled forces the ninth dot of a line graphic character to be identical to the eighth dot of the character. The line graphics character codes for the Monochrome emulation mode are hex C0 through hex DF.

For character fonts that do not utilize the line graphics character codes in the range of hex C0 through hex DF, bit 2 should be a logical 0. Otherwise unwanted video information will be displayed on the CRT screen.

BIOS will set this bit, the correct dot clock, and other registers when a 9-dot alphanumeric mode is set.

Bit 1 Mono Emulation - A logical 1 indicates a monochrome emulation mode is set. A logical 0 indicates a color emulation mode is set.

Bit 0 Graphics/Alphanumeric Mode - A logical 0 selects alphanumeric mode. A logical 1 selects graphics mode.

Overscan Color Register

This is a read/write register pointed to by the value in the Attribute Address register. This value must be hex 11 before writing can take place. The system microprocessor output port address for this register is hex 03C0. The system microprocessor input port address for this register is hex 03C1.

Bit	Function
7	P7
6	P6
5	P5
4	P4
3	P3
2	P2
1	P1
0	P0

Figure 4-100. Overscan Color Register, Index Hex 11

Bits 7 - 0 Overscan Color - This 8-bit register determines the overscan (border) color displayed on the CRT screen.

The border is a band of color around the perimeter of the display area. Its width is the same as one 80-column character. This border is not supported in the 40-column alphanumeric modes or the 320-PEL graphics modes, except for mode hex 13.

Color Plane Enable Register

This is a read/write register pointed to by the value in the Attribute Address register. This value must be hex 12 before writing can take place. The system microprocessor output port address for this register is 03C0. The system microprocessor input port address for this register is 03C1.

Bit	Function
7, 6	Reserved = 0
5, 4	Video Status MUX
3 - 0	Enable Color Plane

Figure 4-101. Color Plane Enable Register, Index Hex 12

Bits 7, 6 Reserved

Bits 5, 4 Video Status MUX - Selects two of the eight color outputs to be available on the status port. The following figure illustrates the combinations available and the color output wiring.

Color Plane Register		Input Status Register 1	
Bit 5	Bit 4	Bit 5	Bit 4
0	0	P2	P0
0	1	P5	P4
1	0	P3	P1
1	1	P7	P6

Figure 4-102. Color Output Wiring

Bits 3 - 0 Enable Color Plane - Writing a logical 1 in any of bits 0 through 3 enables the respective display memory color plane.

Horizontal PEL Panning Register

This is a read/write register pointed to by the value in the Attribute Address register. This value must be hex 13 before writing can take place. The system microprocessor output port address for this register is hex 03C0. The system microprocessor input port address for this register is hex 03C1.

Bit	Function
7 - 4	Reserved = 0
3 - 0	Horizontal PEL Panning

Figure 4-103. Horizontal PEL Panning Register, Index Hex 13

Bits 7 - 4 Reserved

Bits 3 - 0 Horizontal PEL Panning - This 4-bit register selects the number of picture elements (PELs) to shift the video data horizontally to the left. PEL panning is available in both A/N and APA modes. In monochrome emulation A/N modes, and modes 0+, 1+, 2+, 3+, the image can be shifted a maximum of 8 PELs. In 256-color APA mode, the image can be shifted a maximum of three PELs. Further panning may be accomplished by changing the start address in the CRT controller. In all other A/N and APA modes, the image can be shifted a maximum of seven PELs. The sequence for shifting the image is given below:

PEL Panning Register Value	Number of PELs Shifted to the Left		
	0+, 1+, 2+, 3+, 7, 7+	All Other Modes	Mode 13
0	1	0	0
1	2	1	-
2	3	2	1
3	4	3	-
4	5	4	2
5	6	5	-
6	7	6	3
7	8	7	-
8	0	-	-

Figure 4-104. Image Shifting

Color Select Register

This is a read/write register pointed to by the value in the Attribute Address register. This value must be hex 14 before writing can take place. The system microprocessor port address for this register is hex 03C0 (write), and 03C1 (read).

Bit	Function
7 - 4	Reserved = 0
3	S_color 7
2	S_color 6
1	S_color 5
0	S_color 4

Figure 4-105. Color Select Register, Index Hex 14

Bits 3, 2 S_color 7-6 - In all modes but the 256 color graphics, these bits are the two high-order bits of the 8-bit digital color value sent off-chip. In 256-color graphics, the 8-bit attribute stored in video memory becomes the 8-bit digital color value sent off-chip to the video DAC. These bits are also used to rapidly switch between sets of colors in the video DAC. Also see "Video Graphics Array Programming Considerations."

Bits 1, 0 S_color 5-4 - These bits can be used in place of the P4 and P5 bits from the Attribute Palette registers to form the 8-bit digital color value sent off-chip. (See Attribute Mode Control register bit 7 on page 4-102.) This feature is used to rapidly switch between sets of colors in the video DAC.

Video Graphics Array Programming Considerations

The following are some programming considerations for the Video Graphics Array.

- Certain internal timings must be guaranteed by the user, in order to have the CRTC perform properly. This is due to the physical design of the chip. These timings can be guaranteed by ensuring that the rules listed below are followed when programming the CRTC.

  1. The Horizontal Total register (R0) must be greater than or equal to a value of 25 decimal.

2. The minimum positive pulse width of the HSYNC output must be four character clock units.

3. Register R5 (Horizontal Sync End) must be programmed such that the HSYNC output goes to a logic 0 a minimum of one character clock time before the 'horizontal display enable' signal goes to a logical 1.

4. Register R16 (Vsync Start) must be a minimum of one horizontal scan line greater than register R18. Register R18 defines where the 'vertical display enable' signal ends.

All the above rules are satisfied when the video mode is set by the BIOS.

- When bit 5 of the Attribute Mode Control register equals 1, a successful line compare (See Line Compare register on page 4-90) in the CRT Controller forces the output of the PEL Panning register to 0's until Vsync occurs. When Vsync occurs, the output returns to the programmed value. This allows the portion of the screen indicated by the Line Compare register to be operated on by the PEL Panning register.

- A write to the Character Map Select register becomes valid on the next whole character line. No deformed characters are displayed by changing character generators in the middle of a character scan line.

- For 256-color 320 x 200 graphics mode hex 13, the attribute controller is configured so that the 8-bit attribute stored in video memory for each PEL becomes the 8-bit address (P0 - P7) into the integrated DAC. The user should not modify the contents of the internal Palette registers when using this mode.

- The following sequence should be followed when accessing any of the Attribute Data registers pointed to by the Attribute Index register:

  1. Disable interrupts
  2. Reset read/write flip/flop
  3. Write to Index register
  4. Read from or write to a data register
  5. Enable interrupts.

- The Color Select register in the Attribute Controller section may be used to rapidly switch between sets of colors in the video DAC. When bit 7 of the Attribute Mode Control register equals 0, the 8-bit color value presented to the video DAC is composed of 6 bits from the internal Palette registers and bits 2 and 3 from the Color Select register. When bit 7 of the Attribute Mode Control register equals 1, the 8-bit color value presented to the video DAC is composed of the lower four bits from the internal Palette registers and the four bits in the Color Select register. By changing the value in the Color Select register, software rapidly switches between sets of colors in the video DAC. Note that BIOS does not support multiple sets of colors in the video DAC. The user must load these colors if this function is to be used. Also see the Attribute Controller block diagram on page 4-26. Note that the above discussion applies to all modes except 256 Color Graphics mode. In this mode the Color Select register is not used to switch between sets of colors.

- An application that saves the "Video State" must store the 4 bytes of information contained in the system microprocessor latches in the graphics controller subsection. These latches are loaded with 32 bits from video memory (8 bits per map) each time the system microprocessor does a read from video memory. The application needs to:

  1. Use write mode 1 to write the values in the latches to a location in video memory that is not part of the display buffer. The last location in the address range is a good choice.

  2. Save the values of the latches by reading them back from video memory.

  Note: If in a chain 4 or odd/even mode, it will be necessary to reconfigure the memory organization as four sequential maps prior to performing the sequence above. BIOS provides support for completely saving and restoring video state. See the *IBM Personal System/2 and Personal Computer BIOS Interface Technical Reference* for more information.

- The description of the Horizontal PEL Panning register includes a figure showing the number of PELs shifted left for each valid value of the PEL Panning register and each valid video mode. Further panning beyond that shown in the figure may be accomplished by changing the start address in the CRT Controller

registers, Start Address High and Start Address Low. The sequence involved in further panning would be as follows:

1. Use the PEL Panning register to shift the maximum number of bits to the left. See Figure 4-103 on page 4-106 for the appropriate values.
2. Increment the start address.
3. If you are not using Modes 0+, 1+, 2+, 3+,7, or 7+, set the PEL Panning register to 0. If you are using these modes, set the PEL Panning register to 8. The screen will now be shifted one PEL left of the position it was in at the end of step 1. Step 1 through Step 3 may be repeated as desired.

- The Line Compare register (CRTC register hex 18) should be programmed with even values in 200 line modes when used in split screen applications that scroll a second screen on top of a first screen. This is a requirement imposed by the scan doubling logic in the CRTC.
- If the Cursor Start register (CRTC register hex 0A) is programmed with a value greater than that in the Cursor End register (CRTC register hex 0B), then no cursor is displayed. A split cursor is not possible.
- In 8-dot character modes, the underline attribute produces a solid line across adjacent characters, as in the IBM Color/Graphics Monitor Adapter, Monochrome Display Adapter and the Enhanced Graphics Adapter. In 9-dot modes, the underline across adjacent characters is dashed, as in the IBM 327X display terminals. In 9-dot modes, the line graphics characters (C0 - DF character codes) have solid underlines.

Programming the Registers

Each of the video subsections has an Index or Address register and a number of data registers. The Index or Address register serves as a pointer to the other registers on the device. These registers are loaded by the system microprocessor by executing an Out instruction to its I/O address with the index of the selected data register.

The data registers on each subsection are accessed through a common I/O address. They are distinguished by the pointer (index) in the Address register. To write to a data register, the Address register is loaded with the index of the appropriate data register, then the

selected data register is loaded by executing an Out instruction to the common I/O address.

The general registers are not accessed through an address register; they are written to directly.

See "Video DAC/System Microprocessor Interface" on page 4-116, for details on accessing the video DAC.

For compatibility with the IBM Enhanced Graphics Adapter (EGA), the internal VGA palette is programmed the same as the EGA. The video DAC is programmed by BIOS so that the compatible values in the internal VGA palette produce a color compatible with what was produced by EGA. Mode hex 13 (256 colors) is programmed so that the first 16 locations in the DAC produce compatible colors.

Summing - When BIOS is used to load the video DAC palette for a color mode and a monochrome display is connected to the system unit, the color palette is changed. The colors are summed to produce shades of gray that allow color applications to produce a readable screen.

There are 4 bits that should not be modified unless the sequencer is reset by setting bit 1 of the Reset register to 0. These bits are:

- Bit 3, or bit 0 of the Clocking Mode register.
- Bit 3, or bit 2 of the Miscellaneous Output register.

RAM Loadable Character Generator

The character generator is RAM loadable and can support characters up to 32 scan lines high. Three character generators are stored within the BIOS and one is automatically loaded into the RAM by the BIOS when an alphanumeric mode is selected. The Character Map Select register can be programmed to define the function of bit 3 of the attribute byte to be a character generator switch. This allows the user to select between any two character sets residing in map 2. This effectively gives the user access to 512 characters instead of 256. Character tables may be loaded offline. Up to eight tables can be loaded.

The structure of the character tables is described in the following figure. The character generator is in map 2 and must be protected using the map mask function.

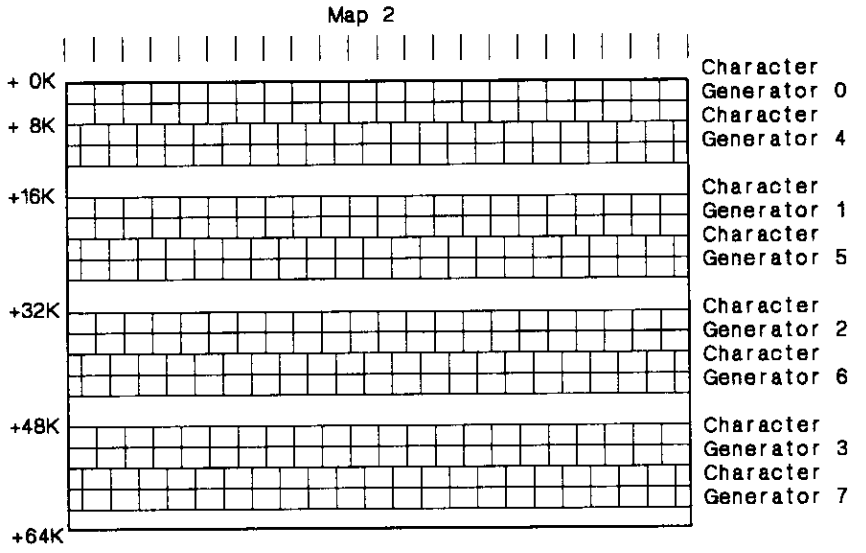


Figure 4-106. Character Table Structure

The following figure illustrates the structure of each character pattern. If the CRT controller is programmed to generate *n* row scans, then *n* bytes must be filled in for each character in the character generator. The example assumes eight row scans per character.

Address	Byte Image								Data
CC * 32 + 0				X	X				18H
1			X	X	X	X			3EH
2		X	X			X	X		66H
3		X	X			X	X		66H
4		X	X	X	X	X	X		7EH
5		X	X			X	X		66H
6		X	X			X	X		66H
7		X	X			X	X		66H

Figure 4-107. Character Pattern Example

CC equals the value of the character code. For example, hex 41 equals an ASCII "A."

Creating a Split Screen

The Video Graphics Array hardware supports a dual screen display. The top portion of the screen is designated as screen A, and the bottom portion of the screen is designated as screen B as in the following figure.

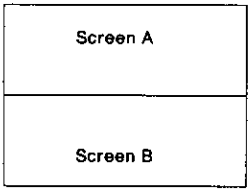


Figure 4-108. Dual Screen Definition

The following figure shows the screen mapping for a system containing a 32K byte alphanumeric storage buffer. Note that the Video Graphics Array has a 32K byte storage buffer in alphanumeric mode. Information displayed on screen A is defined by the Start Address High and Low registers (0CH and 0DH) of the CRTC. Information displayed on screen B always begins at address hex 0000.

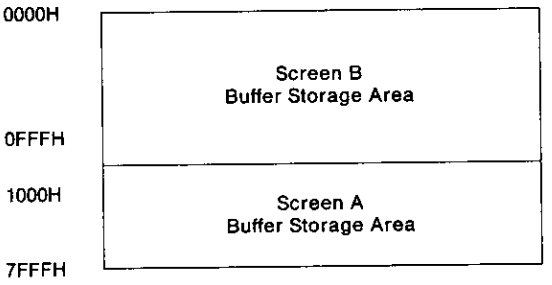


Figure 4-109. Screen Mapping within the Display Buffer Address Space

The Line Compare register (18H) of the CRT Controller performs the split screen function. The CRTC has an internal horizontal scan line counter. The CRTC also has logic that compares the horizontal scan line counter value to the Line Compare register value and clears the memory address generator when a compare occurs. The linear address generator then sequentially addresses the display buffer starting at location 0, and each subsequent row address is determined by the 16-bit addition of the start of line latch and the Offset register.

Screen B can be smoothly scrolled onto the CRT screen by updating the Line Compare in synchronization with the vertical retrace signal. The information on screen B is not affected by scrolling operations that utilize the Start Address High and Low registers to scroll through the Screen A address map.

When bit 5 of the Attribute Mode Control register equals 1, a successful line compare forces the output of the PEL Panning register to 0 until vertical synchronization occurs. When Vsync occurs, the output returns to its programmed value. This feature allows the information on screen B to remain unaffected by PEL-panning operations on screen A.

Video Digital-to-Analog Converter (Video DAC)

The video digital-to-analog converter (DAC) integrates the function of a color look-up table with three internal DACs for driving an analog display.

The size of the color look-up table is 256 by 18 bits to allow the display of 256 colors from a palette of 256K possible colors. Each RGB analog output is driven by a 6-bit DAC. Each register in the color look-up table contains 6 bits each for the red, green, and blue DACs.

Video Digital to Analog Converter (DAC) Addresses in Hex

PEL Address (Write mode)	RW	03C8
PEL Address (Read mode)	WO	03C7
DAC State Register	RO	03C7
PEL Data Register	RW	03C9
PEL Mask *	RW	03C6

RO = Read Only, RW = Read / Write, WO = Write Only.

* This register must not be written to by application code or destruction of the color look-up table may occur.
See also "Video DAC Programming Considerations" on page 4-117.

Figure 4-110. Video DAC I/O Address Usage

Device Operation

The PEL address inputs (P0 - P7) and the blanking input are sampled on the rising edge of the PEL clock. After three further rising edges of the PEL clock, the analog outputs reflect the state of these inputs.

During normal operation the PEL address inputs (P0 - P7) are used as a pointer to one of the 256 internal registers (color look-up table). The value in each register is then, in turn, converted to an analog signal for each of the three analog outputs (red, green, blue). The blanking input can also be used to force the analog outputs to 0 volts. The blanking operation is independent of the state of the PEL address inputs.

During system microprocessor accesses, the 8-bit PEL Address register acts as a pointer to the 256 internal registers. Each internal register is 18 bits wide; 6 bits each for red, green, and blue. The internal registers are accessible through the system microprocessor interface as described below.

The system microprocessor interface is asynchronous with the video path. The timing of this interface is controlled by the 'write enable' and 'read enable' signals.

Video DAC/System Microprocessor Interface

The PEL Address register holds an 8-bit value that is used to address a location within the color look-up table. The PEL Address register may be written to at two different addresses to establish a read or write mode respectively. Once the PEL Address register has been written to and an access has been made to a location in the color-look up table, the PEL Address register automatically increments and further accesses may occur to successive locations.

Each time the PEL Address register is written to at address hex 03C8 it identifies that a write sequence will occur. A write sequence consists of three successive byte writes to the Data register at address hex 03C9. The least-significant 6 bits of each byte are concatenated to form the value placed in the 18-bit Data register. The order is red byte first, then green, and finally blue. Once the third byte has been written, the value in the Data register is written to the location pointed to by the PEL Address register. The order of events for a write cycle is:

1. Write to the PEL Address register at hex 03C8.
2. Three bytes are written to the Data register at hex 03C9.
3. The contents of the Data register are transferred to the location in the color look-up table pointed to by the PEL Address register.
4. The PEL Address register auto-increments by 1.
5. Go to step 2.

Each time the PEL Address register is written to at address hex 03C7 it identifies that a read sequence will occur. A read sequence consists of three successive byte reads from the Data register at address hex 03C9. The least significant 6 bits of each byte taken from

the Data register contain the corresponding color value. The order is red byte first, then green, and finally blue. The order of events for a read cycle is:

1. Write to the PEL Address register at hex 03C7.
2. The contents of the location in the color look-up table pointed to by the PEL Address register are transferred to the Data register.
3. The PEL Address register auto-increments by one.
4. Three bytes are read back from the Data register at hex 03C9.
5. Go to step 2.

If the PEL Address register is written to during either a read or write cycle, a mode is initialized and the unfinished cycle is aborted. The effects of writing to the Data register during a read cycle or reading from the Data register during a write cycle are undefined and may change the look-up table contents.

A read from address hex 03C7 returns 0's in bit positions 0 and 1, if the DAC is currently in a read mode. A read from address hex 03C7 returns ones in bit positions 0 and 1, if the DAC is currently in a write mode.

Reads from the PEL Address register at hex 03C8 or the State register at hex 03C7 do not interfere with read or write cycles and may take place at any time.

Video DAC Programming Considerations

1. As explained in "Video DAC/System Microprocessor Interface" on page 4-116, the effects of writing to the Data register during a read cycle or reading from the Data register during a write cycle are undefined and may change the look-up table contents. Therefore, the following sequence must be followed to ensure the color look-up table integrity during accesses to it:
   a. Write out address to the PEL Address register
   b. Disable Interrupts
   c. Write or read three bytes of data
   d. Go to step C. Repeat this step for the desired number of locations.

e. Enable interrupts.

Note: The above sequence assumes that any interrupting process will return the DAC in the correct mode (write or read). If this is not the case, the sequence shown below should be followed:

a. Disable interrupts

b. Write out address to PEL Address register

c. Write or read three bytes of data

d. Go to step b. Repeat this step for the desired number of locations.

e. Enable interrupts.

2. There is a timing requirement on the minimum amount of time that must separate the trailing edge of one Read or Write command to the DAC and the leading edge of the next Read or Write command. The minimum separation is 240 nanoseconds. Software must ensure that the 240-nanosecond separation exists between two successive accesses to the DAC. Assembly language programs can meet this requirement by placing a JMP instruction between successive accesses to the DAC.

3. To prevent "snow" on the screen, an application reading data from or writing data to the DAC's Data register should ensure that the BLANK input to the DAC is asserted. This can be accomplished either by restricting data transfers to retrace intervals (use Input Status register 1 to determine when retrace is occurring) or by using the Screen Off bit located in the Clocking Mode register of the Sequencer subsection.

   Note: BIOS provides read and write interfaces to the Video DAC.

4. The Mask register (address hex 03C6) must not be written to by application code, or destruction of the color look-up table may result. This register is correctly initialized to hex FF by BIOS during a video mode set.

Auxiliary Video Connector

The Auxiliary Video connector is a 20-pin connector located in line with one of the channel connectors on the system board. This connector allows video data to be passed to an adapter. The system board video buffers can be turned off and video from the adapter can drive the video DAC and the 15-pin video output connector. The full channel is available for use by the adapter. Video cannot be passed in both directions at the same time. The DCLK signal cannot be used to drive both the EXTCLK VGA input and the PCLK DAC input.

For auxiliary video connector signal descriptions, electrical specifications, and connector pin descriptions see Section 2, "Micro Channel Architecture" on page 2-1. Timing diagrams for the signals that interface with the video DAC are contained on page 2-88.

A functional block diagram of the auxiliary video connector and timing diagrams for the display control signals appear on the following pages.

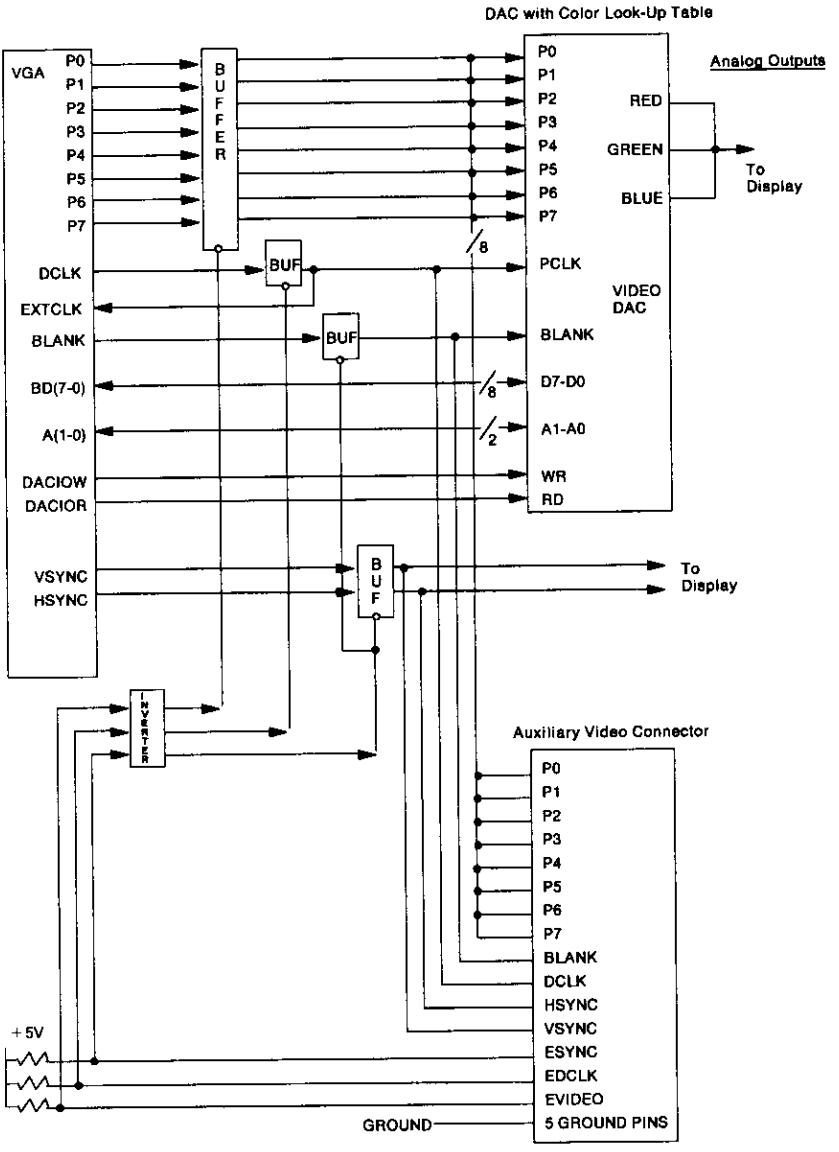


Figure 4-111. Auxiliary Video Connector Block Diagram

15-Pin Display Connector Timing (Sync Signals)

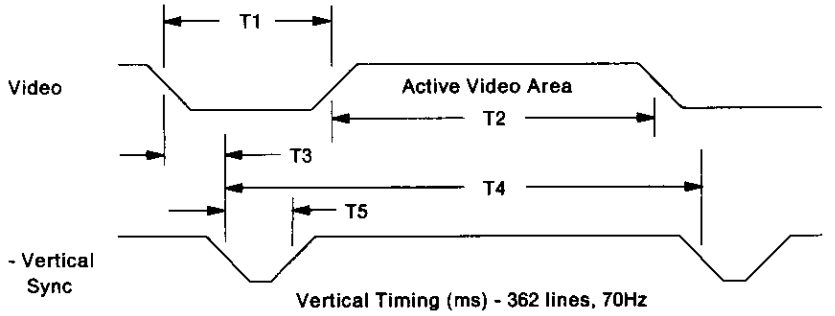
BIOS sets the VGA registers to generate the video modes. The video modes are shown in Figure 4-14 on page 4-27. All of these modes are 70 Hz vertical retrace except for modes 11 and 12. These two modes are 60 Hz vertical retrace. The VGA generates timings that are within the specifications for the supported displays using these modes.

The analog displays operate from 50 to 70 Hz vertical retrace frequency. The following timing diagrams represent only the vertical frequencies set by BIOS.

Note: The vertical size of the display is encoded using the polarity of the sync signals as shown in the following figure. See "Miscellaneous Output Register" on page 4-59 for more information.

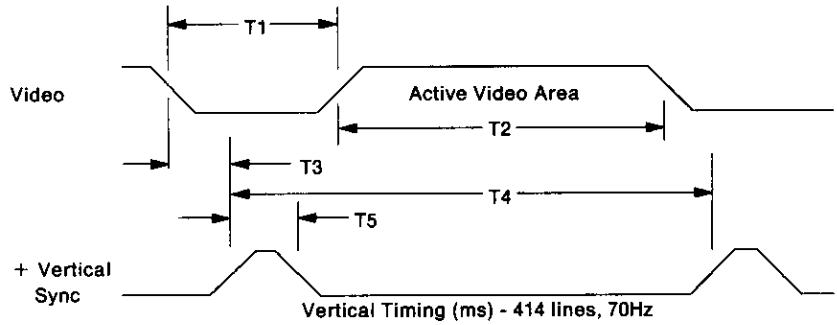
VSYNC Polarity	HSYNC Polarity	Vertical Size
+	+	Reserved
-	+	400 lines
+	-	350 lines
-	-	480 lines

Figure 4-112. Display Vertical Size



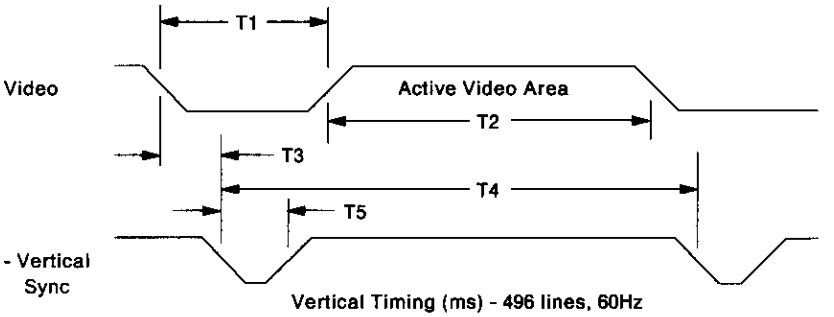
	Signal Time
T1	2.765 milliseconds
T2	11.504 milliseconds
T3	0.985 milliseconds
T4	14.268 milliseconds
T5	0.064 milliseconds

Figure 4-113. Display Vertical Sync, 350 Lines



	Signal Time
T1	1.112 milliseconds
T2	13.156 milliseconds
T3	0.159 milliseconds
T4	14.268 milliseconds
T5	0.064 milliseconds

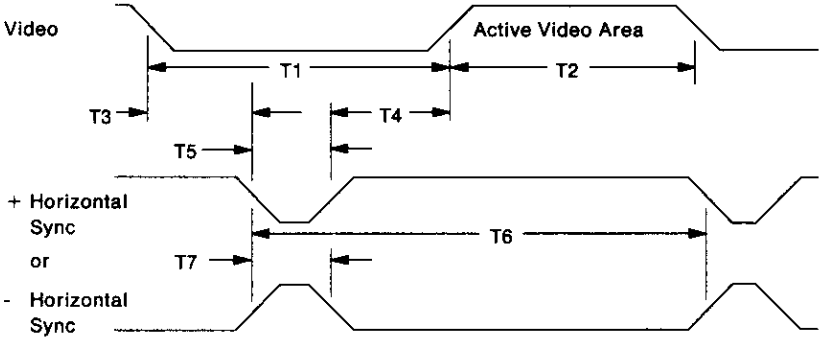
Figure 4-114. Display Vertical Sync, 400 Lines



Vertical Timing (ms) - 496 lines, 60Hz

	Signal Time
T1	0.922 milliseconds
T2	15.762 milliseconds
T3	0.064 milliseconds
T4	16.683 milliseconds
T5	0.064 milliseconds

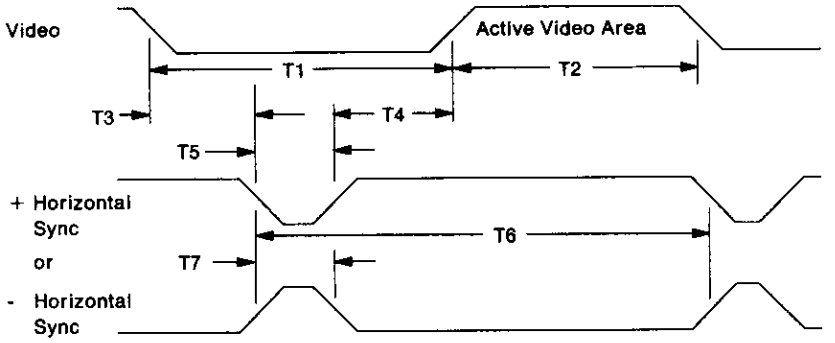
Figure 4-115. Display Vertical Sync, 480 Lines



Horizontal Timing (μs) – 80 column with border

	Signal Time
T1	5.720 microseconds
T2	26.058 microseconds
T3	0.318 microseconds
T4	1.589 microseconds
T5	3.813 microseconds
T6	31.778 microseconds
T7	3.813 microseconds

Figure 4-116. Display Horizontal Timing, 80 Column with Border



Horizontal Timing (μs) – 40/80 column, no border

	Signal Time
T1	6.356 microseconds
T2	25.422 microseconds
T3	0.636 microseconds
T4	1.907 microseconds
T5	3.813 microseconds
T6	31.778 microseconds
T7	3.813 microseconds

Figure 4-117. Display Horizontal Timing, 40/80 Column, no Border

Display Connector

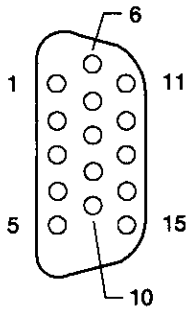


Figure 4-118. 15-Pin D-Shell Display Connector

			Display Type	
Pin	**I/O**	**Output**	**Monochrome**	**Color**
1	O	Red	No Pin	Red
2	O	Green	Mono	Green
3	O	Blue	No Pin	Blue
4	NA	Reserved	No Pin	No Pin
5	NA	Digital G	Self Test	Self Test
6	NA	Red Rtn	Key Pin	Red Rtn
7	NA	Green Rtn	Mono Rtn	Green Rtn
8	NA	Blue Rtn	No Pin	Blue Rtn
9	NA	Plug	No Pin	No Pin
10	NA	Digital G	Digital G	Digital G
11	NA	Reserved	No Pin	Digital G
12	NA	Reserved	Digital G	No Pin
13	O	Hsync	Hsync	Hsync
14	O	Vsync	Vsync	Vsync
15	NA	Reserved	No Pin	No Pin

Red Rtn, Green Rtn, Blue Rtn = Analog Grounds
Digital G = digital ground for sync returns and self test.

Figure 4-119. 15-Pin D-Shell Display Connector Signals

Sequencer Registers

Name	Port (hex)	Index (hex)
Sequencer Address	03C4	-
Reset	03C5	00
Clocking Mode	03C5	01
Map Mask	03C5	02
Character Map Select	03C5	03
Memory Mode	03C5	04

Figure 4-41. Sequencer Register Overview

Sequencer Address Register

The Sequencer Address register is a pointer register located at address hex 03C4. This register is loaded with a binary value that points to the Sequencer Data register where data is to be written. This value is referred to as "Index" in the figure above.

Bit	Function
7 - 3	Reserved = 0
2 - 0	Sequencer Address

Figure 4-42. Sequencer Address Register

Bits 7 - 3 Reserved

Bits 2 - 0 Sequencer Address Bits - A binary value pointing to the register where data is to be written.

Reset Register

This is a read/write register pointed to when the value in the Address register is hex 00. The port address for this register is hex 03C5.

Bit	Function
7 - 2	Reserved = 0
1	Synchronous Reset
0	Asynchronous Reset

Figure 4-43. Reset Register, Index Hex 00

Bits 7 - 2 Reserved