VADEM VG-468

PC CARD SOCKET CONTROLLER

DATA MANUAL

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PREFACE

PRODUCT OVERVIEW

The Vadem VG-468 is a compact, highly integrated PC Card controller chip implementing the latest PCMCIA specifications along with ExCA™ extensions. It is register -compatible to the Intel® 82365SL. Supporting two PC Card sockets, it is uniquely designed for space-limited, cost-sensitive applications where battery life is an important factor. For systems requiring more than two sockets, the VG-468 can be cascaded to support up to eight sockets without external logic. With external decoder logic, unlimited cascading is possible. Typical VG-468 applications include small notebook computers, palmtops and other personal information devices.

The VG-468 supports the system bus timing of standard ISA and EISA architectures, including those based on the Intel 386SL. A programmable configuration mechanism allows the system manufacturer to control many PC Card setup parameters in software or firmware.

Power management based on activity monitoring together with the VG-468's very low current-draw combine to minimize its demand for battery power.

VADEM VG-468
PC CARD SOCKET CONTROLLER

PRODUCT FEATURES

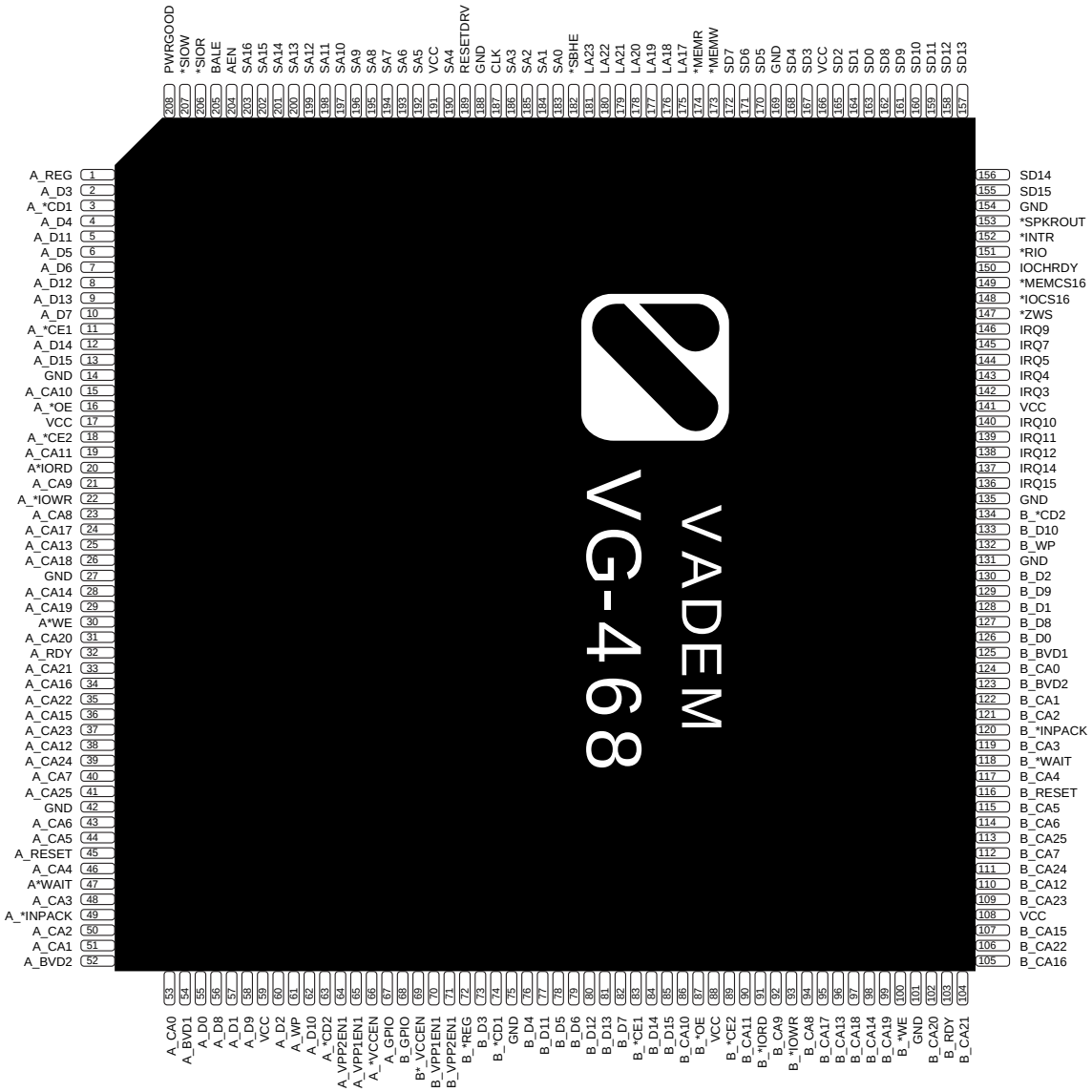
- 208-pin chip provides full ExCA implementation of two PCMCIA PC Card sockets.
  - — Supports both memory cards and I/O cards (miniature peripherals).
  - — Supports PCMCIA-ATA hard disks and semiconductor disks.
  - — Memory-saving execute-in-place standard (XIP).
  - — Supports overlapping I/O windows across sockets and duplicate I/O cards via *INPACK signal.
  - — All ExCA extensions.
  - — Cascadable up to eight sockets without “glue,” unlimited cascading with external logic.
- Register-compatible with Intel 82365SL.
- Five mappable memory windows and two mappable I/O windows for each socket.
- Internal buffering supports “hot” insertion and removal of cards.
- Selectable programming voltage for various programmable devices.
- Integrated timer supports power management based on activity monitoring.
- Includes two GPIO pins.

Pin Diagram

This section provides the pin assignment, signal description, block diagram, and pin descriptions for the VG-468 PC Card Socket Controller.

Pin Diagram
Figure 1-1

DEFAULT PIN ASSIGNMENT



ALTERNATIVE PIN DEFINITIONS

PIN #	DEFAULT	ALTERNATIVE(S)
32,103	RDY/*BSY	*IREQ
52,123	BVD2	*SPKR
54,125	BVD1	*STSCHG, *RI
61,132	WP	*IOIS16
67,68	GPIO	*VPPVALID

(ALSO SEE PAGE 21)

Signal Description

Pin #	Signal Names	Type	Characteristics	# Pins
204	AEN	I	TTL Compatible	1
205	BALE	I	TTL Compatible	1
54, 125	BVD1 (*STSCHG/*RI)	I	CMOS Schmitt Trigger	2
52, 123	BVD2 (*SPKR)	I	CMOS Schmitt Trigger	2
15,19,21, 23-26,28,29 31,33-41,43 44,46,48,50 51,53,86,90 92,94-99, 102,104-107 109-115,117 119,121,122 124	CA[25:0]	O	4mA Tri-State	52
63,3,134,74	*CD[2:1]	I	CMOS Schmitt Trigger	4
89,83,18,11	*CE[2:1]	O	4mA Tri-State	4
187	CLK	I	TTL Compatible	1
2,4-10,12,13 55-58,60,62 73,76-82,84 85,126-130 133	D[15:0]	I/O	I = TTL Compatible O = 4mA Output	32
14,27,42,75 101,131,135 154,169,188	GND			10
67,68	GPIO	I/O	I = CMOS Schmitt Trigger O = 4mA Tri-State	2
49,120	*INPACK	I	TTL Compatible	2
152	*INTR	I/O	I = TTL Compatible O = 4mA Tri-State	1
150	IOCHRDY	O	16 mA Tri-State	1
148	*IOCS16	O	16 mA 5V Open Drain	1
20,91	*IORD	O	4mA Tri-State	2
22,93	*IOWR	O	4mA Tri-State	2
136-140 146-142	IRQs	O	4mA Tri-State	10

Signal Description (cont.)

Pin #	Signal Names	Type	Characteristics	# Pins
181-175	LA[23:17]	I	TTL Compatible	7
149	*MEMCS16	O	16 mA 5V Open Drain	1
174	*MEMR	I	TTL Compatible	1
173	*MEMW	I	TTL Compatible	1
16,87	*OE	O	4mA Tri-State	2
208	PWRGOOD	I	Schmitt Trigger	1
32,103	RDY/*BSY (*IREQ)	I	CMOS Schmitt Trigger	2
1,72	*REG	O	4mA Tri-State	2
45,116	RESET	O	4mA Tri-State	2
189	RESETDRV	I	Schmitt Trigger with pull-down	1
151	*RIO/LED	I/O	I = TTL Compatible O = 4mA Tri-State	1
203-192,190 186-183	SA[16:0]	I	TTL Compatible	17
182	*SBHE	I	TTL Compatible	1
206	*SIOR	I	TTL Compatible	1
207	*SIOW	I	TTL Compatible	1
155-162, 172-170,168 167,165-163	SD[15:0]	I/O	I = TTL Compatible O = 8mA Tri-State	16
153	*SPKROUT	I/O	I = TTL Compatible O = 4mA Tri-State	1
17,59,88, 108,141,166 191	VCC			7
66,69	*VCCEN	O	4mA Output	2
65,70	VPP1EN1	O	4mA Output	2
64,71	VPP2EN1	O	4mA Output	2
47,118	*WAIT	I	TTL Compatible	2
30,100	*WE/*PRGM	O	4mA Tri-State	2
61,132	WP (*IOIS16)	I	TTL Compatible	2
147	*ZWS	O	16mA 5V Open Drain	1

Pin Descriptions

Symbol	Type	Pin No.	Description
AEN	I	204	System Address Enable. High during DMA cycles, low otherwise.
BALE	I	205	Bus Address Latch Enable. An active high input used to latch LA[23:17] at the beginning of a bus cycle.
BVD1 (*STSCHG/*RI)	I	54,125	If BVD1 is negated by a memory PC Card with a battery, it indicates that the battery is no longer serviceable and data is lost. For I/O PC Cards, this signal is held high when either or both the Signal on Change bit and Changed bit in the Card Status Register on the PC Card are set to zero. When both the bits are one, the signal is held low. The Changed bit is the logical OR of the bits CVBAT1, CVBAT2, CWP and CBSYRDY in the Pin Replacement Register on the PC Card. Or this pin is connected to Ring Indicate, which is qualified by Ring Indicate Enable to be passed on to the *RIO pin.
BVD2 (*SPKR)	I	52,123	BVD1 and BVD2 are generated by memory PC Cards with onboard batteries. These signals indicate the health of the battery. Both are asserted high when the battery is in good condition. When BVD2 is negated while BVD1 is still asserted, the battery should be replaced, although data integrity on the memory PC Card is still assured. When the I/O interface is selected, BVD2 may be used to provide a single amplitude Digital Audio waveform intended to be passed through to the system's speaker without signal conditioning.
CA[25:0]	O	15,19,21 23-26,28 28,31 33-41,43 44,46,48 50,51,53 86,90,92 94-99,102 104-107 109-115,117 119,121,122 124	Card Address.

Pin Descriptions (continued)

Symbol	Type	Pin No.	Description
*CD[2:1]	I	63,3 134,74	Detects proper card insertion. The signals are connected to ground internally on the PC Card and will be forced low whenever a card is placed in a host socket. Status is available to software through the Interface Status Register.
*CE[2:1]	O	89,83 18,11	Active low card enable signals. *CE1 is used to enable even bytes, *CE2 for odd bytes. A multiplexing scheme based on A0, *CE1, *CE2 allows 8-bit hosts to access all data on Card Data[7:0] if desired.
CLK	I	187	System clock.
D[15:0]	I/O	2,4-10 12,13 55-58 60,62,73 76-82 84,85 126-130 133	Card data.
GPIO	I/O	67,68	General purpose input/output. May be used for one of several purposes. - An active low input indicates that Vpp power line has reached the user specified range. - An input indication a card eject or card insertion pending. - An input source for generating a card status change interrupt. - Programmable chip select output.
*INPACK	I	49,120	Input Acknowledge. Asserted by some PC Cards during I/O read cycles. This signal is used by the VG-468 to control the enable of its input data buffer between the card and CPU.

Pin Descriptions (continued)

Symbol	Type	Pin No.	Description
*INTR	I/O	152	Interrupt Request output: Active low output requesting a nonmaskable interrupt to the CPU. Also, a resistor strapping input during RESETDRV to determine the mapping of socket A and socket B to one of four groups.
IOCHRDY	O	150	I/O Channel Ready. This active high signal indicates that the current I/O bus cycle has completed. When a PC Card needs to extend a Read or Write cycle, the VG-468 pulls IOCHRDY low. IOCHRDY can be deasserted by either *WAIT, or by programming to add wait states for 16-bit memory and I/O cycles. If *WAIT is used in 16-bit mode, the wait state generator has to be set to 1 wait state.
*IOCS16	O	148	This active low I/O 16-bit chip select signal indicates to the host system the current I/O cycle is a 16-bit access. A 16-bit to 8-bit conversion is done if it is inactive.
*IORD	O	20,91	I/O Read signal is driven active to read data from the PC Card's I/O space. The *REG signal and at least one of the Card Enable signals must also be active for the I/O transfer to take place.
*IOWR	O	22,93	I/O Write signal is driven active to write data to the PC Card's I/O space. The *REG signal and at least one of the Card Enable signals must also be active for the I/O transfer to take place.
IRQs	O	136-140 146-142	IRQ[15, 14, 12:9, 7, 5:3].
LA[23:17]	I	181-175	Local Address bus used to address memory devices on the ISA-bus. Together with the system address signals, they address up to 16MB on the ISA bus.
*MEMCS16	O	149	This active low 16-bit memory chip select signal indicates to the host system that the current memory cycle is a 16-bit access. A 16-bit to 8-bit conversion is done if it is inactive.

Pin Descriptions (continued)

Symbol	Type	Pin No.	Description
*MEMR	I	174	Active low signal indicates a memory read cycle.
*MEMW	I	173	Active low signal indicates a memory write cycle.
*OE	O	16,87	Active low signal used to gate memory reads from memory cards.
PWRGOOD	I	208	Power Good is an active high signal which indicates that power to the system is stable. Combined with RESETDRV, it will indicate to VG-365 whether a cold reset, or a resume reset has occurred, to decide whether to reset the slot configuration registers. System implementations without a "POWERGOOD" as resume indication should tie this signal low.
RDY/*BSY (*IREQ)	I	32,103	Memory PC Cards drive Ready / *Busy low to indicate that the memory card circuits are busy processing a previous write command. It is set high when they are ready to accept a new data transfer command. For I/O PC Cards, this pin is used as an interrupt request and driven low to indicate to the host that a device on the I/O PC Card requires service by the host software. The signal is held at the inactive level when no interrupt is requested.
*REG	O	1,72	Select attribute memory. This signal is set inactive (high) for all accesses to common memory of a PC Card. When it is active, access is limited to Attribute Memory when *WE or *OE are active, and to I/O ports when *IORD or *IOWR are active. I/O PC Cards will not respond to *IORD or *IOWR when the *REG signal is inactive. During DMA operations the *REG signal is inactive.

Pin Descriptions (continued)

Symbol	Type	Pin No.	Description
RESET	O	45,116	Provides a hard reset to a PC Card and clears the Card Configuration Option Register, thus placing card in an unconfigured (memory interface) state.
RESETDRV	I	189	Active high indicates a main system reset.
*RIO/LED	I/O	151	Ring Indicate Output. Pass through of Ring Indicate output from I/O PC Card. VG-468 can also be configured to activate *RIO on card detect changes. *RIO will be functional in *CS controlled power down. When disk drive LED enable is set this signal becomes a driver for disk drive LED. Also, a resistor strapping input during RESETDRV to determine the functions of pin B_CA[11:4].
SA[16:0]	I	203-192 190 186-183	System Address bus used to address memory and I/O devices on the ISA bus. These signals are latched and are valid throughout the bus cycle.
*SBHE	I	182	System Byte High Enable. When asserted, this active low signal indicates that a data transfer is occurring on the upper byte of the system data bus.
SD[15:0]	I/O	155-162, 172-170, 168,167 165-163	System Data Bus.
*SIOR	I	206	This active low I/O read signal instructs the VG-468 to drive data onto the data bus.
*SIOW	I	207	This active low I/O write signal instructs the VG-468 to latch the data on the data bus.
*SPKROUT	I/O	153	Digital audio signal which provides a single amplitude (digital) audio waveform to drive the system's speaker. Passes through *SPKR from an I/O PC Card. This signal must be held high when no audio signal is present. Also, a resistor strapping input during RESETDRV to determine the mapping of socket A and socket B to one of four groups.

Pin Descriptions (continued)

Symbol	Type	Pin No.	Description
*VCCEN	O	66,69	Power Control signal for card Vcc.
VPP1EN1	O	65,70	Power Control signal for card Vpp1.
VPP2EN1	O	64,71	Power Control signal for card Vpp2.
*WAIT	I	47,118	This signal is driven by the PC Card to delay completion of the memory or I/O cycle in progress.
*WE/*PRGM	O	30,100	The host uses *WE for gating memory write data, and for memory PC Cards that employ programmable memory.
WP (*IOIS16)	I	61,132	Reflects the status of the Write Protect switch on some memory PC Cards. If the memory PC Card has no write protect switch, the card will connect this line to ground (the card can always be written) or to Vcc (permanently write protected). When the I/O interface is selected, this pin is used for the "I/O is 16-bit Port" function: asserted by the PC Card when the address on the bus corresponds to an address to which the PC Card responds, and the I/O Port which is addressed is capable of 16-bit access. If this signal is not asserted during a 16-bit I/O access, the system will generate 8-bit references to the even and odd byte of the 16-bit port being accessed. If 8-bit window size is selected, *IOIS16 is ignored.
*ZWS	O	147	Zero Wait State. An active low output indicates that the PC Card wishes to terminate the present bus cycle without inserting additional wait states. This cycle will not be driven during a 16-bit I/O access.

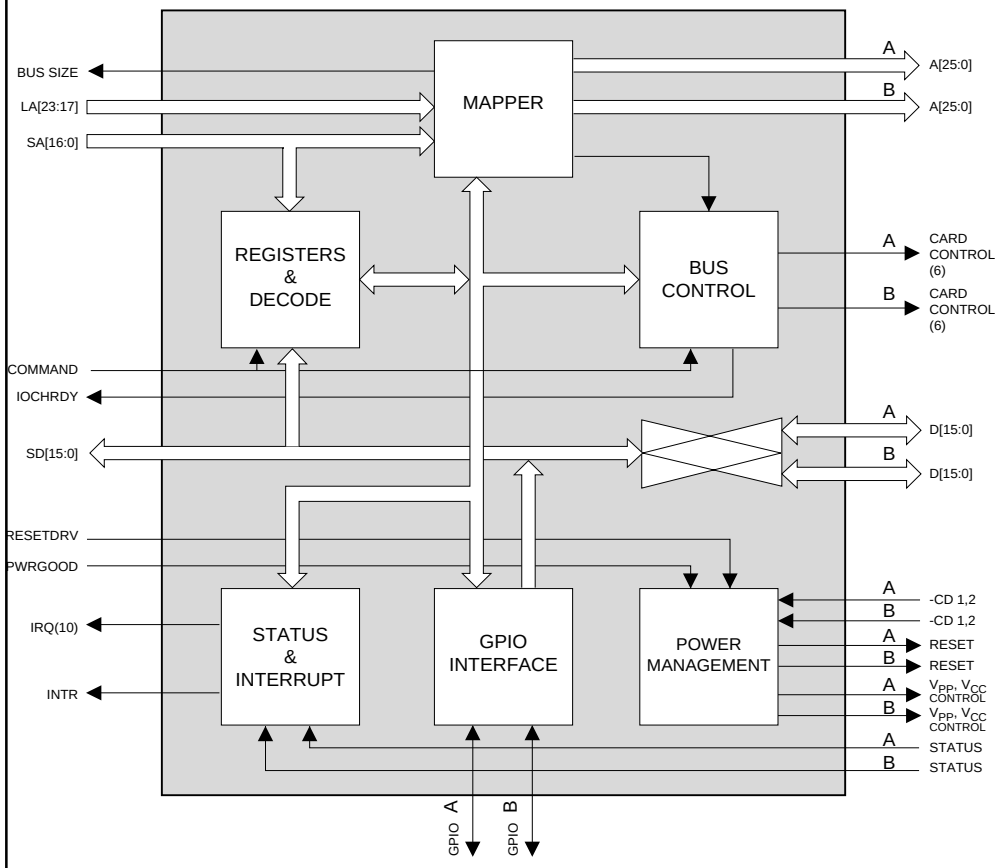
NOTES

Chapter 2
Functional Description

This section provides a description of the functional blocks that comprise the VG-468 PC Card Socket Controller (VG-468). Chief functional blocks of the VG-468 include the ISA bus interface, PC Card socket interface, memory and I/O window mapping, power management support, interrupt handling, configuration, status and control registers and GPIO.

Functional Block Diagram
Figure 2-1

VG-468 BLOCK DIAGRAM



ISA INTERFACE

The VG-468 interfaces directly to a synchronous or asynchronous ISA bus. No external buffers or transceivers are needed. For systems based on the 386SL, the VG-468 provides the special signals PWRGOOD, *SPKROUT, and *INTR.

PCMCIA/JEIDA PC CARD SOCKET INTERFACE

The 68-pin PCMCIA/JEIDA PC Card socket interface consists of 60 signals and 8 power connections. A single VG-468 supports two PC Card sockets directly. Up to eight PC Card sockets may be supported by cascading VG-468's. If an external decoder is used, any number of sockets can be supported. Each VG-468 is uniquely selected using pull-up/pull-down resistors (see Register Addressing section on page 19).

PC Card Status

The status of the PC Card including detection of card insertion or removal, memory write protect status, battery voltage warnings, PC Card power status, and Ready/Busy is accessible through the interface status register. A change in status can cause a card status change interrupt (such as when a PC Card is inserted or removed). The various sources of the interrupt may be enabled separately.

Control/Status Signal Multiplexers

The VG-468 supports two PC Card types (either memory or I/O) interchangeably. A number of the PC Card signals have different uses based on the PC Card type. The VG-468 incorporates multiplexers to redirect the appropriate signals that are defined differently for memory and I/O PC Cards. These signals are configured correctly based upon the setting of the PC Card type bit in the Interrupt and General Control Register.

PC Card Insertion and Removal

The VG-468 incorporates power sequencing time delays specified by ExCA and PCMCIA, which can be enabled under software control.

When installing a card, there is a 65 ms minimum debounce time on the card detects. Card removal is detected immediately and is not debounced. Three bits in the Power and RESETDRV Control Register are involved: Output Enable, Auto Power Switch Enable, and PC Card Power Enable.

When installing a PC Card, if Auto Power Switch Enable and PC Card Power Enable are true, card power goes on after the debounce time. If Auto Power Switch Enable is false, PC Card Power Enable controls card power directly, and card detects have no effect on card power. At least 330 ms after debounced card detect is true and card power is on, the card interface signal outputs will be enabled if Output Enable is true.

When a PC Card is removed, the interface signal outputs are tristated after a minimum of 500 microseconds delay. If a bus cycle is in progress the outputs will not turn off until the end of the cycle. If Auto Power Switch Enable is true, card power also turns off 500 microseconds after that. If Auto Power Switch Enable is false, card power remains on.

At any time, clearing PC Card Output Enable tristates the card interface signal outputs immediately, and clearing PC Card Power Enable turns card power off immediately. When card power turns off, the card interface signal outputs also turn off immediately.

MEMORY AND I/O MAPPING

Multiple PC Cards in a system can conflict if they try to utilize the same system memory and I/O range. The VG-468 allows the operating system to map PC Card memory into up to five separate memory ranges, and PC Card I/O into two separate I/O ranges, thus avoiding system configuration conflicts.

The VG-468 provides I/O address mapping, memory paging and memory address mapping for both PC Card attribute and common memory. The VG-468 includes registers which provide access to the card information structure and card configuration registers within PC Card's attribute memory described by the PCMCIA/JEIDA PC Card Standard.

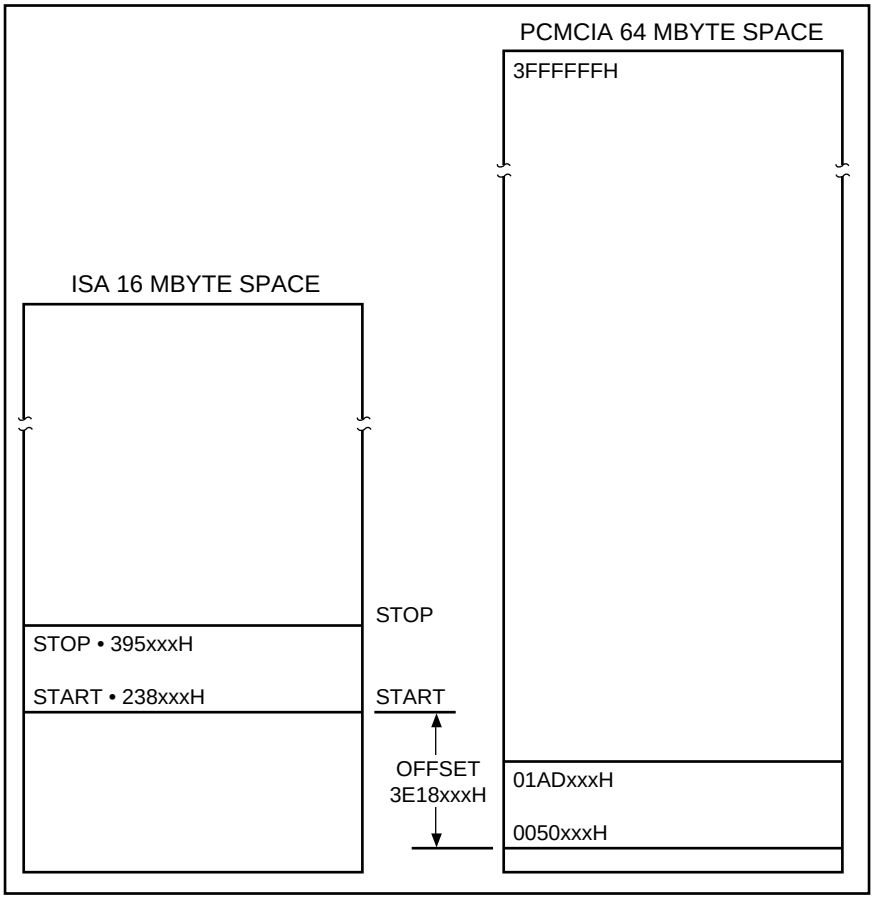
PC Card Memory Addressing

The VG-468 provides logic to map portions of the 64MB common memory and/or 64MB attribute memory spaces found on PC Cards into the smaller 16MB system (ISA) address space. These mapping functions allow expansion of the system address space up to the full 64MB PC Card capability.

The VG-468 supports 5 independently enabled and controlled system memory address mapping windows. Each system memory window may map into either the common or attribute memory space of the PC Card and may independently control memory data bus width, system bus wait states, software write protect, and card enable.

Mapping of each system memory window starts and stops on any 4K byte boundary of ISA system memory above 64K. The VG-468 does not allow mapping of a system memory window between 0 and 64K in the system address space. Only I/O address windows are allowed to be mapped into that range. This limitation allows the VG-468 to resolve conflicts when accessing I/O PC Cards that contain memory.

Memory Map
Figure 2-2



Opening a Window

To open a window, software sets the system memory start address (Start), system memory stop address (Stop), and PC Card memory offset appropriately. If Start = Stop, the minimum size of 4K bytes is realized. The offset address is set by the software to be equal to the 2's complement of the difference between Start and the start address of the PC Card , and is added to the system address to generate the address for the PC Card.

PC Card memory is accessed only when all of the following conditions are satisfied:

1. The system memory address mapping window is enabled.
2. The system memory address is greater than or equal to the system memory address mapping start register A[23:12].
3. The system memory address is less than or equal to the system memory address mapping stop register A[23:12].

All the system memory address mapping windows can be configured by software to be independently used, or can be used together for special memory mapping requirements, like LIM/EMS or XIP.

Multiple ROM executable images on a single PC Card may be organized by the system memory address mapping windows. These images must be aligned to start on a 4 K byte boundary of the memory PC Card. Software can access these ROM executable images by setting the size of a system memory address mapping window to the size of the executable image (minimum 4 K block), and setting the PC Card memory offset from the system memory start address (Start) to generate the address of the first byte of the executable image on the PC Card.

The PC Card memory offset can be either a positive or negative value. Furthermore, the VG-468 does not check for a window whose size and offset allow it to wrap from the last PC Card address to the first PC Card address. *Software must check to prevent address wrapping*.

PC Card I/O Addressing

The ISA system bus is limited to 768 bytes of common I/O address space between I/O addresses 100H and 3FFH. The VG-468 supports system I/O address decode from 0 to 64K. A PC Card can request specific common I/O address locations or it can request a block of I/O space by the size required. When I/O space is requested by size, the system is free to locate the PC Card anywhere in the 64K system I/O address space. The PC Card decodes the *CE[2:1], *IORD, and *IOWR signals to respond to an I/O access.

The VG-468 provides two independently enabled and controlled I/O address windows which are defined by 16-bit addresses to achieve a 1 byte resolution. Each window has independent control of I/O data bus width, zero wait state system bus access, and generation of *IOCS16.

A PC Card I/O address is accessed only when all of the following conditions are satisfied:

1. The I/O address window is enabled.
2. The system address is greater than or equal to the I/O address start register A[15:0].
3. The system address is less than or equal to the I/O address stop register A[15:0].
4. The access is not a DMA transfer. AEN = 0 to access the I/O PC Card.

It is the responsibility of the system software to account for each I/O address range assigned to a particular PC Card. The reservation of a particular I/O address range for each PC Card can reduce card power consumption since only one PC Card is enabled during each I/O access.

The VG-468 can directly map the system I/O address space to the PC Card I/O ports with single byte granularity. Each PC Card is guaranteed a reserved system I/O address space, and an I/O cycle will be generated to the PC Card only within the assigned space.

Memory Paging

System memory paging is supported in the VG-468 through the use of multiple system memory address mapping windows. When using LIM or XIP, software should assign a window to each page required to support the LIM/XIP function. The software has the responsibility to set up the system memory address mapping windows to be in one contiguous system address space with each window controlling a single page in the PC Card memory. When changing the page pointer only the PC Card memory offset address value needs to be altered to change the mapping.

Attribute Memory Address Mapping

PC Card attribute memory can be accessed through any of the system memory address mapping windows. Software sets the REG active bit in the Card Memory Offset Address Register to one. The system memory window to attribute memory can be mapped from any ISA address above 64K to any PC Card address.

Multiple system memory address mapping windows to separate attribute memory address spaces can be opened simultaneously. Each of these windows can be configured to use a different number of wait states, software write protect, and data width.

Common Memory Address Mapping

PC Card common memory can be accessed through any of the system memory address mapping windows. Software sets the REG active bit in the Card Memory Offset Address Register to zero. The system memory window into PC Card common memory can be mapped from any ISA address above 64K to any PC Card memory address.

Multiple system memory address mapping windows into separate PC Card common memory address spaces can be opened simultaneously. Each of these windows can be configured to use a different number of wait states, software write protect, and data width.

POWER MANAGEMENT

The VG-468 implements power management for each PC Card socket. Programming the Power and RESETDRV control register controls socket power management. Power sequencing time delays specified by ExCA and PCMCIA are implemented in hardware.

The VG-468 will automatically enter into lower power consumption state when memory windows and I/O windows are disabled, and when sockets become empty. Further, the lowest power consumption level can be achieved by putting the VG-468 into *CS controlled power down mode. This mode is entered by disabling all the I/O, memory windows, output buffers, enabling the power down mode, and driving the *CS to high.

During the *CS controlled down, VG-468's Vcc will still be powered up, and the internal register contents will be maintained. The interrupt (IRQs) can still be generated to the host system from either card status change, or PC Card interrupt requests. *RIO can still be armed to route either *RI or Card detect change. *INTR can still be armed for card status change interrupts but will not be generated until power down mode is exited.

A unique feature is provided to VG-468 to support host system suspend/resume operation. When the host system enters suspend mode, the VG-468 can be powered at 3.3V, and still maintain the ability to route the *RI signals from both sockets to *RIO signal as the resume indication to the host system.

INTERRUPT HANDLING

Since multiple PC Cards in a system can conflict if they try to utilize the same interrupt, the VG-468 can be programmed to eliminate this conflict by routing each PC Card interrupt request to a different system interrupt. Based upon four bits in the Interrupt and General Control Register, the interrupt request signal (*IREQ) from an I/O PC Card will be directed to one of ten interrupt request lines on the system bus.

The VG-468 provides a card status change interrupt which can notify the system of a change in the battery voltage levels, card insertion/removal detection, Ready/*Busy condition, and status change. It can be directed to one of the ten interrupt request lines on the system bus based upon four bits in the Card Status Change Interrupt Configuration Register. When used with a CPU that supports SMI, it should be configured as the *INTR signal and connected to the *EXTSMI input of the CPU.

The ten interrupt request lines can all be configured as edge-triggered to support the standard interrupt from I/O cards and card status change interrupts, or as level mode interrupts to support I/O cards with pulse-mode interrupt requests.

Also, the VG-468 can be configured to have IRQ14 in level mode, while all other IRQ's in edge-trigger mode, therefore can support PC cards with pulse mode and edge-mode interrupts and card status change interrupts simultaneously.

CONFIGURATION, STATUS AND CONTROL REGISTERS

The VG-468 provides a register containing the type of PC Card supported at the socket and the revision level of the VG-468. Through other registers, the VG-468 provides complete control of a PC Card. Among the functions provided are bit programmable memory write protect for the attribute and common memory, Vcc, Vpp1 and Vpp2 power control, and interrupt steering. Control of the signal multiplexers for directing the appropriate memory or I/O signals to the socket is also provided, as well as control bits to set memory and I/O data path size. Other registers set the boundaries of the memory and I/O mapping windows. Finally, a number of registers reflect the status of the PC Card.

Register Addressing

All VG-468 control registers are byte wide and accessed using an indirect indexing scheme. Two I/O addresses, one for index register and one for data register, are required to access each group of the control registers for each socket. Each group contains a block of 64 indirectly accessed registers. In order to support up to four VG-468's in a system, two selectable sets of I/O addresses are available — 3E0h/3E1h and 3E2h/3E3h.

The I/O address and the starting base of the index register values in each VG-468 are selected by pullup/pulldown strapping resistors on the *INTR and *SPKROUT pins, according to the table. While RESETDRV is true these pins become inputs, the falling edge of RESETDRV latches the pulled up or down state of the pins, and thereafter the pins resume their normal function.

The index register is a read/write register, although to avoid contention in systems with multiple VG-468's, only the one whose index register points to an index within the range determined by resistor strapping will respond to index register read accesses. The data registers are read/write registers except as noted in the register descriptions. Following and assertion of RESETDRV with PWRGOOD low, the VG-468 will not respond to a data register read or write operation or to an index register read operation until a value within the range specified by the strapping resistors has been written to the index register.

Strapping Option Table for Selecting the Index Base Values and I/O Addresses:

*INTR Resistor	*SPKROUT Resistor	Index Base Value	I/O Address
Pullup	Pullup	00h	3E0h/3E1h
Pullup	Pulldown	80h	3E0h/3E1h
Pulldown	Pullup	00h	3E2h/3E3h
Pulldown	Pulldown	80h	3E2h/3E3h

The VG-468 can also be configured to respond to an external chip select input, allowing an unlimited number of VG-468's to exist in a system. Up to three VG-468's using internal decoding can also coexist with an unlimited number using external decoding. The devices which use external decoding may have the same or different strapping resistor configurations, which must be different from the configurations used by all devices which use internal decoding. Each device using internal decoding must have a unique strapping resistor configuration.

DIGITAL AUDIO SUPPORT

The VG-468 supports special signals such as digital audio. These signals are passed through to the system bus without signal conditioning. The digital audio signal (*SPKR) from the socket is passed through to the speaker output pin (*SPKROUT) of the VG-468.

FULL Vpp SUPPORT

VG-468 has two Vpp control pins per socket to independently switch Vpp1 and Vpp2 between 5V and 12V if Vcc is enabled. Some systems may wish to implement a third level (0V or no-connect) for Vpp when Vcc is on. To this end VG-468 provides a resistor strapping option on the *RIO/LED pin to change the definition of the B_CA[11:4] pins. B_CA[11:4] in this configuration will be handled by an external buffer controlled by B_*ENABLE.

Strapping Option Table for Alternate Definition of B_CA[11:4]

Pin Definition w/ *RIO/LED Pullup	Alternate Definition w/ *RIO/LED Pulldown
B_CA11	A_VPP2EN0
B_CA10	A_VPP1EN0
B_CA9	B_VPP2EN0
B_CA8	B_VPP1EN0
B_CA7	B_*ENABLE
B_CA6	*CS
B_CA5	A_GPO/PCS
B_CA4	B_GPO/PCS
A_GPIO	A_*GPI
B_GPIO	B_*GPI

Note that GPIOs are multiplexed between GPI, GPO/PCS, and *CS in the regular definition. In the alternate definition all functions are decoupled.

NOTES

Chapter 3
Register Summary

This section defines the registers used by the VG-468 PC Card Socket Controller. The General Registers, Interrupt Registers, I/O Registers and Memory Registers are all fully compatible with the Intel 82365 SL. All other registers are unique to the VG-468. All reserved bits must be set to zero to avoid unpredictable problems.

General Setup Registers

Name	Socket A Index	Socket B Index	Access
Identification and Revision	00H	40H	RO
Interface Status	01H	41H	RO
Power and RESETDRV Control	02H	42H	R/W
Card Status Change	04H	44H	R/W
Address Window Enable	06H	46H	R/W
Card Detect and General Control Register	16H	56H	R/W
Global Control Register	1EH	5EH	R/W

Interrupt Registers

Name	Socket A Index	Socket B Index	Access
Interrupt and General Control	03H	43H	R/W
Card Status Change Interrupt Configuration	05H	45H	R/W

I/O Registers

Name	Socket A Index	Socket B Index	Access
I/O Control	07H	47H	R/W
I/O Address 0 Start Low Byte	08H	48H	R/W
I/O Address 0 Start High Byte	09H	49H	R/W
I/O Address 0 Stop Low Byte	0AH	4AH	R/W
I/O Address 0 Stop High Byte	0BH	4BH	R/W
I/O Address 1 Start Low Byte	0CH	4CH	R/W
I/O Address 1 Start High Byte	0DH	4DH	R/W
I/O Address 1 Stop Low Byte	0EH	4EH	R/W
I/O Address 1 Stop High Byte	0FH	4FH	R/W

Memory Registers

Name	Socket A Index	Socket B Index	Access
System Memory Address 0 Mapping Start Low Byte	10H	50H	R/W
System Memory Address 0 Mapping Start High Byte	11H	51H	R/W
System Memory Address 0 Mapping Stop Low Byte	12H	52H	R/W
System Memory Address 0 Mapping Stop High Byte	13H	53H	R/W
Card Memory Offset Address 0 Low Byte	14H	54H	R/W
Card Memory Offset Address 0 High Byte	15H	55H	R/W
System Memory Address 1 Mapping Start Low Byte	18H	58H	R/W
System Memory Address 1 Mapping Start High Byte	19H	59H	R/W
System Memory Address 1 Mapping Stop Low Byte	1AH	5AH	R/W
System Memory Address 1 Mapping Stop High Byte	1BH	5BH	R/W
Card Memory Offset Address 1 Low Byte	1CH	5CH	R/W
Card Memory Offset Address 1 High Byte	1DH	5DH	R/W
System Memory Address 2 Mapping Start Low Byte	20H	60H	R/W
System Memory Address 2 Mapping Start High Byte	21H	61H	R/W
System Memory Address 2 Mapping Stop Low Byte	22H	62H	R/W
System Memory Address 2 Mapping Stop High Byte	23H	63H	R/W

Memory Registers (continued)

Name	Socket A Index	Socket B Index	Access
Card Memory Offset Address 2 Low Byte	24H	64H	R/W
Card Memory Offset Address 2 High Byte	25H	65H	R/W
System Memory Address 3 Mapping Star1 Low Byte	28H	68H	R/W
System Memory Address 3 Mapping Start High Byte	29H	69H	R/W
System Memory Address 3 Mapping Stop Low Byte	2AH	6AH	R/W
System Memory Address 3 Mapping Stop High Byte	2BH	6BH	R/W
Card Memory Offset Address 3 Low Byte	2CH	6CH	R/W
Card Memory Offset Address 3 High Byte	2DH	6DH	R/W
System Memory Address 4 Mapping Start Low Byte	30H	70H	R/W
System Memory Address 4 Mapping Start High Byte	31H	71H	R/W
System Memory Address 4 Mapping Stop Low Byte	32H	72H	R/W
System Memory Address 4 Mapping Stop High Byte	33H	73H	R/W
Card Memory Offset Address 4 Low Byte	34H	74H	R/W
Card Memory Offset Address 4 High Byte	35H	75H	R/W

Unique Registers

Name	Socket A Index	Socket B Index	Access
Control	38H	78H	R/W
Activity Timer	39H	79H	R/W
Miscellaneous	3AH	7AH	R/W
Programmable Chip Select Configuration	3EH	7EH	R/W
GPIO Configuration	3BH	7BH	R/W
Programmable Chip Select	3DH	7DH	R/W
ATA	3FH	7FH	R/W

NOTES

General Setup Registers

RESETDRV clears all read/write registers, unless the RESETDRV is a result of a Resume (PWRGOOD = 1) and the disable resume RESETDRV bit is set to one in the Power and RESETDRV Control Register.

Identification and Revision Register

Name: Identification and Revision Register
Type: Read Only
Address: Socket A Index (Base + 00H)
Socket B Index (Base + 40H)

Bit	Function
D[7:6]	PCSC Interface Type. Type of PC Card supported by the socket. These bits do not identify the type of card that is present at the socket. 00: I/O only. 01: Memory Only. 10: Memory & I/O. 11: Reserved.
D[5:4]	Reserved.
D[3:0]	The function of these bits changes under control of the UNLOCK and VADEMREV bits in the DMA register, according to the table:

UNLOCK	VADEMREV	D3	Revision
0	X	RO	0011 (Intel)
1	0	RW	X011 (D3 is R/W to identify Vadem chip)
1	1	RO	1011 (Vadem)

Interface Status Register

Name: Interface Status Register
Type: Read Only
Address: Socket A Index (Base + 01H)
Socket B Index (Base + 41H)

Bit	Function
D7	GPI. The logic value of this bit is the complement of the *GPI pin. When the VG-468 is configured in the alternate pin definition mode, the logic value of this bit is the complement of the *GPI pin. When in the standard pin configuration mode, and GPSEL [2:0] = 000, the logic value of this bit is the complement of the GPIO pin. Otherwise, it reads 1.
D6	PC Card Power Active. 0: Power to the socket is off (Vcc, Vpp1 and Vpp2 are all no connects) 1: Power to the socket is on (Vpp1 and Vpp2 are set according to D[3:0] in the Power Control Register).
D5	Ready / *Busy. 0: PC Card is busy. 1: PC Card is ready.
D4	Memory Write Protect. Bit value is the logic level of the WP signal on the memory PC Card interface. 0: PC Card is not write protected. 1: PC Card is write protected.
D[3:2]	Card Detect. Complement of the values of *CD[2:1] on the PC Card interface. Bit is set to 1 if the corresponding *CD is active, set to 0 if inactive.
D[1:0]	Battery Voltage Detect. Following are the values of BVD[2:1] signals for memory PC Cards. 00: battery dead. 01: battery warning. 10: battery dead. 11: battery good. For I/O PC Cards, bit 0 indicates the current status of the *STSCHG / *RI signal from the PC Card.
Note: This register provides the current status of the PC Card socket interface signals.	

Power and RESETDRV Control Register

Name: Power and RESETDRV Control Register
Type: Read/Write
Address: Socket A Index (Base + 02H)
Socket B Index (Base + 42H)

Bit	Function
D7	Output Enable. If this bit is set to zero CA[25:12], *CE[2:1], *IORD, *IOWR, *OE, *REG, RESET and *WE are tri-stated.
	Note: This bit should not be set until after this register has been written to set PC Card Power Enable.
D6	Disable Resume RESETDRV. If this bit is set to one and the RESETDRV is a result of a resume (PWRGOOD = 1), the resettable registers of the PCSC will remain intact and will not be reset. If this bit is set to zero and the RESETDRV is the result of a resume, the resettable registers will be reset. If the RESETDRV is the result of a system reset (PWRGOOD = 0), the resetable registers will be reset regardless of the setting of the bit.
D5	Auto Power Switch Enable. 0: automatic socket power switching based on card detects is disabled. 1: automatic socket power switching based on card detects is enabled.
D4	PC Card Power Enable. 0: power to the socket is disabled (Vcc, Vpp1, and Vpp2 are all no connects). 1: power is provided to the socket (Vcc = 5V and Vpp1 and Vpp2 are set according to bits [3:0] in this register).

Power and RESETDRV Control Register (continued)

Name: Power and RESETDRV Control Register (continued)
Type: Read/Write
Address: Socket A Index (Base + 02H)
Socket B Index (Base + 42H)

Bit	Function
D[3:2]	PC Card Vpp2 Power Control. VG-468 generates two power control outputs for Vpp2 (VPP2EN[1:0]). VPP2EN1 is always available, VPP2EN0 is available only if *RIO/LED resistor is strapped low. In either case, VPP2ENx will be 0 if PC Card Power Enable bit is 0.

D[3:2]	VPP2EN0 not available	VPP2EN0 available	VPP2EN[1:0]
00:	Vpp2 gets Vcc	Vpp2 gets no connect	00
01:	Vpp2 gets Vcc	Vpp2 gets Vcc	01
10:	Vpp2 gets Vpp	Vpp2 gets Vpp	10
11:	Reserved (Vcc)	Reserved (no connect)	00

Bit	Function
D[1:0]	PC Card Vpp1 Power Control. VG-468 generates two power control outputs for Vpp2 (VPP2EN[1:0]). VPP1EN1 is always available, VPP1EN0 is available only if *RIO/LED resistor is strapped low. In either case, VPP1ENx will be 0 if PC Card Power Enable bit is 0.

D[1:0]	VPP1EN0 not available	VPP1EN0 available	VPP1EN[1:0]
00:	Vpp2 gets Vcc	Vpp2 gets no connect	00
01:	Vpp2 gets Vcc	Vpp2 gets Vcc	01
10:	Vpp2 gets Vpp	Vpp2 gets Vpp	10
11:	Reserved (Vcc)	Reserved (no connect)	00

Card Status Change Register

Name: Card Status Change Register
Type: Read/Write
Address: Socket A Index (Base + 04H)
Socket B Index (Base + 44H)

Bit	Function
D7	Activity Timeout. Bit is set to one when activity timer times out (if compatibility bit in the Control register is set).
D[6:5]	Reserved, always 0.
D4	GPI Change. This bit will contain the status of the GPI card status change interrupt. This bit will be set to 0 as long as the GPI Enable bit in the Card Detect and General Control Register is set to 0. When the GPI Enable bit is set to 1 and the GPI input has transition (the edge that generates an interrupt will depend on the setting of the GPI Transition control bit in the Card Detect and General Control Register), then this bit will be set to 1 indicating that a card status change interrupt has occurred. Acknowledgement of this card status change interrupt will be done in the same way that the other sources of the card status change interrupt are acknowledged.
D3	Card Detect Change. This bit will stay at 0 as long as the Card Detect Enable bit is set to 0. When the Card Detect Enable bit is set to 1, this bit will be set to one when a debounced change has been detected on *CD[2:1].
D2	Ready Change. This bit will stay at 0 as long as the Ready Enable bit is set to 0. When the Ready Enable bit is set to 1, this bit will be set to one when a low to high has been detected on the Ready/*Busy signal indicating that the memory PC Card is ready to accept a new data transfer. Bit reads zero for I/O PC Cards.
D1	Battery Warning. This bit will stay at 0 as long as the Battery Warning Enable bit is set to 0. When the Battery Warning Enable bit is set to 1, this bit will be set to one when a battery warning condition has been detected. Bit reads zero for I/O PC Cards.

Card Status Change Register (continued)

Name: Card Status Change Register (continued)
Type: Read/Write
Address: Socket A Index (Base + 04H)
Socket B Index (Base + 44H)

Bit	Function
D0	Battery Dead/*STSCHG. For memory PC Cards, bit is set to one when a battery dead condition has been detected. This bit reads zero if Battery Dead Enable bit is set to 0. For I/O PC Cards, bit is set to one if ring indicate enable bit in the interrupt and general control register is set to zero and the *STSCHG/*RI signal from the I/O PC Card has been pulled low. The system software then has to read the status change register in the PC Card to determine the cause of *STSCHG. This bit reads zero if the ring indicate enable bit in the interrupt and general control register is set to one.

Notes:

1. This register contains the status for sources of the card status change interrupt. These sources can be enabled to generate a card status change interrupt by setting the corresponding Enable bit in the Card Status Change Interrupt Configuration Register or the Card Detect and General Control Register (except for the activity timer and GPI which are enabled by other registers). The bits in this register will be read as 0 if the corresponding Enable bits are set to 0.
2. If the Explicit Write Back bit is set in the Global Control Register, the acknowledgment of sources for the card status change interrupt will be done by writing back 1 to the appropriate bit in the Card Status Change Register that was read as a 1. Once acknowledged, that particular bit in the Card Status Change Register will be read back as 0. The interrupt signal caused by card status change, if enabled on a system IRQ line, will be active until all of the bits in this register are zero.
3. If the Explicit Write Back bit is not set, the card status change interrupt when enabled on a system IRQ line, will remain active until this register is read. Reading this register causes the register bits that were read as set to be reset to zero.

Address Window Enable Register

Name: Address Window Enable Register
Type: Read/Write
Address: Socket A Index (Base + 06H)
Socket B Index (Base + 46H)

Bit	Function
D[7:6]	I/O Window Enable [1:0]. 0: Inhibit the card enable signals to the PC Card when an I/O access occurs within the corresponding I/O address window. 1: Generate the card enable signals to the PC Card when an I/O access occurs within the corresponding I/O address window. I/O accesses pass addresses from the system bus directly through to the PC Card. The start and stop register pairs must all be set to the desired window values before setting this bit to one.
D5	MEMCS16 Decode A[23:12]. 0: *MEMCS16 is generated from a decode of the ISA address A[23:17] only. This means that at a minimum, a 128K block of memory address space is set aside as 16-bit memory. 1: *MEMCS16 is generated from decode of the address lines A[23:12].
D[4:0]	Memory Window Enable [4:0]. 0: Inhibit the card enable signals to the PC Card when a memory access occurs within the corresponding system memory address window. 1: Generate the card enable signals when a memory access occurs within the corresponding system memory address window. When the system address is within the window, the computed address will be generated to the PC Card. The start, stop, and offset registers pairs must all be set to the desired window values before setting bit to one.
Note: This register controls the enabling of the memory and I/O mapping windows to the PC Card memory or I/O space.	

Card Detect and General Control Register

Name: Card Detect and General Control Register
Type: Read/Write
Address: Socket A Index (Base + 16H)
Socket B Index (Base + 56H)

Bit	Function
D[7:6]	These bits reserved.
D5	Software Card Detect Interrupt. If the Card Detect Enable bit is set to 1 in the Card Status Change Inerrupt Configuration Register, then writing a 1 to this bit will cause a card detect card status change interrupt for the associated slot. The functionality and acknowledgement of this software interrupt will work the same way as the hardware generated interrupt. This bit will always read back as a 0. The functionality of the hardware card detect card status change interrupt will not be affected. If a card status change occurs on the *CD1 and *CD2 inputs, a H/W card detect card status change interrupt will be generated. If the Card Detect Enable bit is set to 0 in the Card Status Change Interrupt Configuration Register, then writing a 1 to the S/W Card Detect Interrupt bit has no effect.
D4	Card Detect Resume Enable. The default state of this bit is 0. If this bit is set to 1, then once a card detect change has been detected on the *CD1 and *CD2 inputs, the *RIO output will go from high to low and the Card Detect Change bit in the Card Status Change Register will be set to 1. The *RIO output will remain low until either a read or a write of 1 to the Card Detect Change bit in the Card Status Change register, (acknowledge cycle) which will cause the Card Detect Change bit to be cleared and the *RIO output to go from low to high. The Card Detect Enable bit must be set in the Card Status Change Interrupt Configuration Register in order to generate the *RIO. If the card status change is routed to either the *INTR signal or any of the IRQ signals, the setting of Card Detect Resume Enable bit to one will prevent *INTR and IRQ signal from going active as a result of H/W card detect status change. Once the resume software has detected a card detect change interrupt from *RIO (by reading the Card Status Change Register), the software should initiate a software card detect change so the card detect change condition will generate active interrupt on the IRQ or *INTR signals (depending on the active configuration).

Card Detect and General Control Register (continued)

Name: Card Detect and General Control Register (continued)
Type: Read/Write
Address: Socket A Index (Base + 16H)
Socket B Index (Base + 56H)

Bit	Function
D4 (cont.)	If this bit is set to zero, then the card detect resume functionality is disabled. This means that the *RIO output will not go low due to a card detect change. The *RIO output will be the logical AND of all the active low sources for ring indicate output including the *RI inputs from slot A and slot B and the card detect changes on *CD1, *CD2 from both slots.
D3	GPI Transition Control. The default state of this bit is 0. Setting the General Purpose Input (GPI) Enable bit to 1 enables a card status change interrupt once the *GPI input goes high to low if the GPI Transition Control bit is set to 0. If the GPI Enable bit is set to one and the GPI Transition Control bit is set to 1, then once the *GPI input has gone from low to high, a card status change interrupt will be generated.
D2	GPI Enable. The default state of this bit is 0. Setting it to 0 disables the generation of a card status change interrupt based on the *GPI input transitioning. Setting it to 1 enables a card status change interrupt based on the *GPI input transition. The GPI Transition Control bit sets the triggering edge of *GPI. The GPI card status change interrupt functions independent of the setting of the PC Card Type bit in the Interrupt and General Control Register.
D1	Configuration Reset Enable. The default state of this bit is 0. If it is set to 0, the configuration register reset function based on card detects is disabled. When it is set to 1, when both the *CD1 and *CD2 inputs for a particular slot go high, a reset pulse will be generated to reset the configuration registers for that particular slot to their default state (zero's). The registers involved are all I/O registers, all Memory registers, Interrupt and General Control register (exept INTR ENABLE bit) and Address Window Enable Register (except MEMCS16 Decode A[23:12]).

Card Detect and General Control Register (continued)

Name: Card Detect and General Control Register (continued)
Type: Read/Write
Address: Socket A Index (Base + 16H)
Socket B Index (Base + 56H)

Bit	Function
D0	16-Bit Memory Delay Inhibit. The default state of this bit is 0. If it is set to 0 and a system memory window is set up to be 16-bit by setting the Data Size bit in the System Memory Address Mapping Start High Byte Register to 1, the falling edge of the control strobes *WE and *OE for the corresponding slot will be delayed synchronously by CLK. The falling edge of the control strobes will be generated from the first falling edge of CLK after the falling edge of *MEMW or *MEMR gated by a valid system memory window decode. The rising edge of the control strobes will be generated from the rising edge of *MEMW or *MEMR. If it is set to 1, the control strobe falling edge will not be synchronously delayed.

Global Control Register

Name: Global Control Register
Type: Read/Write
Address: Socket A Index (Base + 1EH)
Socket B Index (Base + 5EH)

Bit	Function
D[7:4]	These bits reserved.
D3	IRQ14 Pulse Mode Enable. When this bit is set to 1 and bit 1 (level mode interrupt enable) is 0, and PC Card Type bit is set to 1 (I/O card), and the Card *IREQ is steered to IRQ14, IRQ14 will operate in level mode and all other IRQ's will operate in edge-triggered mode. This is intended to support a PC card which generates a PCMCIA pulse mode *IREQ, while other IRQ's operate in ISA/EISA edge-triggered mode.
D2	Explicit Write Back Card Status Change Acknowledge. Setting this bit to a one will require an explicit write of a one to the Card Status Change Register bit which indicates an interrupting condition. When this bit is set to zero (default state), the card status change interrupt is acknowledged by reading the Card Status Change Register, and the register bits are cleared upon a read.
D1	Level Mode Interrupt Enable. Level mode refers to EISA level mode operation, not necessarily PCMCIA level mode. If this bit is low (default), all IRQ outputs operate as ISA rising edge-triggered interrupts. All IRQ's will normally be tristated. An IRQ will go low when an interrupt is steered to it, and will go high when the interrupt becomes active. In the case of the card *IREQ, the IRQ will go low when *IREQ goes inactive (high). If caused by a card status change, IRQ will go low when the status is cleared. If this bit is high, all IRQ outputs operate as EISA active low level-triggered interrupts. An IRQ will go from tristate to low when the interrupt steered to it becomes active. Level mode can also be used to enable interrupt sharing in an ISA system (which uses edge-triggered interrupts) when all interrupt sources on the shared level operate in pulse mode. If the shared IRQ is used for status change interrupts, the Vadem proprietary STATIRQSHARE bit must also be set. If the shared IRQ is used for PCMCIA card *IREQ interrupt, the cards must operate in PCMCIA pulse mode. The IRQ pulse will go low for the duration of the *IREQ pulse or for the same duration as *INTR would, and the host will respond to the rising edge of the IRQ.

Global Control Register (continued)

Name: Global Control Register (continued)
Type: Read/Write
Address: Socket A Index (Base + 1EH)
Socket B Index (Base + 5EH)

Bit	Function
D0	Power Down. When it is set to 1, and all I/O memory windows are disabled, and *CS signal is driven to inactive high, the VG-468 enters the *CS controlled powered-down. During *CS controlled power-down, all internal registers are inaccessible, outputs remain inactive, and the chip is at minimum power consumption level. IRQ's and *RIO will still be active to monitor the card status change and *RI status for resume indication. If a status change occurs during power down mode an d INTR is enabled, the *INTR will occur upon exit from power down mode.

Note: 1. This register is not duplicated per slot. Thus, this register can be accessed from either the slot A or slot B index.

2. If the *CS pin is not available and the GPIO pin is not programmed to be either *CS or Power Down Control, then Power Down mode can still be entered if the other Power Down conditions are satisfied, but internal registers will remain writeable.

Interrupt Registers

Interrupt and General Control Register

Name: Interrupt and General Control Register
Type: Read/Write
Address: Socket A Index (Base + 03H)
Socket B Index (Base + 43H)

Bit	Function
D7	Ring Indicate Enable. 0: For I/O PC Cards, (PC Card type bit is set to one), the *STSCHG/*RI signal from the I/O PC Card is used as the status change signal *STSCHG. The current status of the signal is then available to be read from the Interface Status Register and this signal can be configured as a source for the card status change interrupt. 1: For I/O PC Cards (PC Card type bit is set to one), the *STSCHG / *RI signal from the I/O PC Card is used as a ring indicator signal and is passed through to the *RIO/LED pin. For memory PC Cards, bit has no function.
D6	PC Card Reset. This is a software reset to the PC Card. 0: Activates the RESET signal to the PC Card. The RESET signal will be active until bit is set to one. 1: Deactivates the RESET signal to the PC Card.
D5	PC Card Type. 0: Memory PC Card. 1: I/O PC Card.
D4	INTR Enable. 0: The *INTR signal does not indicate a card status change interrupt and the card status change interrupt is steered to one of the IRQ lines according to bits [7:4] in the Card Status Change Interrupt Configuration Register. 1: Enables the card status change interrupt on the *INTR signal, except in *CS power down mode.

Interrupt and General Control Register (continued)

Name: Interrupt and General Control Register (continued)
Type: Read/Write
Address: Socket A Index (Base + 03H)
Socket B Index (Base + 43H)

Bit	Function
D[3:0]	IRQ Level Selection (I/O Cards only). These bits select the redirection of the PC Card interrupt:

0000:	IRQ not selected.	1000:	Reserved.
0001:	Reserved.	1001:	IRQ9 Enabled.
0010:	Reserved.	1010:	IRQ10 Enabled.
0011:	IRQ3 Enabled.	1011:	IRQ11 Enabled.
0100:	IRQ4 Enabled.	1100:	IRQ12 Enabled.
0101:	IRQ5 Enabled.	1101:	Reserved.
0110:	Reserved.	1110:	IRQ14 Enabled.
0111:	IRQ7 Enabled.	1111:	IRQ15 Enabled.

Notes: 1. This register controls the interrupt steering for the I/O PC Card interrupt as well as general control.

2. RESETDRV clears all bits in this register, unless the RESETDRV is a result of a Resume (PWRGOOD = 1) and the disable resume RESETDRV bit is set to one in the Power and RESETDRV Control Register.

Card Status Change Interrupt Configuration Register

Name: Card Status Change Interrupt Configuration Register
Type: Read/Write
Address: Socket A Index (Base + 05H)
Socket B Index (Base + 45H)

Bit	Function
D[7:4]	Interrupt Steering for the Card Status Change Interrupt. These bits select the redirection of the card status change interrupt if the interrupt is not selected to the output on the *INTR pin. With INTR Enable bit inactive: 0000: IRQ not selected. 1000: Reserved. 0001: Reserved. 1001: IRQ9 Enabled. 0010: Reserved. 1010: IRQ10 Enabled. 0011: IRQ3 Enabled. 1011: IRQ11 Enabled. 0100: IRQ4 Enabled. 1100: IRQ12 Enabled. 0101: IRQ5 Enabled. 1101: Reserved. 0110: Reserved. 1110: IRQ14 Enabled. 0111: IRQ7 Enabled. 1111: IRQ15 Enabled.
D3	Card Detect Enable. 0: Disables the generation of a card status change interrupt when the card detect signals change state. 1: Enables a card status change interrupt when a change has been detected on the *CD1 or *CD2 signals.
D2	Ready Enable (memory PC Cards only). 0: Disables the generation of a card status change interrupt when a low to high transition has been detected on the Ready/*Busy signal. 1: enables a card status change interrupt when a low to high transition has been detected on the Ready/*Busy signal.
D1	Battery Warning Enable (memory PC Cards only). 0: Disables the generation of a card status change interrupt when a battery warning condition has been detected. 1: Enables a card status change interrupt when a battery warning condition has been detected.
D0	Battery Dead Enable / *STSCHG. 0: For memory PC Cards, disables the generation of a card status change interrupt. For I/O PC Cards, bit is ignored when the Ring Indicate Enable bit in the Interrupt and General Control Register is set to one. 1: For memory PC Cards, enables a card status change interrupt when a battery dead condition has been detected. For I/O PC Cards, enables a card status change interrupt if the *STSCHG/*RI signal has been pulled low by the I/O PC Card, assuming that the Ring Indicate Enable bit in the Interrupt and General Control Register is set to zero.

Card Status Change Interrupt Configuration Register (continued)

Name: Card Status Change Interrupt Configuration Register (continued)
Type: Read/Write
Address: Socket A Index (Base + 05H)
Socket B Index (Base + 45H)

Note: 1. This register controls interrupt routing of the card status change interrupt and enables the sources for card status change interrupt.

I/O Registers

I/O Control Register

Name: I/O Control Register
Type: Read/Write
Address: Socket A Index (Base + 07H)
Socket B Index (Base + 47H)

Bit	Function
D7	I/O Window 1 Wait State. 0: 16-bit system accesses occur without additional wait states. 1: 16-bit system accesses occur with 1 additional wait state.
D6	I/O Window 1 Zero Wait State for 8-bit I/O Access. 0: System I/O access will occur with additional wait states. 1: System I/O access will occur with no additional wait states and the *ZWS signal will be returned to the system bus.
D5	I/O Window 1 *IOCS16 Source. 0: *IOCS16 is generated based on the value of the data size bit. 1: *IOCS16 is generated based on the *IOIS16 signal from the PC Card.
D4	I/O Window 1 Data Size. 0: 8-bit I/O data path. 1: 16-bit I/O data path.
D3	I/O Window 0 Wait State. 0: 16-bit system accesses occur without additional wait states. 1: 16-bit system accesses occur with 1 additional wait state.
D2	I/O Window 0 Zero Wait State. 0: System I/O access will occur with additional wait states. 1: System I/O access will occur with no additional wait states and the *ZWS signal will be returned to the system bus.
D1	I/O Window 0 *IOCS16 Source. 0: *IOCS16 is generated based on the value of the data size bit. 1: *IOCS16 is generated based on the *IOIS16 signal from the PC Card.
D0	I/O Window 0 Data Size. 0: 8-bit I/O data path. 1: 16-bit I/O data path.

I/O Control Register (Continued)

Name: I/O Control Register (continued)
Type: Read/Write
Address: Socket A Index (Base + 07H)
Socket B Index (Base + 47H)

Notes:
1. This register indicates the configuration for both I/O mapping windows. This register is set based on information read from the PC Card's card information structure. Dynamic bus sizing on a cycle by cycle basis is implemented to the PC Card interface if the source of the *IOCS16 signal is the PC Card as determined by the window's *IOCS16 source bit. In order to be compatible with some software and hardware implementations such as an IDE interface, the PC Card must decode two consecutive I/O addresses to determine the cycle data width. In order to meet the system bus timing, this type of PC Card must decode the address lines A[9:0] prior to the card enable signal becoming active at the interface. The card decodes the address and responds to a 16-bit cycle by enabling *IOIS16. The PCSC qualifies *IOIS16 with the card enable signals to generate *IOCS16 to the system bus.
2. These bits set the data path size and select zero wait states for the appropriate bus access, and are used to determine system bus signal *IOCS16.
3. *IOWR is delayed so that data will be valid at the falling edge of *IOWR, as required by the PCMCIA specification. This does not lengthen normal 8 bit cycles but adds one wait state to 16 bit write cycles. Setting bit D2 or D6 will inhibit this delay in the corresponding window.

I/O Address Start Register Low Byte

Name: I/O Address Start Register Low Byte
Type: Read/Write
Address: Socket A Index (Base + 08H, 0CH) for windows 0-1
Socket B Index (Base + 48H, 4CH) for windows 0-1

Bit	Function
D[7:0]	I/O Window Start Address A[7:0]. Low order address bits used to determine the start address of the corresponding I/O address window. This provides a minimum 1 byte window for the I/O address window.

I/O Address Start Register High Byte

Name: I/O Address Start Register High Byte
Type: Read/Write
Address: Socket A Index (Base + 09H, 0DH) for windows 0-1
Socket B Index (Base + 49H, 4DH) for windows 0-1

Bit	Function
D[7:0]	I/O Window Start Address A[15:8]. High order address bits used to determine the start address of the corresponding I/O address Window .

I/O Address Stop Register Low Byte

Name: I/O Address Stop Register Low Byte
Type: Read/Write
Address: Socket A Index (Base + 0AH, 0EH) for windows 0-1
Socket B Index (Base + 4AH, 4EH) for windows 0-1

Bit	Function
D[7:0]	I/O Window Stop Address A[7:0]. Low order address bits used to determine the stop address of the corresponding I/O address window. This provides a minimum 1 byte window for the I/O address window.

I/O Address Stop Register High Byte

Name: I/O Address Stop Register High Byte
Type: Read/Write
Address: Socket A Index (Base + 0BH, 0FH) for windows 0-1
Socket B Index (Base + 4BH, 4FH) for windows 0-1

Bit	Function
D[7:0]	I/O Window Stop Address A[15:8]. High order address bits used to determine the stop address of the corresponding I/O address window.

Memory Registers

System Memory Address Mapping Start Register Low Byte

Name: System Memory Address Mapping Start Register Low Byte
Type: Read/Write
Address: Socket A Index (Base + 10H, 18H, 20H, 28H, 30H) for windows 0-4
Socket B Index (Base + 50H, 58H, 60H, 68H, 70H) for windows 0-4

Bit	Function
D[7:0]	System Memory Window Start Address A[19:12]. Low order address bits used to determine the start address of the corresponding system memory address mapping window. This provides a minimum memory mapping window of 4K bytes.

Note: A memory window cannot be set up below the first 64K of address space.

System Memory Address Mapping Start Register High Byte

Name: System Memory Address Mapping Start Register High Byte
Type: Read/Write
Address: Socket A Index (Base + 11H, 19H, 21H, 29H, 31H) for windows 0-4
Socket B Index (Base + 51H, 59H, 61H, 69H, 71H) for windows 0-4

Bit	Function
D7	Data Size. 0: 8-bit memory data path. 1: 16-bit memory data path.
D6	Zero Wait State. 0: System memory access will complete in 3 CLKs (16-bit) or 6 CLKs (8-bit) with IOCHRDY high. 1: System memory access completes in 2 CLKs (16-bit) or 3 CLKs (8-bit) with *ZWS signal driven low. The *WAIT signal will override this bit. If the Compatibility bit is low, *ZWS will not be asserted for accesses to an 8 bit memory window when both A0 and *SBHE are low. If the Compatibility bit is low, *ZWS will not be qualified with *MEMR or *MEMW during accesses to a 16 bit memory window.
D[5:4]	Scratch bits. These bits can be used for general purpose register storage and retrieval.
D[3:0]	System Memory Window Start Address A[23:20]. High order address bits used to determine the start address of the corresponding system memory address mapping window.

Note: Bits in this register control the data path and additional wait states associated with each system memory window.

System Memory Address Mapping Stop Register Low Byte

Name: System Memory Address Mapping Stop Register Low Byte
Type: Read/Write
Address: Socket A Index (Base + 12H, 1AH, 22H, 2AH, 32H) for windows 0-4
Socket B Index (Base + 52H, 5AH, 62H, 6AH, 72H) for windows 0-4

Bit	Function
D[7:0]	System Memory Window Stop Address A[19:12]. Low order address bits used to determine the stop address of the corresponding system memory address mapping window. This provides a minimum memory mapping window of 4K bytes.

System Memory Address Mapping Stop Register High Byte

Name: System Memory Address Mapping Stop Register High Byte
Type: Read/Write
Address: Socket A Index (Base + 13H, 1BH, 23H, 2BH, 33H) for windows 0-4
Socket B Index (Base + 53H, 5BH, 63H, 6BH, 73H) for windows 0-4

Bit	Function
D[7:6]	Wait States Select for 16-bit Memory Access. These bits determine the number of additional wait states for a 16-bit access to the system memory window. If the PC Card supports the *WAIT signal, wait states will be generated by the PC Card asserting the *WAIT signal. 00: standard 16-bit cycle (3 CLKs per access). 01: 1 additional wait state (4 CLKs per access). 10: 2 additional wait states (5 CLKs per access). 11: 3 additional wait states (6 CLKs per access).
D[5:4]	Reserved
D[3:0]	System Memory Window Stop Address A[23:20]. High order address bits used to determine the stop address of the corresponding system memory address mapping window.

Note: Two bits in this register select the number of wait states for a 16-bit access to the corresponding system memory window.

Card Memory Offset Address Register Low Byte

Name: Card Memory Offset Address Register Low Byte
Type: Read/Write
Address: Socket A Index (Base + 14H, 1CH, 24H, 2CH, 34H) for windows 0-4
Socket B Index (Base + 54H, 5CH, 64H, 6CH, 74H) for windows 0-4

Bit	Function
D[7:0]	Card Memory Offset Address A[19:12]. Low order address bits which are added to the system address bits A[19:12] to generate the memory address for the PC Card.

Card Memory Offset Address Register High Byte

Name: Card Memory Offset Address Register High Byte
Type: Read/Write
Address: Socket A Index (Base + 15H, 1DH, 25H, 2DH, 35H) for windows 0-4
Socket B Index (Base + 55H, 5DH, 65H, 6DH, 75H) for windows 0-4

Bit	Function
D7	Write Protect. 0: write operations to the PC Card through the corresponding system memory window are allowed. 1: write operations to the PC Card through the corresponding system memory window are inhibited.
D6	REG Active. 0: access to the system memory will result in common memory on the PC Card being accessed. 1: access to the system memory will result in attribute memory on the PC Card being accessed.
D[5:0]	Card Memory Offset Address A[25:20]. High order address bits which are added to the system address bits A[23:20] to generate the memory address for the PC Card.
Note:	For each corresponding system memory window, this register controls the software write protect of PC Card memory and whether the window is mapped to attribute or common memory on the PC Card.

Unique Registers

After reset, the Vadem unique registers are locked and cannot be read or written. To unlock, first write base + 0EH to the index register and then write base + 37H to the index register. Any index or data register access between these two writes will abort the unlock sequence.

Control Register

Name: Control Register
Type: Read/Write
Address: Socket A Index (Base + 38H)
Socket B Index (Base + 78H)

Bit	Function
D7	Compatibility. This bit controls several compatibility functions. When set, it allows the activity timer status to be read on bit 7 of the Card Status Change register. See System Memory Address Mapping Start Register High Byte for more information.
D6	POL. VCCEN polarity. 0: *VCCEN pin low to turn card power on. 1: *VCCEN pin high to turn card power on.
D5	INPACKEN: INPACK Enable. 0: VG-468 ignores *INPACK and always drives the SD bus. 1: VG-468 drives the SD bus during card I/O read cycles only when the card asserts *INPACK.
D4	DELAYENABLE. 0: Card detect debounce and power sequencing delays are disabled. 1: Card detect debounce and power sequencing delays are enabled. Output enable will be synchronized to bus cycles so that turn-off will not occur in the middle of a cycle.
D3	TSSI: Tri-states *SPKROUT, *INTR, and *RIO/LED to save power in pullup/pulldown resistors. 0: *SPKROUT, *INTR, and *RIO/LED outputs are enabled. 1: *SPKROUT, *INTR are tri-stated. *RIO/LED is also tri-stated unless Ring Indicate is enabled in either socket, or Card Detect Resume Enable bit is set.
D2	This bit reserved.
D1	ASYNC. Set when CLK is asynchronous to ISA bus read/write strobes. Setting this bit will cause a wait state in certain cycles.

Control Register

Name: Control Register (continued)
Type: Read/Write
Address: Socket A Index (Base + 38H)
Socket B Index (Base + 78H)

Bit	Function
D0	SLOW. 0: Normal PCMCIA memory timing. 1: Enable 600 ns PCMCIA memory cycle timing. This delays the *OE or *WE command strobe to the PC Card and generates automatic wait states, for both 8 and 16 bit CPU and DMA cycles. If wait states have been programmed in the memory map registers, those will be in addition to the automatic wait states, and will be generated for 8 and 16 bit CPU and DMA cycles. One additional wait state should be programmed if CLK is greater than 6 MHz; two if CLK is 8 MHz. Read cycles will have two more automatic wait states than write cycles.

Timer Register

Name: Timer Register
Type: Read/Write (except bits 5 and 6)
Address: Socket A Index (Base + 39H)
Socket B Index (Base + 79H)

Bit	Function
D7	TMRES: Timer resolution. 0: 15 seconds. 1: 1 minute.
D6	TMRSTAT: Activity timer status, a read-only bit. Timed out when set.
D5	SIGEN: This bit is read-only. When set, it indicates to software that the card is powered up, the PCMCIA interface outputs are enabled, and all power-up delays have been satisfied.
D4	ZEROPWR: Zero power. 0: CDATA[15:0] are controlled as described in the Power and RESETDRV Register description. 1: CDATA[15:0] are controlled as described in the Power and RESETDRV Register description, except that when both card detects are high and card Vcc is off, CDATA[15:0] becomes low instead of tristate. This reduces power dissipation in the chip.
D[3:0]	Activity Timer Timeout.

Note: 1. This register controls the activity timer. The activity timer is programmable from 1 to 15 steps of 15 seconds, or 1 minute. The timer is disabled when set to 0. The timer is retriggered by an access to the card, or a card interrupt, or status change interrupt (except for card detect interrupts) when the card is present, powered up and the card interface is enabled. It is also retriggered when this register is written. A status change interrupt will be generated when the timer times out. The timer status is readable on bit D6, and if the Compatibility bit in the Control Register is set, it is also readable with the other interrupt status bits in the Card Status Change register.

2. In order for the timer status to be properly latched into bit D6, following a card status change interrupt, the Card Status Change register must be read first.

Miscellaneous Register

Name: Miscellaneous Register
Type: Read/Write
Address: Socket A Index (Base + 3AH)
Socket B Index (Base + 7AH)

Bit	Function
D7	UNLOCK: reads back as a 1 when Unique indexed registers are unlocked and accessible, undefined when registers are locked. Registers can be locked by writing a 0 to this bit.
D6	VADEMREV: When VADEMREV and UNLOCK are set, Identification and Revision Register reads Vadem PCSC revision. Otherwise, it reads revision of similar Intel part.
D[5:4]	These bits reserved.
D3	DMAWSB. 0: Enables wait states as specified in the System Memory Address Mapping Stop Register High Byte to be generated for DMA cycles. For use with 8 MHz DMA cycles. 1: Wait states specified in the System Memory Address Mapping Stop Register High Byte are not generated for DMA cycles. For use with standard ISA DMA cycles.
D2	GPIO. When GPSEL[2:0] = 0X0 the input on the GPIO pin can be read by reading this bit. When the GPIO or GPO/*PCS pin is programmed as a GP output, its value can be written to and read back from this bit.
D[1:0]	These bits reserved.

GPIO Configuration Register

Name: GPIO Configuration Register
Type: Read/Write
Address: Socket A Index (Base + 3BH)
Socket B Index (Base + 7BH)

Bit	Function
D7	EXTDECODE: Enables external chip select. This bit disables internal address decoding for the VG-468 index and data registers. If EXTDECODE is set and the *CS pin is available (full Vpp control mode), *CS will become the external chip select input, and the GPO/*PCS pin will be programmable by D[6:4]. If EXTDECODE is set and the *CS pin is not available, D[6:4] are ignored, and the GPIO pin becomes the external chip select input.
D[6:4]	GPSEL[2:0]. These 3 bits decode the function of GPIO if external chip select is disabled (EXTDECODE=0). 000: GPIO = *GPI input. 010: GPIO = GP input. 011: GPIO = GP output. 100: GPIO = *PCS output. 110: GPIO = Power Down Control input. The VG-468 will enter Power Down mode when the Power Down bit in the Global Control register is set, and the GPIO pin is high. Only 011 and 100 are valid to control GPO/*PCS pin (alternate pin definition mode). When EXTDECODE = 1, GPIO = *CS input.
D[3:0]	These bits reserved.

Note: This register controls the GPIO pin. All bits in this register are 0 after reset. Since GPIO defaults to an input, a 1 Megohm pullup resistor is required if this pin will be used as *PCS. If *GPI is not assigned to a GPIO pin, bit 7 of the Interface Status Register will always read 1.

Programmable Chip Select Register

Name: Programmable Chip Select Register
Type: Read/Write
Address: Socket A Index (Base + 3DH)
Socket B Index (Base + 7DH)

Bit	Function
D[7:0]	A[9:2] for I/O; A[23:16] for memory.

Note: This register selects the base address for the programmable chip select output. In an I/O cycle, AEN must be low, and address bits A[9:2] are compared to the value in this register. In a memory cycle, address bits A[23:16] are compared. Boundary alignment must correspond to the block size specified in the Programmable Chip Select Configuration Register.

Programmable Chip Select Configuration Register

Name: Programmable Chip Select Configuration Register
Type: Read/Write
Address: Socket A Index (Base + 3EH)
Socket B Index (Base + 7EH)

Bit	Function
D[7]	Reserved.
D[6:5]	PCSSIZE[1:0]: select the size of the decoded block. 00: 64 Kbyte (Memory), 4 byte (I/O). 01: 128 Kbyte (Memory), 8 byte (I/O). 10: 256 Kbyte (Memory), 16 byte (I/O). 11: 512 Kbyte (Memory), 32 byte (I/O).
D4	PCSIO 0: Memory mode. 1: I/O mode.
D3	STATIRQSHARE. Enables sharing of status interrupts in an ISA system if status interrupt is steered to an IRQ pin, and bit 1 in the Global Control Register is also set. When a status change occurs, the IRQ will pulse low for at least 4 clock periods. 0: Status IRQ is active high level. 1: Status IRQ is active low, open drain pulse.
D[2:0]	Reserved.

ATA Register

Name: ATA Register
Type: Read/Write
Address: Socket A Index (Base + 3FH)
Socket B Index (Base + 7FH)

Bit	Function
D[7:3]	General Purpose Outputs for ATA drive. When ATA bit is true, these bits drive CA[25:21].
D2	TSBIT7. 0: host bus bit SD7 functions normally. 1: When the host reads the ATA Drive Address register at port 3F7h or 377h, bit SD7 of the host bus will remain tristated to avoid contention with a floppy disk interface on the host bus.
D1	BVD2LED: defines the definition of BVD2 in I/O mode. 0: *SPKR input. 1: LED input to be used with ATA drive.
D0	ATA. 0: normal operation for CA[25:21]. 1: CA[25:21] become GP outputs controlled by D[7:3].

DC Characteristics

Symbol	Parameter	V_{cc} Max.	0°C to + 70°C	Units
V_{IH} (TTL)	Minimum High Level Input Voltage	5.5	2.0	V
V_{IL} (TTL)	Minimum Low Level Input Voltage	5.5	0.8	V
V_{OH}	Minimum High Level Output Voltage 4mA Buffer, I_{OH} = -4mA 8mA Buffer, I_{OH} = -8mA 12mA Buffer, I_{OH} = -12mA	5.5	2.4	V
V_{OL}	Maximum High Level Output Voltage 4mA Buffer, I_{OL} = 4mA 8mA Buffer, I_{OL} = 8mA 12mA Buffer, I_{OL} = 12mA	5.5	0.4	V
I_{IL}	Maximum Input Leakage Current	5.5	±10	µA
I_{OL}	Maximum Output Leakage Current	5.5	±10	µA

Capacitance

Symbol	Parameter	0°C to + 70°C	Units
C_{IN}	Maximum Input Capacitance	10	pF
C_{OUT}	Maximum Output Capacitance	10	pF
C_{IO}	Maximum I/O Capacitance	10	pF

Absolute Maximum Ratings*

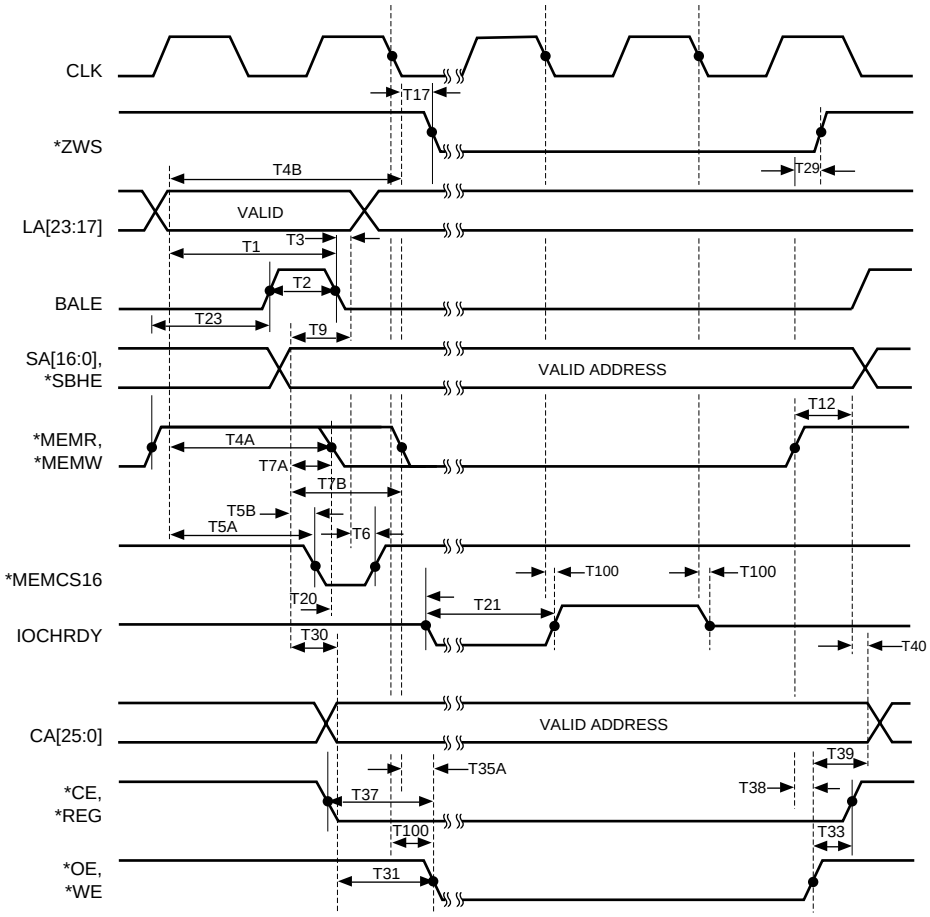
Symbol	Parameter	Value	Units
V_{CC}	DC Power Supply Voltage	-0.5 to + 7.0	V
V_{IN},V_{OUT}	DC Input, Output Voltage	-0.5 to V_{DD} + 0.5	V
I	DC Current Drain V_{DD} and V_{SS} Pins	100	mA
T_{STG}	Storage Temperature	-55 to + 150	°C
T_L	Lead Temperature	250	°C
T_{OPER}	Operating Temperature	0 to + 70	°C

***Note:** Stress beyond ranges listed in this table may cause physical damage to a device and should be avoided. This table does not imply that operations at conditions above those listed in AC Timings is possible. This is a stress rating and operation of a device at or above this rating for an extended period of time may cause failure or affect reliability.

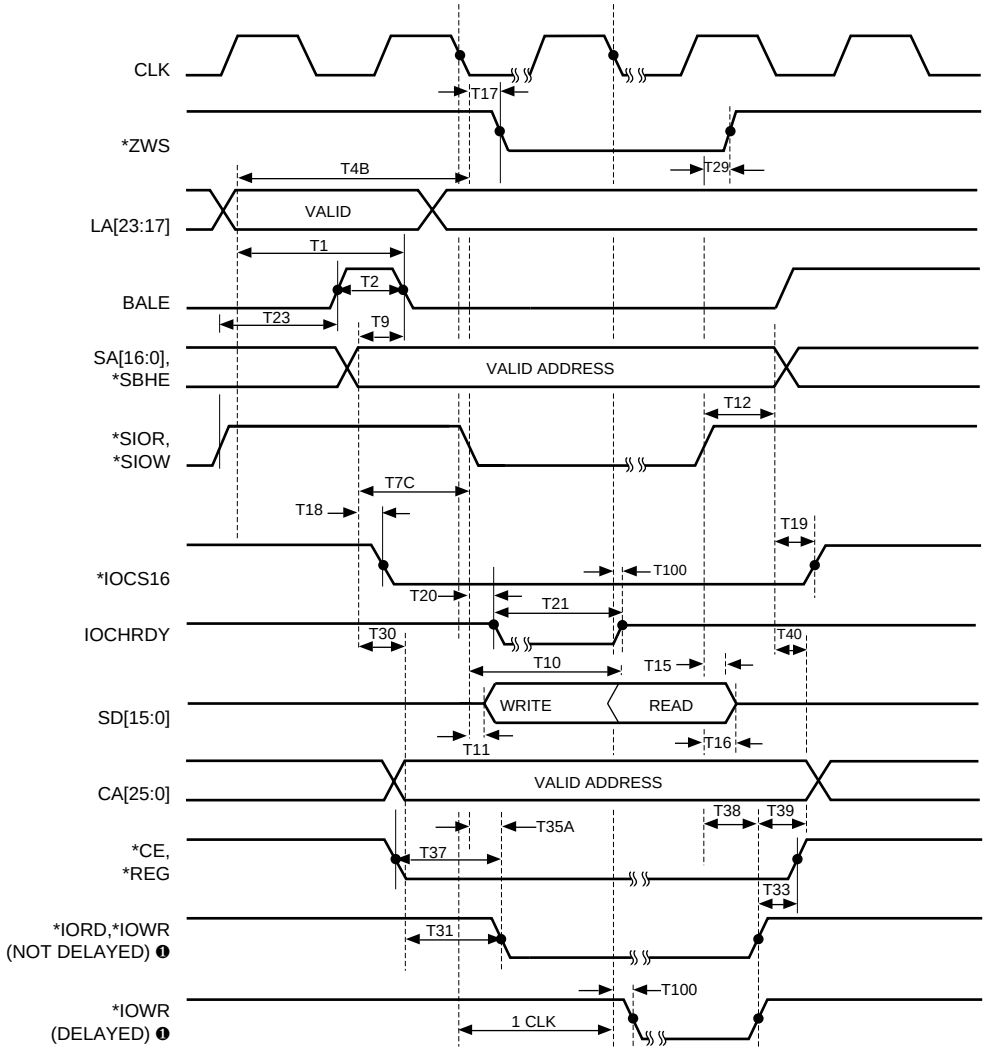
ICC Specifications

Symbol	Parameter	Typ	Max	Units
I_{CC}	Supply Current	12	-	mA
I_{CC1}	Supply Current / Suspend Mode Outputs Tri-stated / No Clock / Inputs Not Toggling	10	-	µA

Memory: Standard/ Extended/Zero Wait State

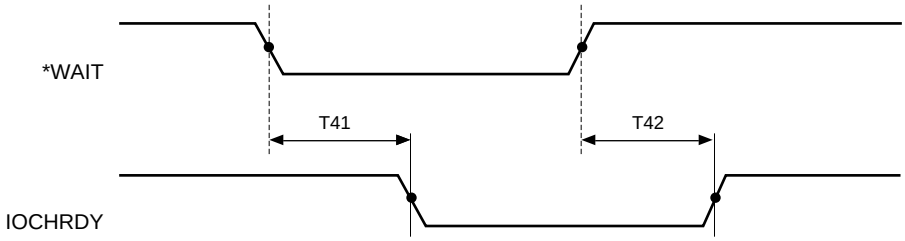


I/O: Standard/ Extended/Zero Wait State

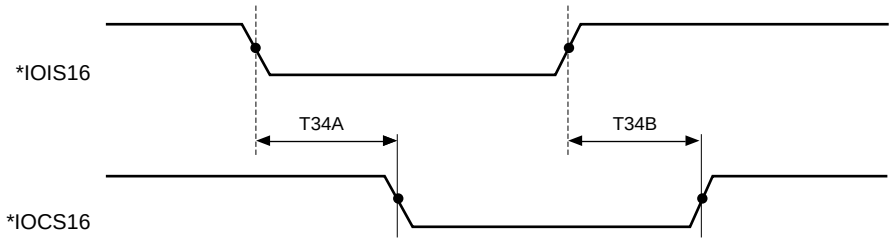


❶ SEE I/O CONTROL REGISTER DESCRIPTION

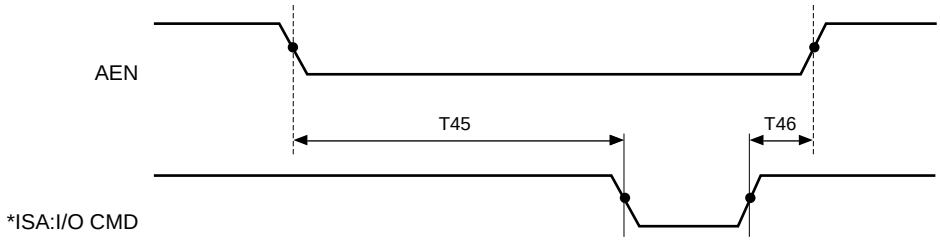
WAIT



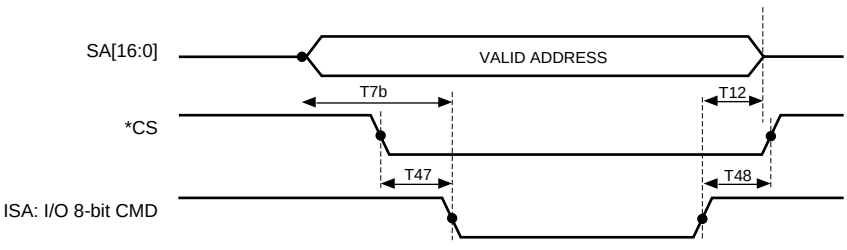
IOIS16



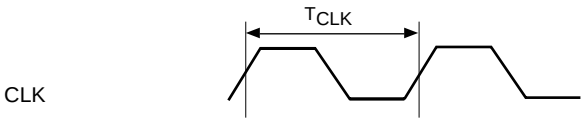
AEN Setup and Hold



External Chip Select to Access PCSC Registers

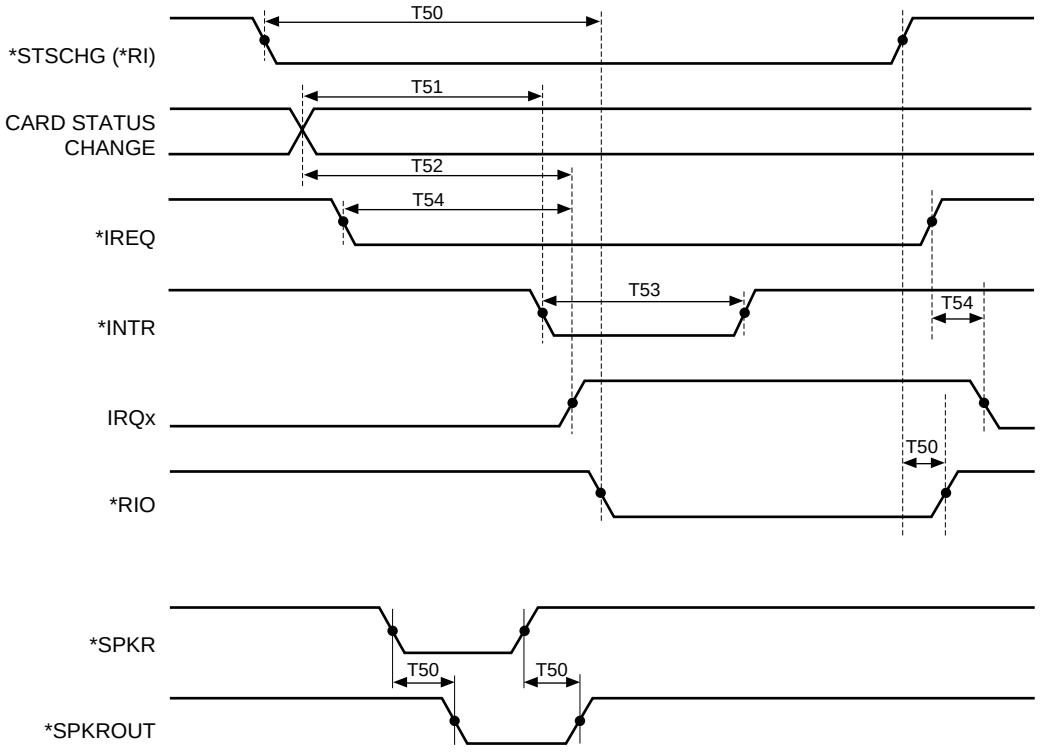


CLK

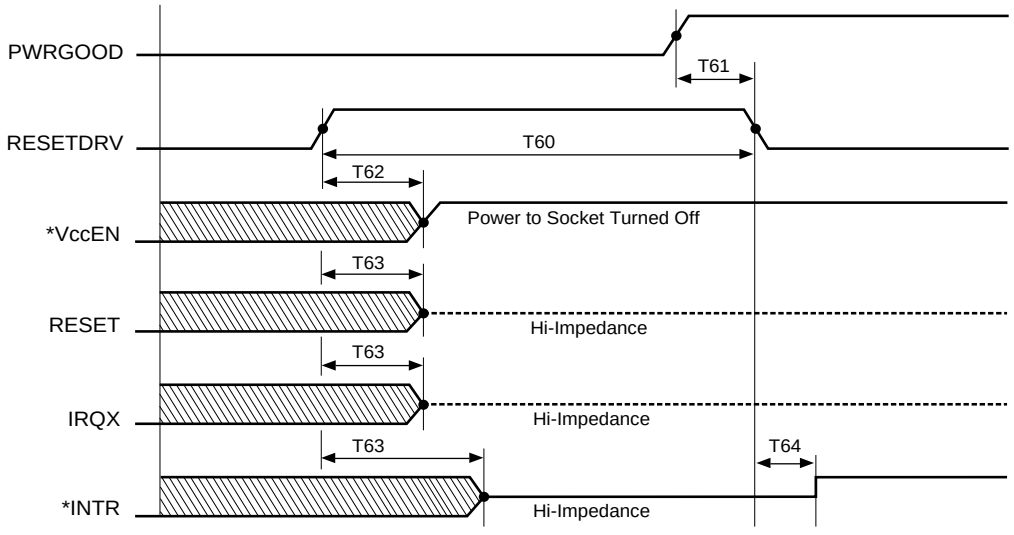


Parameter	Description	Min	Max	Max
T_{CLK}	CLK Period	120	210	ns

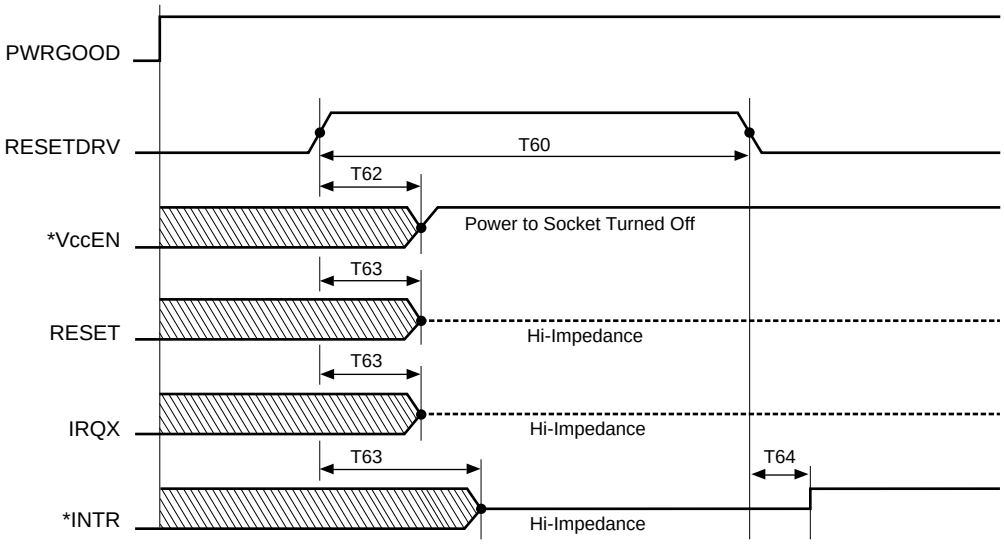
Interrupt, Ring Indicate, Speaker Timings



Reset from PWRGOOD



Reset, with Disable Resume RESETDRV Bit = 0



AC Characteristics

T = 0°C to + 70°C, CLK = 8.33 MHz, V_{CC} = 4.5V to 5.5V, T in ns

Symbol	Parameter	Min	Max
T1	A[23:17] Setup to BALE	93	-
T2	BALE pulse width	48	-
T3	A[23:17] Hold from BALE	15	-
T4A	A[23:17] Setup to 16-Bit Memory Command	102	-
T4B	A[23:17] Setup to 8-Bit Memory Command	162	-
T5A	*MEMCS16 Valid from A[23:17]	-	58
T5B	*MEMCS16 Valid from A[16:00]	-	24(1) 26(2)
T6	*MEMCS16 Hold from A[23:17]	0	-
T7A	A[16:12] and *SBHE to 16-Bit Memory Command	23	-
T7B	A[16:12] and *SBHE to 8-Bit Memory Command	89	-
T7C	A[15:00] and *SBHE Setup to I/O Command	89	-
T9	A[16:00] and *SBHE Setup to BALE Falling	26	-
T10	PCSC Register Read Data D[7:0] Access	-	60
T11	Data Valid from *SIOW active		40
T12	A[16:00] and *SBHE Hold from Command	25	-
T15A	PCSC Register Read Data D[7:0] Hold	0	-
T15B	PCSC Register Write Data D[7:0] Hold	25	-
T16	PCSC Register Access Command Off to D[7:0] Tri-State	-	30
T17	*ZWS Valid from 8 bit command	-	67
T18	*IOCS16 Valid from A[15:00]	-	69
T19	*IOCS16 Hold from A[15:00]	0	-
T20	*IOCHRDY Low from 16-Bit Command (Internal Wait State Generation)	-	65

AC Characteristics (continued)

Symbol	Parameter	Min	Max
T21A	*IOCHRDY Active Pulse Width (Memory Cycle) (Internal Wait State Generation)	1X BUSCLK	3X BUSCLK
T21B	*IOCHRDY Active Pulse Width (I/O Cycle) (Internal Wait State Generation)	.5X BUSCLK	1X BUSCLK
T23	BALE Active from Command Hold	33	-
T29	*ZWS Hold from 8-Bit Command	0	-
T30A	SA[15:12] to CA[25:12] Valid Delay, Memory Cycles	-	50
T30B	SA[15:12] to CA[15:12] Valid Delay, I/O Cycles	-	25
T31A	CA[15:12] to Socket I/O CMD Setup	70	-
T31B	CA[25:12] to Socket Memory CMD Setup	30	-
T33A	Socket CMD to *CE Hold Time	20	-
T33B	Socket CMD to *REG Hold Time	0	-
T34A	*IOIS16 to *IOCS16 Valid Delay	-	45
T34B	*IOCS16 Hold from *IOIS16	30	-
T35A	ISA CMD to SKT CMD Valid Delay for 8-Bit Memory, 8/16 I/O	-	20
T37	*CE, *REG Setup to Socket CMD Setup	5	-
T38	ISA CMD Inactive to Socket CMD Inactive Valid Delay	0	20
T39	Socket CMD Inactive to CA [25:12] Hold Time	20	-
T40A	CA[15:12] Hold from SA[15:12] Memory	0	-
T40B	CA[15:12] Hold from SA[15:12] I/O	0	-
T41	*WAIT Active to IOCHRDY Inactive	-	20
T42	*WAIT Inactive to IOCHRDY Active	0	20

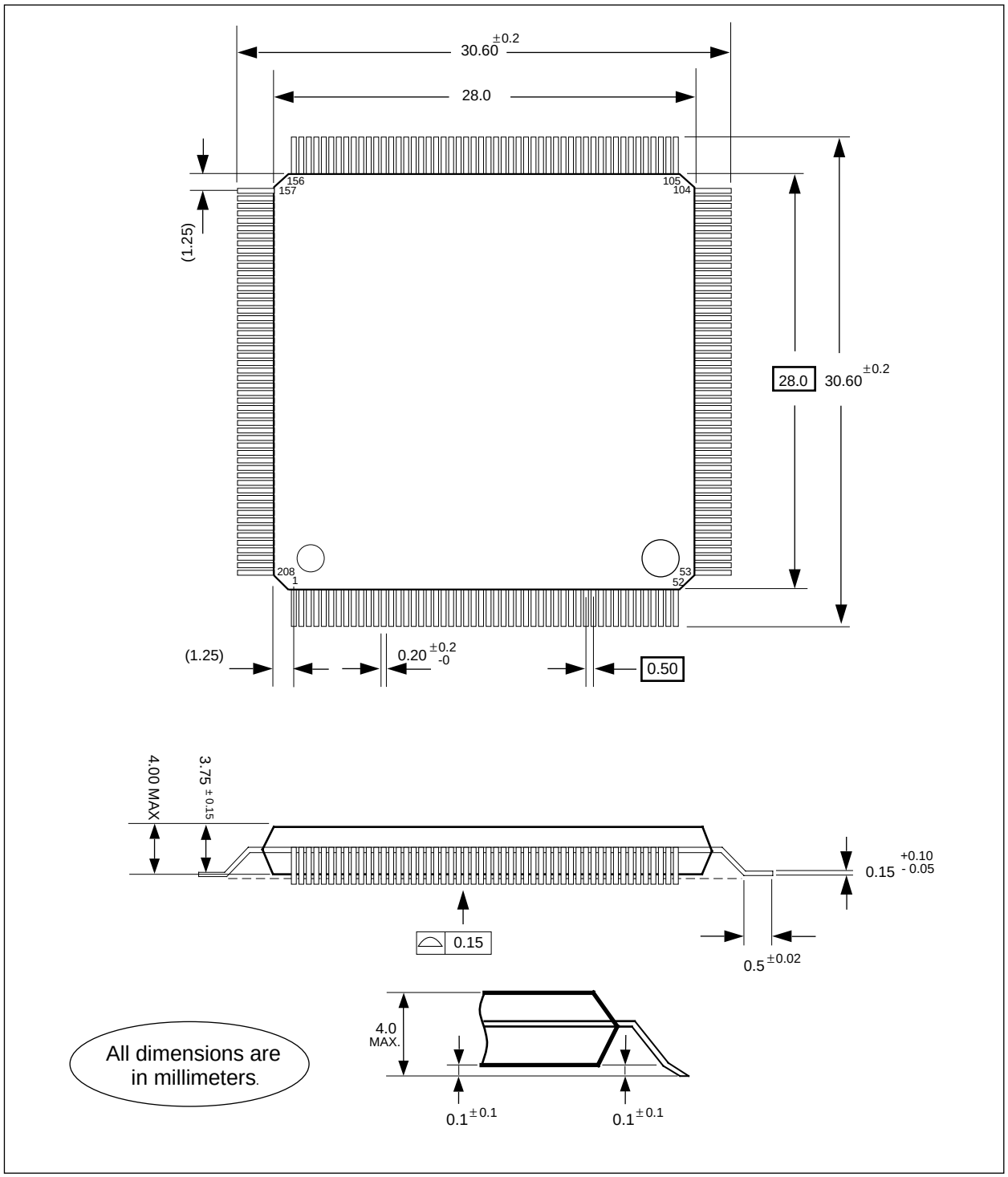
AC Characteristics (continued)

Symbol	Parameter	Min	Max
T45	AEN Valid to ISA CMD Active Setup	100	-
T46	AEN Hold from ISA Command Inactive	30	-
T47	*CS Active to PCSC Register Access CMD Active	30	-
T48	*CS Hold from PCSC Register Access CMD Inactive	0	-
T50	*RI to *RIO Delay, *SPKR to SPKROUT Delay	-	30
T51	Card Status Change to *INTR Valid Delay	-	2 X BUSCLK + 50
T52	Card Status Change to *IRQ Valid	-	50
T53	*INTR Pulse Width	4 x BUSCLK	-
T54	PCMCIA *IREQ to IRQx Delay	-	50
T60	RESETDRV Pulse Width	1µs	-
T61	PWRGOOD Rising to RESETDRV Falling	5	-
T62	Signal Inactive from RESETDRV Rising	-	200
T63	Signal Tri-State from RESETDRV Rising	-	200
T64	*INTR Inactive from RESETDRV Falling	10	50
T100	Clock to output delay	-	20

Notes: 1. *MEMCS16 value based on 30 pF load.
2. *MEMCS16 value based on 80 pF load.

NOTES

208 LEAD QUAD FLAT PACK



VADEM VG-468

PC CARD SOCKET CONTROLLER

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