VLSI TECHNOLOGY, INC.

VL16C552

DUAL ASYNCHRONOUS COMMUNICATIONS ELEMENT WITH FIFO

FEATURES

- IBM PC/AT®-compatible
- Two VL16C550 ACEs
- Enhanced Bidirectional Line Printer Port
- 16 byte FIFO reduces CPU interrupts
- Independent control of transmit, receive, line status and data set interrupts on each channel
- Individual modem control signals for each channel
- Programmable serial interface characteristics for each channel:
  - 5-, 6-, 7- or 8-bit characters
  - Even-, odd- or no-parity bit generation and detection
  - 1, 1 1/2 or 2 stop bit generation
- Three-state TTL drive for the data and control bus on each channel
- Hardware and software compatible with VL16C452 and VL16C452B

DESCRIPTION

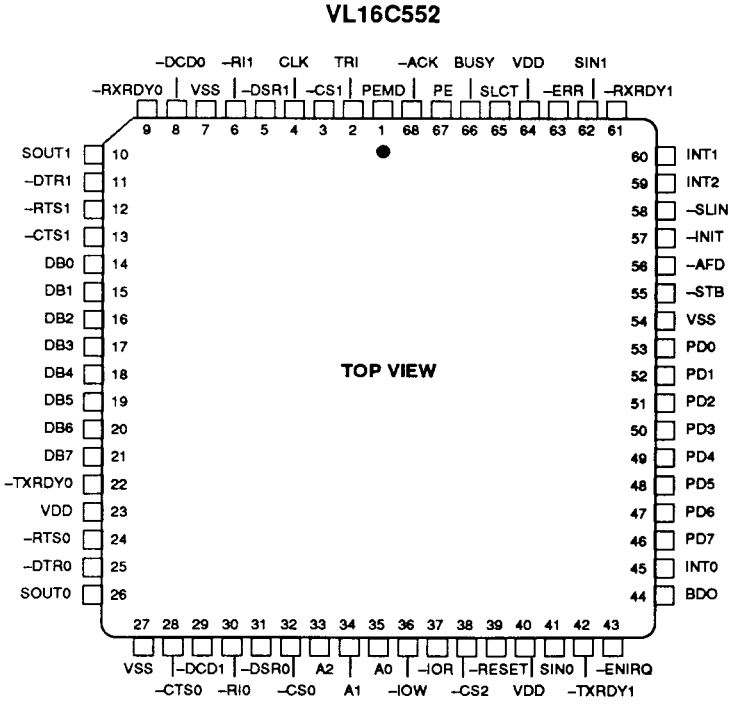
The VL16C552 is an enhanced dual-channel version of the popular VL16C550 asynchronous communications element (ACE). The device serves two serial input/output interfaces simultaneously in microcomputer- or microprocessor-based systems. Each channel performs serial-to-parallel conversion on data characters received from peripheral devices or modems, and parallel-to-serial conversion on data characters transmitted by the CPU. The complete status of each channel of the dual ACE can be read at any time during functional operation by the CPU. The information obtained includes the type and condition of the transfer operations being performed, and error conditions.

In addition to its dual communications interface capabilities, the VL16C552 provides the user with a fully bidirectional parallel data port that fully supports the parallel Centronics type printer. The parallel port, together with the two serial ports, provide IBM PC/AT- compatible computers with a single device to serve the three system ports.

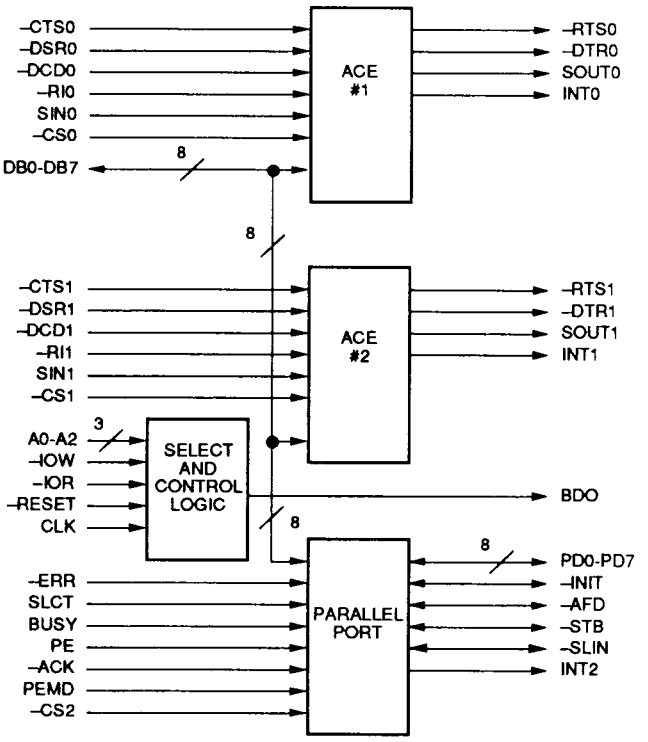
A programmable baud rate generator is included that can divide the timing reference clock input by a divisor between 1 and $(2^{16}-1)$.

The VL16C552 is housed in a 68-lead plastic leaded chip carrier.

PIN DIAGRAM



BLOCK DIAGRAM



ORDER INFORMATION

Part Number	Maximum Clock Frequency	Package
VL16C552-QC	8 MHz	Plastic Leaded Chip Carrier (PLCC)

Note: Operating temperature range is 0°C to +70°C.

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SIGNAL DESCRIPTIONS

Signal Name	Pin Number	Signal Type	Signal Description
PEMD	1	I1	Printer Enhancement Mode - When active (high), the printer port bidirectional capabiities are dependant on bit 5 of the Printer Control Register. When inactive (low), the printer port is output only (PC/AT-compatible).
TRI	2	I4	This pin is used to control the three-state control of all I/O and output pins. When this pin is asserted, all I/O and outputs become high impedance, allowing board level testers to drive the outputs without overdriving internal buffers. This pin is level sensitive. This pin is pulled down with an internal resistor that is approximately 5 KΩ, and is a CMOS input.
–CS0 - –CS2	32, 3, 38	I1	Chip Selects - Each input acts as an enable for the write and read signals for the serial channels 0 (–CS0) and 1 (–CS1). –CS2 enables the the signals to the line printer port.
CLK	4	I1	Clock Input - The external clock input to the baud rate divisor of each ACE.
–DSR0, –DSR1	31, 5	I1	Data Set Ready Inputs - The inverse state of the –DSR pins is reflected in MSR(5) of its associated Modem Status Register. DDSR [MSR(1)] indicates whether the associated –DSR pin has changed state since the previous reading of the MSR.
–RI0, –RI1	30, 6	I1	Ring Indicator Inputs - The –RI signal is a modem control input whose condition is tested by reading MSR(6) (RI) of each ACE. The Modem Status Register output TERI [MSR(2)] indicates whether the –RI input has changed from high to low since the previous reading of the MSR.
–DCD0, –DCD1	29, 8	I1	Data Carrier Detect - –DCD is a modem input whose condition can be tested by the CPU by reading MSR(7) (DCD) of the Modem Status Registers. MSR(3) (DDCD) of the Modem Status Register indicates whether the –DCD input has changed since the previous reading of the MSR. –DCD has no effect on the receiver.
–TXRDY0, –TXRDY1	22, 42	O4	Transmitter Ready (active low) - Two types of DMA signaling are available when operating with the FIFO's enabled (FCR0 equals 1). The mode select is controlled by the status of FCR3. Mode 0 - The –TXRDY signal will be active when in FIFO Mode 0 (FCR0=1, FCR3=0) and the XMIT FIFO or XMIT holding register contain no characters. When the first character is loaded into the holding register of the XMIT FIFO, –TXRDY will go inactive (high). This mode is typically used when single transfer DMA occurs. Mode 1 - The –TXRDY pin will go active in FIFO Mode 1 (FCR0=1, FCR3=1) when there are no characters in the XMIT FIFO. When the XMIT FIFO is completely full, –TXRDY will go inactive. This mode is typically used when continual multiple transfers that fill the FIFO are made. NOTE: When the FIFO's are disabled, the VL16C552 is in VL16C450 mode. In this mode, the UARTs mimic FIFO Mode 0, which allows for single DMA transfers only.
SOUT0, SOUT1	26, 10	O7	Serial Data Outputs - These lines are the serial data outputs from the ACEs' transmitter circuitry. A mark (1) is a logic "one" (high) and space (0) is a logic "zero" (low). Each SOUT is held in the mark condition when the transmitter is disabled, Reset is true, the Transmitter Register is empty, or when in the Loop Mode.
–DTR0, –DTR1	25, 11	O7	Data Terminal Ready Lines - Each DTR pin can be set (low) by writing a logic 1 to MCR(0), Modem Control Register bit 0 of its associated ACE. This signal is cleared (high) by writing a logic 0 to the DTR bit [MCR(0)] or whenever a reset occurs. When active (low), the DTR pin indicates that its ACE is ready to receive data.

SIGNAL DESCRIPTIONS (Cont.)

Signal Name	Pin Number	Signal Type	Signal Description
–RTS0, –RTS1	24, 12	O7	Request to Send Outputs - An –RTS pin is set low by writing a logic 1 to MCR(1) bit 1 of its UART's Modem Control Register. Both –RTS pins are reset high by Reset. A low on the –RTS pin indicates that its ACE has data ready to transmit. In half duplex operations, –RTS is used to control the direction of the line.
–CTS0, –CTS1	28, 13	I1	Clear to Send Inputs - The inverse state of each –CTS pin is reflected in the CTS bit of the (MSR) Modem Status Register [CTS is bit 4 of the MSR, written MSR (4)] of each ACE. A change of state in either –CTS pin since the previous reading of the associated MSR causes the setting of DCTS [MSR(0)] of each Modem Status Register.
DB0-DB7	14-21	IO6	Data Bits DB0-DB7 - The Data Bus provides eight, three-state I/O lines for the transfer of data, control and status information between the VL16C552 and the CPU. These lines are normally in a high-impedance state except during read operations. DB0 is the least significant bit (LSB) and is the first serial data bit to be received or transmitted.
–RXRDY0, –RXRDY1	9, 61	O4	Receiver Ready (active-low) - Two types of DMA signaling are available when operating with the FIFO's enabled (FCR0 = 1). The mode select is controlled by the status of FCR3. Mode 0 - The –RXRDY signal will be active when in FIFO Mode 0 (FCR0=1, FCR3=0) and the RCVR FIFO or RCVR holding register contain at least one character. When there are no more characters in the FIFO or holding register, the –RXRDY pin will go inactive. This mode is typically used when single transfer DMA occurs. Mode 1 - The –RXRDY pin will go low in the FIFO Mode (FCR0=1) when the FCR3 bit is high and the timeout or trigger levels have been reached. It will go inactive when the FIFO or holding register is empty. Mode 1 - The –RXRDY pin will go active in FIFO Mode 1 (FCR0=1, FCR3=1) when the timeout or trigger levels have been reached. It will go inactive when the FIFO or holding register is empty. This mode is typically used when continual multiple transfers that fill the FIFO are made.
A0, A1, A2	35, 34, 33	I1	Address Lines A0-A2 - The address lines select the internal registers during CPU bus operations. See Table 1 for the decode of the serial channels, Table 11 for the decode of the parallel line printer port.
–IOW	36	I1	Input/Output Write Strobe - This is an active low input causing data from the data bus to be input to either ACE or to the parallel port. The destination depends upon the register selected by the address inputs A0, A1, A2 and chip selects –CS0, –CS1 and –CS2.
–IOR	37	I1	Input/Output Read Strobe - This is an active low input which enables the selected channel to output data to the data bus (DB0-DB7). The destination depends upon the register selected by the address inputs A0, A1, A2 and chip select –CS0, –CS1 and –CS2.
–RESET	39	I1	Reset - When low, the reset input forces the VL16C552 into an idle mode in which all serial data activities are suspended. The Modem Control Register (MCR) along with its associated outputs are cleared. The Line Status Register (LSR) is cleared except for the THRE and TEMT bits, which are set. All functions of the device remain in an idle state until programmed to resume serial data activities.

SIGNAL DESCRIPTIONS (Cont.)

Signal Name	Pin Number	Signal Type	Signal Description
SIN0, SIN1	41, 62	I1	Serial Data Inputs - The serial data inputs move information from the communication line or modem to the VL16C552 receiver circuits. A mark (1) is high, and a space (0) is low. Data on serial data inputs is disabled when operating in the Loop Mode.
–ENIRQ	43	I1	Parallel port interrupt source mode selection. When negated (low), the AT mode of interrupts is selected. In this mode, the –ACK input is internally connected to the PIRQ output. If the –ENIRQ input is tied high, the interrupt source will be held in a latched state until the Status Register is read which will then reset the PIRQ output.
BDO	44	O7	Bus Buffer Output - This active high output is asserted when either serial channel or the parallel port is read. This output can be used to control the system bus driver (74LS245).
INT0, INT1	45, 60	O5	Serial Channel Interrupts - Each three-state, serial channel interrupt output (enabled by bit 3 of the MCR) goes active (high) when one of the following interrupts has an active (high) condition and is enabled by the Interrupt Enable Register of its associated channel: Receiver Error flag, Received Data Available, Transmitter Holding Register Empty, and Modem Status. The interrupt is reset low upon appropriate service. Upon reset, the interrupt output will be in the high impedance state.
PD0-PD7	53-46	IO5	Parallel Data Bits (0-7) - These eight lines provide a byte-wide input or output port to the system. They are held in a high-impedance state when PEMD is held in the high state.
–STB	55	O4	Printer Command Data Strobe - This signal is the inversion of bit 0 of the LPT Port Control Register. When LPTPC [0]=0, –STB is high. When LPTPC[0]=1, –STB is low.
–AFD	56	O4	Printer Command Autofeed - This signal is the inversion of bit 1 of the LPT Port Control Register. When LPTPC[1]=0, –AFD is high. When LPTPC[1]=1, –AFD is low.
–INIT	57	O4	Printer Command Initialize - This signal follows bit 2 of the LPT Port Control Register. When LPTPC[2]=0, –INIT is low. When LPTPC[2]=1, –INIT is high.
–SLIN	58	O4	Printer Command Select - This signal is the inversion of bit 3 of the LPT Port Control Register. When LPTPC[3]=0, –SLIN is high. When LPTPC[3]=1, –SLIN is low.
INT2	59	O5	Printer Port Interrupt - This signal is an active high, three-state output, generated by the positive transition of –ACK. It is enabled by bit 4 of the Write Control Register. Upon a reset, the interrupt output will be in the high impedance state.
–ERR	63	I3	Printer Status Error - The status of this signal can be determined by reading bit 3 of the LPT Port Status Register. The LPTSR[3] signal follows the state of the –ERR pin.
SLCT	65	I3	Printer Status Select - The status of this signal can be determined by reading bit 4 of the LPT Port Status Register. The LPTSR[4] signal follows the state of the SLCT pin.
BUSY	66	I3	Printer Status Busy - The status of this signal can be determined by reading bit 7 of the LPT Port Status Register. The LPTSR[7] signal is the inversion of the BUSY pin.
PE	67	I3	Printer Status Paper Empty - The status of this signal can be determined by reading bit 5 of the LPT Port Status Register. The LPTSR[5] signal follows the state of the PE pin.

SIGNAL DESCRIPTIONS (Cont.)

Signal Name	Pin Number	Signal Type	Signal Description
–ACK	68	I3	Printer Status Acknowledge - The status of this signal can be determined by reading bit 6 of the LPT Port Status Register. If bit 4 of the LPT Port Control Register is a 1, a low to high transition of –ACK will generate an interrupt.
VDD	23, 40, 64		Power Supply - The power supply requirement is 5 V ±5%.
VSS	7, 27, 54		Ground (0 V) - All pins must be tied to ground for proper operation.

TEST MODE PINS:
The three test modes which are supported by the VL16C552 are:

Mode	Description
In-Circuit	The In-Circuit Test mode is selected when –IOW and –IOR are simultaneously taken low when DB1 is low, DB0 is high and TRI is high. This mode is normally used to confirm that the VL16C552 has been physically attached to the printed circuit board.
Three-State	The Three-State Test mode is entered when the TRI input is taken high. This mode is used to control the three-state control of all I/O and output pins. When this mode is selected, all I/O and outputs become high impendance, allowing board level testers to drive the outputs without overdriving internal buffers.

Each of these test modes are selected by driving a combination of pins into the desired mode.

SIGNAL TYPE LEGEND

No	mA	Type	Comments
O1	10	TTL	
O2	24	TTL	
O3	10	TTL-OD	Open drain (collector)
O4	23	TTL-ODP	Open drain with 1-5 kΩ pull-up
O5	20	TTL-TS	Three-statable
O6	24	TTL-TS	Three-statable
O7	2	TTL-TS	Three-statable
I1	-	TTL	
I2	-	CMOS	
I3	-	TTL	With 20 kΩ pull-up resistor
I4	-	CMOS	With 1-5 kΩ pull-down resistor
IO1	10	TTL-TS	Bidirectional, three-statable
IO2	24	TTL-TS	Bidirectional, three-statable
IO3	10	TTL-OD	Bidirectional, open drain
IO4	24	TTL-OD	Bidirectional, open drain
IO5	12	TTL-TSP	Bidirectional, three-statable
IO6	4	TTL-TS	Bidirectional, three-statable
OSC	-	XTAL-OSC	Crystal oscillator pad

ICT INPUT			ICT OUTPUT		
Pin	Signal	Type	Pin	Signal	Type
1	PEMD	I	18	DB4	I/O
3	–CS1	I	61	–RXRDY1	O
			15	DB1	I/O
4	CLK	I	53	PD0	I/O
5	–DSR1	I	12	–RTS1	O
6	–RI1	I	60	INT1	O
8	–DCD1	I	10	SOUT1	O
			42	–TXRDY1	O
13	–CTS1	I	11	–DTR1	O
28	–CTS0	I	24	–RTS0	O
29	–DCD0	I	26	SOUT0	O
30	–RI0	I	47	PD6	I/O
			45	INT0	O
31	–DSR0	I	25	–DTR0	O
32	–CS0	I	20	DB6	I/O
			22	–TXRDY0	O
35	A0	I	50	PD3	I/O
34	A1	I	51	PD2	I/O
33	A2	I	52	PD1	I/O
36	–IOW	I	49	PD4	I/O
			46	PD7	I/O
37	–IOR	I	19	DB5	I/O
			44	BDO	I
38	–CS2	I	16	DB2	I/O
			48	PD5	I/O
41	SIN0	I	21	DB7	I/O
			9	–RXRDY0	O
43	–ENIRQ	I	17	DB3	I/O
62	SIN1	I	14	DB0	I/O
63	–ERR	I	57	–INIT	O
65	SLCT	I	56	–AFD	O
66	BUSY	I	55	–STB	O
67	PE	I	58	–SLIN	O
68	–ACK	I	59	INT2	O

The following pins are not mapped:

Pin	Signal	Type
7	VSS	Power connection
27	VSS	Power connection
54	VSS	Power connection
23	VDD	Power connection
40	VDD	Power connection
64	VDD	Power connection
2	TRI	Used to enter ICT mode
39	–RESET	Used to exit ICT mode
4	CLK	Clock pin

REGISTERS

Three types of internal registers are used in the ACE (Control, Status and Data). The control registers are the Bit Rate Select Register DLL (Divisor Latch LSB) and DLM (Divisor Latch MSB), Line Control Register, Interrupt Enable Register, FIFO Control Register and the Modem Control Register. The status registers are the Line Status Registers and the Modem Status Register. The data registers are the Receiver Buffer Register and the Transmitter Holding Register. The Address, Read, and Write inputs are used in conjunction with the Divisor Latch Access Bit in the Line Control Register [LCR(7)] to select the register to be written or read (see Table 1). Individual bits within these registers are referred to by the register mnemonic and the bit number in parenthesis. As an example, LCR(7) refers to Line Control Register Bit 7.

The Transmitter Buffer Register and Receiver Buffer Register are data registers that hold from five to eight bits of data. If less than eight data bits are transmitted, data is right justified to the LSB. Bit 0 of a data word is always the first serial data bit received and transmitted. The ACE data registers are double-buffered so that read and write operations may be performed when the ACE is performing the parallel-to-serial or serial-to-parallel conversion.

LINE CONTROL REGISTER

The format of the data character is controlled by the Line Control Register. The LCR may be read. Its contents are described below and shown in Figure 1.

LCR(0) and LCR(1) Word Length Select bit 1: The number of bits in each serial character is programmed as shown in Figure 1.

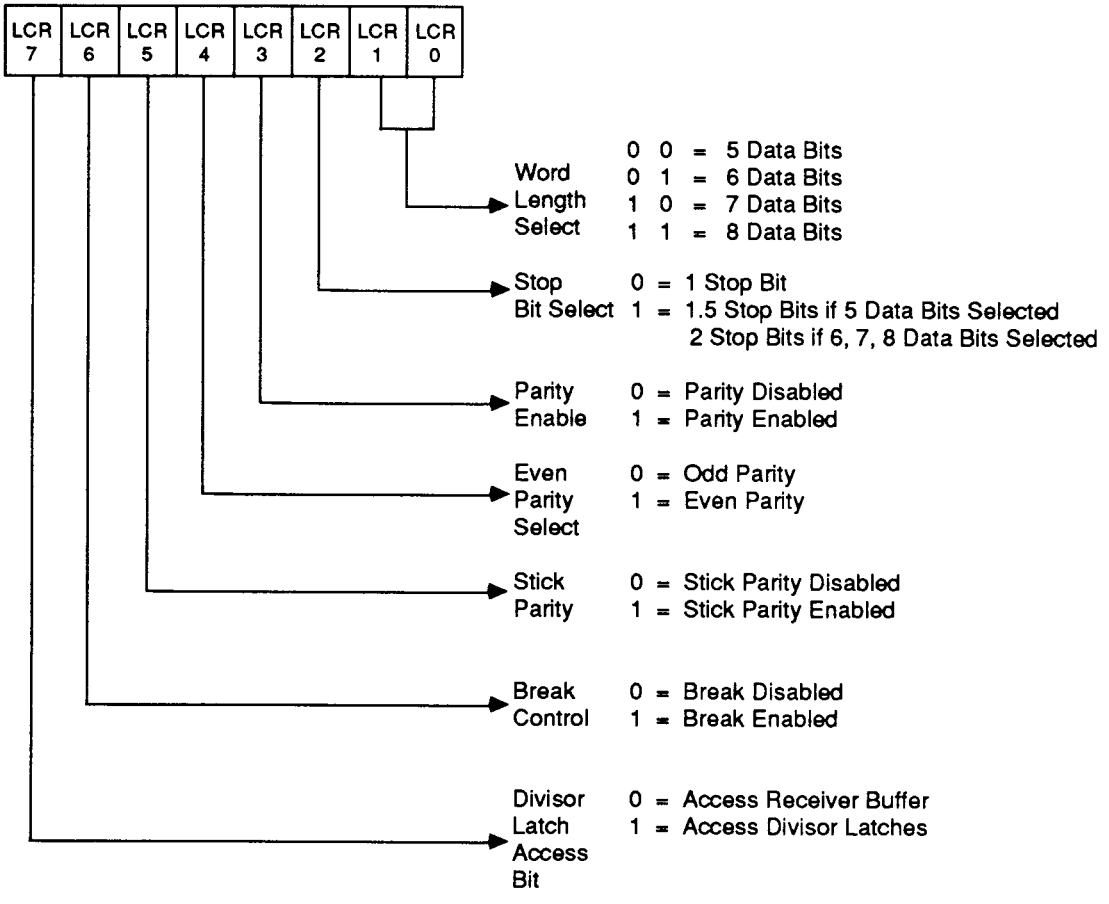
LCR(2) Stop Bit Select: LCR(2) specifies the number of stop bits in each transmitted character. See Figure 1. The receiver always checks for one stop bit.

TABLE 1. SERIAL CHANNEL INTERNAL REGISTERS

DLAB	A2	A1	A0	Mnemonic	Register
0	0	0	0	RBR	Receiver Buffer Register (read only)
0	0	0	0	THR	Transmitter Holding Register (write only)
0	0	0	1	IER	Interrupt Enable Register
X	0	1	0	IIR	Interrupt Identification Register (read only)
X	0	1	0	FCR	FIFO Control Register (write only)
X	0	1	1	LCR	Line Control Register
X	1	0	0	MCR	Modem Control Register
X	1	0	1	LSR	Line Status Register
X	1	1	0	MSR	Modem Status Register
X	1	1	1	SCR	Scratch Register
1	0	0	0	DLL	Divisor Latch (LSB)
1	0	0	1	DLM	Divisor Latch (MSB)

X = "Don't Care" 0 = Logic Low 1 = Logic High

FIGURE 1. LINE CONTROL REGISTER



LCR(3) Parity Enable: When LCR(3) is high, a parity bit between the last data word bit and stop bit is generated and checked.

LCR(4) Even Parity Select: When enabled a one selects even parity.

LCR(5) Stick Parity: When parity is enabled [LCR(3)=1], LCR(5)=1 causes the transmission and reception of a parity bit to be in the opposite state from the value of LCR(4). This forces parity to a known state and allows the receiver to check the parity bit in a known state.

LCR(6) Break Control: When LCR(6) is set to a logic 1, the serial output (SOUT) is forced to the spacing (logic 0) state. The Break Control bit acts only on SOUT and does not effect the transmitter logic. If the following sequence is used, no invalid characters will be transmitted because of the break.

1. Load all "0"s pad character in response to THRE.
2. Set the break in response to the next THRE.
3. Wait for the transmitter to be idle (TEMT=1), then clear the break when the normal transmission has to be restored.

LCR(7) Divisor Latch Access Bit (DLAB); LCR(7) must be set high (logic 1) to access the Divisor Latches DLL and DLM of the Baud Rate Generator during a read or write operation. LCR(7) must be input low (logic 0) to access the Receiver Buffer, the Transmitter Holding, or the Interrupt Enable Registers.

LINE STATUS REGISTER

The Line Status Register (LSR) is a single register that provides status indications.

The Line Status Register shown in Table 2 is described as follows:

LSR(0) Data Ready (DR): Data Ready (DR) bit indicates that the RBR, or FIFO, has been loaded with a received character (including Break) and that the CPU may access this data. This bit is set low by a read of the RBR when in VL16C450 Mode or FIFO Mode 0. When in FIFO Mode 1, this bit is not set low until the last byte is read (read RBR) from the FIFO.

LSR(1) Overrun Error (OE): Overrun Error indicates that data in the Receiver Buffer Register was not read by the CPU before the next character was transferred into the Receiver Buffer Register, overwriting the previous character. The OE indicator is reset whenever the CPU reads the contents of the Line Status Register.

An overrun error will occur in the FIFO Mode after the FIFO is full and the next character is completely received. The overrun error is detected by the CPU on the first LSR read after it happens. The character in the shift register is not transferred to the FIFO but it is overwritten.

TABLE 2. LINE STATUS REGISTER BITS

LSR BITS	1	0
LSR(0) Data Ready (DR)	Ready	Not Ready
LSR(1) Overrun Error (OE)	Error	No Error
LSR(2) Parity Error (PE)	Error	No Error
LSR(3) Framing Error (FE)	Error	No Error
LSR(4) Break Interrupt (BI)	Break	No Break
LSR(5) Transmitter Holding Register Empty (THRE)	Empty	Not Empty
LSR(6) Transmitter Empty (TEMT)	Empty	Not Empty
LSR(7) RCVR FIFO Error	Error in FIFO	No Error in FIFO

LSR(2) Parity Error (PE): Parity Error indicates that the received data character does not have the correct parity, as selected by LCR(3) and LCR(4). The PE bit is set high upon detection of a parity error, and is reset low when the CPU reads the contents of the LSR.

In the FIFO Mode, the Parity Error is associated with a particular character in the FIFO. LSR(2) reflects the error when the character is at the top of the FIFO.

LSR(3) Framing Error (FE): Framing Error indicates that the received character did not have a valid stop bit. LSR(3) is set high when the stop bit following the last data bit or parity bit is detected as a zero bit (spacing level). The FE indicator is reset low when the CPU reads the contents of the LSR. In the FIFO Mode, the Framing Error is associated with a particular character in the FIFO. LSR(3) reflects the error when the character is at the top of the FIFO.

LSR(4) Break Interrupt (BI): Break Interrupt is set high when the received data input is held in the spacing (logic 0) state for a full word transmission time (start bit + data bits + parity + stop bits). The BI indicator is reset when the CPU reads the contents of the Line Status Register.

In the FIFO Mode this is associated with a particular character in the FIFO. LSR(4) reflects the BI when the break character is at the top of the FIFO. The error is detected by the CPU when its associated character is at the top of the FIFO during the first LSR read. Only one zero character is loaded into the FIFO when BI occurs.

LSR(1)-LSR(4) are the error conditions that produce a Receiver Line Status interrupt [priority 1 interrupt in the Interrupt Identification Register (IIR)] when any of the conditions are detected. This interrupt is enabled by setting IER(2)=1 in the Interrupt Enable Register.

LSR(5) Transmitter Holding Register Empty (THRE): THRE indicates that the ACE is ready to accept a new character for transmission. The THRE bit is set high when a character is transferred from the Transmitter Holding Register into the Transmitter Shift Register. LSR(5) is reset low by the loading of the Transmitter Holding Register by the CPU. LSR(5) is not reset by a CPU read of the LSR. In the FIFO Mode when the XMIT FIFO is empty this bit is set. It is cleared when one byte is written to the XMIT FIFO.

When the THRE interrupt is enabled IER(1), THRE causes a priority 3 interrupt in the IIR. If THRE is the interrupt source indicated in IIR, INTRPT is cleared by a read of the IIR.

LSR(6) Transmitter Empty (TEMT): TEMT is set high when the Transmitter Holding Register (THR) and the Transmitter Shift Register (TSR) are both empty. LSR(6) is reset low when a character is loaded into the THR and remains low until the character is transferred out of SOUT. TEMT is not reset low by a CPU read of the LSR. In the FIFO Mode, when both the transmitter FIFO and shift register are empty this bit is set to one.

LSR(7) This bit is always 0 in the VL16C450 Mode. In FIFO Mode, it is set when at least one of the following data errors is in the FIFO: Parity Error, Framing Error or Break Interrupt indication.

Note: The Line Status Register may be written. However, this function is intended only for factory test. It should be considered Read Only by applications software.

FIFO CONTROL REGISTER

This write only register is at the same location as the IIR. It is used to enable and clear the FIFOs, set the trigger level of the RCVR FIFO, and select the type of DMA signaling.

FCR(0) FIFO Enable: FCR(0) enables both the XMIT and RCVR FIFOs. Programming of other FCR bits is enabled by setting FCR(0) to a one. The FIFO's operate in VL16C450 Mode when FCR(0) is zero. All bytes in both FIFOs can be cleared automatically from the FIFOs when changing from FIFO Mode [FCR(0) is one] to VL16C450 Mode and vice versa.

FCR(1) RCVR FIFO Reset: This bit clears all bytes in the RCVR FIFO and resets the counter logic to 0 when it is set to a one. It does not clear the receive shift register.

FCR(2) XMIT FIFO Reset: This bit clears all bytes in the XMIT FIFO and resets the counter logic to 0 when it is set to a one. This does not clear the transmit shift register.

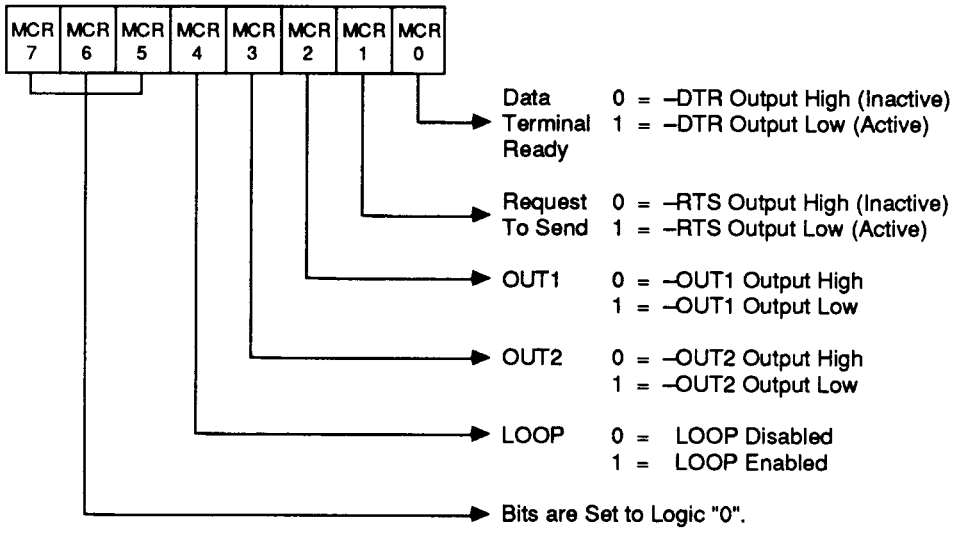
FCR(3) DMA Mode Select: This bit controls the method of DMA signaling that will be used. If FCR(3) is a one, the part will operate in Mode 1. It will be in Mode 0 if FCR(3) is 0. These modes are only valid if FCR(0) is a one, and it directly affects the operation of the –RXRDY and –TXRDY pins.

FCR(4) - FCR(5): These two bits are reserved for future use.

FCR(6) - FCR(7): These two bits are used for setting the trigger level for the RCVR FIFO interrupt.

FCR 7	FCR 6	RCVR FIFO Trigger Level (Bytes)
0	0	01
0	1	04
1	0	08
1	1	14

FIGURE 2. MODEM CONTROL REGISTER



MODEM CONTROL REGISTER

The Modem Control Register (MCR) controls the interface with the modem or data set as described in Figure 2. MCR can be written and read. The –RTS and –DTR outputs are directly controlled by their control bits in this register. A high input asserts a low (true) at the output pins. MCR Bits 0, 1, 2, 3, and 4 are shown below:

MCR(0): When MCR(0) is set high, the –DTR output is forced low. When MCR(0) is reset low, the –DTR output is forced high. The –DTR output of the serial channel may be input into an inverting line driver in order to obtain the proper polarity input at the modem or data set.

MCR(1): When MCR(1) is set high, the –RTS output is forced low. When MCR(1) is reset low, the –RTS output is forced high. The –RTS output of the serial channel may be input into an inverting line driver in order to obtain the proper polarity input at the modem or data set.

MCR(2): When MCR (2) is set high –OUT1 is forced low. This is only seen in loopback mode.

MCR(3): When MCR(3) is set high, the –OUT2 output is forced low.

MCR(4): MCR(4) provides a local loopback feature for diagnostic testing of the channel. When MCR(4) is set high, Serial Output (SOUT) is set to the marking (logic 1) state, and the receiver data input Serial Input (SIN) is disconnected. The output of the Transmitter Shift Register is looped back into the Receiver Shift Register input. The four modem control inputs (–CTS, –DSR, –DCD, and –RI) are disconnected. The four modem control register bits (DTR, RTS, OUT1 and OUT2) are internally connected to (in order) MSR(5), MSR(4), MSR(6), MSR(7). The modem control output pins are forced to their inactive state (high) on the VL16C552.

In the diagnostic mode, data transmitted is immediately received. This allows the processor to verify the transmit and receive data paths of the selected serial channel.

Interrupt control is fully operational. However, interrupts are generated by controlling the lower four MCR bits internally. Interrupts are not generated by activity on the external pins represented by those four bits.

Bits MCR(5)-MCR(7) are permanently set to logic 0.

MODEM STATUS REGISTER

The MSR provides the CPU with status of the modem input lines from the modem or peripheral devices. The MSR allows the CPU to read the serial channel modem signal inputs by accessing the data bus interface of the ACE in addition to the current status information, four bits of the MSR indicate whether the modem inputs have changed since the last reading of the MSR. The delta status bits are set high when a control input from the modem changes state, and reset low when the CPU reads the MSR.

The modem input lines are –CTS, –DSR, –RI, and –DCD. MSR(4)-MSR(7) are status indications of these lines. A status bit = 1 indicates the input is a low. A status bit = 0 indicates the input is high. If the modem status interrupt in the Interrupt Enable Register is enabled [IER(3)], an interrupt is generated whenever MSR(0)-MSR(3) is set to a one. The MSR is a priority 4 interrupt. The contents of the Modem Status Register are described in Table 3.

MSR(0) Delta Clear to Send (DCTS): DCTS displays that the –CTS input to the serial channel has changed state since it was last read by the CPU.

MSR(1) Delta Data Set Ready (DDSR): DDSR indicates that the –DSR input to the serial channel has changed state since the last time it was read by the CPU.

MSR(2) Trailing Edge of Ring Indicator (TERI): TERI indicates that the –RI input to the serial channel has changed state from low to high since the last time it was read by the CPU. High to low transitions on –RI do not activate TERI.

TABLE 3. MODEM STATUS REGISTER BITS

MSR Bit	Mnemonic	Description
MSR(0)	DCTS	Delta Clear To Send
MSR(1)	DDSR	Delta Data Set Ready
MSR(2)	TERI	Trailing Edge of Ring Indicator
MSR(3)	DDCD	Delta Data Carrier Detect
MSR(4)	–CTS	Clear To Send
MSR(5)	–DSR	Data Set Ready
MSR(6)	–RI	Ring Indicator
MSR(7)	–DCD	Data Carrier Detect

MSR(3) Delta Data Carrier Detect (DDCD): DDCD indicates that the –DCD input to the serial channel has changed state since the last time it was read by the CPU.

MSR(4) Clear to Send (CTS): CTS is the complement of the –CTS input from the modem indicating to the serial channel that the modem is ready to receive data from the serial channel's transmitter output (SOUT). If the serial channel is in Loop Mode [(MCR(4)=1], MSR(4) reflects the value of RTS in the MCR.

MSR(5) Data Set Ready (DSR): DSR is the complement of the –DSR input from the modem to the serial channel which indicates that the modem is ready to provide received data to the serial channel receiver circuitry. If the channel is in the Loop Mode [MCR(4)=1], MSR(5) reflects the value of DTR in the MCR.

MSR(6) Ring Indicator (RI): RI is the complement of the –RI input (pin 39). If the channel is in the Loop Mode (MCR(4)=1), MSR(6) reflects the value of –OUT1 in the MCR.

MSR(7) Data Carrier Detect (DCD): Data Carrier Detect indicates the status of the Data Carrier Detect (–DCD) input. If the channel is in the Loop Mode (MCR(4)=1), MSR(7) reflects the value of –OUT2 in the MCR.

Reading the MSR register will clear the delta modem status indications but has no effect on the other status bits.

For LSR and MSR, the setting of status bits is inhibited during status register read operations. If a status condition is generated during a read –IOR operation, the status bit is not set until the trailing edge of the read.

If a status bit is set during a read operation, and the same status condition occurs, that status bit will be cleared at the trailing edge of the read instead of being set again.

Note: In Loop Back Mode, when Modem Status interrupts are enabled, the –CTS, –DSR, –RI and –DCD input pins are ignored. However, a Modem Status interrupt may still be generated by writing to MSR7-MSR4. This is considered a test mode only. Applications software should not write to the Modem Status register.

DIVISOR LATCHES

The ACE serial channel contains a programmable Baud Rate Generator (BRG) that divides the clock (DC to 8 MHz) by any divisor from 1 to $2^{16}-1$ (see also BRG description). The output of the Baud Rate Generator is referrred to as RCLK. The frequency of RCLK is 16X the data rate. The desired divisor number is reached through use of the following equation:

DIVISOR#=Clock/(Baud Rate x 16) or DIVISOR#=Clock/(Data Rate)

Two 8-bit divisor latch registers store the divisor in a 16-bit binary format. These Divisor Latch registers must be loaded during initialization. Upon loading either of the Divisor Latches, a 16-bit baud counter is immediately loaded. This prevents long counts on initial load.

The BRG can use any of three different popular frequencies to provide standard baud rates. These frequencies are 1.8432 MHz, 3.072 MHz, and 8 MHz. With these frequencies, standard bit rates from 50 to 512K bps are available. Tables 5, 6 and 7 illustrate the divisors needed to obtain standard rates using these three frequencies.

SCRATCHPAD REGISTER

Scratchpad Register is an 8-bit Read/ Write register that has no effect on either channel in the ACE. It is intended to be used by the programmer to hold data temporarily.

INTERRUPT IDENTIFICATION REGISTER

In order to minimize software overhead during data character transfers, the serial channel prioritizes interrupts into four levels. The four levels of interrupt conditions are as follows:

1. Receiver Line Status (priority 1)
2. Received Data Ready (priority 2) or character timeout
3. Transmitter Holding Register Empty (priority 3)
4. Modem Status (priority 4)

Information indicating that a prioritized interrupt is pending and the type of interrupt is stored in the Interrupt Identification Register (IIR). The IIR indicates the highest priority interrupt pending. The contents of the IIR are indicated in Table 4 and are described below:

IIR(0) can be used to indicate whether an interrupt is pending. When IIR(0) is low, an interrupt is pending.

IIR(1) and IIR(2) are used to identify the highest priority interrupt pending as indicated in Table 4.

IIR(3): This bit is always logic 0 when in the VL16C450 Mode. This bit is set along with bit 2 when in the FIFO Mode and a trigger change level interrupt is pending.

IIR(4)-IIR(5): These two bits are always logic 0.

IIR(6)-IIR(7): FCR(0)=1 sets these two bits.

INTERRUPT ENABLE REGISTER

The Interrupt Enable Register (IER) is used to independently enable the four serial channel interrupt sources which activate the interrupt (INT) output. All interrupts are disabled by resetting

IER(0)-IER(3) of the Interrupt Enable Register. Interrupts are enabled by setting the appropriate bits of the IER high. Disabling the interrupt system inhibits the Interrupt Identification Register and the active (high) INT output. All other system functions operate in their normal manner, including the setting of the Line Status and Modem Status Registers. The contents of the Interrupt Enable Register is described in Table 9 and below:

IER(0): When set to one, IER(0) enables the Received Data Available interrupt and the timeout interrupts in the FIFO Mode.

IER(1): When set to one, IER(1) enables the Transmitter Holding Register Empty interrupt.

IER(2): When set to one IER(2) enables the Receiver Line Status interrupt.

IER(3): When set to one, IER(3) enables the Modem Status Interrupt.

IER(4)-IER(7): These four bits of the IER are logic 0.

MASTER RESET

After power up, the ACE –RESET input should be held low for five microseconds to reset the ACE circuits to an idle mode until initialization. A low on –RESET causes the following:

1. Initializes the transmitter and receiver internal clock counters.
2. Clears the Line Status Register (LSR), except for Transmitter Shift Register Empty (TEMT) and Transmit Holding Register Empty (THRE), which are set. The Modem Control Register (MCR) is also cleared. All of the discrete lines, memory elements and miscellaneous logic associated with these register bits are also cleared or turned off. The Line Control Register (LCR), Divisor Latches, Receiver Buffer Register, Transmitter Buffer Register are not effected.

Following the removal of the reset condition (reset low), the ACE remains in the idle mode until programmed.

A hardware reset of the ACE sets the THRE and TEMT status bit in the LSR. When interrupts are subsequently enabled, an interrupt occurs due to THRE.

A summary of the effect of a reset on the ACE is given in Table 8.

PROGRAMMING

The serial channel of the ACE is programmed by the control registers LCR, IER, DLL and DLM, MCR and FCR. These control words define the character length, number of stop bits, parity, baud rate, and modem interface.

While the control register can be written in any order, the IER should be written last because it controls the interrupt enables. Once the serial channel is programmed and operational, these registers can be updated any time the ACE serial channel is not transmitting or receiving data.

FIFO INTERRUPT MODE OPERATION

The following RCVR interrupts will occur when the RCVR FIFO and receive interrupts are enabled. All interrupts reflect the byte at the top of the FIFO. The interrupt descriptions are in order of their priority. (The first description is the highest priority.)

1. IIR = 01 indicates that there are no interrupts pending.
2. IIR=06 (Receive Line Status Interrupt) indicates that the byte at the top of the FIFO has some sort of error in it (OE, PE, FE, or BI). This interrupt is cleared by reading the LSR. Reading the LSR also tells the

TABLE 4. INTERRUPT IDENTIFICATION REGISTER

FIFO Mode Only	Interrupt Identification Register			Interrupt Set and Reset Functions			
Bit 3	Bit 2	Bit 1	Bit 0	Priority Level	Interrupt Type	Interrupt Source	Interrupt Reset Control
0	0	0	1	–	None	None	–
0	1	1	0	First	Receiver Line Status	OE, PE, FE or BI	LSR Read
0	1	0	0	Second	Received Data Available	Receiver Data Available for 450 or 550 mode, or Trigger Level Reached for FIFO mode.	RBR Read or FIFO Drops Below the Trigger Level
1	1	0	0	Second	Trigger Change Level Indication	Minimum of One Character in the RCVR FIFO and No Character Input or Removed During a Time Period Depending on How Many Characters are in FIFO and What the Trigger Level is Set at (3.5 to 4.5 character times*.) * The exact time will be [(word length) x 7 – 2] x 8 + [(trigger level – number of characters) x 8 +1] RCLKS.	RBR Read
0	0	1	0	Third	THRE	THRE	Read of IIR or THR Write
0	0	0	0	Fourth	Modem Status	–CTS, –DSR, –RI or –DCD	MSR Read

user which one of the errors is in that byte.

3. The IIR will equal an 04 when received data is available in the RCVR FIFO. In Mode 0, this occurs when a complete character is transferred from the receiver shift register to the RCVR FIFO. In Mode 1, the Receiver FIFO must be filled at or above the trigger level with data. This interrupt is cleared by reading the data from the RBR, until it either is empty (Mode 0) or the amount of data in it is less than the trigger level (Mode 1). The LSR(0) bit, when it is 1, says that the data in the top byte in the RCVR FIFO is available. When the FIFO is emptied by reading the Receive Buffer Register, LSR(0) is reset to a zero.

   The Trigger Level Change Interrupt (IIR = 0C) description is found in the following section. It has the same priority as the Receiver Data Available Interrupt (IIR = 04).

   A. If the following conditions exist, a FIFO Trigger Change Level Interrupt will occur.

      - Minimum of one character in FIFO
      - Last received serial character was longer than 3.5 to 4.5 continuous previous character times. (If two stop bits are programmed, the second one is included in the time delay.) Once 3.5 character times have been met and no accesses have been made to the FIFO, the trigger level matches the number of FIFO characters, the trigger change level interrupt will be returned to its original programmed value.
      - The last CPU read of the FIFO was more than 3.5 to 4.5 continuous character times ago. At 300 baud and 12-bit characters, the FIFO timeout interrupt causes a latency of 160 ms maximum from received character to interrupt issued.

   B. By using the RCLK input for a clock signal the character times can be calculated. (The delay is proportional to the baud rate.)

   C. The trigger change level timer is reset after the CPU reads the RCVR FIFO or after a new character is received when there has been no trigger change level interrupt.

   D. A trigger change level interrupt is cleared and the timer is reset when the CPU reads a character from the RCVR FIFO.

4. IIR = 02 (THRE interrupt) indicates that the Transmit Holding Register is empty. This interrupt is cleared by either writing a byte to the THR or by reading the IIR.

5. IIR = 00 (Modem Status interrupt) indicates that there has been some change in the status of the modem. This interrupt is cleared by reading the MSR, which also tells the user what type of status change occured.

XMIT interrupts will occur as follows when the transmitter and XMIT FIFO interrupts are enabled (FCR0=1,IER1=1)

1. The XMIT FIFO empty indications will be delayed one character time minus the last stop bit time whenever the following occurs:

   THRE=1 and there have not been a minimum of two bytes at the same time in XMIT FIFO, since the last THRE=1.

2. When the transmitter FIFO is empty, the transmitter holding register interrupt (IIR=02) occurs. The interrupt is cleared as soon as the transmitter holding register is written to or the IIR is read.

When FCR0 is enabled, an interrupt does not occur immediately if enabled (IER=1). The first XMIT interrupt occurs due to the conditions stated in 1 and 2 above only after data has first been entered into the XMIT FIFO.

RCVR FIFO trigger level and character trigger change level interrupts have the same priority as the transmitter FIFO empty.

FIFO POLLED MODE OPERATION

Resetting IER0, IER1, IER2, IER3 or all to zero, with FCR0=1, puts the ACE into the FIFO Polled Mode. Since the RCVR and XMITER are controlled separately, either or both can be in the Polled Mode.

In the FIFO Polled Mode, there is no timeout condition indicated or trigger level reached. The RCVR and XMIT FIFOs still have the capability of holding characters, however.

TABLE 5. BAUD RATES (1.8432 MHz CLOCK)

Baud Rate Desired	Divisor Used to Generate 16 x Clock	Percent Error Difference Between Desired and Actual
50	2304	—
75	1536	—
110	1047	0.026
134.5	857	0.058
150	768	—
300	384	—
600	192	—
1200	96	—
1800	64	—
2000	58	0.69
2400	48	—
3600	32	—
4800	24	—
7200	16	—
9600	12	—
19200	6	—
38400	3	—
56000	2	2.86

TABLE 6. BAUD RATES (3.072 MHz CLOCK)

Baud Rate Desired	Divisor Used to Generate 16 x Clock	Percent Error Difference Between Desired and Actual
50	3840	—
75	2560	—
110	1745	0.026
134.5	1428	0.034
150	1280	—
300	640	—
600	320	—
1200	160	—
1800	107	0.312
2000	96	—
2400	80	—
3600	53	0.628
4800	40	—
7200	27	1.23
9600	20	—
19200	10	—
38400	5	—

TABLE 7. BAUD RATES (8 MHz CLOCK)

Baud Rate Desired	Divisor Used to Generate 16 x Clock	Percent Error Difference Between Desired and Actual
50	1000	—
75	6667	0.005
110	4545	0.010
134.5	3717	0.013
150	3333	0.010
300	1667	0.020
600	833	0.040
1200	417	0.080
1800	277	0.080
2000	250	—
2400	208	0.160
3600	139	0.080
4800	104	0.160
7200	69	0.644
9600	52	0.160
19200	26	0.160
38400	13	0.160
56000	9	0.790
128000	4	2.344
256000	2	2.344
512000	1	2.400

TABLE 8. MASTER RESET

Register/Signal	Reset Control	Reset
Interrupt Enable Register	Reset	All Bits Low (0-3 Forced and 4-7 Permanent)
Interrupt Identification Register	Reset	Bit 0 is High, Bits 1 and 2 Low Bits 3-7 Are Permanently Low
Line Control Register	Reset	All Bits Low
Modem Control Register	Reset	All Bits Low
FIFO Control Register	Reset	All Bits Low
Line Status Register	Reset	All Bits Low, Except Bits 5 and 6 Are High
Modem Status Register	Reset	Bits 0-3 Low Bits 4-7 Input Signal
SOUT	Reset	High
Intrpt (RCVR Errs)	Read LSR/Reset	Low
Intrpt (RCVR Data Ready)	Read RBR/Reset	Low
Intrpt (THRE)	Read IIR/Write THR/Reset	Low
Intrpt (Modem Status Changes)	Read MSR/Reset	Low
–OUT2	Reset	High
–RTS	Reset	High
–DTR	Reset	High
–OUT1	Reset	High

TABLE 9. SERIAL CHANNEL ACCESSIBLE REGISTERS

Address	Register Mnemonic	Register Bit Number							
		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	RBR (Read Only)	Data Bit 7 (MSB)	Data Bit 6	Data Bit 5	Data Bit 4	Data Bit 3	Data Bit 2	Data Bit 1	Data Bit 0 (LSB)
0	THR (Write Only)	Data Bit 7	Data Bit 6	Data Bit 5	Data Bit 4	Data Bit 3	Data Bit 2	Data Bit 1	Data Bit 0
0*	DLL	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
1*	DLM	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
1	IER	0	0	0	0	(EMSI) Enable Modem Status Interrupt	(ERLSI) Enable Receiver Line Status Interrupt	(EMREI) Enable Transmitter Holding Register Empty Interrupt	(ERDAI) Enable Received Data Available Interrupt
2	FCR (Write Only)	RCVR Trigger (MSB)	RCVR Trigger (LSB)	Reserved	Reserved	DMA Mode Select	XMIT FIFO Reset	RCVR FIFO Reset	FIFO Enable
2	IIR (Read Only)	FIFOs Enabled**	FIFOs Enabled**	0	0	Interupt ID Bit (2)**	Interrupt ID Bit (1)	Interrupt ID Bit (0)	"0" If Interrupt Pending
3	LCR	(DLAB) Divisor Latch Access Bit	Set Break	Stick Parity	(EPS) Even Parity Select	(PEN) Parity Enable	(STB) Number of Stop Bits	(WLSB1) Word Length Select Bit 1	(WLSB0) Word Length Select Bit 0
4	MCR	0	0	0	Loop	Out 2	Out 1	(RTS) Request To Send	(DTR) Data Terminal Ready
5	LSR	Error in RCVR FIFO**	(TEMT) Transmitter Empty	(THRE) Transmitter Holding Register Empty	(BI) Break Interrupt	(FE) Framing Error	(PE) Parity Error	(OE) Overrun Error	(DR) Data Ready
6	MSR	(DCD) Data Carrier Detect	(RI) Ring Indicator	(DSR) Data Set Ready	(CTS) Clear to Send	(DDCD) Delta Data Carrier Detect	(TERI) Trailing Edge Ring Indicator	(DDSR) Delta Data Set Ready	(DCTS) Delta Clear to Send
7	SCR	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0

* DLAB = 1
**These bits are always 0 in the VL16C450 Mode.

PARALLEL PORT REGISTERS

The VL16C552's parallel port interfaces the device to a Centronics-style printer. When Chip Select 2 (–CS2) is low, the parallel port is selected. Table 11 shows the registers associated with this parallel port. The read or write function of the register is controlled by the state of the read (–IOR) and write (–IOW) pin as shown. The Read Data Register allows the microprocessor to read the information on the parallel bus.

The Read Status Register allows the microprocessor to read the status of the printer in the five most significant bits. The status bits are Printer Busy (–BSY), Acknowledge (–ACK) which is a handshake function, Paper Empty (PE), Printer Selected (SLCT), and Error (–ERR). The Read Control Register allows the state of the control lines to be read. The Write Control Register sets the state of the control lines.

They are Interrupt Enable (PIRQEN), Select In (SLIN), Initialize the Printer (–INIT), Autofeed the Paper (AFD), Strobe (STB), which informs the printer of the presence of a valid byte on the parallel bus. The Write Data Register allows the microprocessor to write a byte to the parallel bus.

The parallel port is completely compatible with the parallel port implementation used in the IBM Serial/Parallel Adaptor.

TABLE 10. PARALLEL PORT REGISTERS

Register	Register Bits							
	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Data	PD7	PD6	PD5	PD4	PD3	PD2	PD1	PD0
Status (Read Only)	–BSY	–ACK	PE	SLCT	–ERR	–PIRQ	1	1
Control	1	1	DIR	PIRQEN	SLIN	–INIT	AFD	STB

TABLE 11. PARALLEL PORT REGISTER SELECT

Control Pins			Register Selected
–CS2	A1	A0	
0	0	0	Read Data
0	0	1	Read Status
0	1	0	Read Control
0	1	1	Invalid

LINE PRINTER PORT:
The Line Printer Port (LPT) contains the functionality of the port included in the VL16C552, but offers a hardware programmable Extended Mode, controlled by the Printer Enhancement Mode (PEMD) pin. This enhancement is the addition of a Direction Control Bit, and an Interrupt Status Bit.

Reg 0 - Line Printer Data Register:
The Line Printer Port is either output-only or bidirectional, depending on the state of the Extended Mode pin and Data Direction Control bits.

Compatibility Mode (PEMD pin=0): Reads to the Line Printer Data (LPD) Register and returns the last data that was written to the port. Write operations immediately output data to the PD0-PD7 pins.

Extended Mode (PEMD pin=1): Read operations return either the data last written to the LPD Register if the direction bit is set to write (low) or the data that is present on PD0-PD7 if the direction is set to read (high). Writes to the LPD Register latch data into the output register, but only drive the LPT port when the direction bit is set to write.

The table below summarizes the possible combinations of Extended Mode and the direction control bit.

PEMD	DIR	PD0-PD7 Function
0	X	PC/AT Mode - Output
1	0	PS/2 Mode - Output
1	1	PS/2 Mode - Input

Reg 1 Read - Line Printer Status Register:
The Line Printer Status (LPS) Register is a read-only register that contains interrupt and printer status of the LPT connector pins. In the table below (in the default column), are the values of each bit in the case of the printer being disconnected from the port. The bits are described as follows:

Bit	Description	Default
0	Reserved	1
1	Reserved	1
2	–PIRQ	1
3	–ERR	1
4	SLCT	1
5	PE	1
6	–ACK	1
7	–BSY	0

Bits 0 and 1 - Reserved. Read as ones.

Bit 2 - Printer Interrupt (–PIRQ, active low) Status bit, when set (low) indicates that the printer has acknowledged the previous transfer with a ACK handshake (bit 4 of the control register must be set to 1). The bit is set to zero on the active to inactive transition of the –ACK signal. This bit is set to a one after a read from the status port. The default (power on reset) value for this bit is one.

Bit 3 - Error (–ERR, active low) Status bit corresponds to –ERR input.

Bit 4 - Select (SLCT) Status bit corresponds to SLCT input.

Bit 5 - Paper Empty (PE) Status bit corresponds to PE input.

Bit 6 - Acknowledge (–ACK, active low) Status bit corresponds to –ACK input.

Bit 7 - Busy (–BSY, active low) Status bit corresponds to BUSY input.

Reg 2 - Line Printer Control Register:
The Line Printer Control (LPC) register is a read/write port that is used to control the PD0-PD7 direction and drive the Printer Control lines. Write operations set or reset these bits, while read operations return the state of the last write operation to this register. The bits in this register are defined as follows:

Bit	Description
0	STB
1	AFD
2	–INIT
3	SLIN
4	PIRQEN
5	DIR
6	Reserved (1)
7	Reserved (1)

Bit 0 - Printer Strobe (STB) Control bit; when one, the –STB signal is asserted on the LPT interface; when zero, the signal is negated.

Bit 1 - Auto Feed (AFD) Control bit; when one, the –AFD signal will be asserted on the LPT interface; when zero, the signal is negated.

Bit 2 - Initialize Printer (–INIT) Control bit; when one, the –INIT signal is negated; when zero, the –INIT signal is asserted on the LPT interface.

Bit 3 - Select Input (SLIN) Control bit; when one, the SLCT signal is asserted on the LPT interface; when zero, the signal is negated.

Bit 4 - Interrupt Request Enable (PIRQEN) Control bit; when one, enables interrupts from the LPT port whenever a low to high transition of –ACK occurs; when zero, diables interrupts.

Bit 5 - Direction (DIR) Control bit (only used when –PEMD is high); when one, the output buffers in the LPT port are disabled allowing data driven from external sources to be read from the LPT port.

AC CHARACTERISTICS: TA = 0°C to +70°C, VDD = 5 V ±5%

Symbol	Parameter	Min	Max	Units	Conditions
tDIW	–IOR Strobe Width	125		ns	
RC	Read Cycle	280		ns	Note 3
tDD	–IOR to Drive Disable Delay		40	ns	100 pF Load (Note 2)
tDDD	Delay from –IOR to Data		110	ns	100 pF Load (Note 2)
tDW	Data Valid Width	0	100	ns	100 pF Load (Note 2)
tDOW	–IOW Strobe Width	100		ns	
WC	Write Cycle	280		ns	
tDS	Data Setup Time	30		ns	
tDH	Data Hold Time	25		ns	
tRA	Address Hold Time from –IOR	20		ns	Note 1
tRCS	Chip Select Hold Time from –IOR	20		ns	Note 1
tAR	Set up from Address to –IOR	30		ns	Note 1
tCSR	Set up from Chip Selects to –IOR	25		ns	Note 1
tWA	Address Hold Time from –IOW	20		ns	Note 1
tWCS	Chip Select Hold Time from –IOW	20		ns	Note 1
tAW	Set up from Address to –IOW	30		ns	Note 1
tCSW	Chip Select Hold Time from –IOW	25		ns	Note 1
tMRW	Master Reset Pulse Width	5		µs	
tXH	Duration of Clock High Pulse	55		ns	External Clock (8 MHz Max.)
tXL	Duration of Clock Low Pulse	55		ns	External Clock (8 MHz Max.)

Notes: 1. The internal address strobe is always active.
2. VOL, VOH and the external loading determine the charge and discharge time.
3. In FIFO Mode RC=425 ns (min.) between reads of the receiver FIFO and the status registers (IIR or LSR).

AC CHARACTERISTICS (Cont.): TA = 0°C to + 70°C, VDD = 5 V ±5%

Symbol	Parameter	Min	Max	Units	Conditions
Transmitter					
tHR1	Delay from Falling Edge of –IOW (WR THR) to Reset Interrupt		175	ns	100 pF Load
tIRS	Delay from Initial INTR Reset to Transmit Start	0	16	–BAUDOUT CYCLES	Note 3
tSI	Delay from Initial Write to Interrupt	8	24	–BAUDOUT CYCLES	Note 1, 3
tSTI	Delay from Start Bit Low to Interrupt (THRE) High	8	24	–BAUDOUT CYCLES	Note 1,3
tIR	Delay from –IOR (RD IIR) to Reset Interrupt (THRE)		250	ns	100 pF Load
tSXA	Delay from Start to –TXRDY Active	8	24	–BAUDOUT CYCLES	100 pF Load, Note 3
tWXI	Delay from Write to –TXRDY Inactive		195	ns	100 pF Load
Modem Control					
tMDO	Delay from –IOW (WR MCR) to Output		200	ns	100 pF Load
tSIM	Delay to Set Interrupt from Modem Input		250	ns	100 pF Load
tRIM	Delay to Reset Interrupt from –IOR (RD MSR)		250	ns	100 pF Load
Receiver					
tSCD	Delay from RCLK to Sample Time		2	µs	
tSINT	Delay from Sample of Stop to Set Interrupt		1	RCLK	Note 2
tRINT	Delay from –IOR (RD RBR/RD LSR) to Reset Interrupt		1	µs	100 pF Load
TRXI	Delay from –RDRBR to –RXRDY Inactive	290		ns	

Notes:
1. If the Transmitter Interrupt Delay is active, this delay will be lengthened by one character time, minus the last stop bit time.
2. The receiver data available indication, the overrun error indication, the trigger level interrupts and the active –RXRDY indication will be delayed three RCLKs in the FIFO Mode (FCR0=1). After the first byte has been received status indicators (PE, FE, BI) will be delayed three RCLKs. These indicators will be updated immediately for any further bytes received after RDRBR goes inactive. There are eight RCLK delays for trigger change level interrupts.
3. Baudout cycle defined as per Baud Rate Generator section.

FIGURE 3. READ TIMING

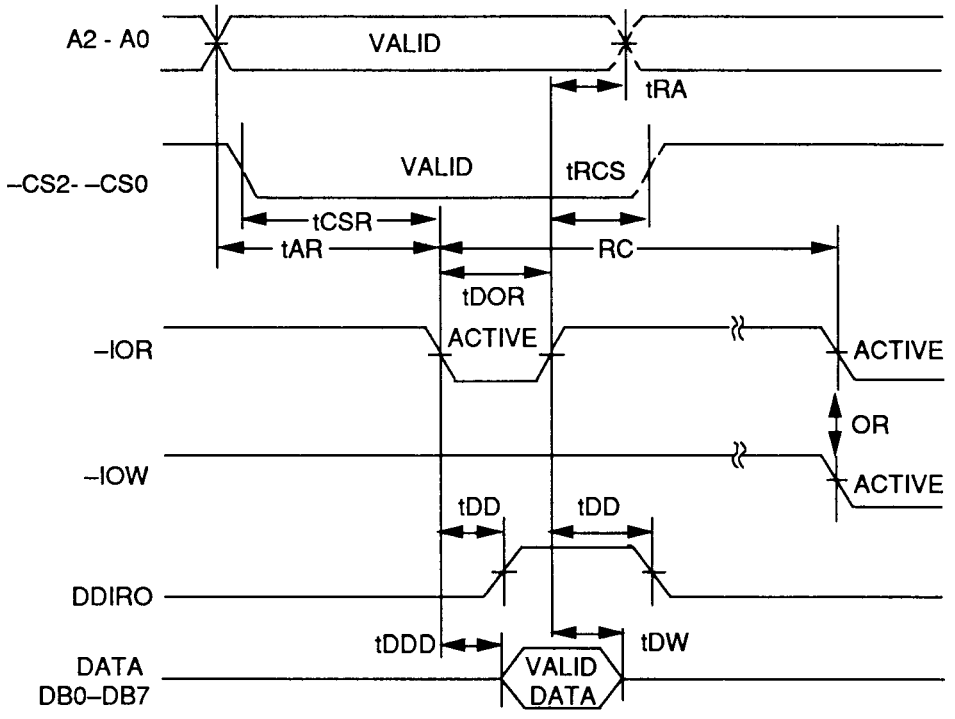


FIGURE 4. WRITE TIMING

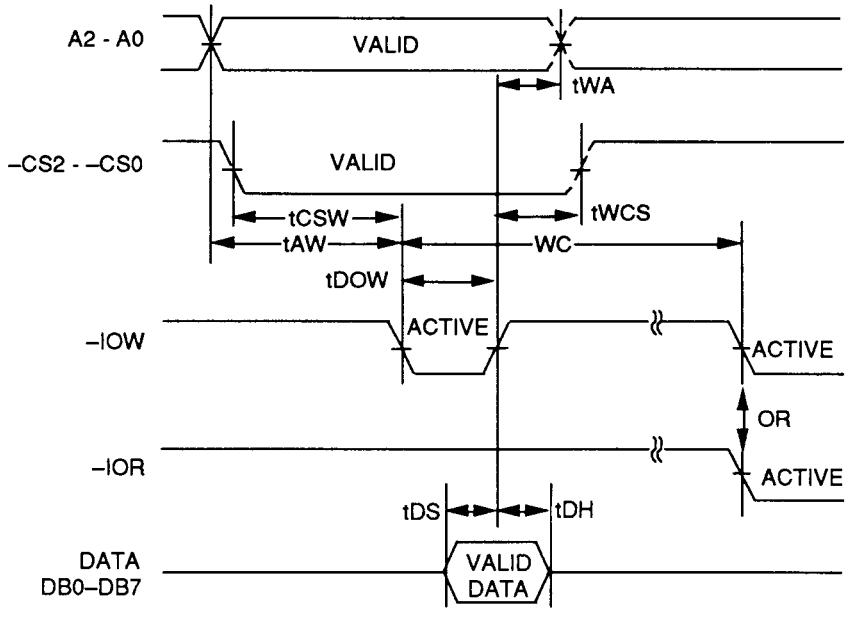


FIGURE 5. MODEM TIMING

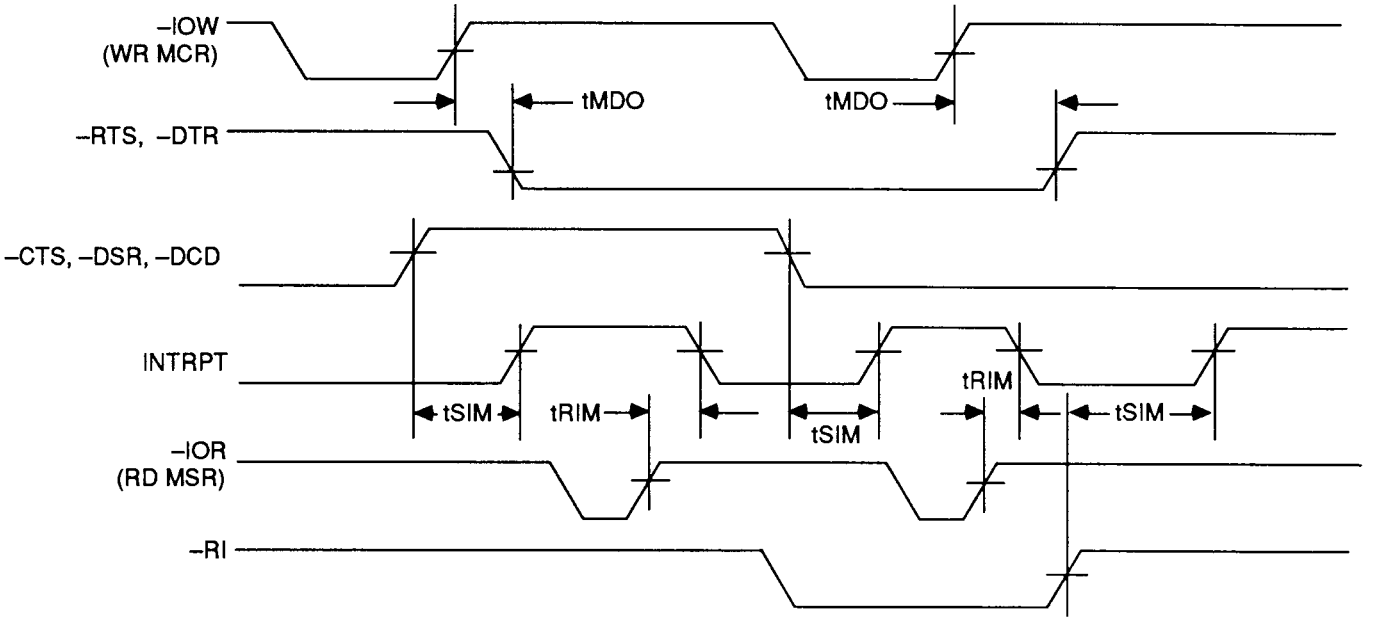
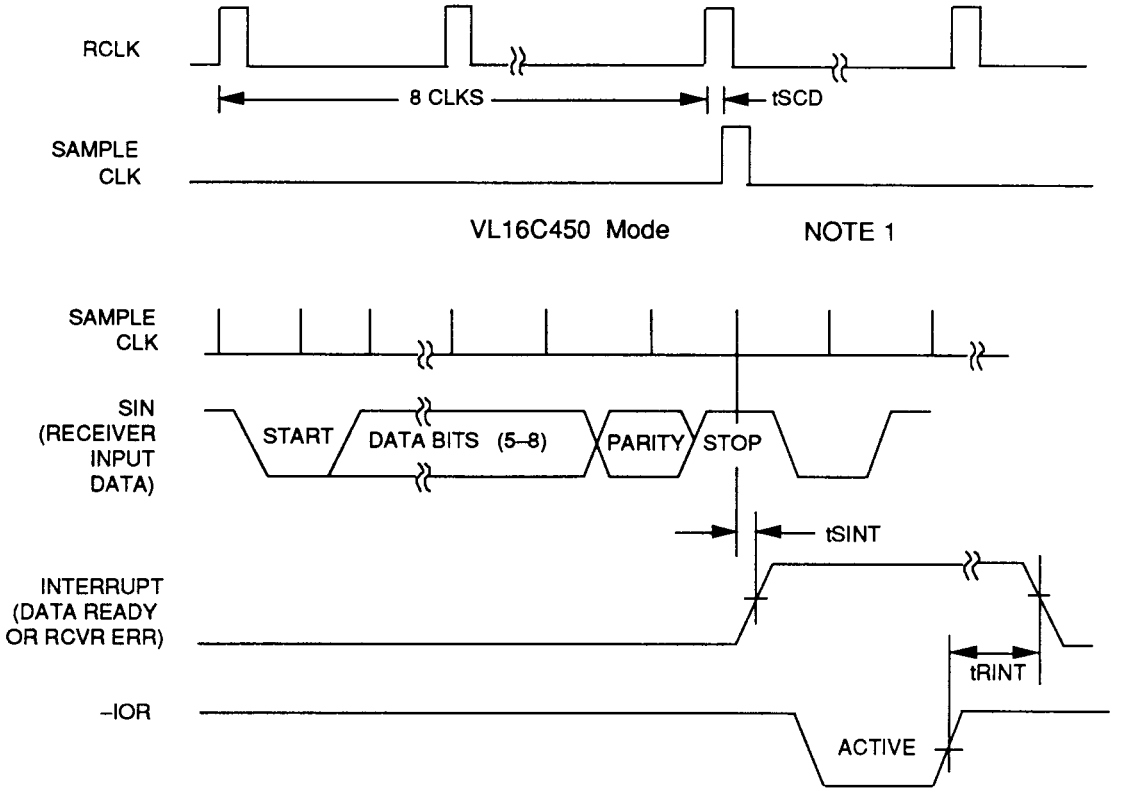


FIGURE 6. RECEIVER TIMING



Note 1: Start bit is sampled two times to ensure start is valid.

FIGURE 7. RECEIVER READY (PIN 29)-MODE 0

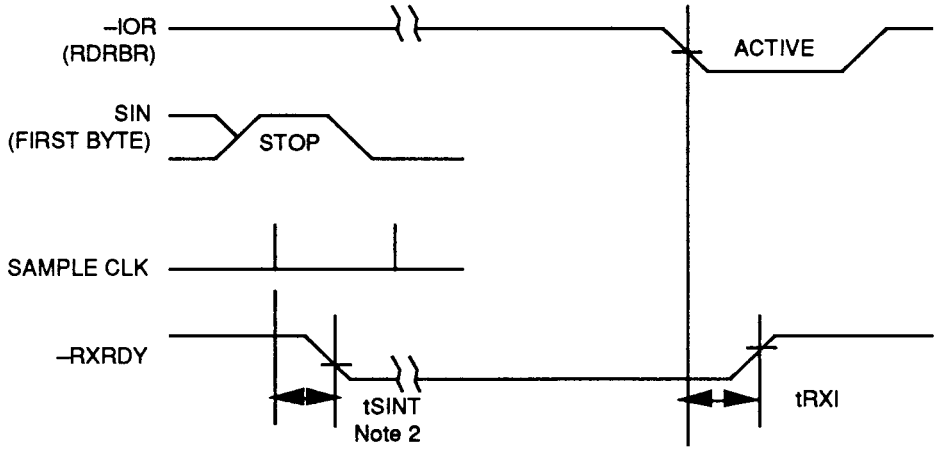
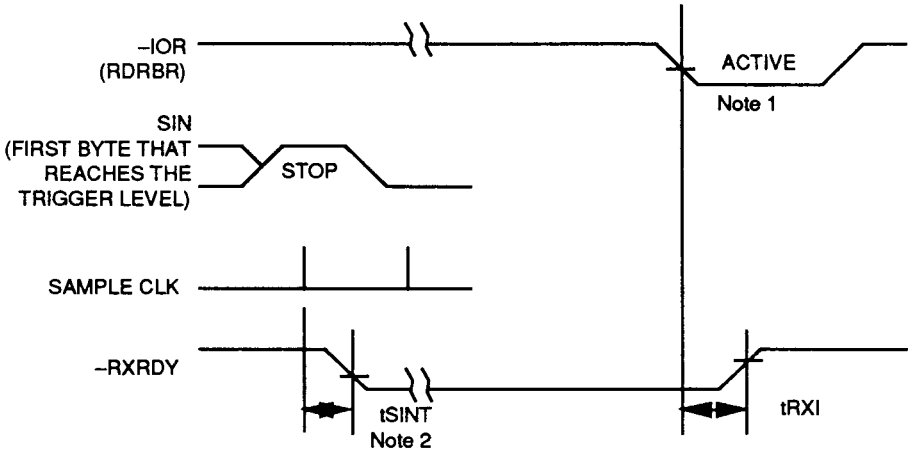


FIGURE 8. RECEIVER READY (PIN 29)-MODE 1



Notes: 1. This is the reading of the last byte in the FIFO.
2. If FCR0=1, then tSINT=3 RCLKs. For a trigger change level interrupt, tSINT=8 RCLKs.

FIGURE 9. TRANSMITTER TIMING

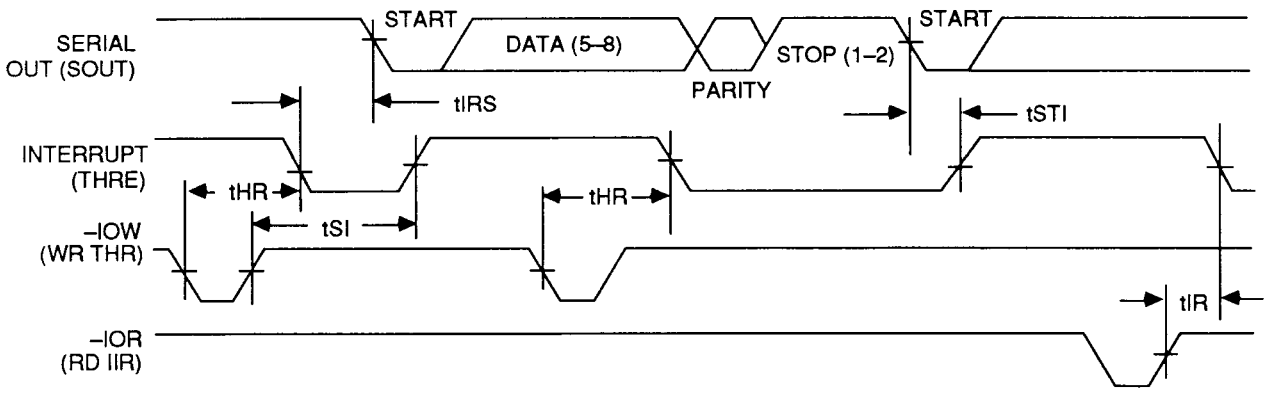


FIGURE 10. TRANSMITTER READY (PIN 24)-MODE 0

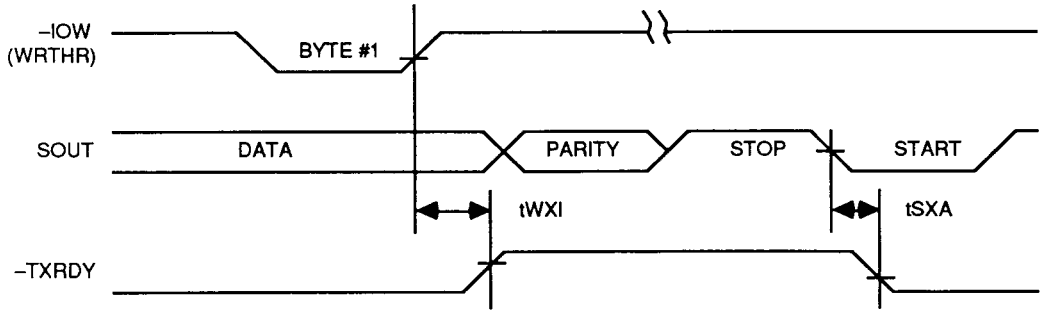


FIGURE 11. TRANSMITTER READY (PIN 24)-MODE 1

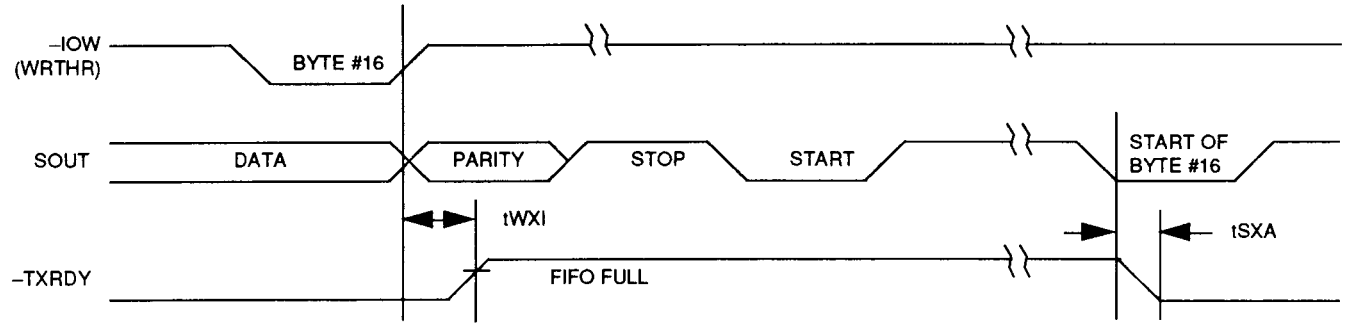


FIGURE 12. RCVR FIFO FIRST BYTE (This sets RDR.)

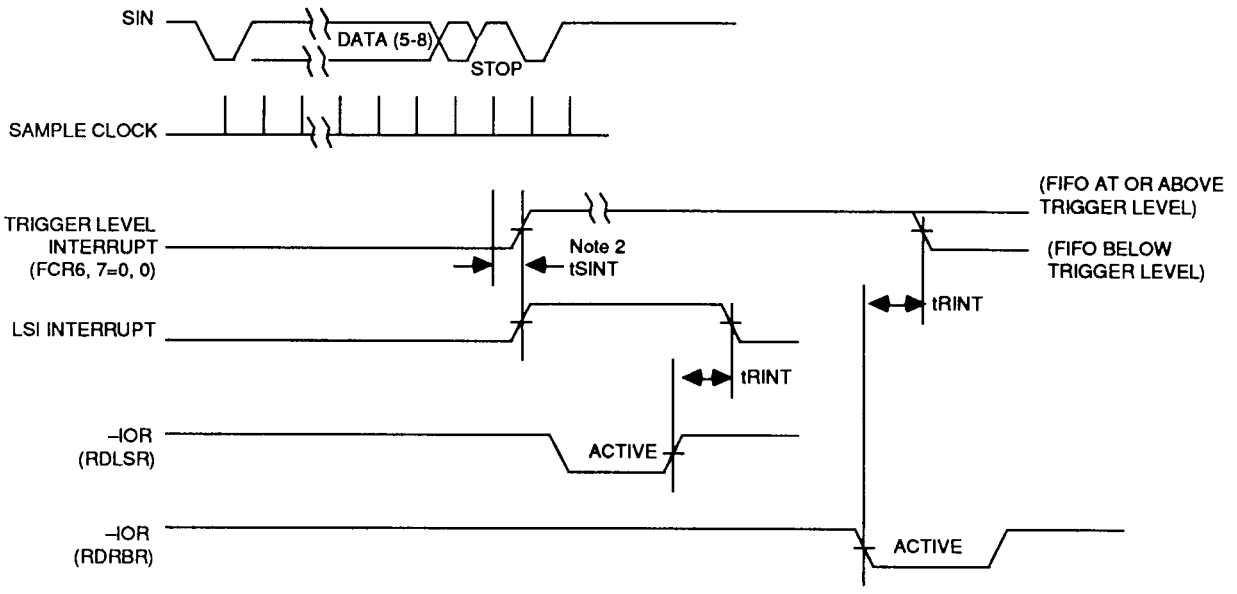
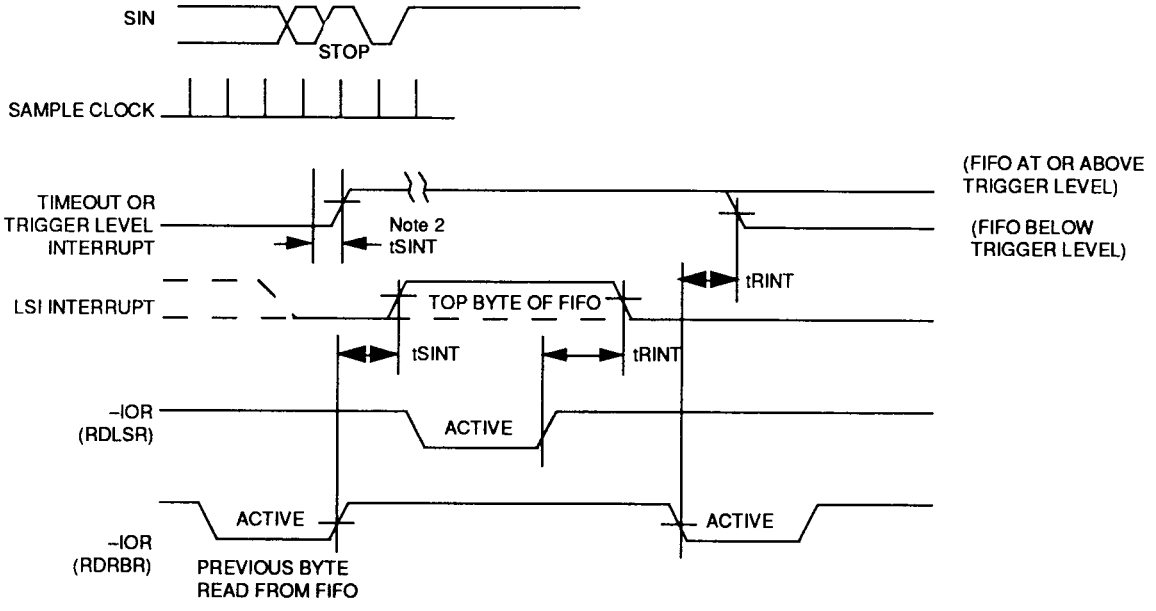


FIGURE 13. RCVR FIFO REMAINING BYTES (RDR is already set.)



Notes: 1. This is the reading of the last byte in the FIFO.
2. If FCR0=1, then tSINT=3 RCLKs. For a trigger change level interrupt, tSINT=8 RCLKs.

FIGURE 14. TEST CIRCUIT

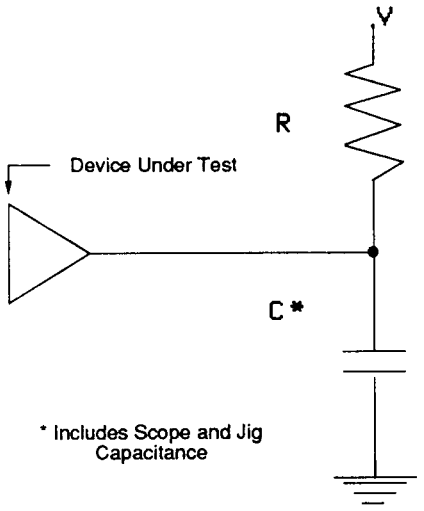
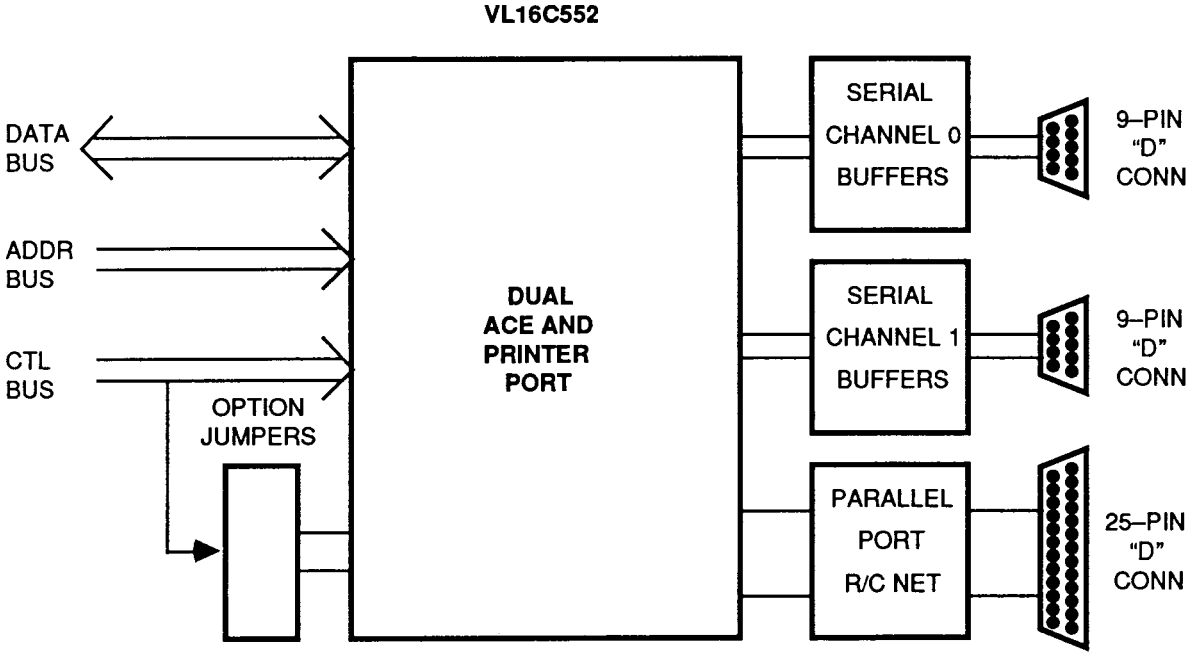


FIGURE 14. BASIC CONFIGURATION



ABSOLUTE MAXIMUM RATINGS

Ambient Operating Temperature	–10°C to +70°C
Storage Temperature	–65°C to +150°C
Supply Voltage to Ground Potential	–0.5 V to VDD +0.3 V
Applied Output Voltage	–0.5 V to VDD +0.3 V
Applied Input Voltage	–0.5 V to +7.0 V
Power Dissipation	500 mW

Stresses above those listed may cause permanent damage to the device. These are stress ratings only. Functional operation of this device at these or any other conditions above those indicated in this data sheet is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

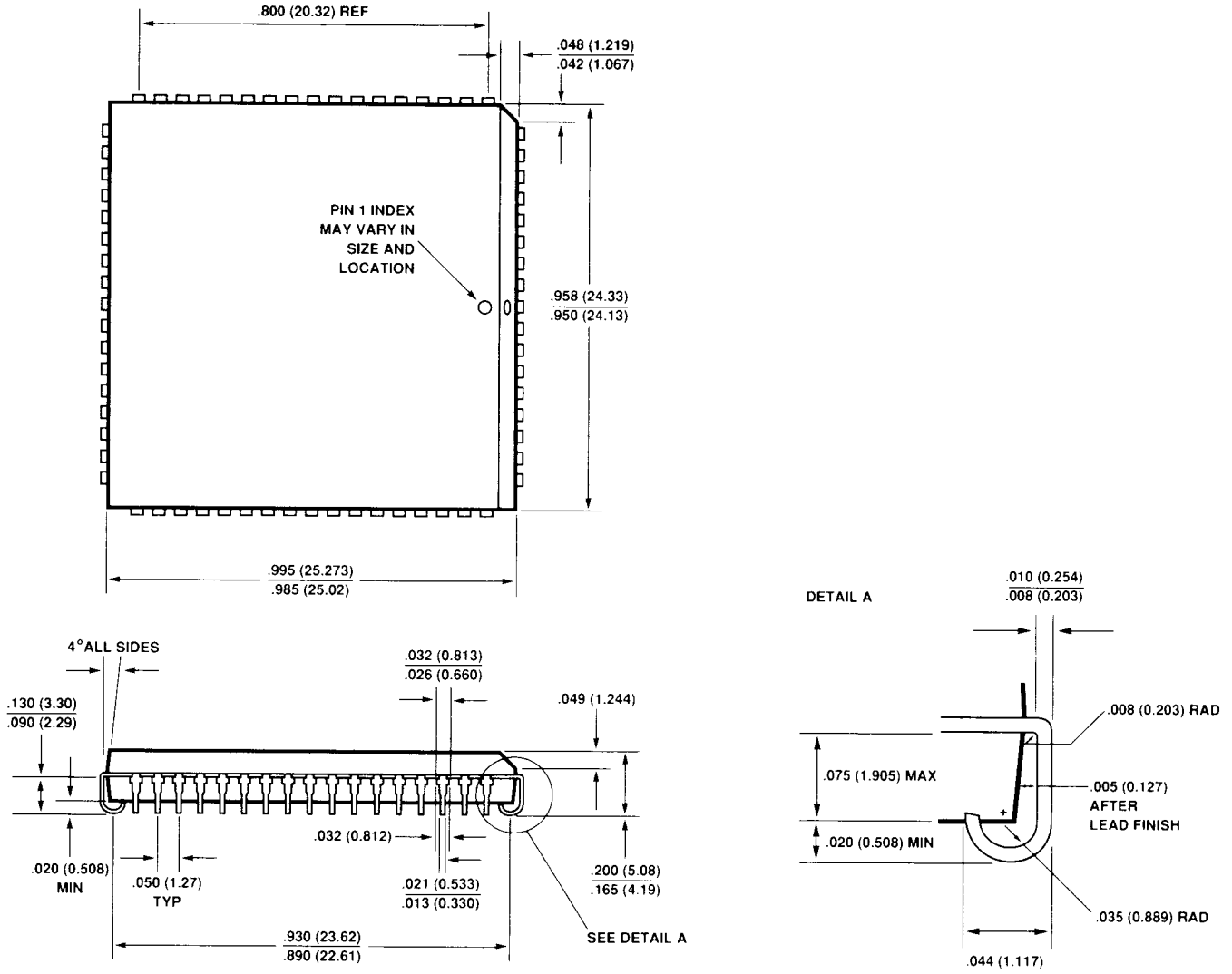
DC CHARACTERISTICS: TA = 0°C to +70°C, VDD = 5 V ±5%

Symbol	Parameter	Min	Max	Units	Conditions
VIL	Input Low Voltage	–0.5	0.8	V	
VIH	Input High Voltage	2.0	VDD	V	
VOL	Output Low Voltage		0.4	V	IOL = 4.0 mA on DB0 - DB7 IOL = 12 mA on PD0 - PD7 IOL = 10 mA on –INIT, –AFD, –STB, and –SLIN (see Note 1) IOL = 2.0 mA on all other outputs
VOH	Output High Voltage	2.4		V	IOH = –0.4 mA on DB0 - DB7 IOH = –2.0 mA on PD0 - PD7 IOH = –100 µA on –INIT, –AFD, –STB, –SLIN, –TXRDY1, –TXRDY0, –RXRDY1 and –RXRDY0 IOH = –0.2 mA on all other outputs
IDD	Power Supply Current		50	mA	VDD = 5.25 V. No loads on SIN0,1; –DSR0,1; –DCD0,1; –CTS0,1. –RI0, –RI1 = 2.0 V. Other inputs = 0.8 V. Baud rate generator = 8 MHz. Baud rate = 56K
IIL	Input Leakage		±10	µA	VDD = 5.25 V, VSS = 0 V. All other pins floating.
IOZ	Three-State Leakage		±20	µA	VDD = 5.25 V, VSS = 0 V. VOUT = 0 V, 5.25 V 1) Chip deselected 2) Chip and write mode selected

Note 1: Open drain pads used. VOH not tested, as it is dependant upon external pull-up value.

PACKAGE OUTLINE:

68-PIN PLASTIC LEADED CHIP CARRIER (PLCC)



NOTES: UNLESS OTHERWISE SPECIFIED.
1. TOLERANCE TO BE +/- .005 (0.127).
2. LEADFRAME MATERIAL: COPPER.
3. LEAD FINISH: MATTE TIN PLATE OR SOLDER DIP.
4. SPACING TO BE MAINTAINED BETWEEN FORMED LEAD AND MOLDED PLASTIC ALONG FULL LENGTH OF LEAD.
5. MOLDED PLASTIC DIMENSION DOES NOT INCLUDE SIDE FLASH BURR, WHICH IS .010 (0.254) MAX ON FOUR SIDES.
6. CONTROLLING DIMENSIONS ARE METRIC, ALL METRIC DIMENSIONS ARE IN PARENTHESES.

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