VL16C451/VL16C451B

PARALLEL/ASYNCHRONOUS COMMUNICATIONS ELEMENT

FEATURES

- IBM PC/AT-compatible and National NS16450-compatible
- VL16C450 with on-board Centronics printer interface
- VL16C451B is completely pin- and upward-compatible with the Dual Serial Channel VL16C451

  Direct drive of interrupt request signals on slot-bus
- Enhanced bidirectional parallel data port (VL16C451B only)
- Crystal and oscillator clock inputs (VL16C451B only)
- General purpose input/output port (VL16C451B only)
- Three-state control pin and in-circuit-test feature for board level testability (VL16C451B only)
- Programmable serial interface characteristics:
  - 5-, 6-, 7- or 8-bit characters
  - Even-, odd- or no-parity bit generation and detection
  - 1, 1 1/2 or 2 stop bit generation
- Three-state TTL drive for the data and control bus

DESCRIPTION

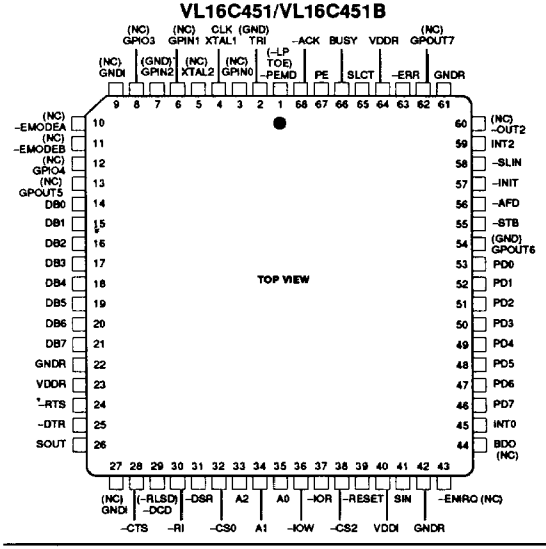
The VL16C451B is an enhanced version of the popular VL16C450 asynchronous communications element (ACE). The serial channel performs serial-to-parallel conversion on data characters received from peripheral devices or modems, and parallel-to-serial conversion on data characters transmitted by the CPU. The complete status of the Parallel/Asynchronous Communications Element (P/ACE) can be read at any time during functional operation by the CPU. The information obtained includes the type and condition of the transfer operation being performed, and error conditions. It is fully pin- and upward-compatible with the dual serial channel VL16C452/VL16C452B.

The VL16C451B also provides the user with a fully bidirectional parallel data port that fully supports the parallel Centronics interface. The parallel port, together with the serial port, provide IBM PC/AT-compatible computers with a single device to serve the two system ports.

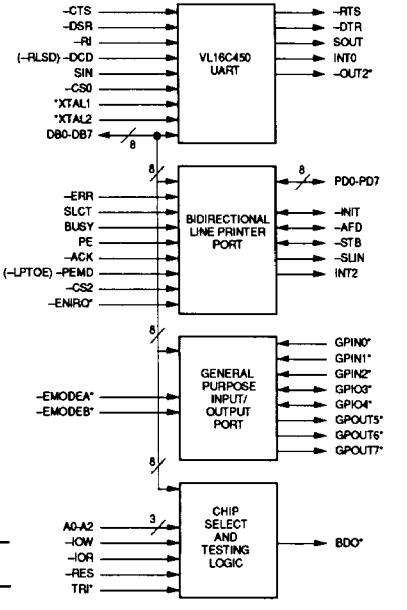
A programmable baud rate generator is included that can divide the timing reference clock input by a divisor between 1 and (2^{16} –1).

The VL16C451/VL16C451B is housed in a 68-pin plastic leaded chip carrier.

PIN DIAGRAM



BLOCK DIAGRAM



* VL16C451B only

VL16C451 pin names are in parenthesis.

ORDER INFORMATION

Part Number	Maximum Clock Frequency	Package
VL16C451-QC	3.1 MHz	Plastic Leaded Chip Carrier (PLCC)
VL16C451B-QC	8 MHz	Plastic Leaded Chip Carrier (PLCC)

Note: Operating temperature range is 0°C to +70°C.

SIGNAL DESCRIPTIONS (VL16C451 signal names are shown in parenthesis.)

Signal Name	Pin Number	Signal Type	Signal Description
–RTS	24	O7	Request To Send output (three-state, active low) - This signal is asserted to indicate the UART is ready to transmit data to an external modem. In half duplex applications the –RTS line is used to control the transmission direction. The signal is negated on reset.
–DTR	25	O7	Data Terminal Ready output (three-state, active low) - This signal is asserted to indicate the UART is ready to receive data. The signal is negated on reset.
SOUT	26	O7	Serial Output (three-state, active low) - SOUT is the data output of the UART. This signal is negated whenever the transmitter is disabled, –RES is active, the Transmitter Register is empty, or the UART is in Loop Mode.
–CTS	28	I1	Clear To Send input (active low) - This signal is a status line from the external modem to indicate that it is ready to transmit data. A change is status of this line sets the Delta CTS bit in the Modem Status Register.
–DSR	31	I1	Data Set Ready input (active low) - –DSR is a status line indicating that the external modem is ready to transfer data to/from the UART. A change in status of this line sets the Delta DSR bit in the Modem Status Register.
–DCD (–RLSD)	29	I1	Data Carrier Detect input (active low) - This signal is used to indicate that the external modem has detected a carrier. If the –RI line changes state while the modem status interrupts are enabled, an interrupt will be generated.
–RI	30	I1	Ring Indicator input (active low) - This signal is used to indicate that the telephone ring signal has been detected by an external modem. The modem status register TERI bit is used to indicate that a Trailing Edge of the Ring Indicator has been detected. If modem status interrupts are enabled when this occurs, an interrupt will be generated.
SIN	41	I1	Serial Input (active low) - This is the data input to the UART. This input is ignored when Loop Mode is enabled.
INT0	45	O5	Gated Interrupt Request (three-state, active high output) - This signal is asserted whenever the UART attempts to generate an interrupt. This signal is negated upon an interrupt being serviced. This signal is enabled/ three-stated by setting the Interrupt Enable (bit 3) signal in the Modem Control Register. This signal is suitable for directly driving the SIRQ signal on the slot-bus of the PC/AT.
–CS0	32	I1	Chip Select input (active low) - –CSO is used to indicate that an access is being made to the UART registers.
–OUT2 (NC)	60	O4	Output - User defined output for modem control logic that can be set to an active low by programming bit 3 of the Modem Control Register to a high level. This signal is cleared (high) by writing a logic 0 to the –OUT2 bit (MCR) or whenever a reset occurs. In PC/AT or PS/2 applications, this signal normally indicates that the SIO interrupts have been enabled for system level interrupts.
PARALLEL PRINTER PORT:			
PD0	53	IO5	Printer data port bit 0 - These signals, PD0-PD7 provide a bidirectional eight-bit I/O port usually connected to a printer. These lines are driven when the PEMD signal is negated (low) or when PEMD is asserted and the direction control bit is set to 0 (write).
PD1	52	IO5	Printer data port bit 1.
PD2	51	IO5	Printer data port bit 2.

SIGNAL DESCRIPTIONS (Cont.)

Signal Name	Pin Number	Signal Type	Signal Description
PD3	50	IO5	Printer data port bit 3.
PD4	49	IO5	Printer data port bit 4.
PD5	48	IO5	Printer data port bit 5.
PD6	47	IO5	Printer data port bit 6.
PD7	46	IO5	Printer data port bit 7.
–INIT	57	O4	Printer Command Initialize - This is an active low, open drain signal that is used to issue an initialize command to the printer.
–AFD	56	O4	Printer Command Autofeed - This is an active low, open drain signal that is used to issue an autofeed command to the printer.
–STB	55	O4	Printer Command Data Strobe - This is an active low, open drain signal that is used to latch the parallel data into the printer.
–SLIN	58	O4	Printer Command Select - This is an active low, open drain signal that is used to issue a select command to the printer.
–ERR	63	I3	Printer Status Error input - This signal is used to monitor the printer for error reporting. This pin will float high with no input connected.
SLCT	65	I3	Printer Status Select input - SLCT is used to indicate when the printer is on-line (selected). This pin will float high with no input connected.
BUSY	66	I3	Printer Status Busy input - BUSY is used to indicate when the printer is busy and cannot receive data. This pin will float high with no input connected.
PE	67	I3	Printer Status Paper Empty input - PE is used to indicate that the printer is out of paper. This pin will float high with no input connected.
–ACK	68	I3	Printer Status ACK input - This signal is used as a handshake signal from the printer indicating the last transaction has completed. An interrupt is generated by a low-to-high transition on this signal. This pin will float high with no input connected.
INT2	59	O5	Printer Interrupt Request (three-state, active high output) - This signal is asserted whenever the –ACK signal is asserted. This signal is enabled/three-stated by setting the Interrupt Enable (bit 4) signal in the Printer Control Register. This signal is suitable for directly driving the INT2 signal on the slot-bus of the PC/AT. This pin is also used during Test Mode. (See the description of the TEST signal below.)
PEMD	1	I1	Printer Enhancement Mode - When asserted (high) this signal enables the bidirectional printer port capabilities. When negated (low) the printer port is output only (PC/AT-compatible).
(–LPTOE)	1	I1	(VL16C451 only) Parallel Data Output Enable - When low, this signal enables the Write Data Register to the PD0-PD7 lines. A high puts the PD0-PD7 lines in the high-impedance state allowing them to be used as inputs. –LPTOE is usually tied low for printer operation.
–CS2	38	I1	Parallel Port Select input - –CS2 is used to indicate that an access is being directed to the printer port registers.
–ENIRQ (NC)	43	I1	Parallel Port Interrupt Source Mode Selection - When negated (low), the AT mode of interrupts is selected. In this mode, the –ACK input is internally connected to the INT2 output. If the –ENIRQ input is tied high, the interrupt source will be held in a latched state until the Status Register is read which will then reset the INT2 output.

SIGNAL DESCRIPTIONS (Cont.)

Signal Name	Pin Number	Signal Type	Signal Description
COMMON CONTROL SIGNALS:			
–IOR	37	I1	I/O Read Strobe input (active-low) is used to drive data from the VL16C451B to the data bus (DB0-DB7). The output data depends on the register selected by the address inputs A0, A1, A2 and the Chip Selects (CS0 for the UART, and CS2 for the Printer Port).
–IOW	36	I1	I/O Write Strobe input (active low) - This signal is used to latch data into the VL16C451B from the data bus (DB0-DB7). The input data depends on the register selected by the address inputs A0, A1, A2 and the Chip Selects (CS0 for the UART, and CS2 for the Printer Port).
DB0	14	IO6	Data I/O Bits 0-7 (three-state, active high) - These are lines used to interface to the slot bus. These signals are normally high impedance except during read cycles. Data bit 0 is the least significant bit.
DB1	15	IO6	Data I/O signal.
DB2	16	IO6	Data I/O signal.
DB3	17	IO6	Data I/O signal.
DB4	18	IO6	Data I/O signal.
DB5	19	IO6	Data I/O signal.
DB6	20	IO6	Data I/O signal.
DB7	21	IO7	Data I/O signal (MSB).
A0	35	I1	Address line inputs - A0-A2 are used to decode which register is selected during CPU accesses to the VL16C451B.
A1	34	I1	Address line input.
A2	33	I1	Address line input.
XTAL1 (CLK)	4	I1	Crystal Input 1 or External Clock input - This is used for the UART baud rate generator.
XTAL2 (NC)	5	I1	Crystal Input 2 - XTAL2 may be tied to VCC, GND or left open if an external clock source is tied to XTAL1.
–RES (–RESET)	39	I1	Reset input (active low) - This signal is used to force the VL16C451B into an idle state with all serial transfers suspended. The Modem Control Register and Line Status Register are both initialized.
BDO (NC)	44	O7	Bus Drive Output (three-state, active high) - BDO is used to indicate to external octal transceivers that the VL16C451B is driving the data pins. It can be directly connected to the direction pin of a 74LS245.
–EMODEA (NC)	10	I3	Enhanced Mode Select A - This input signal is used in conjunction with the –EMODEB signal to configure the General Purpose I/O port. The GPIO port can be configured as follows:

EMODE A	EMODE B	GPIN0-GPIN2	GPIO3	GPIO4	GPOUT5-GPOUT7
H	H	NC	NC	NC	NC
H	L	IN	IN	OUT	OUT
L	H	IN	OUT	OUT	OUT
L	L	IN	IN	IN	OUT

SIGNAL DESCRIPTIONS (Cont.)

Signal Name	Pin Number	Signal Type	Signal Description
–EMODEB (NC)	11	I3	Enhanced Mode Select B input.
GENERAL PURPOSE I/O PORT:			
GPIN0 (NC)	3	I3	General Purpose Input Port Bit 0 (LSB) - This signal if enabled as an input via the –EMODEA and –EMODEB configuration inputs can be read at bit 0 of the General Purpose I/O (PGIO) Port Register. It can be tied to GND, VCC or left open if not used. This pin will float high with no input connected.
GPIN1 (NC)	6	I3	General Purpose Input Port Bit 1 - Read at bit 1 GPIO Port Register if enabled.
GPIN2 (GND)	7	I3	General Purpose Input Port Bit 2 - Read at bit 2 GPIO Port Register if enabled.
GPIO3 (NC)	8	IO5	General Purpose Input/Output Port Bit 3 - This signal can be configured to be an input or an output control bit via the –EMODEA and –EMODEB configuration inputs. If the signal is configured as an output it is initially reset to a 0 (low) state when –RES is asserted. It can be set high by programming bit 3 of the GPIO Port Register to a 1. It will be set low by programming bit 3 to a 0. If configured as an input, it can be read at bit 3 of the GPIO Port. If the bit is changed from an output port to an input port and then subsequently back to an output port, its initial state will always be reset to a logical 0 (low).
GPIO4 (NC)	12	IO5	General Purpose Input/Output Port Bit 4 - Set or read at bit 4 of the GPIO Port.
GPOUT5 (NC)	13	O4	General Purpose Output Port Bit 5 - This signal is configured as an output control bit via the –EMODEA and –EMODEB configuration inputs. If the signal is configured as an output it is initially reset to a 0 (low) state when –RES is asserted. It can be set high by programming bit 5 of the GPIO Port Register to a 1. It will be set low by programming bit 5 to a 0.
GPOUT6 (GND)		54	O4 General Purpose Output Port Bit 6 - This bit is set or cleared by writing bit 5 of the GPIO Port Register.
GPOUT7 (NC)	62	O4	General Purpose Output Port Bit 7 (MSB) - This bit is set or cleared by writing bit 7 of the GPIO Port Register.

POWER BUSSING:

The power connections to the VL16C451B are split into an internal supply for the logic, and a ring supply for the I/O drivers. Each supply should be individually bypassed with decoupling capacitors.

VDDR	23, 64	Ring Power Supply - +5 V
VDDI	40	Internal Power Supply - +5 V
GNDR	22, 42, 61	Ring Ground
GNDI	9, 27	Internal Ground

TEST MODE PINS:

The three test modes which are supported by the VL16C451B are:

Component	The Component Test Mode is selected when –IOW and –IOR are simultaneously taken low when DB0 is low, DB1 is high and TRI is high. The mode is used to put the VL16C451B into a component level test mode.
In-Circuit	The In-circuit Test Mode is selected when –IOW and –IOR are simultaneously taken low when DB1 is low, DB0 is high and TRI is high. This mode is normally used to confirm that the VL16C451B has been physically attached to the printed circuit board.

SIGNAL DESCRIPTIONS (Cont.)

Three-State The Three-state Test Mode is entered when the TRI input is taken high. This mode is used to control the three-state control of all I/O and output pins. When this mode is selected, all I/O and outputs become high impedance, allowing board level testers to drive the outputs without overdriving internal buffers.

Each of these test modes are selected by driving a combination of pins into the desired mode.

Signal Name	Pin Number	Signal Type	Signal Description
TRI (GND)	2	I4	This pin is used to control the three-state control of all I/O and output pins. When this pin is asserted, all I/O and outputs become high impedance, allowing board level testers to drive the outputs without overdriving internal buffers. This pin is level sensitive. This pin is pulled down with an internal resistor that is approximately 5 kΩ, and is a CMOS input.

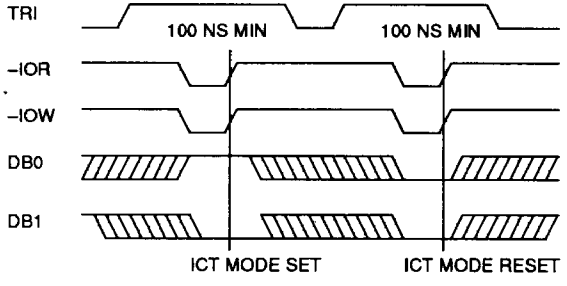
IN-CIRCUIT-TEST DESCRIPTION:
During In-circuit-test (ICT) all of the inputs except TRI and –RES can toggle one or more outputs. This allows for a board level tester to test the solder connections for each signal pin.

The sequence for enabling ICT is as follows:
1. Tester drives TRI signal to 1.
2. Tester drives DB0 to DB1 and DB1=0.
3. Tester pulses –IOR and –IOW low for 100 ns (minimum).
4. Tester drives TRI signal to 0 (outputs now enabled).
5. VL16C451B is now in ICT mode.

The sequence for disabling ICT is either assertion of the –RES signal or the sequence as follows:
1. Tester drives TRI signal to 1.
2. Tester drives both DB0 and DB1 to 1 or both to 0.
3. Tester pulses –IOR and –IOW low for 100 ns (minimum).
4. Tester drives TRI signal to 0 (outputs now enabled).
5. VL16C451B is now out of ICT mode.

Functionally ICT can be entered and exited as shown in Figure 1.

FIGURE 1.



Note: ICT Mode is set by an illegal combination of –IOR, –IOW, DB1 and DB0, while TRI is asserted. ICT Mode can be reset by either the –RES pin or the same combination but with DB0 and DB1 set = 0 or 1.

TABLE 1. PIN MAPPING FROM INPUT TO OUTPUT (VL16C451B ONLY)

INPUT			OUTPUT		
Pin	Signal	Type	Pin	Signal	Type
1	–PEMD	I	8	GPIO3	I/O
3	GPIN0	I	9	GPIO4	I/O
6	GPIN1	I	12	GPOUT5	O
7	GPIN2	I	24	–RTS	O
10	–EMODEA	I	25	–DTR	O
11	–EMODEB	I	26	SOUT	O
38	–CS2	I	54	GPOUT6	O
28	–CTS	I	44	BD0	O
29	–DCD	I	45	INT0	O
30	–RI	I	21 46	DB7 PD7	I/O I/O
31	–DSR	I	20 47	DB6 PD6	I/O I/O
32	–CS0	I	19 48	DB5 PD5	I/O I/O
33	A2	I	18 49	DB4 PD4	I/O I/O
34	A1	I	17 50	DB3 PD3	I/O I/O
35	A0	I	16 51	DB2 PD2	I/O I/O
36	–IOW	I	15 52	DB1 PD1	I/O I/O
37	–IOR	I	14 53	DB0 PD0	I/O I/O
41	SIN	I	55	–STB	O
43	–ENIRQ	I	56	–AFD	O
63	–ERR	I	57	–INIT	O
65	SLCT	I	58	–SLIN	O
66	BUSY	I	59	INT2	O
67	PE	I	60	–OUT2	O
68	–ACK	I	62	GPOUT7	O

TABLE 2. PINS NOT MAPPED (VL16C451B ONLY)

Pin	Signal	Type
2	TRI	I
9	GNDI	GND
22	GNDR	GND
23	VDDR	PWR
27	GNDI	GND
39	–RES	I
40	VDDI	PWR
42	GNDR	GND
61	GNDR	GND
64	VDDR	PWR

I/O LEGEND (O = Output, I = Input, IO = Input/Output)

No.	mA	Type	Comments
O1	10	TTL	
O2	24	TTL	
O3	10	TTL-OD	Open Drain (collector)
O4	12	TTL-ODP	Open Drain with Three kΩ Pull-up
O5	10	TTL-TS	Three-state
O6	24	TTL-TS	Three-state
O7	2	TTL-TS	Three-state
I1	–	TTL	
I2	–	CMOS	
I3	–	TTL	With 20 kΩ Pull-up Resistor
I4	–	CMOS	With 1 kΩ Pull-down Resistor
IO1	10	TTL-TS	Bidirectional, Three-state
IO2	24	TTL-TS	Bidirectional, Three-state
IO3	10	TTL-OD	Bidirectional, Open Drain
IO4	24	TTL-OD	Bidirectional, Open Drain
IO5	12	TTL-TSP	Bidirectional, Three-state
IO6	4	TTL-TS	Bidirectional, Three-state

FUNCTIONAL DESCRIPTION

SERIAL CHANNEL REGISTERS

Three types of internal registers are used in the serial channel of the VL16C451B. They are used in the operation of the device, and are the control, status, and data registers. The control registers are the Baud Rate Select Register DLL (Divisor Latch LSB) and DLM (Divisor Latch MSB), Line Control Register, Interrupt Enable Register, and the Modem Control registers, while the status registers are the Line Status Registers and the Modem Status Register. The data registers are the Receiver Buffer Register and the Transmitter Holding Register. The Address, Read, and Write inputs are used in conjunction with the Divisor Latch Access Bit in the Line Control Register [LCR(7)] to select the register to be written or read (see Table 3). Individual bits within these registers are referred to by the register mnemonic and the bit number in parenthesis. An example, LCR(7) refers to Line Control Register Bit 7.

The Transmitter Buffer Register and Receiver Buffer Register are data registers holding from five to eight bits of data. If less than eight data bits are transmitted, data is right justified to the LSB. Bit 0 of a data word is always the first serial data bit received and transmitted. The VL16C451B data registers are double-buffered so that read and write operations can be performed at the same time the ACE is performing the parallel-to-serial and serial-to-parallel conversion.

LINE CONTROL REGISTER

The format of the data character is controlled by the Line Control Register. The contents of the LCR may be read, eliminating the need for separate storage of the line characteristics in system memory. The contents of the LCR are described in Figure 2.

LCR (0) and LCR(1) word length select bit 1: The number of bits in each serial character is programmed as shown in Figure 2.

LCR(2) Stop Bit Select: LCR(2) specifies the number of stop bits in each transmitted character. If LCR(2) is a logic 0, one stop bit is generated in the transmitted data. If LCR(2) is a logic 1 when a 5-bit word length is selected, 1.5 stop bits are generated. If LCR(2) is a logic 1 when either a 6-, 7-, or 8-bit word length is selected, two stop bits are generated. The receiver checks for one stop bit.

LCR(3) Parity Enable: When LCR(3) is high, a parity bit between the last data word bit and stop bit is generated and checked.

LCR(4) Even Parity Select: When parity is enabled [LCR(3)=1], LCR(4)=0 selects odd parity, and LCR(4)=1 selects even parity.

LCR(5) Stick Parity: When parity is enabled [LCR(3)=1], LCR(5)=1 causes the transmission and reception of a parity bit to be in the opposite state from the value of LCR(4). This allows the user to force parity to a known state and for the receiver to check the parity bit in a known state.

LCR(6) Break Control: When LCR(6) is set to a logic "1", the serial output (SOUT) is forced to the spacing (logic 0) state. The break is disabled by setting LCR(6) to a logic "0". The Break Control bit acts only on SOUT and has no effect on the transmitter logic. If the following sequence is used, no erroneous or extraneous characters will be transmitted because of the break.

1. Load an all "0"s pad character in response to THRE.
2. Set break in response to the next THRE.
3. Wait for the transmitter to be idle (TEMT=1), and clear break when normal transmission has to be restored.

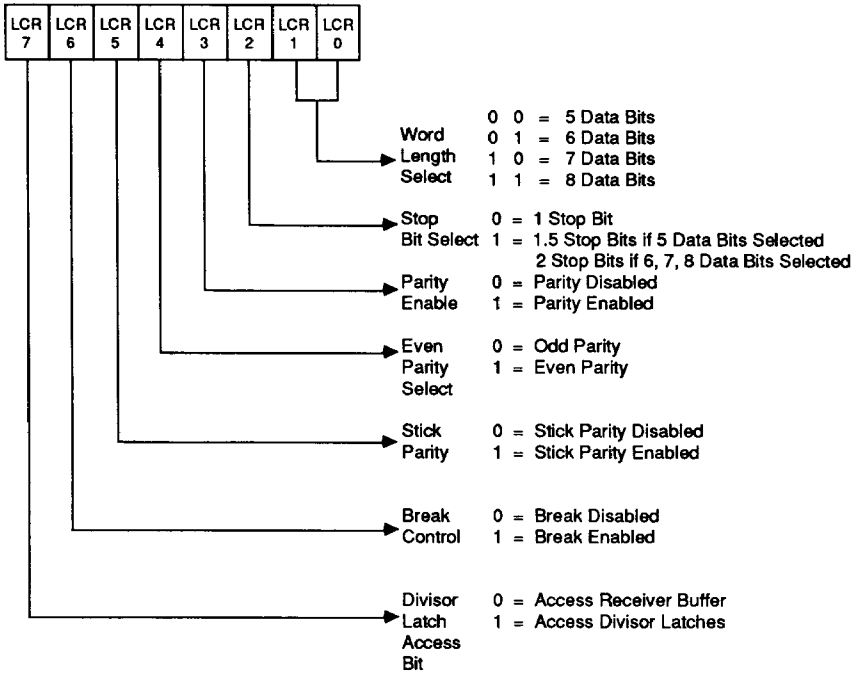
TABLE 3. SERIAL CHANNEL INTERNAL REGISTERS

DLAB	A2	A1	A0	Mnemonic	Register
0	0	0	0	RBR	Receiver Buffer Register (read only)
0	0	0	0	THR	Transmitter Holding Register (write only)
0	0	0	1	IER	Interrupt Enable Register
X	0	1	0	IIR	Interrupt Identification Register (read only)
X	0	1	1	LCR	Line Control Register
X	1	0	0	MCR	Modem Control Register
X	1	0	1	LSR	Line Status Register
X	1	1	0	MSR	Modem Status Register
X	1	1	1	SCR	Scratch Register
1	0	0	0	DLL	Divisor Latch (LSB)
1	0	0	1	DLM	Divisor Latch (MSB)

X = "Don't Care" 0 = Logic Low 1 = Logic High

Note: The serial channel is accessed when –CS0 is low.

FIGURE 2. LINE CONTROL REGISTER



LCR(7) Divisor Latch Access Bit (DLAB): LCR(7) must be set high (logic "1") to access the Divisor Latches DLL and DLM of the Baud Rate Generator during a read or write operation. LCR(7) must be input low to access the Receiver Buffer, the Transmitter Holding, or the Interrupt Enable Registers.

LINE STATUS REGISTER

The Line Status Register (LSR) is a single register that provides status indications.

The contents of the Line Status Register shown in Table4 are described below:

LSR(0) Data Ready (DR): Data Ready is set high when an incoming character has been received and transferred into the Receiver Buffer Register. LSR(0) is reset low by a CPU read of the data in transferred into the Receiver Buffer Register.

LSR(1) Overrun Error (OE): Overrun Error indicates that data in the Receiver Buffer Register was not read by the CPU before the next character was transferred into the Receiver Buffer Register, overwriting the previous character. The OE indicator is reset whenever the CPU reads the contents of the Line Status Register.

LSR(2) Parity Error (PE): Parity Error indicates that the received data character does not have the correct even or odd parity, as selected by the Even Parity Select bit (LCR(4). The PE bit is set high upon detection of a parity error, and is reset low when the CPU reads the contents of the LSR.

LSR(3) Framing Error (FE): Framing Error indicates that the received character did not have a valid stop bit. LSR(3) is set high when the stop bit following the last data bit or parity bit is detected as a zero bit (spacing level). The FE indicator is reset low when the CPU reads the contents of the LSR.

LSR(4) Break Interrupt (BI): Break Interrupt is set high when the received data input is held in the spacing (logic 0) state for longer than a full word transmission time (start bit + data bits + parity + stop bits). The BI indicator is reset when the CPU reads the contents of the Line Status Register.

LSR(1) - LSR(4) are the error conditions that produce a Receiver Line Status interrupt (priority 1 interrupt in the Interrupt Identification Register (IIR)) when any of the conditions are detected. This interrupt is enabled by setting IER(2)=1 in the Interrupt Enable Register.

LSR(5) Transmitter Holding Register Empty (THRE): THRE shows that the serial channel is ready to accept a new character for transmission. The THRE bit is set high when a character is transferred from the Transmitter Holding Register into the Transmitter Shift Register. LSR(5) is reset low by the loading of the Transmitter Holding Register by the CPU. LSR(5) is not reset by a CPU read of the LSR.

TABLE 4. LINE STATUS REGISTER BITS

LSR BITS	1	0
LSR (0) Data Ready (DR)	Ready	Not Ready
LSR (1) Overrun Error (OE)	Error	No Error
LSR (2) Parity Error (PE)	Error	No Error
LSR (3) Framing Error (FE)	Error	No Error
LSR (4) Break Interrupt (BI)	Break	No Break
LSR (5) Transmitter Holding Register Empty (THRE)	Empty	Not Empty
LSR (6) Transmitter Empty (TEMT)	Empty	Not Empty
LSR (7) Not Used		

When the THRE interrupt is enabled [IER(1)=1]. THRE causes a priority 3 interrupt in the IIR. If THRE is the interrupt source indicated in IIR, INTRPT is cleared by a read of the IIR.

LSR(6) Transmitter Empty (TEMT): TEMT is set high when the Transmitter Holding Register (THR) and the Transmitter Shift Register (TSR) are both empty. LSR(6) is reset low when a character is loaded into the THR and remains low until the character is transferred out of SOUT. TEMT is not reset low by a CPU read of the LSR.

LSR(7): This bit is always 0.

Note: The Line Status Register may be written. However, this function is intended only for factory test. It should be considered READ ONLY by applications software.

MODEM CONTROL REGISTER

The Modem Control Register (MCR) controls the interface with the modem or data set as described in Figure 3. The MCR can be written and read. The –RTS and –DTR outputs are directly controlled by their control bits in this register. A high input asserts a low (true) at the output pins. MCR Bits 0, 1, 3, and 4 are shown below:

MCR(0): When MCR(0) is set high, the –DTR output is forced low. When MCR(0) is reset low, the –DTR output is forced high. The –DTR output of the serial channel may be input into an inverting line driver in order to obtain the proper polarity input at the modem or data set.

MCR(1): When MCR(1) is set high, the –RTS output is forced low. When MCR(1) is reset low, the –RTS output is forced high. The –RTS output of the serial channel may be input into an inverting line driver in order to obtain the proper polarity input at the modem or data set.

MCR(3): When MCR(3) is set high, the INT output is enabled.

MCR(4): MCR(4) provides a local loopback feature for diagnostic testing of the channel. When MCR(4) is set high, Serial Output (SOUT) is set to the marking (logic "1") state, and the receiver data input Serial Input (SIN) is disconnected. The output of the Transmitter Shift Register is looped back into the Receiver Shift Register input. The three modem control inputs (–CTS, –DSR, –DCD (–RLSD) and –RI) are disconnected. The modem control outputs (–DTR, OUT2 and –RTS) are internally connected to –CTS, –DCD (–RLSD) and –DSR. –RI is connected to –MCR(2). The modem control output pins are forced to their inactive state (high). In the diagnostic mode, data transmitted is immediately received. This allows the processor to verify the transmit and receive data paths of the selected serial channel.

Bits MCR(5) - MCR(7) are permanently set to logic 0.

MODEM STATUS REGISTER

The MSR provides the CPU with status of the modem input lines from the modem or peripheral devices. The MSR allows the CPU to read the serial channel modem signal inputs by accessing the data bus interface of the VL16C451B. In addition to the current status information, four bits of the MSR indicate whether the modem inputs have changed since the last reading of the MSR. The delta status bits are set high when a control input from the modem changes state, and reset low when the CPU reads the MSR.

The modem input lines for the channel are –CTS, –DSR, –RI, and –DCD (–RLSD). MSR(4) - MSR(7) are status indications of these lines. A status bit=1 indicates the associated signal is low, a bit=0 indicates a high. If the modem status interrupt in the Interrupt Enable Register is enabled [IER(3)], an interrupt is generated whenever MSR(0) is set to a one. The MSR is a priority 4 interrupt. The contents of the Modem Status Register are described in Table 3.

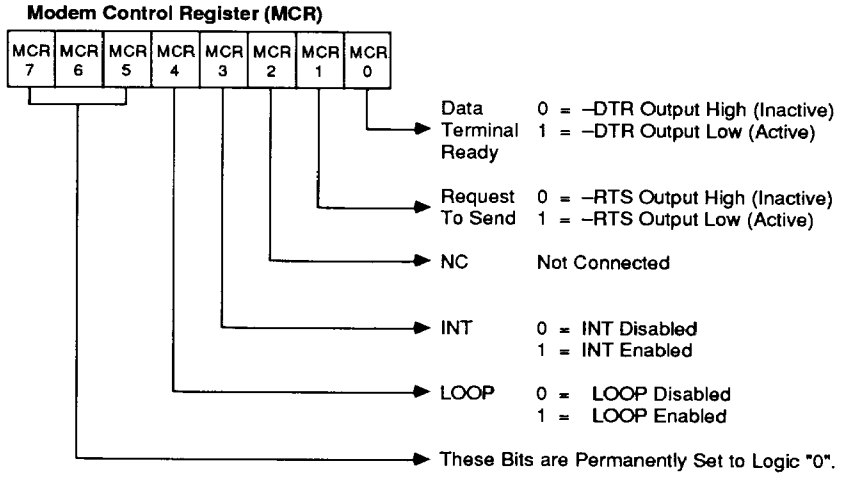
MSR(0) Delta Clear to Send (DCTS): DCTS indicates that the –CTS input to the serial channel has changed state since the last time it was read by the CPU.

MSR(1) Delta Data Set Ready (DDSR): DDSR indicates that the –DSR input to the serial channel has changed state since the last time it was read by the CPU.

TABLE 5. MODEM STATUS REGISTER BITS

MSR Bit	Mnemonic	Description
MSR(0)	DCTS	Delta Clear to Send
MSR(1)	DDSR	Delta Data Set Ready
MSR(2)	TERI	Trailing Edge of Ring Indicator
MSR(3)	DDCD	Delta Data Carrierl Detect
MSR(4)	CTS	Clear To Send
MSR(5)	DSR	Data Set Ready
MSR(6)	RI	Ring Indicator
MSR(7)	–DCD	Data Carrier Detect

FIGURE 3. MODEM CONTROL REGISTER



MSR(2) Trailing Edge of Ring Indicator (TERI): TERI indicates that the –RI input to the serial channel has changed state from low to high since the last time it was read by the CPU. High to low transitions on –RI do not activate TERI.

MSR(3) Delta Data Carrier Detect (DDCD): DDCD indicates that the –DCD input to the serial channel has changed state since the last time it was read by the CPU.

MSR(4) Clear to Send (CTS): Clear to Send (CTS) is the complement of the –CTS input from the modem indicating to the serial channel that the modem is ready to receive data from the serial channel's transmitter output (SOUT). If the serial channel is in Loop Mode [MCR(4)=1], this bit reflects the value of –RTS in the MCR.

MSR(5) Data Set Ready (DSR): Data Set Ready (DSR) is the complement of the –DSR input from the modem to the serial channel which indicates that the modem is ready to provide received data to the serial channel receiver circuitry. If the channel is in the Loop Mode [MCR(4)=1], this bit reflects the value of –DTR in the MCR.

MSR(6) Ring Indicator: Is the complement of the RI input (pin 39). If the channel is in the Loop Mode [MCR(4)=1], this bit reflects the state of MCR(2).

MSR(7) Data Carrier Detect/Receive Line Signal Detect : Data Carrier Detect indicates the status of the Data Carrier Detect (–DCD) input. If the channel is in the Loop Mode [MCR(4)=1], this bit reflects the state of INT0 of the MCR.

The modem status inputs (–RI, –DCD (–RLSD), –DSR, and –CTS) reflect the modem input lines with any change of status. Reading the MSR register will clear the delta modem status indications but has no effect on the other status bits.

For LSR and MSR, the setting of status bits is inhibited during status register read operations. If a status condition is generated during a read operation, the status bit is not set until the trailing edge of –IOR.

If a status bit is set during a read operation, and the same status condition occurs, that status bit will be cleared at the trailing edge of –IOR instead of being set again.

Note: In Loop Back Mode, when Modem Status interrupts are enabled, the –CTS, –DSR, –RI and –DCD input pins are ignored. However, a Modem Status interrupt may still be generated by writing to MSR7-MSR4. This is considered a test mode only. Applications software should not write to the Modem Status Register.

DIVISOR LATCHES

The VL16C451B serial channel contains a programmable Baud Rate Generator (BRG) that divides the clock (DC to 3.1 MHz) by any divisor from 1 to 2^{16-1} (see also BRG description). The output frequency of the Baud Generator is 16X the data rate [divisor # = clock ÷ (baud rate x 16)]. Two 8-bit divisor latch registers store the divisor in a 16-bit binary format. These Divisor Latch registers must be loaded during initialization. Upon loading either of the Divisor latches, a 16-bit baud counter is immediately loaded. This prevents long counts on initial load.

RECEIVE BUFFER REGISTER

The receiver circuitry in the serial channel of the VL16C451B is programmable for 5, 6, 7, or 8 data bits per character. For words of less than 8 bits, the data is right justified to the least significant bit LSB = Data Bit 0 [RBR(0)]. Data Bit 0 of a data word [RBR(0)] is the first data bit received. The unused bits in a character less than 8 bits 0's.

Received data at the SIN input pin is shifted into the Receiver Shift Register by the 16X clock provided at the RCLK input. This clock is synchronized to the incoming data based on the position of the start bit. When a complete character is shifted into the Receiver Shift Register, the assembled data bits are

parallel loaded into the Receiver Buffer Register. The DR flag in the LSR register is set.

Double buffering of the received data permits continuous reception of data without losing received data. While the Receiver Shift Register is shifting a new character into the serial channel, the Receiver Buffer Register is holding a previously received character for the CPU to read. Failure to read the data in the RBR before complete reception of the next character result in the loss of the data in the Receiver Register. The OE flag in the LSR register indicates the overrun condition.

TRANSMITTER HOLDING REGISTER
The Transmitter Holding Register (THR) holds the character until the Transmitter Shift Register is empty and ready to accept a new character. The transmitter and receiver word lengths are the same. If the character is less than eight bits, unused bits are ignored by the transmitter.

Data Bit 0 [THR(0)] is the first serial data bit transmitted. The THRE flag [LSR(5)] reflect the status of the THR. The TEMT flag [LSR(5)] indicates if both the THR and TSR are empty.

SCRATCHPAD REGISTER
Scratchpad Register is an 8-bit Read/ Write register that has no effect on either channel in the VL16C451B. It is intended to be used by the programmer to hold data termporarily.

INTERRUPT IDENTIFICATION REGISTER
In order to minimize software overhead during data character transfers, the serial channel prioritizes interrupts into four levels. The four levels of interrupt conditions are as follows:

1. Réceiver Line Status (priority 1)
2. Received Data Ready (priority 2)
3. Transmitter Holding Register Empty (priority 3)
4. Modem Status (priority 4)

Information indicating that a prioritized interrupt is pending and the type of interrupt is stored in the Interrupt Identification Register (IIR). The IIR indicates the highest priority interrupt pending. The logic equivalent of the interrupt control circuit is shown in Figure 3. The contents of the IIR are indicated in Table 4 and are described below.

IIR(0): IIR(0) can be used to indicate whether an interrupt is pending. When IIR(0) is low, an interrupt is pending.

IIR(1) and IIR(2) are used to identify the highest priority interrupt pending as indicated in Table 2.

IIR(3) - IIR(7): These five bits of the IIR are logic 0.

INTERRUPT ENABLE REGISTER
The Interrupt Enable Register (IER) is a Write register used to independently enable the four serial channel interrupt sources which activate the interrupt (INTRPT) output. All interrupts are disabled by resetting IER(0) - IER(3) of the Interrupt Enable Register. Interrupts are enabled by setting the appropriate bits of the IER high. Disabling the interrupt system inhibits the Interrupt Identification Register and the active (high) INTRPT output. All other system functions operate in their normal manner, including the setting of the Line Status and Modem Status Registers. The contents of the Interrupt Enable Register is described in Figure 2 and below:

IER(0): When set to one, IER(0) enables Received Data Available interrupt.

IER(1): When set to one, IER(1) enables the Transmitter Holding Register Empty interrupt.

IER(2): When set to one, IER(2) enables the Receiver Line Status interrupt.

IER(3): When set to one, IER(3) enables the Modem Status Interrupt.

IER(4) - IER(7): These four bits of the IER are Logic 0.

TRANSMITTER
The serial transmitter section consists of a Transmitter Holding Register (THR), Transmitter Shift Register (TSR), and associated control logic. The Transmitter Holding Register Empty (THRE) and Transmitter Empty (TEMT) are two bits in the Line Status Register which indicate the status of THR and TSR. The microprocessor should perform a write to the THR only if THRE is one. This causes the THRE to be reset to 0. THRE is set high when the word is automatically transferred from the THR to the TSR during the transmission of the start bit.

TEMT remains low for at least the duration of the transmission of the data word. Since the data word cannot be transferred from the THR to the TSR until the TSR is empty, THRE remains low until the TSR has completed sending the word.

RECEIVER
Serial asynchronous data is input into the SIN pin. A start bit detect circuit continually searches for a high to low transition from the idle state. When the transition is detected, a counter is reset, and counts the 16X clock to 7 1/2, which is the center of the start bit. The start bit is valid if the SIN is still low. Verifying the start bit prevents the receiver from assembling a false data character due to a low going noise spike on the SIN input.

The Line Control Register determines the number of data bits in a character [LCR(0), LCR(1)], if parity is used LCR(3), and the polarity of parity LCR(4).

Status for the receiver is provided in the Line Status Register. When a full character is received including parity and stop bit, the Data Received indication in LSR(0) is set high. The CPU reads the Receiver Buffer Register which resets LSR(0). If the character is not read prior to a new character transfer from the RSR to the RBR, the overrun error status indication is set in LSR(1). If there is a parity error, the parity error is set in LSR(2). If a stop bit is not detected, a framing error indication is set in LSR(3).

If the data into SIN is symmetrical square wave, the center of the data cells will occur within ±3.125% of the actual center, providing an error margin of 46.875%. The start bit can begin as much as one 16X clock cycle prior to being detected.

BAUD RATE GENERATOR (BRG)
The BRG generates the clocking for the UART function, providing standard ANSI/CCITT bit rates. The oscillator driving the BRG is provided by an external clock into CLK.

The data rate is determined by the Divisor Latch registers DLL and DLM and the external frequency. The bit rate is selected by programming the two divisor latches, Divisor Latch Most Significant Byte and Divisor Latch Least Significant Byte. Setting DLL=1 and DLM=0 selects the divisor to divide by 1 (divide by 1 gives maximum baud rate for a given input frequency at the CLK input).

The BRG can use any of three different popular frequencies to provide standard baud rates. These frequencies are 1.8432 MHz, 3.072 MHz, and 8 MHz. With these frequencies, standard bit rates from 50 to 512K bps are available. Tables 5, 6 and 7 illustrate the divisors needed to obtain standard rates using these three crystal frequencies.

RESET

After power up, the VL16C451B –RES input should be held low for 500 ns to reset the VL16C451B circuits to an idle mode until initialization. A low on –RES causes the following:

1. Initializes the transmitter and receiver internal clock counters.
2. Clears the Line Status Register (LSR), except for Transmitter Shift Register Empty (TEMT) and Transmit Holding Register Empty (THRE), which are set. The Modem Control Register (MCR) is also cleared. All of the discrete lines, memory elements and miscellaneous logic associated with these register bits are also cleared or turned off. The Line Control Register (LCR), Divisor Latches, Receiver Buffer Register, Transmitter Buffer Register are not affected.

Following removal of the reset condition (Reset high), the VL16C451B remains in the idle mode until programmed.

A hardware reset of the VL16C451B sets the THRE and TEMT status bit in the LSR. When interrupts are subsequently enabled, an interrupt occurs due to THRE.

A summary of the effect of a reset on the VL16C451B is given in Table 8.

PROGRAMMING

The serial channel of the VL16C451B is programmed by the control registers LCR, IER, DLL and DLM, and MCR. These control words define the character length, number of stop bits, parity, baud rate, and modem interface.

While the control register can be written in any order, the IER should be written to last because it controls the interrupt enables. Once the serial channel is programmed and operational, these registers can be updated any time the VL16C451B serial channel is not transmitting or receiving data.

SOFTWARE RESET

A software reset of the serial channel is a useful method for returning to a completely known state without a system reset. Such a reset consists of writing to the LCR, Divisor Latches, and MCR registers. The LSR and RBR registers should be read prior to enabling interrupts in order to clear out any residual data or status bits which may be invalid for subsequent operation.

CLOCK INPUT OPERATION

The maximum input frequency of the external clock of the VL16C451B is 8 MHz. For VL16C451, the maximum input frequency of the external clock is 3.1 MHz.

TABLE 4. INTERRUPT IDENTIFICATION REGISTER

INTERRUPT IDENTIFICATION				INTERRUPT SET AND RESET FUNCTIONS		
Bit 2	Bit 1	Bit 0	Priority Level	Interrupt Flag	Interrupt Source	Interrupt Reset Control
X	X	1		None	None	
1	1	0	First	Receiver Line Status	OE, PE FE, or BI	LSR Read
1	0	0	Second	Received Data Available	Received Data Available	RBR Read
0	1	0	Third	THRE	THRE	IIR Read if THRE is the Interrupt Source or THR Write
0	0	0	Fourth	Modem Status	–CTS, –DSR –RI, –DCD	MSR Read

X = Not Defined.

FIGURE 3. INTERRUPT CONTROL LOGIC

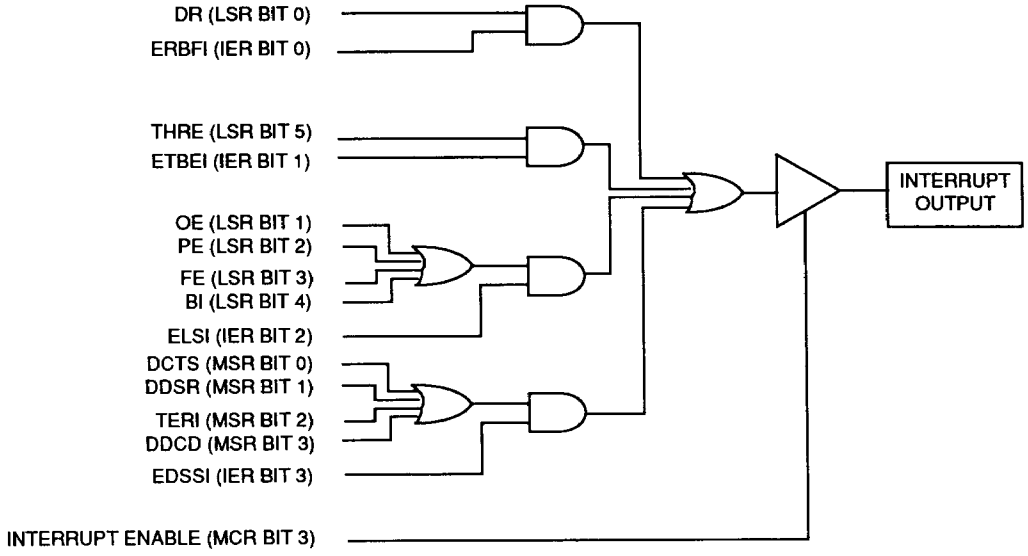


TABLE 5. BAUD RATES (1.8432 MHz CLOCK)

Desired Baud Rate	Divisor Used	Percent Error Difference Between Desired and Actual
50	2304	–
75	1536	–
110	1047	0.026
134.5	857	0.058
150	768	–
300	384	–
600	192	–
1200	96	–
1800	64	–
2000	58	0.69
2400	48	–
3600	32	–
4800	24	–
7200	16	–
9600	12	–
19200	6	–
38400	3	–
56000	2	2.86

TABLE 6. BAUD RATES (3.072 MHz CLOCK)

Desired Baud Rate	Divisor Used	Percent Error Difference Between Desired and Actual
50	3840	–
75	2560	–
110	1745	0.026
134.5	1428	0.034
150	1280	–
300	640	–
600	320	–
1200	160	–
1800	107	0.312
2000	96	–
2400	80	–
3600	53	0.628
4800	40	–
7200	27	1.23
9600	20	–
19200	10	–
38400	5	–

TABLE 7. BAUD RATES (8 MHz CLOCK)

Baud Rate Desired	Divisor Used to Generate 16 x Clock	Percent Error Difference Between Desired and Actual
50	1000	—
75	6667	0.005
110	4545	0.010
134.5	3717	0.013
150	3333	0.010
300	1667	0.020
600	833	0.040
1200	417	0.080
1800	277	0.080
2000	250	—
2400	208	0.160
3600	139	0.080
4800	104	0.160
7200	69	0.644
9600	52	0.160
19200	26	0.160
38400	13	0.160
56000	9	0.790
128000	4	2.344
256000	2	2.344
512000	1	2.400

TABLE 8. RESET

Register/Signal	Reset Control	Reset
Interrupt Enable Register	Reset	All Bits Low (0-3 Forced and 4-7 Permanent)
Interrupt Identification Register	Reset	Bit 0 is High, Bits 1 and 2 Low Bits 3-7 Are Permanently Low
Line Control Register	Reset	All Bits Low
Modem Control Register	Reset	All Bits Low
Line Status Register	Reset	All Bits Low, Except Bits 5 and 6 Are High
Modem Status Register	Reset	Bits 0-3 Low Bits 4-7 Input Signal
SOUT	Reset	High
Intrpt (RCVR Errs)	Read LSR/Reset	Low
Intrpt (RCVR Data Ready)	Read RBR/Reset	Low
Intrpt (THRE)	Read IIR/Write THR/Reset	Low
Intrpt (Modem Status Changes)	Read MSR/Reset	Low
–OUT2	Reset	High
–RTS	Reset	High
–DTR	Reset	High
–OUT1	Reset	High

DEVICE APPLICATION

TYPICAL COMPONENT VALUES

Crystal	RP	RX2	C1	C2
8 MHz	1 MΩ	1.5 KΩ	10 - 30 pF	40 - 90 pF
3.072 MHz	1 MΩ	1.5 KΩ	10 - 30 pF	40 - 90 pF
1.843 MHz	1 MΩ	1.5 KΩ	10 - 15 pF	65 - 100 pF

VL16C451/VL16C451B

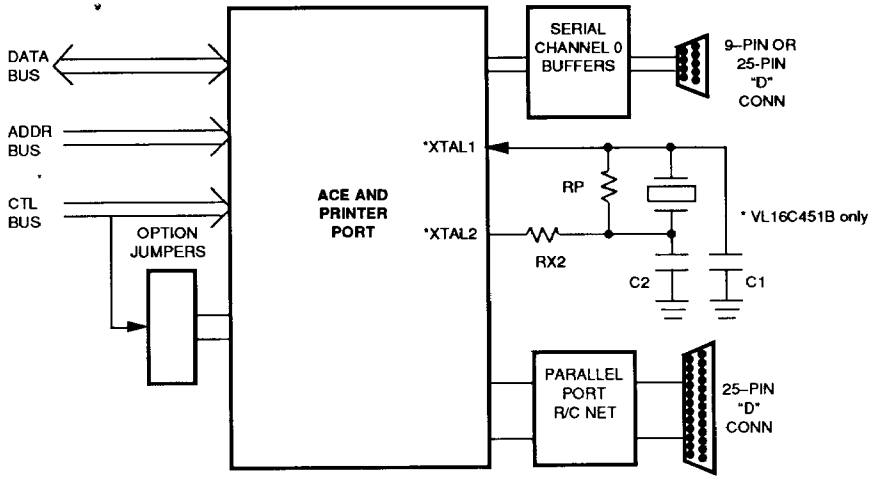


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TABLE 9. SERIAL CHANNEL ACCESSIBLE REGISTERS

Register Mnemonic	Register Bit Number							
	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
RBR (Read Only)	Data Bit 7 (MSB)	Data Bit 6	Data Bit 5	Data Bit 4	Data Bit 3	Data Bit 2	Data Bit 1	Data Bit 0 (LSB)*
THR (Write Only)	Data Bit 7	Data Bit 6	Data Bit 5	Data Bit 4	Data Bit 3	Data Bit 2	Data Bit 1	Data Bit 0
DLL	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
DLM	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
IER	0	0	0	0	(EDSSI) Enable Modem Status Interrupt	(ELSI) Enable Receiver Line Status Interrupt	(ETBEI) Enable Transmitter Holding Register Empty Interrupt	(ERBFI) Enable Received Data Available Interrupt
IIR (Read Only)	0	0	0	0	0	Interrupt ID Bit (1)	Interrupt ID Bit (0)	"0" If Interrupt Pending
LCR	(DLAB) Divisor Latch Access Bit	Set Break	Stick Parity	(EPS) Even Parity Select	(PEN) Parity Enable	(STB) Number of Stop Bits	(WLSB1) Word Length Select Bit 1	(WLSB0) Word Length Select Bit 0
MCR	0	0	0	Loop	INT	NC	(RTS) Request To Send	(DTR) Data Terminal Ready
LSR	0	(TEMT) Transmitter Empty	(THRE) Transmitter Holding Register Empty	(BI) Break Interrupt	(FE) Framing Error	(PE) Parity Error	(OE) Overrun Error	(DR) Data Ready
MSR	(DCD) Data Carrier Detect	(RI) Ring Indicator	(DSR) Data Ready Set	(CTS) Clear to Send	(DDCD) Delta Data Carrier Detect	(TERI) Trailing Edge Ring Indicator	(DDSR) Delta Data Set Ready	(DCTS) Delta Clear to Send
SCR	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0

*LSB Data Bit 0 is the first bit transmitted or received.

PARALLEL PORT REGISTERS

The VL16C451B's parallel port interfaces the device to a Centronics-style printer. When Chip Select 2 (–CS2) is low, the parallel port is selected. Table 10 shows the registers associated with this parallel port. The read or write function of the register is controlled by the state of the read (–IOR) and write (–IOW) pin as shown. The Read Data Register allows the microprocessor to read the information on the parallel bus.

The Read Status Register allows the microprocessor to read the status of the printer in the five most significant bits.

The status bits are Printer Busy (BSY), Acknowledge (–ACK) which is a handshake function, Paper Empty (PE), Printer Selected (SLCT), and Error (–ERR). The Read Control Register allows the state of the control lines to be read. The Write Control Register sets the state of the control lines. They are Interrupt Enable (IRQ ENB), Select In (–SLIN), Initialize the Printer (–INIT), Autofeed the Paper (–AFD) and Strobe (–STB). The Write Data Register allows the microprocessor to write a byte to the parallel bus.

The parallel port is completely compatible with the parallel port implementation used in the IBM Serial/Parallel Adaptor when –PEMD (pin 1) is held low. (VL16C451B only.)

The following two paragraphs apply to the VL16C451 only.

Figure 4 describes the operation of the –LPTOE input. When –LPTOE goes Low, the internal data latch is enabled to the PD0-PD7 lines. PD0-PD7 will then contain the same information as the latch.

When –LPTOE goes gigh, the internal data latch is disabled from the PD0-PD7 lines. An external device can place data on the PD0-PD7 lines, and reading the data reads the PD0-PD7 lines.

TABLE 10. PARALLEL PORT REGISTERS

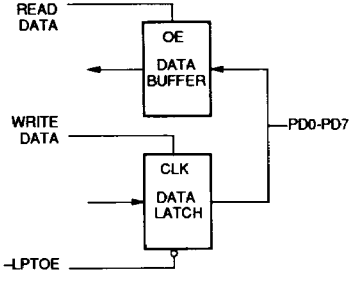
Register	Register Bits							
	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Read Port	PD7	PD6	PD5	PD4	PD3	PD2	PD1	PD0
Read Status	–BSY	–ACK	PE	SLCT	–ERR	1	1	1
Read Control	1	1	1	IRQ ENB	SLIN	–INIT	AFD	STB
Write Port	PD7	PD6	PD5	PD4	PD3	PD2	PD1	PD0
Write Control	1	1	1	IRQ ENB	SLIN	–INIT	AFD	STB

TABLE 11. PARALLEL PORT REGISTER SELECT

Control Pins					Register Selected
–IOR	–IOW	–CS2	A1	A0	
0	1	0	0	0	Read Port
0	1	0	0	1	Read Status
0	1	0	1	0	Read Control
0	1	0	1	1	Invalid
1	0	0	0	0	Write Port
1	0	0	0	1	Invalid
1	0	0	1	0	Write Control
1	0	0	1	1	Invalid *

* See General Purpose I/O Register Description (VL16C451B only).

FIGURE 4. –LPTOE FUNCTION (VL16C451 ONLY)



THE FOLLOWING TWO PAGES PERTAIN TO VL16C451B ONLY.

Line Printer Port:

The Line Printer Port contains the functionality of the port included in the VL16C451, but offers a hardware programmable Extended Mode, controlled by the Printer Enhancement Mode (–PEMD) pin. This enhancement is the addition of a Direction Control Bit, and an Interrupt Status Bit.

Register 0 - Line Printer Data Register:

The Line Printer (LPD) port is either output-only or bidirectional, depending on the state of the Extended Mode pin and Data Direction Control bits.

Compatibility Mode (–PEMD pin=0): Reads to the LPD register return the last data that was written to the port. Write operations immediately output data to the PD0-PD7 pins.

Extended Mode (–PEMD pin=1): Read operations return either the data last written to the LPT Data Register if the Direction Bit is set to Write (low) or the data that is present on PD0-PD7 if the direction is set to Read (high). Writes to the LPD register latch data into the output register, but only drive the LPT port when the Direction Bit is set to Write.

The table below summarizes the possible combinations of Extended Mode and the Direction control bit.

–PEMD	DIR	PD0-PD7 Function
0	X	PC/AT Mode - Output
1	0	PS/2 Mode - Output
1	1	PS/2 Mode - Input

In either case, the bits of the LPD Register are defined as follows:

Bit	Description
0	PD0
1	PD1
2	PD2
3	PD3
4	PD4
5	PD5
6	PD6
7	PD7

Register 1 Read - Line Printer Status Register:

The Line Printer Status (LPS) Register is a read-only register that contains interrupt and printer status of the LPT connector pins. In the table below (in the Default column) are the values of each bit in the case of the printer being disconnected from the port. The bits are described as follows:

Bit	Description	Default
0	Reserved	1
1	Reserved	1
2	–PIRQ	1
3	–ERR	1
4	SLCT	1
5	PE	1
6	–ACK	1
7	–BSY	0

Bits 0 and 1 - Reserved, read as 1's.

Bit 2 - Printer Interrupt (–PIRQ, active low) Status bit, when set (low) indicates that the printer has acknowledged the previous transfer with an –ACK handshake (bit 4 of the control register must be set to 1). The bit is set to 0 on the active to inactive transition of the –ACK signal. This bit is set to a 1 after a read from the status port. The default (power on reset) value for this bit is 1.

Bit 3 - Error (–ERR, active low) Status bit corresponds to –ERR input.

Bit 4 - Select (SLCT) Status bit corresponds to SLCT input.

Bit 5 - Paper Empty (PE) Status bit corresponds to PE input.

Bit 6 - Acknowledge (–ACK, active low) Status bit corresponds to –ACK input.

Bit 7 - Busy (–BSY, active low) Status bit corresponds to BUSY input.

Register 2 - Line Printer Control Register:

The Line Printer Control (LPC) Register is a read/write port that is used to control the PD0-PD7 direction and drive the Printer Control lines. Write operations set or reset these bits, while read operations return the state of the last write operation to this register (except for bit 5 which is write only). The bits in this register are defined as follows:

Bit	Description
0	STB
1	AFD
2	–INIT
3	SLIN
4	PIRQ EN
5	DIR (write only)
6	Reserved (1)
7	Reserved (1)

Bit 0 - Printer Strobe (STB) Control bit, when 1 the strobe signal is asserted on the LPT interface. When 0 the signal is negated.

Bit 1 - Auto Feed (AFD) Control bit, when 1 the –AFD signal will be asserted on the LPT interface. When 0 the signal is negated.

Bit 2 - Initialize Printer (–INIT) Control bit, when 1 the –INIT signal is negated. When 0 the INIT signal is asserted on the LPT interface.

Bit 3 - Select Input (SLIN) Control bit, when 1 the SLIN signal is asserted, on the LPT interface. When 0 the signal is negated.

Bit 4 - Interrupt Request Enable (PIRQ EN) Control bit, when 1 enables interrupts from the LPT port whenever the –ACK signal is asserted. When 0 disables interrupts.

Bit 5 - Direction (DIR) Control bit (only used when –PEMD is high), when 1 the output buffers in the LPD port are disabled, allowing data driven from external sources to be read from the LPD port.

GPIO - General Purpose I/O Register: The General Purpose I/O (GPIO) Register is an additional register in the VL16C451B which is used to control the general purpose I/O signals. This register can be accessed when –CS2 is asserted low, A0 and A1 are high and the enhanced mode control signals have configured the GPIO signals.

Reads to those bits programmed as outputs will return the state of the last write operation to that bit. Writes to those bits programmed as inputs will not have any affect. The bits in the register are defined as follows:

Bit	Description
0	GPIN0
1	GPIN1
2	GPIN2
3	GPIO3
4	GPIO4
5	GPOUT5
6	GPOUT6
7	GPOUT7

AC CHARACTERISTICS (VL16C451B ONLY): TA= 0°C to +70°C, VDD= 5 V ±5% (Note 4)

Symbol	Parameter	Min	Max	Units	Conditions
tDIW	–IOR Strobe Width	125		ns	
RC	Read Cycle = tAR(1)+tDIW+tRC	280		ns	
tDDD	Delay from –IOR to Data		110	ns	100 pF Load
tHZ	–IOR to Floating Data Delay	0	100	ns	100 pF Load, Note 3
tDOW	–IOW Strobe Width	100		ns	
WC	Write Cycle = tAW+tDOW+TVC	280		ns	
tDS	Data Setup Time	30		ns	
tDH	Data Hold Time	25		ns	
tRA	Address Hold Time from –IOR	20		ns	Note 1
tRCS	Chip Select Hold Time from –IOR	20		ns	Note 1
tAR	–IOR Delay from Address	30		ns	Note 1
tCSR	–IOR Delay from Chip Select	25		ns	Note 1
tWA	Address Hold Time from –IOW	20		ns	Note 1
tWCS	Chip Select Hold Time from –IOW	20		ns	Note 1
tAW	–IOW Delay from Address	30		ns	Note 1
tCSW	–IOW Delay from Select	25		ns	Note 1
tRW	Reset Pulse Width	5		µs	
tXH	Duration of Clock High Pulse	55		ns	External Clock (8 MHz Max.)
tXL	Duration of Clock Low Pulse	55		ns	External Clock (8 MHz Max.)
tRC	Read Cycle Delay	125		ns	
tWC	Write Cycle Delay	150		ns	

Notes:
1. The internal address strobe is always active.
2. RCLK = tXH and tXL.
3. Charge and discharge time is determined by VOL, VOH and the external loading.
4. All timings are referenced to valid 0 and valid 1. (See AC Test Points.)

AC CHARACTERISTICS (VL16C451 ONLY): TA= 0°C to +70°C, VDD= 5 V ±5% (Note 4)

Symbol	Parameter	Min	Max	Units	Conditions
tDIW	–IOR Strobe Width	125		ns	
RC	Read Cycle	360		ns	
tDDD	Delay from –IOR to Data		125	ns	100 pF Load
tHZ	–IOR to Floating Data Delay	0	100	ns	100 pF Load, Note 3
tDOW	–IOW Strobe Width	100		ns	
WC	Write Cycle	360		ns	
tDS	Data Setup Time	40		ns	
tDH	Data Hold Time	40		ns	
tRA	Address Hold Time from –IOR	20		ns	Note 1
tRCS	Chip Select Hold Time from –IOR	20		ns	Note 1
tAR	–IOR Delay from Address	60		ns	Note 1
tCSR	–IOR Delay from Chip Select	50		ns	Note 1
tWA	Address Hold Time from –IOW	20		ns	Note 1
tWCS	Chip Select Hold Time from –IOW	20		ns	Note 1
tAW	–IOW Delay from Address	60		ns	Note 1
tCSW	–IOW Delay from Select	50		ns	Note 1
tRW	Reset Pulse Width	5		µs	
tXH	Duration of Clock High Pulse	140		ns	External Clock
tXL	Duration of Clock Low Pulse	140		ns	External Clock

Notes:
1. The internal address strobe is always active.
2. RCLK = tXH and tXL.
3. Charge and discharge time is determined by VOL, VOH and the external loading.
4. All timings are referenced to valid 0 and valid 1. (See AC Test Points.)

AC CHARACTERISTICS (Cont.): TA = 0°C to +70°C, VDD = 5 V ±5% (Note 4)

Symbol	Parameter	Min	Max	Units	Conditions
Transmitter					
tHR1	Delay from Rising Edge of –IOW (WR THR) To Reset Interrupt		175	ns	100 pF Load
tIRS	Delay from Initial INT0 Reset to Transmit Start		16	CLK Cycles	Note 2
tSI	Delay from Initial Write to Interrupt	8	24	CLK Cycles	Note 2
tSTI	Delay from Stop to Interrupt (THRE)		8	CLK Cycles	Note 2
tIR	Delay from –IOR (RD IIR) to Reset Interrupt (THRE)		250	ns	100 pF Load
Modem Control					
tMDO	Delay from –IOW (WR MCR) to Output		250	ns	100 pF Load
tSIM	Delay to Set Interrupt from Modem Input		250	ns	100 pF Load
tRIM	Delay to Reset Interrupt from –IOR (RS MSR)		250	ns	100 pF Load
Receiver					
tSINT	Delay from Stop to Set Interrupt		1	CLK Cycles	Note 2
tRINT	Delay from –IOR (RD RBR/RD LSR) to Reset Interrupt		1	µs	100 pF Load

Notes:
1. The internal address strobe is always active.
2. RCLK = tXH and tXL.
3. Charge and discharge time is determined by VOL, VOH and the external loading.
4. All timings are referenced to valid 0 and valid 1 (see AC Test Points).

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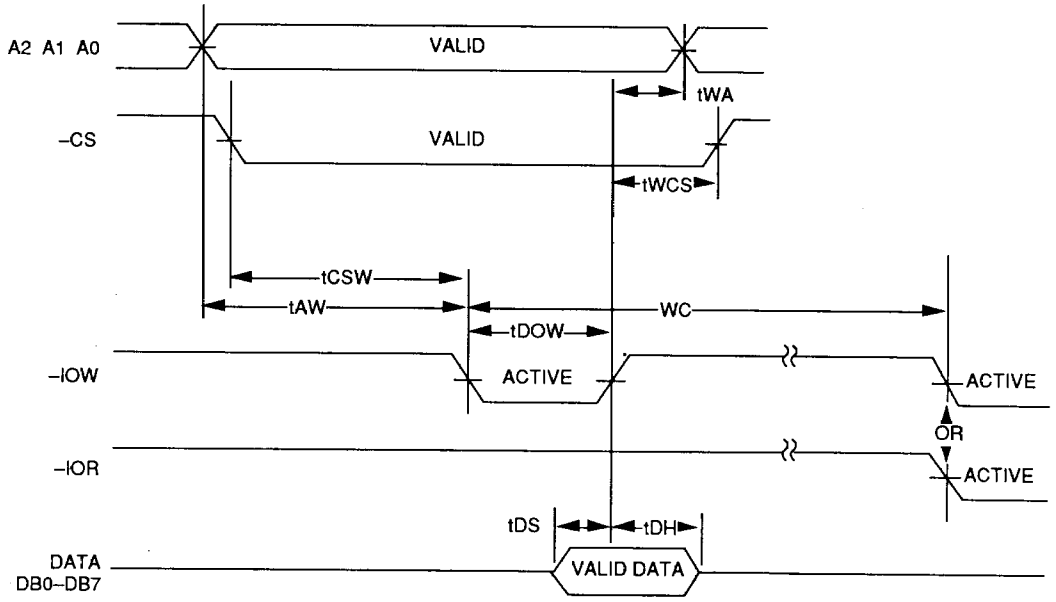
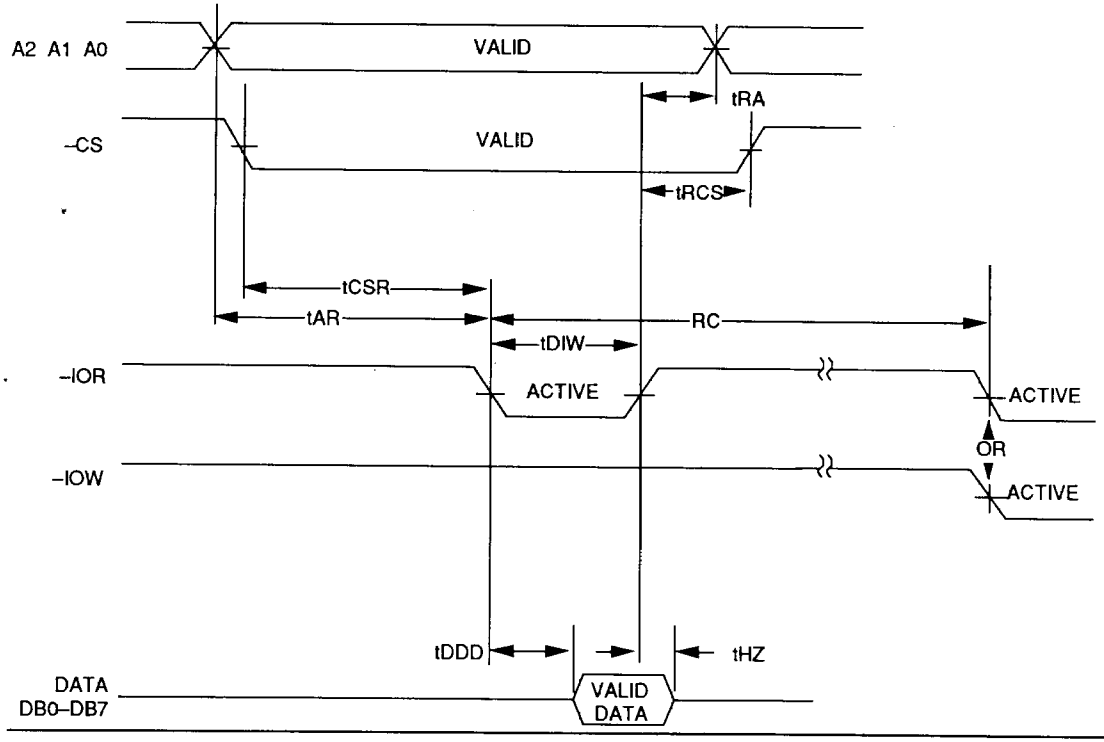
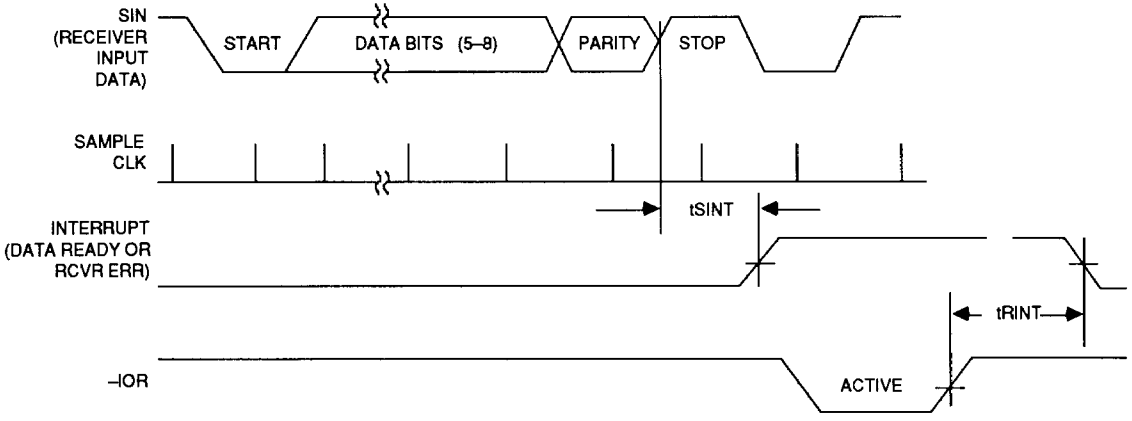
WRITE CYCLE TIMING



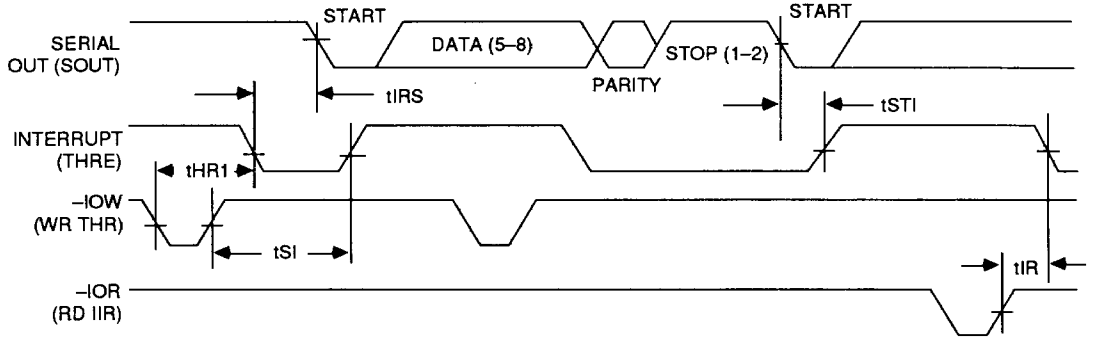
READ CYCLE TIMING



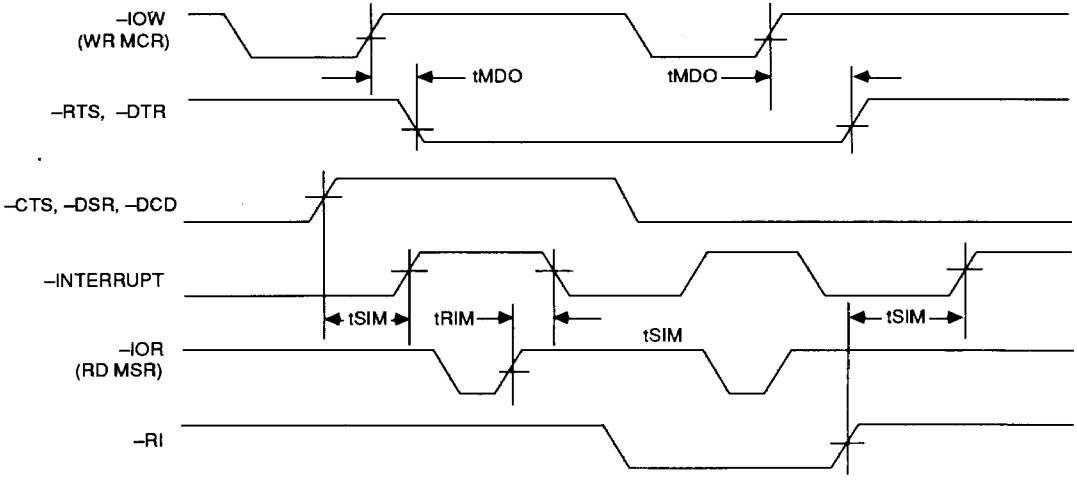
RECEIVER TIMING



TRANSMITTER TIMING



MODEM TIMING



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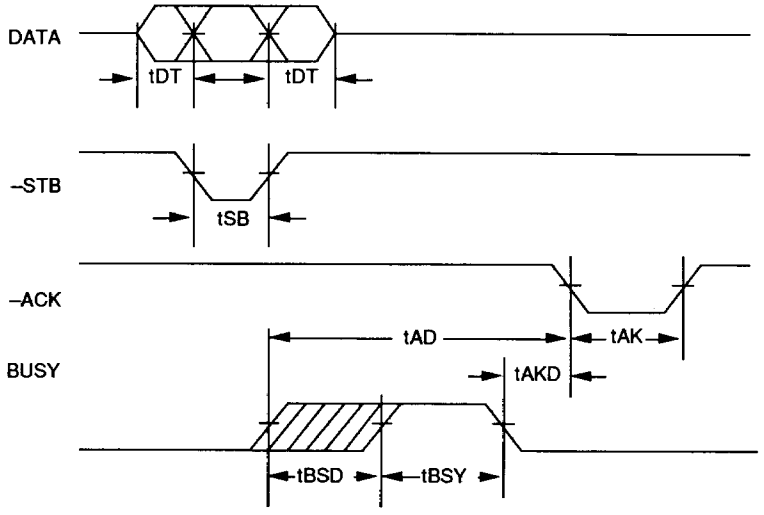
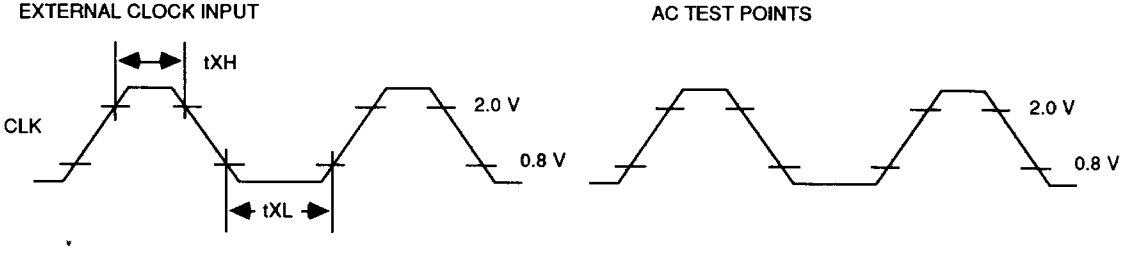
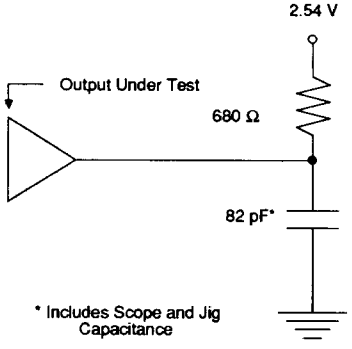
PARALLEL PORT TIMING



AC TESTING INPUT/OUTPUT WAVEFORMS



TEST CIRCUIT



ABSOLUTE MAXIMUM RATINGS

Ambient Operating Temperature	–10°C to +70°C
Storage Temperature	–65°C to +150°C
Supply Voltage to Ground Potential	–0.5 V to VDD +0.3 V
Applied Output Voltage	–0.5 V to VDD +0.3 V
Applied Input Voltage	–0.5 V to +7.0 V
Power Dissipation	500 mW

Stresses above those listed may cause permanent damage to the device. These are stress ratings only. Functional operation of this device at these or any other conditions above those indicated in this data sheet is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC CHARACTERISTICS: TA = 0°C to +70°C, VDD = 5 V ±5%

Symbol	Parameter	Min	Max	Units	Conditions
VILX	Clock Input Low Voltage	–0.3	0.3	V	
VIHX	Clock Input High Voltage	GND –0.3	GND +0.3	V	
VIL	Input Low Voltage	–0.5	0.8	V	
VIH	Input High Voltage	2.0	VDD	V	
VOL	Output Low Voltage		0.4	V	IOL = 4.0 mA on DB0-DB7 IOL = 12 mA on PD0-PD7, GPIO3, GPIO4, GPOUT5-GPOUT7 IOL = 10 mA on –INIT, –AFD, –STB, and –SLIN (see Note 1)
VOH	Output High Voltage	2.4		V	IOH = –0.4 mA on DB0-DB7 IOH = –2.0 mA on PD0-PD7, GPIO3, GPIO4, GPOUT5-GPOUT7. IOH = –250 µA on –INIT, –AFD, –STB, and –SLIN
IDD	Power Supply Current		50	mA	VDD = 5.25 V, no loads on outputs. SIN, –DSR, –RLS, –CTS, –RI = 2.0 V. Other inputs = 0.8 V. Clock = max. specified clock frequency. Baud rate = 56K
IIL	Input Leakage		±10	µA	VDD = 5.25 V, GND = 0 V. All other pins floating.
ICL	Clock Leakage		±10	µA	VIN = 0 V, 5.25 V
IOZ	3-State Leakage		±20	µA	VDD = 5.25 V, GND = 0 V. VOUT = 0 V, 5.25 V 1) Chip deselected 2) Chip and write mode selected
VIL(RES)	Reset Schmitt VIL		0.8	V	
VIH(RES)	Reset Schmitt VIH	2.0		V	

Notes:
1. –INIT, –AFD, –STB, –SLIN –OUT2, GPOUT5, GPOUT6, and GPOUT7 are open collector output pins that each have an internal pull-up resistor (2.5 kΩ-3.5 kΩ). In addition to this internal current, each pin will sink at least 10 mA, while maintaining the VOL specification of 0.4 V maximum.
2. –ERR, SLCT, BUSY, PE and –ACK are inputs with pull-up resistors of approximately 20 KΩ to cause them to float high similarly to TTL inputs.
3. TRI is an input with an internal pull-down resistor of approximately three KΩ. This allows this pin to be left as a NC in customer applications, and be driven high by a board level tester.

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