TB-515
TECHNICAL BULLETIN
SARA Chipset, TXC-05501/05601

Differences Between the "A" and "B" Versions of the SARA Chipset

PURPOSE OF THIS TECHNICAL BULLETIN

During August, 1995, TranSwitch issued an Informational Notification entitled Functional "B" SARA Devices Will Replace Functional "A" SARA Devices (Document Number TXC-05501-CIN2 Ed. 1, August 1995). This document indicated that functional "B" versions will be replacing the functional "A" versions, affecting devices with the following part numbers:

	Functional "A" Parts	Functional "B" Parts
SARA-S	TXC-05501-ACPQ	TXC-05501-BCPQ
SARA-R	TXC-05601-ACPQ	TXC-05601-BCPQ

The document also indicated that, relative to the current "A" SARA devices, the new speed-enhanced "B" SARA devices would operate at 65% higher clock speeds and consume 30% less power, while remaining form/fit/function backward compatible.

This Technical Bulletin is intended to document in detail the differences between the "A" versions of the SARA-R and SARA-S devices and the "B" versions, pending issue of a formal updated Edition of the SARA Chipset Technical Manual, which currently describes only the "A" versions (Document Number TXC-95000-TM Edition 5B, April 1995).

Documentation of the "B" version devices requires information only on their different DC and AC characteristics. All other characteristics are the same as described for the "A" versions in the Technical Manual. These DC and AC characteristics for the "A" versions are presented in sections 3.4 and 3.5 of the Technical Manual, respectively, where the +5V power supply current for each device is shown as 400 mA and the minimum clock period is shown as 50 ns (i.e., 20 MHz maximum). For the "B" version, these characteristics are represented by the revised forms of sections 3.4 and 3.5 that are included in this Technical Bulletin, where the +5V power supply current for each device is shown as 280 mA and the minimum clock period is shown as 30 ns (i.e., 33 MHz maximum).

The information for the functional "B" version devices that is contained in this Technical Bulletin will be added to the next Edition of the Technical Manual, which will serve as the descriptive technical document for both the "A" and "B" functional versions of the SARA chipset.

DC AND AC CHARACTERISTICS OF THE "B" FUNCTIONAL VERSION SARA CHIPSET

The following pages of this Technical Bulletin contain revised forms of sections 3.4 and 3.5 of the current SARA Chipset Technical Manual, which have been modified to reflect the characteristics of the "B" functional version SARA-S and SARA-R devices. The section, table and figure numbers used in the Technical Manual have been retained in this Technical Bulletin to facilitate comparison with the corresponding parts of the Technical Manual, which show the characteristics of the "A" version devices.

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3.4 DC Characteristics

Based on the temperature and supply voltage given below, Table 3-20 shows the DC Characteristics which are applicable to the "B" functional versions of each of the SARA-S and SARA-R devices. Table 3-21 shows the corresponding capacitance characteristics.

Temperature, T_A 0°C to 70°C

Supply Voltage, V_{CC} 4.75 V to 5.25V

Parameter Symbol	Parameter Description	Test Conditions	Min.	Max.	Unit
V_{IL}	Input Low Voltage			0.8	V
V_{IH}	Input High Voltage		2.0		V
V_{OL}	Output Low Voltage	I_{OL}=Max		0.4	V
V_{OH}	Output High Voltage	$I_{OH}=I_{OL}$	2.4		V
I_{OL}(open drain outputs)	Output Low Current			8.0	mA
I_{OL}(all other outputs)	Output Low Current			4.0	mA
I_{OH}	Output High Current			I_{OL}	mA
I_{OZ1}	Output Leakage Current	$0.4V < V_{OUT} < V_{CC}$	-10	10	µA
I_{OZ2}	Bi-Directional Tri-State I/O Output Leakage Current	$V_{OH} = V_{SS}$ or V_{CC}	-200	10	µA
I_{IX}	Input Leakage Current	$0V < V_{IN} < V_{CC}$	-10	200	µA
I_{CC}	Power Supply Current	V_{CC}=Max. f(CLK)=33 MHz		280	mA

Table 3-20. SARA DC Characteristics Over Commercial Operating Ranges

Parameter Symbol	Parameter Description	Test Conditions	Min.	Max.	Unit
C_{IN}	Input Pins[a]			10	pF
$C_{I/O}$	Bidirectional pins			10	pF
Output Drive Capability	Microprocessor Outputs			100	pF
	All Other Outputs			50	pF

Table 3-21. SARA Capacitance Characteristics

a. Unused input pins must be tied to inactive state.

3.5 AC Characteristics

3.5.1 Switching Characteristics

Table 3-22 shows the switching characteristics of both the SARA-R and SARA-S timings for the “B” functional version devices over commercial operating conditions. The significance of the timing parameter symbols is illustrated in section 3.5.2. The notation NA indicates “Not Applicable”.

Symbol	Parameter	SARA-S (TXC-05501-BCPQ)		SARA-R (TXC-05601-BCPQ)		Units
		Min	Max	Min	Max	
T1	Clock Period	30		30		ns
T2	Clock High	12		12		ns
T3	Clock Low	12		12		ns
T4	CCHLD to CLK Setup (SARA-R)	NA	NA	6		ns
T5	CLK to CCHLD Hold (SARA-R)	NA	NA	2		ns
T6	CLK to CCHLD Valid (SARA-S)		16	NA	NA	ns
T7	CCXFER to CLK Setup (SARA-S)	0		NA	NA	ns
T8	CLK to CCXFER Hold (SARA-S)	4		NA	NA	ns
T9	CLK to CCXFER Valid (SARA-R)	NA	NA		16	ns
T10	CCDATA to CLK Setup (SARA-S)	0		NA	NA	ns
T11	CLK to CCDATA Hold (SARA-S)	5		NA	NA	ns
T12	CLK to CCDATA Valid (SARA-R)	NA	NA		16	ns
T13	CBRXMIT to CLK Setup (SARA-S)	Async.		NA	NA	ns
T14	CLK to CBRXMIT Hold (SARA-S)	Async.		NA	NA	ns
T15	CLK to CBRDONE Valid (SARA-S)		16	NA	NA	ns
T16	CLK to CBRMT* Valid (SARA-R)	NA	NA		16	ns
T21	WRT, A(7:0), D(15:0) to CS*, DS* Setup	0		0		ns
T22	CS*, DS* to WRT, A(7:0), D(15:0) Hold	0		0		ns
T23	CS*, DS* to RDY* Low		(3*T1 + 21)		(3*T1 + 21)	ns
T24	CS*, DS* to RDY* Deasserted		14		14	ns
T25	CS*, DS* to D(15:0) Enabled (Read)	0		0		ns
T26	D(15:0) to RDY* Setup		(T1 - 18)		(T1 - 18)	ns
T27	CS*, DS* to D(15:0) Deasserted (Read)		20		20	ns
T28	CS*, DS* High	(1.5 * T1)		(1.5 * T1)		ns

Table 3-22. Switching Characteristics over Commercial Operating Conditions

Symbol	Parameter	SARA-S (TXC-05501-BCPQ)		SARA-R (TXC-05601-BCPQ)		Units
		Min	Max	Min	Max	
T29	INTR* High	(4 *T1 - 24)		(4 *T1 - 24)		ns
T30	RST* Low	(3*T1 + 5)		(3*T1 + 5)		ns
T31	CLAV to CLK Setup (SARA-R)	NA	NA	2		ns
T32	CLK to CLAV Hold (SARA-R)	NA	NA	5		ns
T33	CLK to FFRD(0) Valid (SARA-R)	NA	NA		14	ns
T34	FFMT to CLK Setup (SARA-R)	NA	NA	4		ns
T35	CLK to FFMT Hold (SARA-R)	NA	NA	2		ns
T36	FFD(17:0) to CLK Setup (SARA-R)	NA	NA	8		ns
T37	CLK to FFD(17:0) Hold (SARA-R)	NA	NA	3		ns
T38	CLK to FFLUSH Valid (SARA-R)	NA	NA		15	ns
T39	FLSHDONE to CLK Setup (SARA-R)	NA	NA	2		ns
T40	CLK to FLSHDONE Hold (SARA-R)	NA	NA	5		ns
T41	RDCLK to CELAVL* Valid (SARA-S)		11	NA	NA	ns
T42	RDEN to RDCLK Setup (SARA-S)	8		NA	NA	ns
T43	RDCLK to RDEN Hold (SARA-S)	2		NA	NA	ns
T44	RDCLK to FFD(17:0) Valid (SARA-S)		11	NA	NA	ns
T45	RDCLK Period	T1		T1		ns
T46	RDCLK Low	T3		T3		ns
T47	RDCLK High	T2		T2		ns
T51	CLK to CREQ Valid		13		13	ns
T52	CLK to CMULR Valid		13		13	ns
T53	CGRT to CLK Setup	4		8		ns
T54	CLK to CGRT Hold	4				ns
T55	CLK to CCYCST* Valid		11		11	ns
T56	CRDY* to CLK Setup	5		8		ns
T57	CLK to CRDY* Hold	4				ns
T58	CLK to CWRT Valid		11		12	ns
T59	CGRT to CA(23:0) Asserted		10		10	ns
T60	CLK to CA(23:0) Valid		9		10	ns

Table 3-22. Switching Characteristics over Commercial Operating Conditions

Symbol	Parameter	SARA-S (TXC-05501-BCPQ)		SARA-R (TXC-05601-BCPQ)		Units
		Min	Max	Min	Max	
T61	CLK to CA(23:0) Deasserted		15		15	ns
T62	CD(17:0) to CLK Setup (Read)	5		8		ns
T63	CLK to CD(17:0) Hold (Read)	3		3		ns
T64	CLK to CD(17:0) Asserted (Write)		11		13	ns
T65	CLK to CD(17:0) Valid (Write)		11		13	ns
T66	CLK to CD(17:0) Deasserted (Write)		15		15	ns
T71	CLK to PREQ Valid		12		12	ns
T72	PGRT to CLK Setup	8		8		ns
T73	CLK to PGRT Hold	3		3		ns
T74	CLK to PCYCST* Valid		10		10	ns
T75	PRDY* to CLK Setup	6		4		ns
T76	CLK to PRDY* Hold	4		4		ns
T77	CLK to PA(15:0) Asserted		13		11	ns
T78	CLK to PA(15:0) Valid		13		11	ns
T79	CLK to PA(15:0) Deasserted		15		15	ns
T80	CLK to PD(31:0) Asserted (PM Address)		12		11	ns
T81	CLK to PD(31:0) Deasserted		15		15	ns
T82	PD(35:0) to CLK Setup (SARA-S Read)	8		NA	NA	ns
T83	CLK to PD(35:0) Hold (SARA-S Read)	4		NA	NA	ns
T84	PLWADR to PA(15:0) Valid		13		13	ns
T85	CLK to PAMTCH Valid		17		17	ns
T86	CLK to PD(35:0) Valid (SARA-R Write)	NA	NA		11	ns
T87	CLK to PD(35:0) Deasserted (SARA-R Write)	NA	NA		15	ns

Table 3-22. Switching Characteristics over Commercial Operating Conditions

3.5.2 Interface Signal Timings

Figure 3-20 through Figure 3-28 show the timings for the congestion control interface, processor, cell interface, control memory interface, and packet memory interface for both the SARA-R and SARA-S.

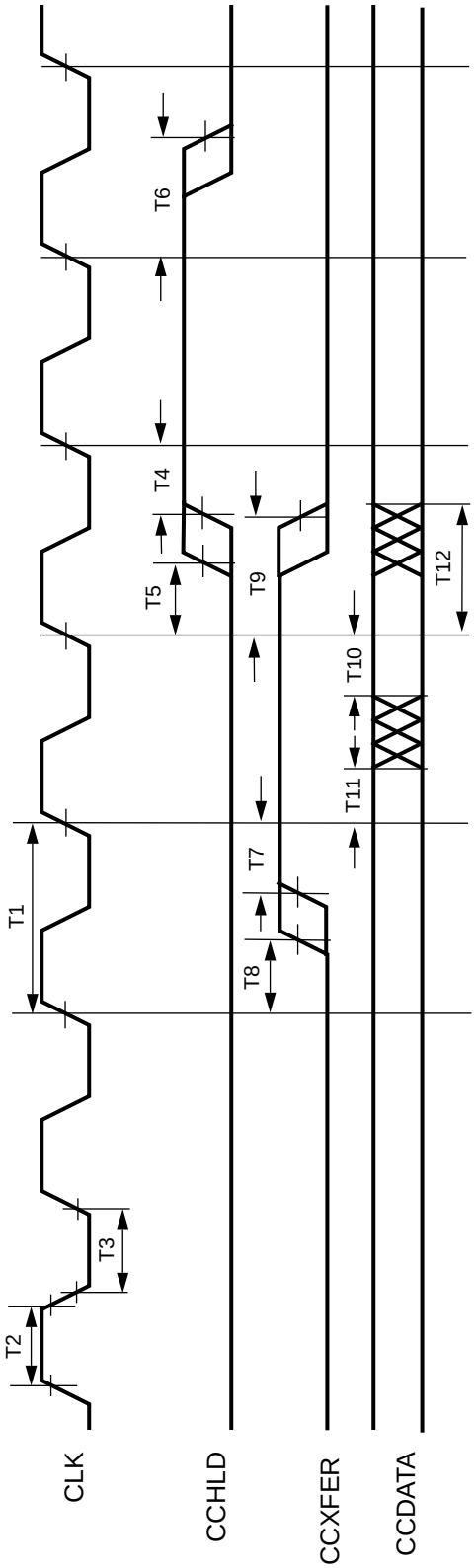


Figure 3-20. Congestion-Control Interface Signals Between the SARA-S and SARA-R

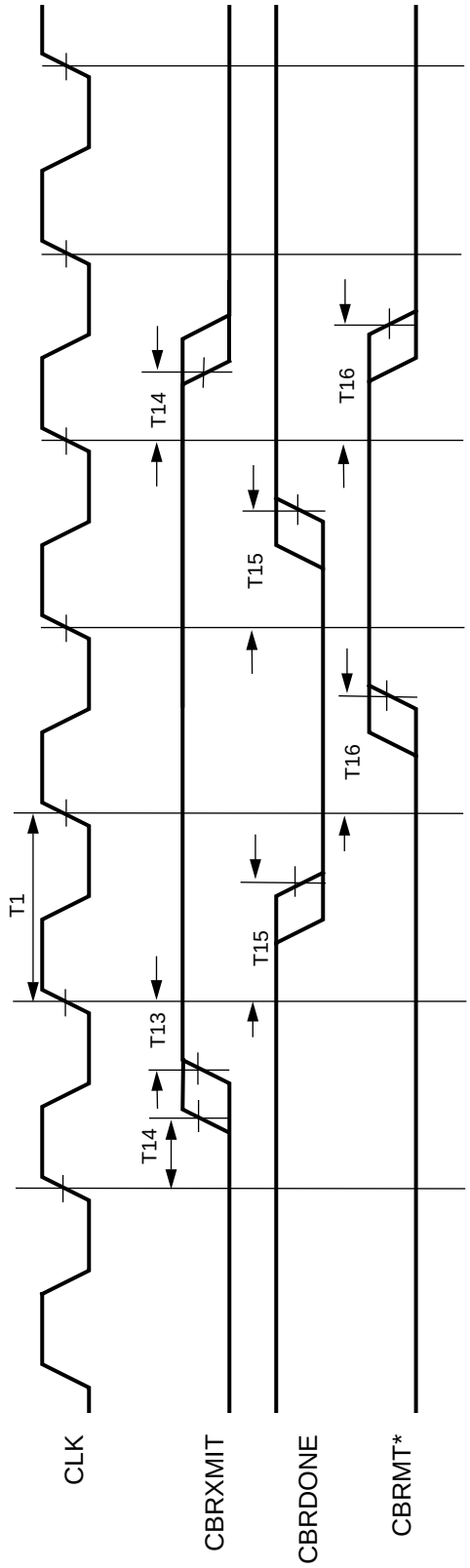


Figure 3-21. Constant Bit Rate Interface Signals of SARA-S & SARA-R

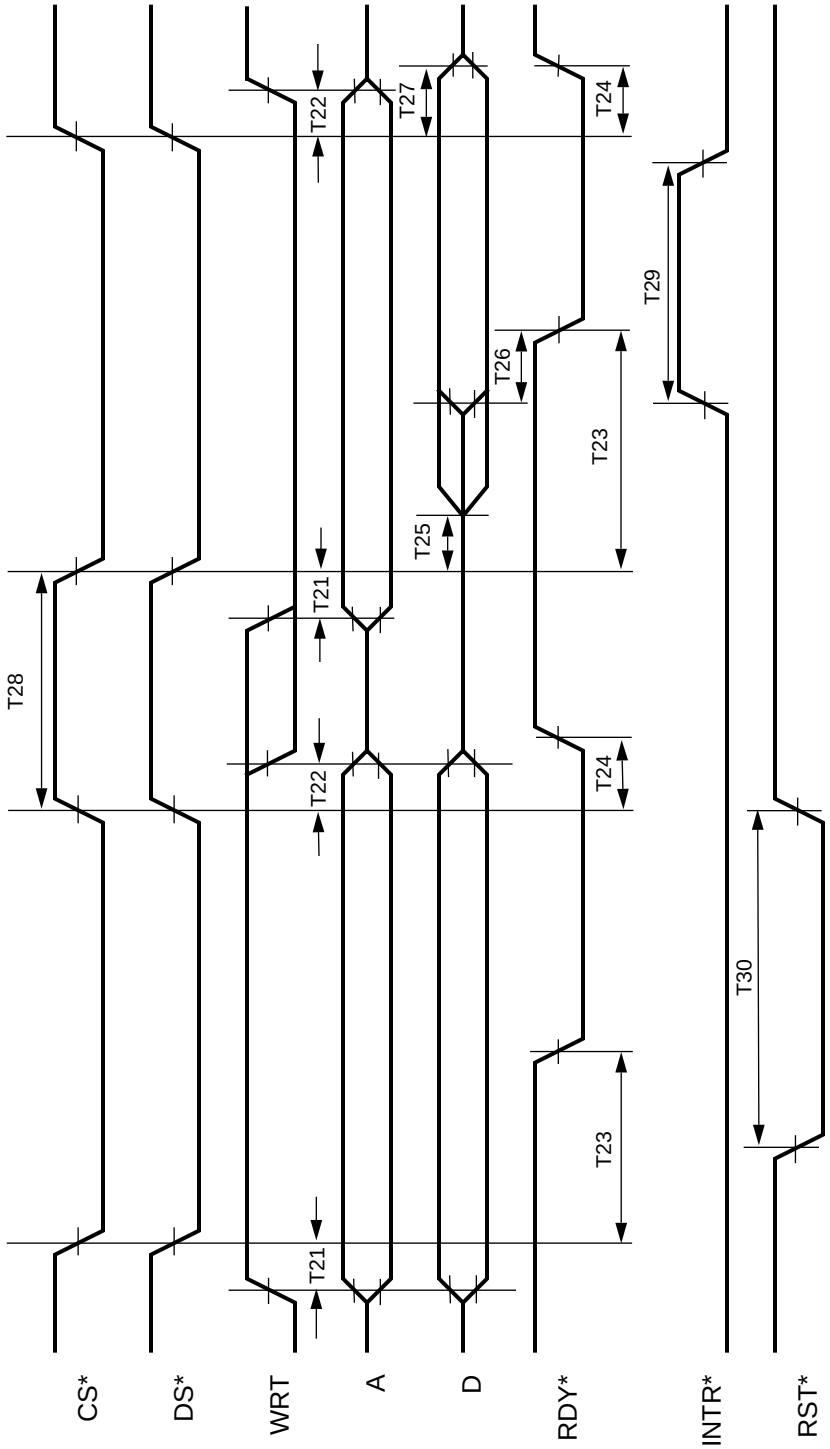


Figure 3-22. Processor-Interface Signal Timing

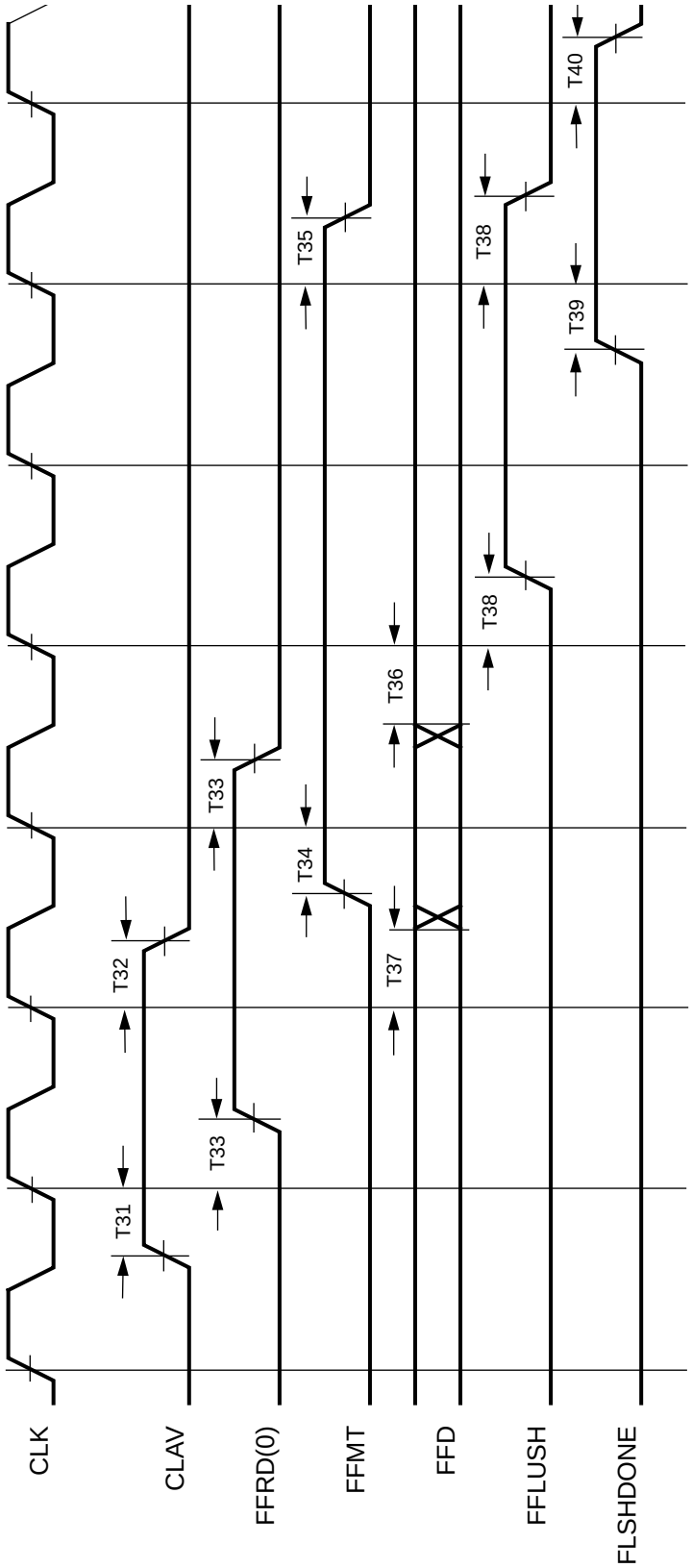
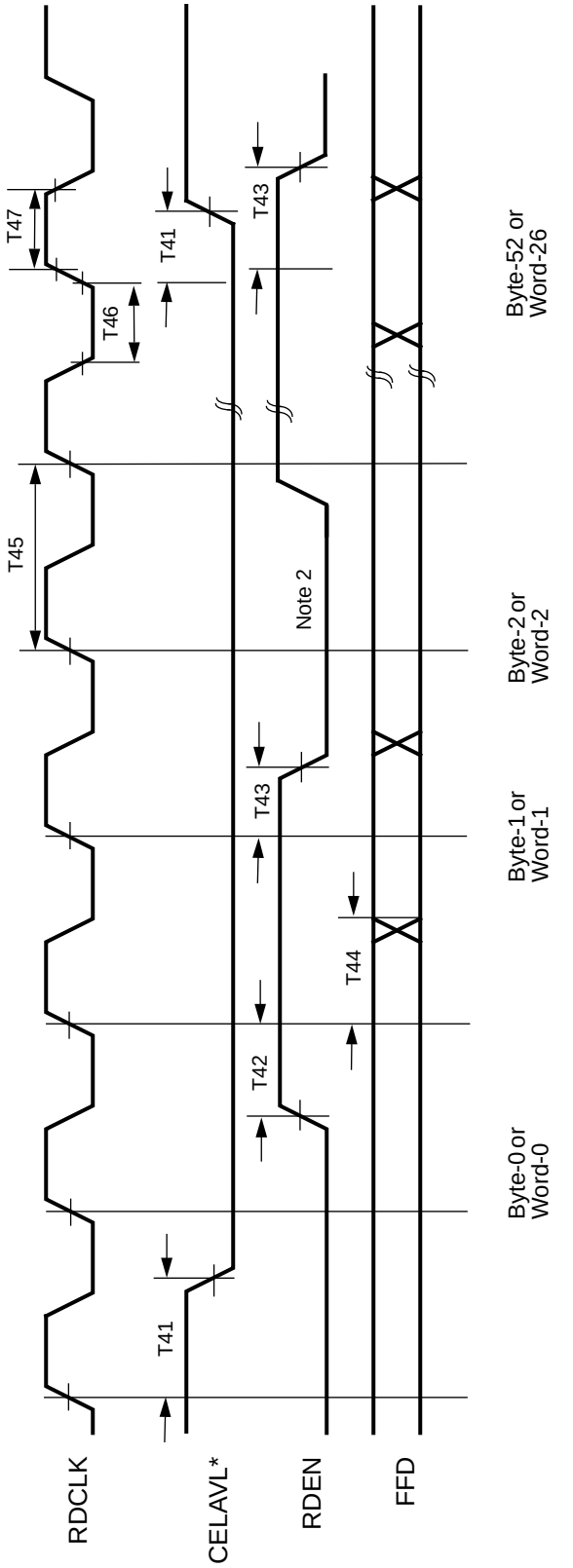


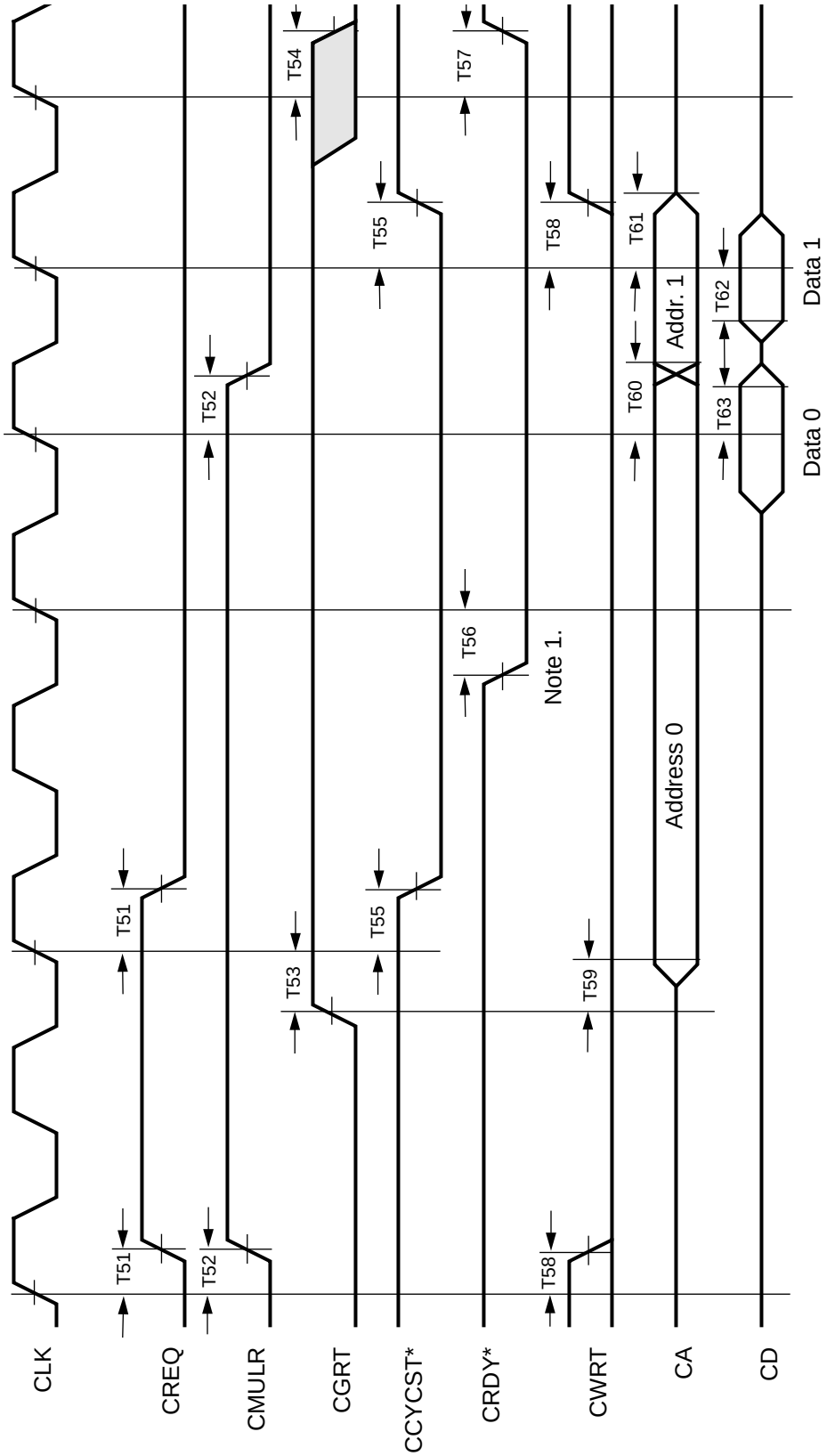
Figure 3-23. Cell-Interface Signals for the SARA-R



Note:

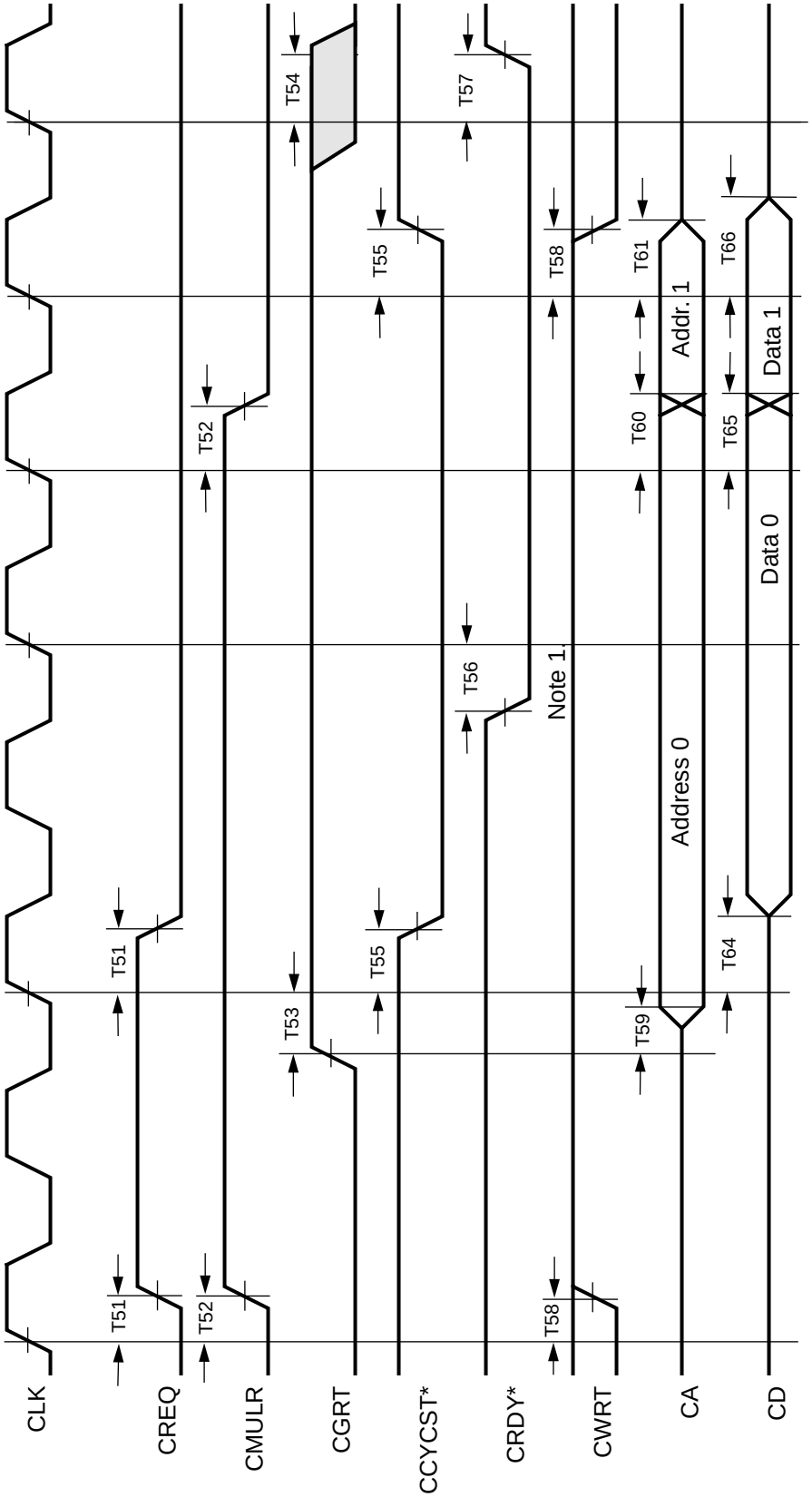
1. CELAVL* will be active for the entire cell transfer duration.
2. RDEN can be held false to temporarily freeze data transfer.

Figure 3-24. Cell-Interface Signals for the SARA-S



Note:
1. Data transfer does not occur on the very first clock cycle when CRDY becomes active.
2. Mode settings are:CM_WAIT_EN=1 and CM_EARLY_WR=0.

Figure 3-25. Control Memory Interface Signal Timing-Read Operation



Note:

1. Data transfer does not occur on the very first clock cycle when CRDY becomes active.
2. Mode settings are:CM_WAIT_EN=1 and CM_EARLY_WR=0.

Figure 3-26. Control Memory Interface Signal Timings-Write Operation

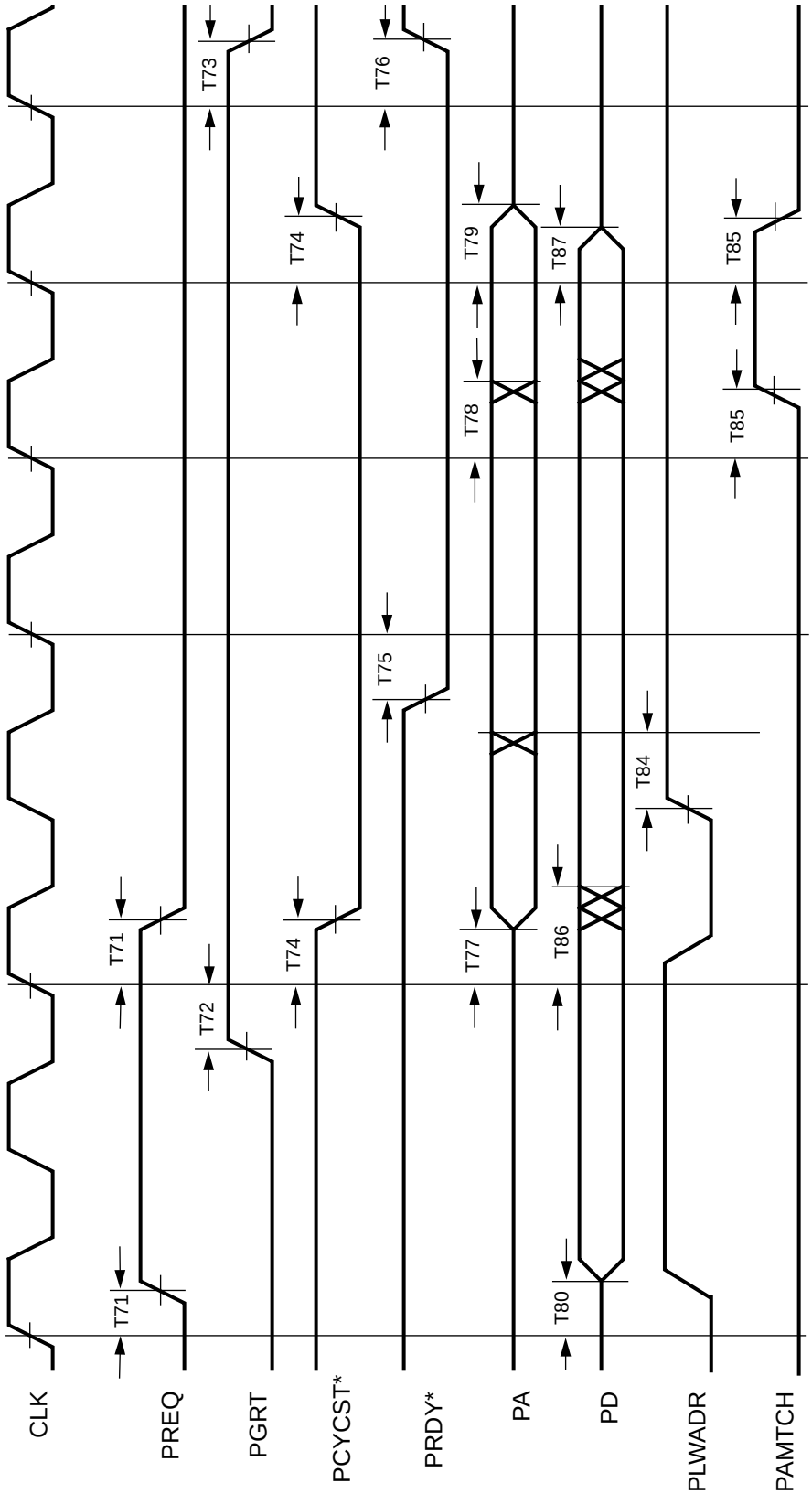


Figure 3-27. Packet Memory Interface Signal Timings-Write Operation for the SARA-R

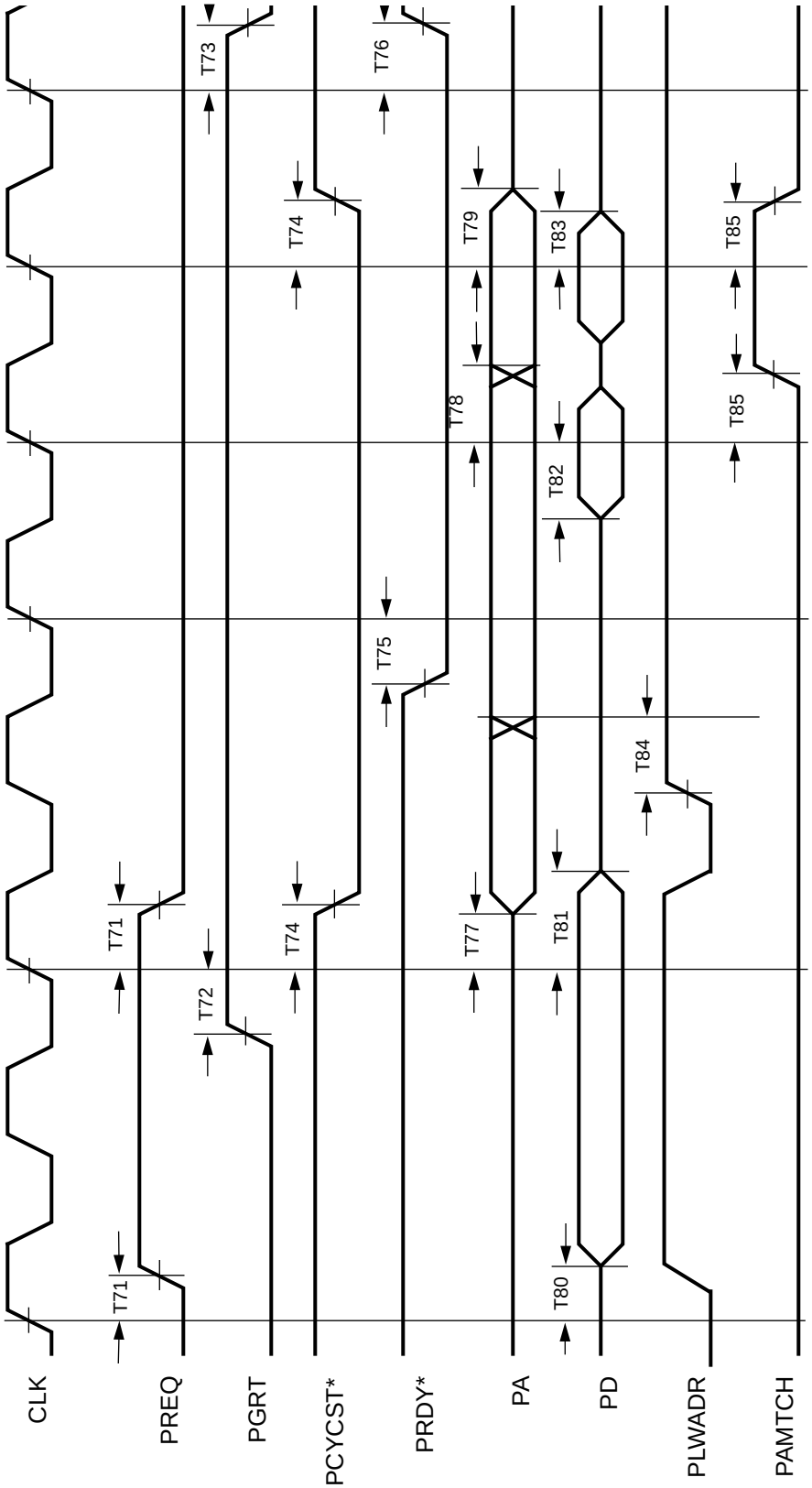
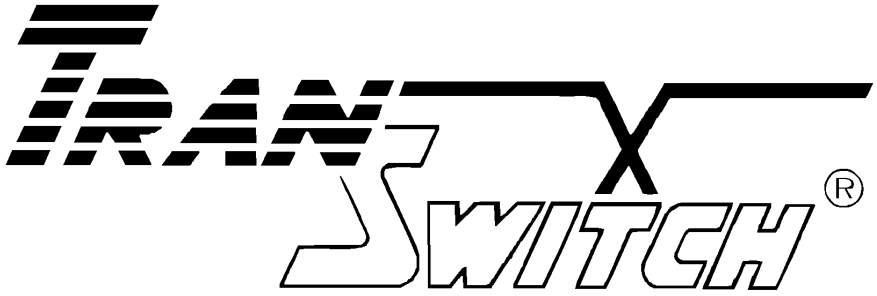


Figure 3-28. Packet Memory Interface Signal Timings-Read Operation for the SARA-S

- NOTES -



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