TMS28F010
1 048 576-BIT FLASH
ELECTRICALLY ERASABLE PROGRAMMABLE READ-ONLY MEMORY

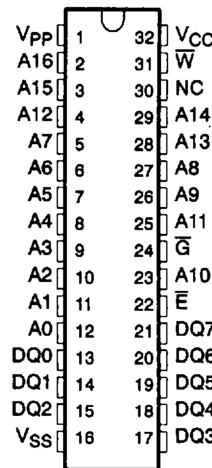
SMJS011A–DECEMBER 1992–REVISED MARCH 1993

- **Organization . . . 128K × 8-Bit Flash Memory**
- **Pin Compatible with Existing 1-Megabit EPROMs**
- **All Inputs/Outputs TTL Compatible**
- **Maximum Access/Minimum Cycle Time**

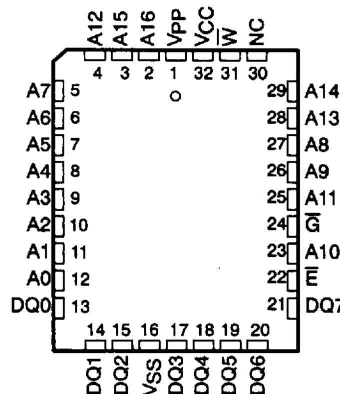
V_{CC} ± 10%	
'28F010-10	100 ns
'28F010-12	120 ns
'28F010-15	150 ns
'28F010-17	170 ns

- **Industry-Standard Programming Algorithm**
- **PEP4 Version Available With 168-Hour Burn-In, and Choice of Operating Temperature Ranges**
- **Chip Erase Before Reprogramming**
- **10 000, 1 000, and 100 Program/Erase Cycle Versions Available**
- **Low Power Dissipation (V_{CC} = 5.50 V)**
  - **Active Write . . . 55 mW**
  - **Active Read . . . 165 mW**
  - **Electrical Erase . . . 82.5 mW**
  - **Standby . . . 0.55 mW (CMOS-Input Levels)**
- **Automotive Temperature Range: – 40°C to + 125°C**

N PACKAGE†
(TOP VIEW)



FM PACKAGE†
(TOP VIEW)



† The packages shown are for pinout reference only.

PIN NOMENCLATURE	
A0–A16	Address Inputs
$\overline{E}$	Chip Enable
$\overline{G}$	Output Enable
NC	No Internal Connection
$\overline{W}$	Write Enable
DQ0–DQ7	Data In/Data Out
V_{CC}	5-V Power Supply
V_{PP}	12-V Power Supply
V_{SS}	Ground

description

The TMS28F010 is a 1048 576-bit, programmable read-only memory that can be electrically bulk-erased and reprogrammed.

The TMS28F010 is available in 10 000, 1 000, and 100 program/erase endurance cycle versions.

The TMS28F010 Flash EEPROM is offered in a dual in-line plastic package (N suffix) designed for insertion in mounting-hole rows on 15,2 mm (600-mil) centers, a 32-lead plastic leaded-chip carrier package using 1,25 mm (50-mil) lead spacing (FM suffix), a 32-lead thin small outline package (DD suffix), and a reverse pinout TSOP package (DU suffix).

The TMS28F010 is offered with three choices of temperature ranges of 0°C to 70°C (NL, FML, DDL, and DUL suffixes), –40°C to 85°C (NE, FME, DDE, and DUE suffixes), and –40°C to 125°C (NQ, FMQ, DDQ, and DUQ suffixes). All package types are offered with 168 hour burn-in (4 suffix).

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ADVANCE INFORMATION concerns new products in the sampling or preproduction phase of development. Characteristic data and other specifications are subject to change without notice.

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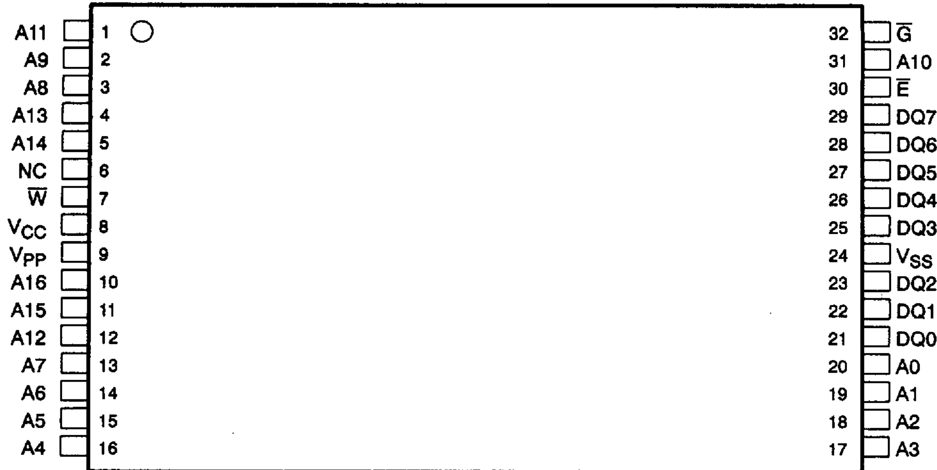
DD PACKAGE†
(TOP VIEW)



DU PACKAGE†
REVERSE PINOUT
(TOP VIEW)

† The packages shown are for pinout reference only.

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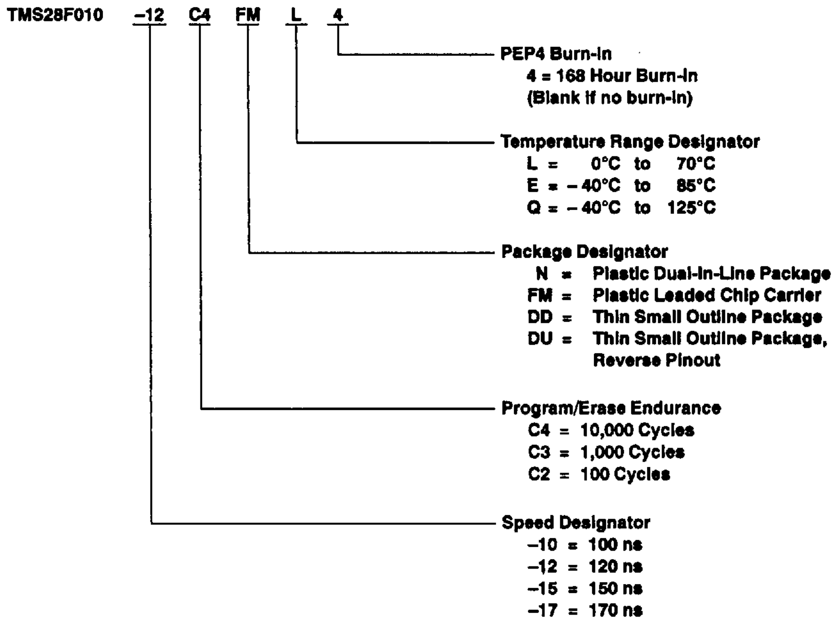
device symbol nomenclature



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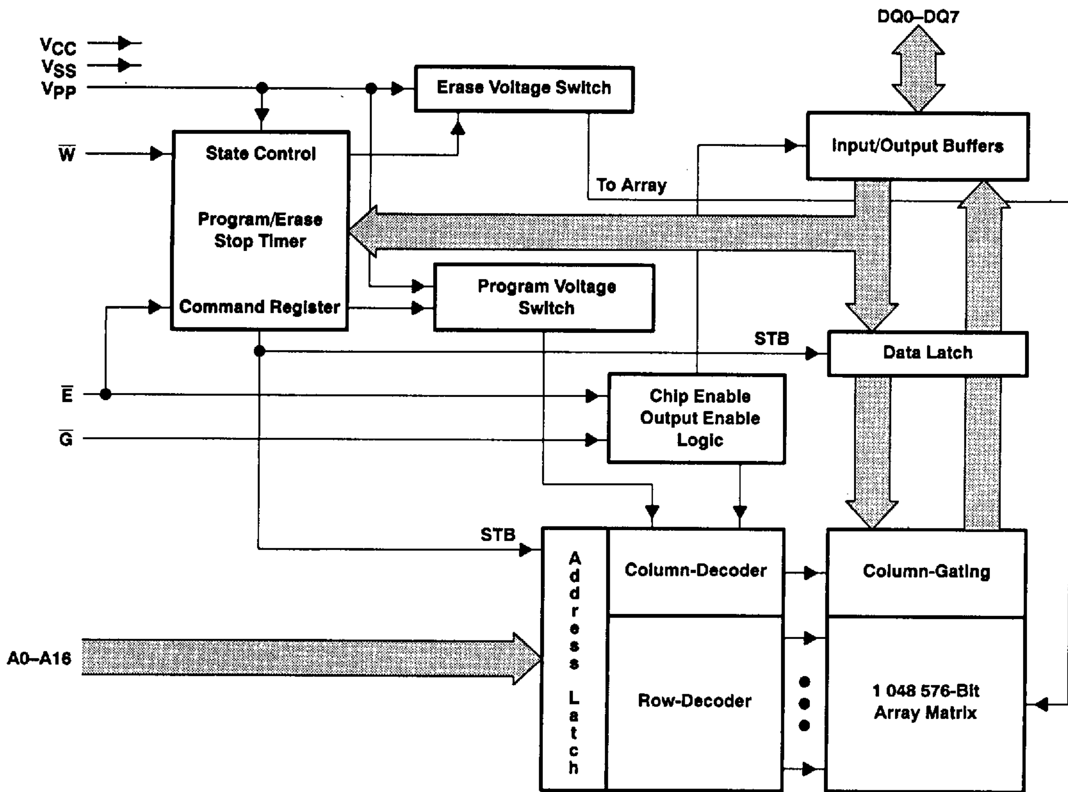
functional block diagram



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TEXAS INSTR (ASIC/MEMORY)

Table 1. Operation Modes

MODE†		FUNCTION						
		Vpp§ (1)	$\overline{E}$ (22)	$\overline{G}$ (24)	A0 (12)	A9 (26)	$\overline{W}$ (31)	DQ0–DQ7 (13–15, 17–21)
Read	Read	V_{PPL}	V_{IL}	V_{IL}	X†	X	V_{IH}	Data Out
	Output Disable	V_{PPL}	V_{IL}	V_{IH}	X	X	V_{IH}	HI-Z
	Standby and Write Inhibit	V_{PPL}	V_{IH}	X	X	X	X	HI-Z
	Signature Mode	V_{PPL}	V_{IL}	V_{IL}	V_{IL}	V_H‡	V_{IH}	MFG Code 97h
					V_{IH}			Device Code 75h
Read/Write	Read	V_{PPH}	V_{IL}	V_{IL}	X	X	V_{IH}	Data Out
	Output Disable	V_{PPH}	V_{IL}	V_{IH}	X	X	V_{IH}	HI-Z
	Standby and Write Inhibit	V_{PPH}	V_{IH}	X	X	X	X	HI-Z
	Write	V_{PPH}	V_{IL}	V_{IH}	X	X	V_{IL}	Data In

† X can be V_{IL} or V_{IH}
‡ $11.5\ V < V_H < 13.0\ V$
§ $V_{PPL} \le V_{CC} + 2\ V$; V_{PPH} is the programming voltage specified for the device. For more details, refer to the recommended operating conditions.

operation

read/output disable

When the outputs of two or more TMS28F010s are connected in parallel on the same bus, the output of any particular device in the circuit can be read with no interference from the competing outputs of other devices.

To read the output of the TMS28F010, a low-level signal is applied to the $\overline{E}$ and $\overline{G}$ pins. All other devices in the circuit should have their outputs disabled by applying a high-level signal to one of these pins.

standby and write inhibit

Active I_{CC} current can be reduced from 30 mA to 1 mA by applying a high TTL level on $\overline{E}$ or to 100 µA with a high CMOS level on $\overline{E}$. In this mode, all outputs are in the high-impedance state. The TMS28F010 draws active current when it is deselected during programming, erasure, or program/erase verification. It will continue to draw active current until the operation is terminated.

signature mode

The signature mode provides access to a binary code identifying the manufacturer and device type. This mode is activated when A9 (pin 26) is forced to V_H. Two identifier bytes are accessed by toggling A0. All other addresses must be held low. A0 low selects the manufacturer's code 97h, and A0 high selects the device code 75h, as shown in the signature mode table below:

IDENTIFIER†	PINS									
	A0	DQ7	DQ6	DQ5	DQ4	DQ3	DQ2	DQ1	DQ0	HEX
Manufacturer Code	V_{IL}	1	0	0	1	0	1	1	1	97
Device Code	V_{IH}	0	1	1	1	0	1	0	1	75

† $\overline{E} = \overline{G} = V_{IL}$, A1–A8 = V_{IL}, A9 = V_H, A10–A16 = V_{IL}, $V_{PP} = V_{PPL}$.

programming and erasure

In the erased state, all bits are at a logic 1. Before erasing the device, all memory bits must be programmed to a logic 0. Afterwards, the entire chip is erased. At this point, the bits, now logic 1's, may be programmed accordingly. Refer to the Fastwrite and Fasterase algorithms for further detail.

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command register

The command register controls the program and erase functions of the TMS28F010. The signature mode may be activated using the command register in addition to the above method. When V_{PP} is high, the contents of the command register, and therefore the function being performed, may be changed. The command register is written to when $\overline{E}$ is low and $\overline{W}$ is pulsed low. The address is latched on the leading edge of the pulse, while the data is latched on the trailing edge. Accidental programming or erasure is minimized because two commands must be executed to invoke either operation.

power supply considerations

Each device should have a 0.1 µF ceramic capacitor connected between V_{CC} and V_{SS} to suppress circuit noise. Changes in current drain on V_{PP} will require it to have a bypass capacitor as well. Printed circuit traces for both power supplies should be appropriate to handle the current demand.

Table 2. Command Definitions

COMMAND	REQUIRED BUS CYCLES	FIRST BUS CYCLE			SECOND BUS CYCLE		
		OPERATION (see Note 1)	ADDRESS	DATA	OPERATION	ADDRESS	DATA
Read	1	Write	X	00h	Read	RA	RD
Signature Mode	3	Write	X	90h	Read	0000 0001	97h 75h
Set-up Erase/Erase	2	Write	X	20h	Write	X	20h
Erase Verify	2	Write	EA†	A0h	Read	X	EVD
Set-up Program/Program	2	Write	X	40h	Write	PA	PD
Program Verify	2	Write	X	C0h	Read	X	PVD
Reset	2	Write	X	FFh	Write	X	FFh

NOTE 1: Modes of operation are defined in Table 1.

† Description of Terms

- EA Address of memory location to be read during erase verify.
- RA Address of memory location to be read.
- PA Address of memory location to be programmed. Address is latched on the falling edge of $\overline{W}$.
- RD Data read from location RA during the read operation.
- EVD Data read from location EA during erase verify.
- PD Data to be programmed at location PA. Data is latched on the rising edge of $\overline{W}$.
- PVD Data read from location PA during program verify.

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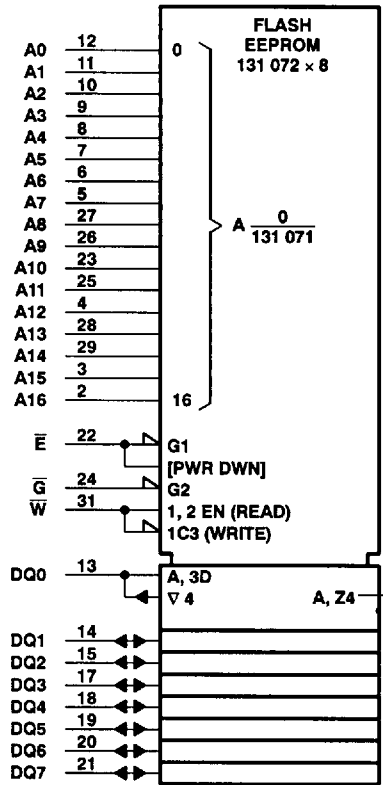
logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for the N package.

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command definitions

read command

Memory contents can be accessed while V_{PP} is high or low. When V_{PP} is high, writing 00h into the command register invokes the read operation. Also, when the device is powered up, the default contents of the command register are 00h and the read operation is enabled. The read operation remains enabled until a different, valid command is written to the command register.

signature mode command

The signature mode is activated by writing 90h into the command register. The manufacturer's code (97h) is identified by the value read from address location 0000h, and the device code (75h) is identified by the value read from address location 0001h.

set-up erase/erase commands

The erase algorithm initiates with $\overline{E} = V_{IL}$, $\overline{W} = V_{IL}$, $\overline{G} = V_{IH}$, V_{PP} = 12 V, and V_{CC} = 5 V. To enter the erase mode, write the set-up erase command, 20h, into the command register. After the TMS28F010 is in the erase mode, writing a second erase command, 20h, into the command register invokes the erase operation. The erase operation begins on the rising edge of $\overline{W}$ and ends on the rising edge of the next $\overline{W}$. The erase operation requires 10 ms to complete before the erase-verify command, A0h, can be loaded.

Maximum erase timing is controlled by the internal stop timer. When the stop timer terminates the erase operation, the device enters an inactive state and remains inactive until a valid erase verify, read, or reset command is received.

erase-verify command

All bytes must be verified following an erase operation. After the erase operation is complete, an erased byte can be verified by writing the erase-verify command, A0h, into the command register. This command causes the device to exit the erase mode on the rising edge of $\overline{W}$. The address of the byte to be verified is latched on the falling edge of $\overline{W}$. The erase-verify operation remains enabled until a valid command is written to the command register.

To determine whether or not all the bytes have been erased, the TMS28F010 applies a margin voltage to each byte. If FFh is read from the byte, then all bits in the designated byte have been erased. The erase-verify operation continues until all of the bytes have been verified. If FFh is not read from a byte, then an additional erase operation needs to be executed. Figure 2 shows the combination of commands and bus operations for electrically erasing the TMS28F010.

set-up program/program commands

The programming algorithm initiates with $\overline{E} = V_{IL}$, $\overline{W} = V_{IL}$, $\overline{G} = V_{IH}$, V_{PP} = 12 V, and V_{CC} = 5 V. To enter the programming mode, write the set-up program command, 40h, into the command register. The programming operation will be invoked by the next write-enable pulse. Addresses are latched internally on the falling edge of $\overline{W}$, and data is latched internally on the rising edge of $\overline{W}$. The programming operation begins on the rising edge of $\overline{W}$ and ends on the rising edge of the next $\overline{W}$ pulse. The program operation requires 10 μs for completion before the program-verify command, C0h, can be loaded.

Maximum program timing is controlled by the internal stop timer. When the stop timer terminates the program operation, the device enters an inactive state and remains inactive until a valid program verify, read, or reset command is received.

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program-verify command

The TMS28F010 can be programmed sequentially or randomly because it is programmed one byte at a time. Each byte must be verified after it is programmed.

The program-verify operation prepares the device to verify the most recently programmed byte. To invoke the program-verify operation, C0h must be written into the command register. The program-verify operation will end on the rising edge of $\overline{W}$.

While verifying a byte, the TMS28F010 applies an internal margin voltage to the designated byte. If the true data and programmed data match, programming can continue to the next designated byte location; otherwise, the byte must be reprogrammed. Figure 1 shows how commands and bus operations are combined for byte programming.

reset command

To reset the TMS28F010 after set-up erase command or set-up program command operations without changing the contents in memory, write FFh into the command register two consecutive times. After executing the reset command, a valid command must be written into the command register to change to a new state.

Fastwrite algorithm

The TMS28F010 is programmed using the Texas Instruments Fastwrite algorithm shown in Figure 1. This algorithm programs in a nominal time of two seconds.

Fasterase algorithm

The TMS28F010 is erased using the Texas Instruments Fasterase algorithm shown in Figure 2. The memory array needs to be completely programmed (using the Fastwrite algorithm) before erasure begins. Erasure typically occurs in one second.

parallel erasure

To reduce total erase time, several devices may be erased in parallel. Since each Flash EEPROM may erase at a different rate, every device must be verified separately after each erase pulse. After a given device has been successfully erased, the erase command should not be issued to this device again. All devices that complete erasure should be masked until the parallel erasure process is finished. See Figure 3, Parallel Erase Flow Diagram.

Examples of how to mask a device during parallel erase include driving the device's $\overline{E}$ pin high, writing the read command (00h) to the device when the others receive a setup erase or erase command, or disconnecting it from all electrical signals with relays or other types of switches.

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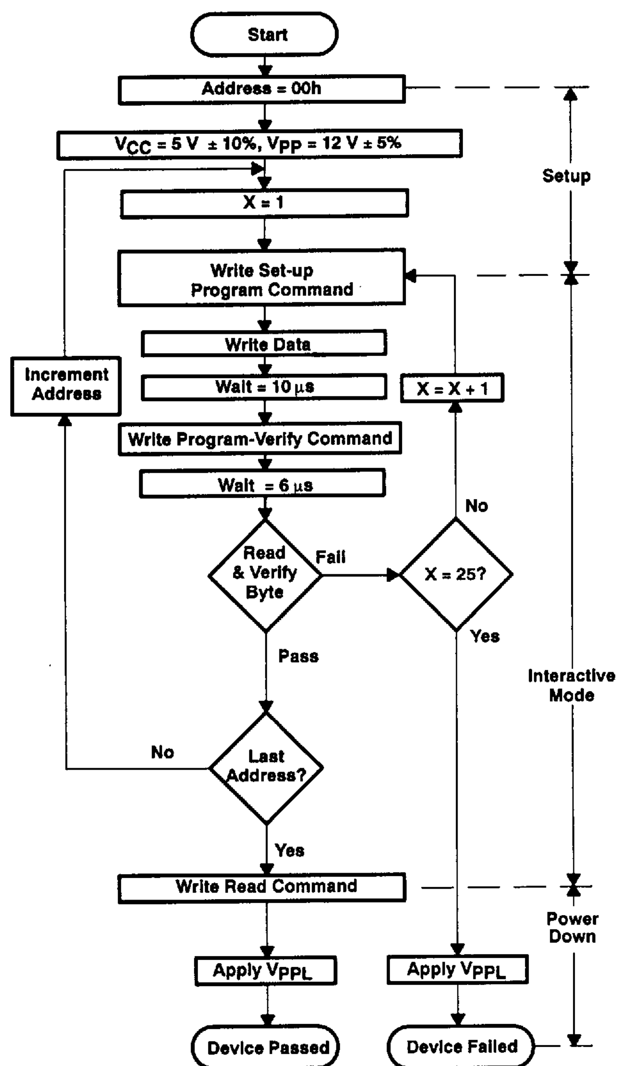

Bus Operation	Command	Comments
Initialize Address		
Standby		Wait for Vpp to Ramp to V_{PPH} (see Note 2) Initialize Pulse Count
Write	Set Up Program Write	Data = 40h
Write	Write Data	Valid Address/Data
Standby		Wait = 10 µs
Write	Program-Verify	Data = C0h; Ends Program Operation
Standby		Wait = 6 µs
Read		Read Byte to Verify Programming; Compare Output to Expected Output
Write	Read	Data = 00h; Resets Register for Read Operations
Standby		Wait for Vpp to Ramp to V_{PPL} (see Note 3)

NOTES: 2. Refer to the recommended operating conditions for the value of V_{PPH}.
3. Refer to the recommended operating conditions for the value of V_{PPL}.

Figure 1. Programming Flowchart: Fastwrite Algorithm

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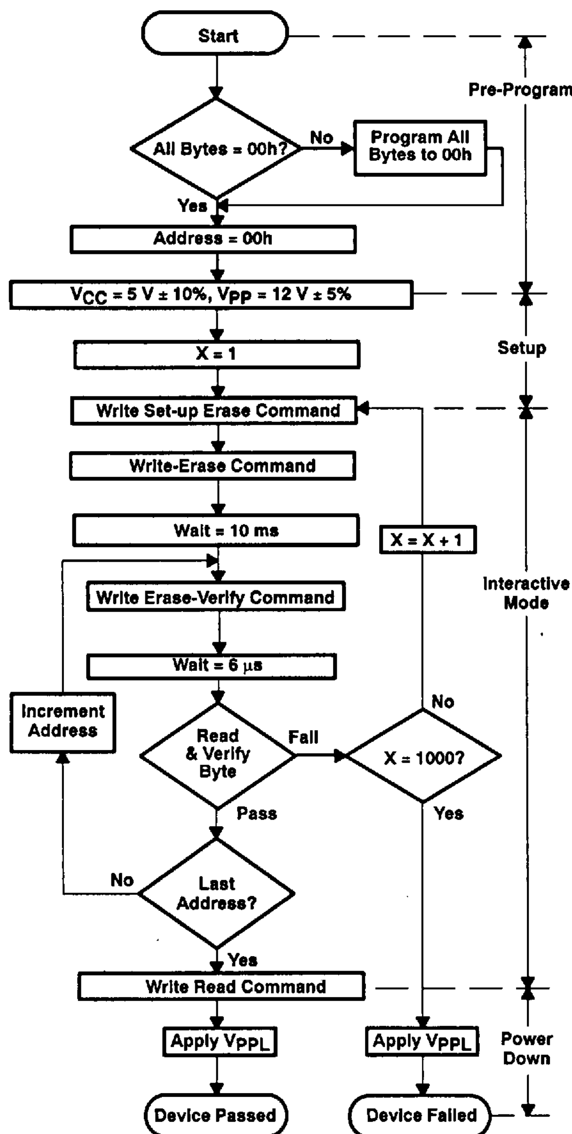

Bus Operation	Command	Comments
		Entire Memory Must = 00h Before Erasure Use Fastwrite Programming Algorithm
		Initialize Addresses
Standby		Wait for Vpp to Ramp to V_{PPH} (see Note 2)
		Initialize Pulse Count
Write	Set Up Erase	Data = 20h
Write	Erase	Data = 20h
Standby		Wait = 10 ms
Write	Erase Verify	Addr = Byte to Verify; Data = A0h; Ends the Erase Operation
Standby		Wait = 6 µs
Read		Read Byte to Verify Erasure; Compare Output to FFh
Write	Read	Data = 00h; Resets Register for Read Operations
Standby		Wait for Vpp to Ramp to V_{PPL} (see Note 3)

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NOTES: 2 Refer to the recommended operating conditions for the value of V_{PPH}.
3 Refer to the recommended operating conditions for the value of V_{PPL}.

Figure 2. Flash-Erase Flowchart: Fasterase Algorithm

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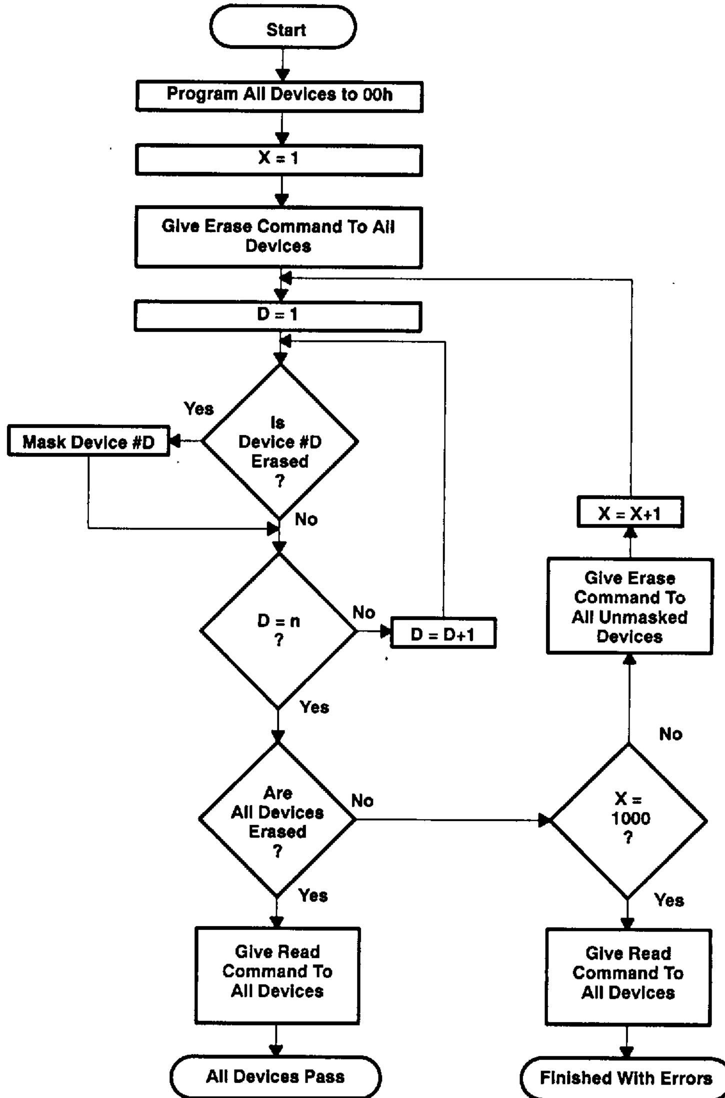

NOTE: n = number of devices being erased.

Figure 3. Parallel-Erase Flow Diagram

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} (see Note 4)	−0.6 V to 7 V
Supply voltage range, V_{PP}	−0.6 V to 14 V
Input voltage range (see Note 5): All inputs except A9	−0.6 V to V_{CC} + 1 V
A9 (see Note 5)	−0.6 V to 13.5 V
Output voltage range (see Note 6)	−0.6 V to V_{CC} + 1 V
Operating free-air temperature range during read/erase/program (NL, FML, DDL, DUL)	0°C to 70°C
Operating free-air temperature range during read/erase/program (NE, FME, DDE, DUE)	− 40°C to 85°C
Operating free-air temperature range during read/erase/program (NQ, FMQ, DDQ, DUQ)	− 40° C to 125°C
Storage temperature range	−65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 4. All voltage values are with respect to GND.
5. The voltage on any input pin may undershoot to −2.0 V for periods less than 20 ns.
6. The voltage on any output pin may overshoot to 7.0 V for periods less than 20 ns.

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recommended operating conditions

			'28F010-10 '28F010-12 '28F010-15 '28F010-17 MIN	TYP	MAX	UNIT
V_{CC} Supply voltage	During write/read/flash erase		4.5	5	5.5	V
V_{PP} Supply voltage	During read only (V_{PPL})		0		$V_{CC}+2$	V
	During write/read/flash erase (V_{PPH})		11.4	12	12.6	V
V_{IH} High-level dc input voltage		TTL	2		V_{CC}+0.5	V
		CMOS	$V_{CC}-0.5$		V_{CC}+0.5	
V_{IL} Low-level dc input voltage		TTL	−0.5		0.8	V
		CMOS	GND − 0.2		GND+0.2	

electrical characteristics over full ranges of operating conditions

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OH} High-level output voltage		I_{OH} = − 2.5 mA	2.4			V
		I_{OH} = − 100 μA	$V_{CC}-0.4$			
V_{OL} Low-level output voltage		I_{OL} = 5.8 mA			0.45	V
		I_{OL} = 100 μA			0.1	
I_I Input current (leakage)	All except A9	V_I = 0 to 5.5 V			±1	μA
	A9	VI = 0 to 13 V			± 200	
I_O Output current (leakage)		V_O = 0 to V_{CC}			±10	μA
I_{PP1} V_{PP} supply current (read/standby)		V_{PP} = V_{PPH}, read mode			200	μA
		VPP = V_{PPL}			±10	μA
I_{PP2} V_{PP} supply current (during program pulse) (see Note 7)		V_{PP} = V_{PPH}			30	mA
I_{PP3} V_{PP} supply current (during flash erase) (see Note 7)		V_{PP} = V_{PPH}			30	mA
I_{PP4} VPP supply current (during program/erase verify) (see Note 7)		V_{PP} = V_{PPH}			5.0	mA
I_{CCS} V_{CC} supply current (stand-by)	TTL-Input level	V_{CC} = 5.5 V, $\overline{E}$ = V_{IH}			1	mA
	CMOS-Input level	V_{CC} = 5.5 V, $\overline{E}$ = V_{CC}			100	μA
I_{CC1} V_{CC} supply current (active read)		V_{CC} = 5.5 V, $\overline{E}$ = V_{IL}, f = 6 MHz, outputs open			30	mA
I_{CC2} V_{CC} average supply current (active write) (see Note 7)		V_{CC} = 5.5 V, $\overline{E}$ = V_{IL}, programming in progress			10	mA
I_{CC3} V_{CC} average supply current (flash erase) (see Note 7)		V_{CC} = 5.5 V, $\overline{E}$ = V_{IL}, erasure in progress			15	mA
I_{CC4} V_{CC} average supply current (program/erase verify) (see Note 7)		V_{CC} = 5.5 V, $\overline{E}$ = V_{IL}, V_{PP} = V_{PPH}, program/erase-verify in progress			15	mA

NOTE 7: Not 100% tested; characterization data available.

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capacitance over recommended ranges of supply voltage and operating free-air temperature, f = 1 MHz†

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
C_i	Input capacitance	$V_I = 0$, f = 1MHz			6	pF
C_O	Output capacitance	$V_O = 0$, f = 1 MHz			12	pF

† Capacitance measurements are made on sample basis only.

PARAMETER MEASUREMENT INFORMATION

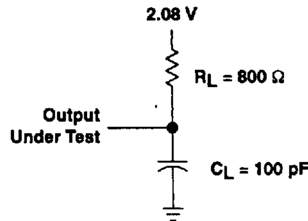
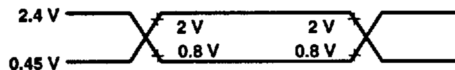


Figure 4. AC Test Output Load Circuit

AC testing input/output wave forms



AC testing inputs are driven at 2.4 V for logic high and 0.45 V for logic low. Timing measurements are made at 2 V for logic high and 0.8 V for logic low on both inputs and outputs. Each device should have a 0.1 μF ceramic capacitor connected between V_{CC} and V_{SS} as close as possible to the device pins.

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switching characteristics over full ranges of recommended operating conditions

DESCRIPTION		TEST CONDITIONS	ALTERNATE SYMBOL	'28F010-10		'28F010-12		'28F010-15		'28F010-17		UNIT
				MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
$t_{a(A)}$	Access time from address	C_L = 100 pF, 1 Series 74 TTL Load, Input $t_r \le 20$ ns, Input $t_f \le 20$ ns	t_{AVQV}		100		120		150		170	ns
$t_{a(E)}$	Access time from chip enable		t_{ELQV}		100		120		150		170	ns
$t_{en(G)}$	Access time from output enable		t_{GLQV}		45		50		55		60	ns
$t_{c(R)}$	Read cycle time		t_{AVAV}	100		120		150		170		ns
$t_{d(E)}$	Delay time, chip enable low to low-Z output		t_{ELQX}	0		0		0		0		ns
$t_{d(G)}$	Delay time, output enable low to low-Z output		t_{GLQX}	0		0		0		0		ns
$t_{dis(E)}$	Chip disable to hi-Z output		t_{EHQZ}	0	55	0	55	0	55	0	55	ns
$t_{dis(G)}$	Hold time, output enable to hi-Z output		t_{GHQZ}	0	30	0	30	0	35	0	35	ns
$t_{h(D)}$	Hold time, data valid from address, $\overline{E}$, or $\overline{G}$†		t_{AXQX}	0		0		0		0		ns
$t_{wr(W)}$	Write recovery time before read		t_{WHGL}	6		6		6		6		µs

† Whichever occurs first.

AC characteristics–write/erase/program operations

DESCRIPTION		ALTERNATE SYMBOL	'28F010-10		'28F010-12		'28F010-15		'28F010-17		UNIT
			MIN	TYP	MIN	TYP	MIN	TYP	MIN	TYP	
$t_{c(W)}$	Write cycle time	t_{AVAV}	100		120		150		170		ns
$t_{su(A)}$	Address setup time	t_{AVWL}	0		0		0		0		ns
$t_{h(A)}$	Address hold time	t_{WLAX}	55		60		60		70		ns
$t_{su(D)}$	Data setup time	t_{DVWH}	50		50		50		50		ns
$t_{hw(D)}$	Data hold time	t_{WHDX}	10		10		10		10		ns
$t_{wr(W)}$	Write recovery time before read	t_{WHGL}	6		6		6		6		µs
$t_{rr(W)}$	Read recovery time before write	t_{GHWL}	0		0		0		0		µs
$t_{su(E)}$	Chip enable setup time before write	t_{ELWL}	20		20		20		20		ns
$t_{h(E)}$	Chip enable hold time	t_{WHEH}	0		0		0		0		ns
$t_{w(W)}$	Write pulse duration (see Note 8)	t_{WLWH}	60		60		60		60		ns
$t_{wh(W)}$	Write pulse duration high	t_{WHWL}	20		20		20		20		ns
$t_{c(W)B}$	Duration of programming operation	t_{WHWH1}	10		10		10		10		µs
$t_{c(E)B}$	Duration of erase operation	t_{WHWH2}	9.5	10	9.5	10	9.5	10	9.5	10	ms
$t_{su(P)E}$	V_{PP} setup time to chip enable low	t_{VPEL}	1.0		1.0		1.0		1.0		µs
$t_{su(E)P}$	Chip enable, setup time to V_{PP} ramp	t_{EHVP}	100		100		100		100		ns
$t_{s(P)R}$	V_{PP} rise time	t_{VPPR}	1		1		1		1		µs
$t_{s(P)F}$	V_{PP} fall time	t_{VPPF}	1		1		1		1		µs

NOTE 8: Rise/fall time ≤ 10 ns.

ADVANCE INFORMATION

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TEXAS INSTR (ASIC/MEMORY)

alternative $\overline{CE}$-controlled writes

DESCRIPTION		ALTERNATE SYMBOL	'28F010-10		'28F010-12		'28F010-15		'28F010-17		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
$t_{c(W)}$	Write cycle time	t_{AVAV}	100		120		150		170		ns
$t_{su(A)}$	Address setup time	t_{AVEL}	0		0		0		0		ns
$t_{hE(A)}$	Address hold time	t_{ELAX}	75		80		80		90		ns
$t_{su(D)}$	Data setup time	t_{DVEH}	50		50		50		50		ns
$t_{hE(D)}$	Data hold time	t_{EHDX}	10		10		10		10		ns
$t_{wr(E)}$	Write recovery time before read	t_{EHGL}	6		6		6		6		µs
$t_{rr(E)}$	Read recovery time before write	t_{GHEL}	0		0		0		0		µs
$t_{su(W)}$	Write enable setup time before chip enable	t_{WLEL}	0		0		0		0		ns
$t_{h(W)}$	Write enable hold time	t_{EHWH}	0		0		0		0		ns
$t_{w(E)}$	Write pulse duration	t_{ELEH}	70		70		70		80		ns
$t_{wh(E)}$	Write pulse duration high	t_{EHEL}	20		20		20		20		ns
$t_{su(P)E}$	V_{PP} setup time to chip enable low	t_{VPEL}	1.0		1.0		1.0		1.0		µs
$t_{c(W)B}$	Duration of programming operation	t_{EHEH}	10		10		10		10		µs

PARAMETER MEASUREMENT INFORMATION

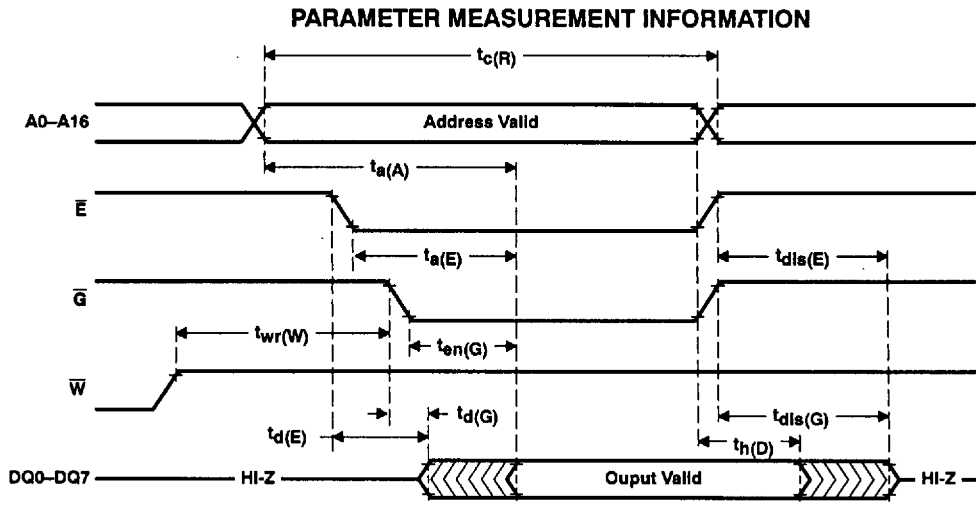

Figure 5. Read Cycle Timing

ADVANCE INFORMATION

TEXAS INSTR (ASIC/MEMORY)

62E D ■ 8961725 0080746 30T ■TII5

PARAMETER MEASUREMENT INFORMATION

Power-Up and Standby
Set-Up Program Command
Program Command Latch Address and Data
Programming
Program Verify Command
Program Verification
Standby/ Power-Down

A0–A16
$t_{c(W)}$ $t_{c(W)}$ $t_{c(W)}$ $t_{c(R)}$
$t_{su(A)}$ $t_{h(A)}$ $t_{h(A)}$ $t_{su(A)}$

$\overline{E}$
$t_{su(E)}$ $t_{su(E)}$ $t_{su(E)}$ $t_{dis(E)}$
$t_{h(E)}$ $t_{h(E)}$ $t_{h(E)}$

$\overline{G}$
$t_{rr(W)}$ $t_{c(W)B}$ $t_{wh(W)}$ $t_{wr(W)}$ $t_{dis(G)}$

$\overline{W}$
$t_{h(D)}$
$t_{hw(D)}$ $t_{hw(D)}$ $t_{hw(D)}$ $t_{en(G)}$
$t_{w(W)}$ $t_{w(W)}$ $t_{w(W)}$ $t_{d(G)}$
$t_{su(D)}$ $t_{su(D)}$ $t_{su(D)}$

DQ0–DQ7
HI-Z
Data In = 40H
Data In
Data In = C0H
$t_{d(E)}$
$t_{a(E)}$
Valid Data Out

V_{CC} 5 V
0 V
$t_{su(P)E}$
V_{PP} 12 V
V_{PPL}
$t_{s(P)R}$ $t_{s(P)F}$
$t_{su(E)P}$

Figure 6. Write Cycle Timing

ADVANCE INFORMATION

TEXAS INSTR (ASIC/MEMORY)

PARAMETER MEASUREMENT INFORMATION

TEXAS INSTR (ASIC/MEMORY)

Power-Up and Standby
Set-Up Program Command
Program Command Latch Address and Data
Programming
Program Verify Command
Program Verification
Standby/ Power-Down

A0–A16
W̄
Ḡ
Ē
DQ0–DQ7
V_{CC}
V_{PP}

$t_{c(W)}$ $t_{c(W)}$ $t_{c(W)}$ $t_{c(R)}$
$t_{su(A)}$ $t_{hE(A)}$ $t_{hE(A)}$ $t_{su(A)}$
$t_{su(W)}$ $t_{su(W)}$ $t_{su(W)}$ $t_{dis(G)}$
$t_{h(W)}$ $t_{h(W)}$ $t_{h(W)}$
$t_{rr(E)}$ $t_{c(w)B}$ $t_{wh(E)}$ $t_{wr(E)}$ $t_{dis(E)}$
$t_{hE(D)}$ $t_{hE(D)}$ $t_{hE(D)}$ $t_{h(D)}$
$t_{w(E)}$ $t_{w(E)}$ $t_{w(E)}$ $t_{en(G)}$ $t_{d(G)}$
$t_{su(D)}$ $t_{su(D)}$ $t_{su(D)}$
HI-Z
Data In = 40H
Data In
Data In = C0H
$t_{d(E)}$
$t_{a(E)}$
Valid Data Out
5 V
0 V
12 V
V_{PPL}
$t_{su(P)E}$
$t_{s(P)R}$
$t_{su(E)P}$
$t_{s(P)F}$

ADVANCE INFORMATION

Figure 7. Write Cycle (Alternative $\overline{CE}$-Controlled Writes) Timing

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PARAMETER MEASUREMENT INFORMATION

Figure 8. Flash-Erase Cycle Timing

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TEXAS INSTR (ASIC/MEMORY)

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