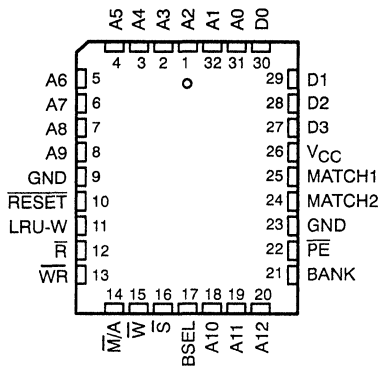
D3365, JANUARY 1990–REVISED JUNE 1990

- **Address to Match Time . . . 17 ns Max**
- **2-Way Architecture Significantly Improves Hit Rate**
- **Implements LRU Replacement Allgorithm**
- **Useful for Bus Watching**
- **On-Chip Parity Generator and Checker**
- **Easily Expandable in Depth and Width**
- **Reliable Advanced CMOS Technology**
- **Fully TTL Compatible**

FM PACKAGE
(TOP VIEW)



description

The SN74ACT2160 is a valuable building block for implementing fast two-way set associative caches. This device consists of two separate 8K x 5 RAMs for tag and parity storage, an 8K x 1 LRU RAM, two high-speed comparators, and the control circuitry necessary to give the designer the freedom to determine how this device will be used. The SN74ACT2160 also includes single-entry invalidation circuitry and parity generation and checking for ease of design and high system reliability.

The SN74ACT2160 is fabricated using advanced silicon-gate CMOS technology for high speed and simple interface with bipolar TTL circuits. By combining the SN74ACT2160 with programmable logic, a cache can be constructed that specifically addresses the individual system requirements. Significant reductions in cache memory component count, board area, and power dissipation can be achieved by using this device.

direct-mapped versus two-way set associative caches

A cache memory is a small high-speed memory that is used to store a portion of the data found in the larger main memory to achieve optimum processor performance and to reduce main memory bus traffic. Since the cache memory is smaller than the main memory, only part of the address, the least significant bits referred to as the index, is used to address the cache memory. The most significant address bits, called the tag, are stored along with the cache data and are used to identify what data is stored in an indexed location. When the processor requests data, the index portion of the processor address points to a word of data in the cache-data RAM and to a tag in the cache tag RAM. If the upper portion of the processor address is equal to the stored tag, a cache hit is said to occur and the cached data can be immediately sent to the processor.

In a direct-mapped or one-way set associative cache, only one data word and tag exist in cache for each index. This means that when the processor requests data, only one cache memory location can contain the requested data. Also, if the requested data is not in the cache and the cache is updated, the data in the indexed cache memory location will be written over regardless of how recently it has been used.

In a two-way set associative cache, two data words and tags exist for each index. This means that the requested data can reside in one of two cache locations. When a miss occurs and the cache is updated, the least recently used data can be written over. As would be expected, studies have shown that the hit rate improves significantly when using a two-way cache design over a one-way or direct-mapped cache design. Through use of the 'ACT2160, the logic complexity and parts count usually associated with a two-way cache are greatly reduced.

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address comparison

The 'ACT2160 compares the contents of the memory location addressed by A0-A12 with the address bits (or tag) applied at D0-D3. An equality is indicated by a high level on the MATCH1 or MATCH2 outputs. MATCH1 is high when the applied tag is equal to the stored tag in bank 1. MATCH2 is high when the applied tag is equal to the stored tag in bank 2.

writing to the cache tag RAMs

The manual/auto ($\overline{M}$/A) input on the 'ACT2160 provides two methods of selecting which tag bank will be written to when the write input ($\overline{W}$) is taken low. When $\overline{M}$/A is low, the bank select input (BSEL) selects the bank to be written to. BSEL low selects bank 1 and BSEL high selects bank 2. When $\overline{M}$/A is high, the least recently used (LRU) circuitry automatically selects the bank written to when $\overline{W}$ is taken low.

writing to the cache data RAMs

When a read or a write miss occurs and the cache is updated, the BANK output will indicate which bank the data should be written to. If BANK is low, bank 1 should be written to. If BANK is high, bank 2 should be written to. When writing a tag with $\overline{M}$/A low, the BANK output will not indicate which bank is being selected by the BSEL input. BANK is the output of the internal 8K x 1 LRU RAM. When a write hit occurs, the match outputs will indicate which data bank to write to.

LRU replacement circuitry

A concept commonly referred to in cache design is the property of locality. An aspect of the property of locality says that the information currently in use is likely to be used again soon. Based on this property, it is desirable to replace the information that has not been used recently when writing to cache. With a set size of two, this is easily done using one bit to indicate which of the two addressed locations is oldest or least recently used. The 'ACT2160 contains an 8K x 1 RAM and the necessary circuitry to implement the LRU replacement algorithm.

The $\overline{M}$/A input allows the user to choose between automatic LRU and manual replacement. When $\overline{M}$/A is high, the LRU RAM output selects which bank to write to. When the LRU bit for a given address is low, a write pulse will write D0-D3 to bank 1. When the LRU bit for a given address is high, a write pulse will write D0-D3 to bank 2. The LRU RAM is updated every time a write, a match (with LRU-W signal), or a word reset occurs.

When a write occurs with $\overline{M}$/A high, the addressed LRU bit is inverted and written back in so that the next write with $\overline{M}$/A high to that address will be to the other bank. When a write occurs with $\overline{M}$/A low, the bank is selected by the BSEL input and the addressed LRU bit is adjusted so that the next write to the same address with $\overline{M}$/A high will be to the other bank.

With a match output high indicating a match, the LRU RAM will also be updated when the LRU-W input is taken low. The logic level at each match output is fed back internally to the LRU circuitry. If MATCH1 or MATCH2 are high, the LRU-W input provides an LRU write timing signal that causes an internal LRU write pulse to be generated. With MATCH1 high, the LRU bit is set high so the next write to the same address with $\overline{M}$/A high will be to bank 2. With MATCH2 high, the LRU bit is set low so the next write to the same address with $\overline{M}$/A high will be to bank 1. When cascading these devices for wider address coverage, the MATCH1 outputs must be wire-ANDed together so an LRU write will not occur unless all MATCH1 outputs are high. In the same manner, the MATCH2 outputs (in width) must be tied together. When MATCH1 and MATCH2 are forced high during deselect, write, read, word reset, or reset, and LRU-W is taken low, a false LRU write will not occur.

parity generation and checking

The 'ACT2160 contains parity generation and checking circuitry. When the $\overline{PE}$ output goes low, a parity error exists in one of the two tag RAMs.

During a write cycle, address bits or data on D0-D3 plus generated odd parity are written into the 5-bit memory location in either bank 1 or bank 2 that is addressed by A0-A12. Also during write, a parity error may be forced for diagnostic purposes by holding the $\overline{R}$ input low. The addressed parity bits are included in the comparator

circuitry of the 'ACT2160 so if a parity error occurs, the corresponding match output will be forced low. The bank written to is selected automatically or manually via the BSEL input depending on the state of the $\overline{M}$/A input. The LRU bit is not parity protected. The BANK outputs of the 'ACT2160s that are cascaded in width could be externally exclusive ORed to provide protection for the LRU bits.

operation as a data RAM

The 'ACT2160 can be used as a two-way 8K x 4 data RAM with parity generation and checking. By tying the manual/auto ($\overline{M}$/A) pin low, the BSEL input can be used to select which bank is being written to or read from. Through the use of the select pin, the 'ACT2160 can be cascaded for a deeper data RAM. Inputs $\overline{WR}$ and LRU-W should be tied high when using the 'ACT2160 as a data RAM.

initialization

A reset input is provided for initialization. When $\overline{RESET}$ is taken low, all three 8K RAM locations are cleared to zero (with valid parity) and the MATCH1 and MATCH2 outputs are forced high. If a D0-D3 input of zero is compared to any memory location that has not been written into since reset, MATCH1 and/or MATCH2 will be high indicating that D0-D3 plus generated parity is equal to the reset memory location. By tying a single data input pin high, this bit will function as a valid bit and a match will not occur unless data has been written into the addressed memory location. When cascading in the width direction, only one bit needs to be tied high regardless of the address width. After reset, $\overline{PE}$ will be high for every addressed memory location indicating no parity error in the RAM data. After power-up, the 'ACT2160 must be initialized by resetting the device to ensure that all memory locations are at a known state. The 'ACT2160 could also be initialized by writing to every memory location (both banks) with $\overline{M}$/A low.

single-entry invalidation

In cache tag systems, it is often necessary to invalidate a tag memory location when data in the cache becomes inconsistent with the data in main memory or in additional caches. The word-reset function on the 'ACT2160 allows any addressed memory location to be cleared to zero with valid parity by taking the word reset pin ($\overline{WR}$) low. By tying one of the D0-D3 input pins high, that particular bit can be used as a valid bit. Whenever D0-D3 is compared to a memory location cleared by $\overline{WR}$ (or by the master $\overline{RESET}$), a miss will occur. If a D0-D3 input pin is not tied high, a false match will occur whenever a D0-D3 of zero is compared to a reset location. Word reset is independent of the input at the D0-D3 pins. The $\overline{M}$/A input must be low for a word reset to occur when $\overline{WR}$ is taken low. Word reset can also be accomplished by holding $\overline{WR}$ low and taking $\overline{M}$/A low to reset the addressed location. At the same time that an addressed location is reset, the addressed LRU bit is updated so that the next write to the same address with $\overline{M}$/A high will be to the reset location. Input BSEL determines which bank $\overline{WR}$ affects. When cascading in width, all devices must receive the word-reset pulse for proper LRU RAM update.

cascading the SN74ACT2160

The 'ACT2160 is easily cascaded in width and depth. Wider addresses can be compared by driving the A0-A12 inputs of each device with the same index and applying the additional address bits to the D0-D3 inputs. The select ($\overline{S}$) input allows this device to be easily cascaded in depth. When a device is deselected, the MATCH1 and MATCH2 outputs are driven high. A decoder can be used to drive the select inputs since the propagation delay from select to match is much faster than from address to match. MATCH1 and MATCH2 are open-drain outputs for easy wire-ANDing. Figure 16 shows the 'ACT2160 cascaded.

cache coherency through bus watching

When implementing cache designs, cache coherency is usually a concern. A solution to this problem is to implement bus watching using the 'ACT2160. By storing the same tags in the bus watcher RAM as are stored in the cache tag RAM, the bus watcher will indicate a hit every time a cached address passes down the main address bus. If data is being modified in main memory, the index can be passed to the cache tag RAM for invalidation. Figure 17 shows a possible bus-watcher implementation.

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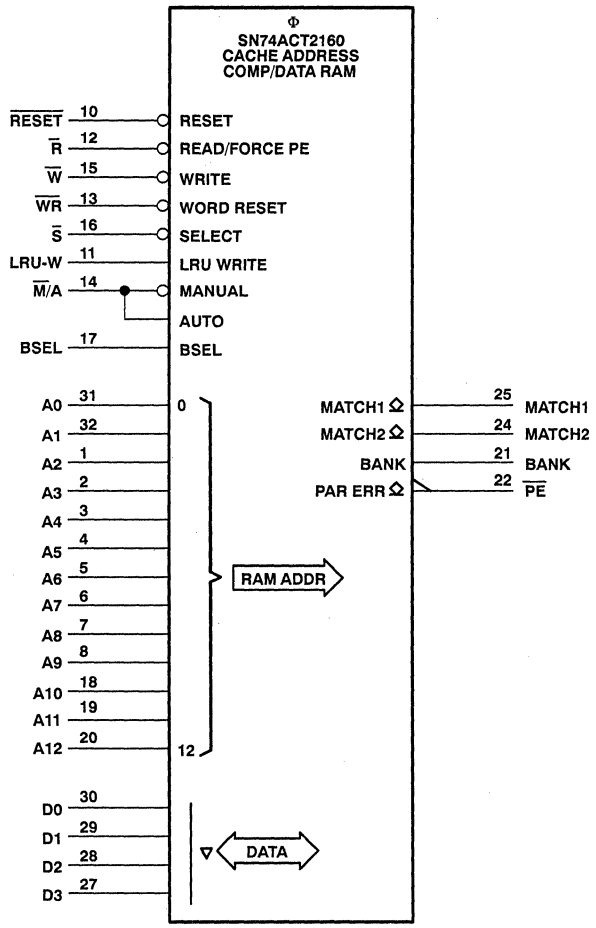
logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984.

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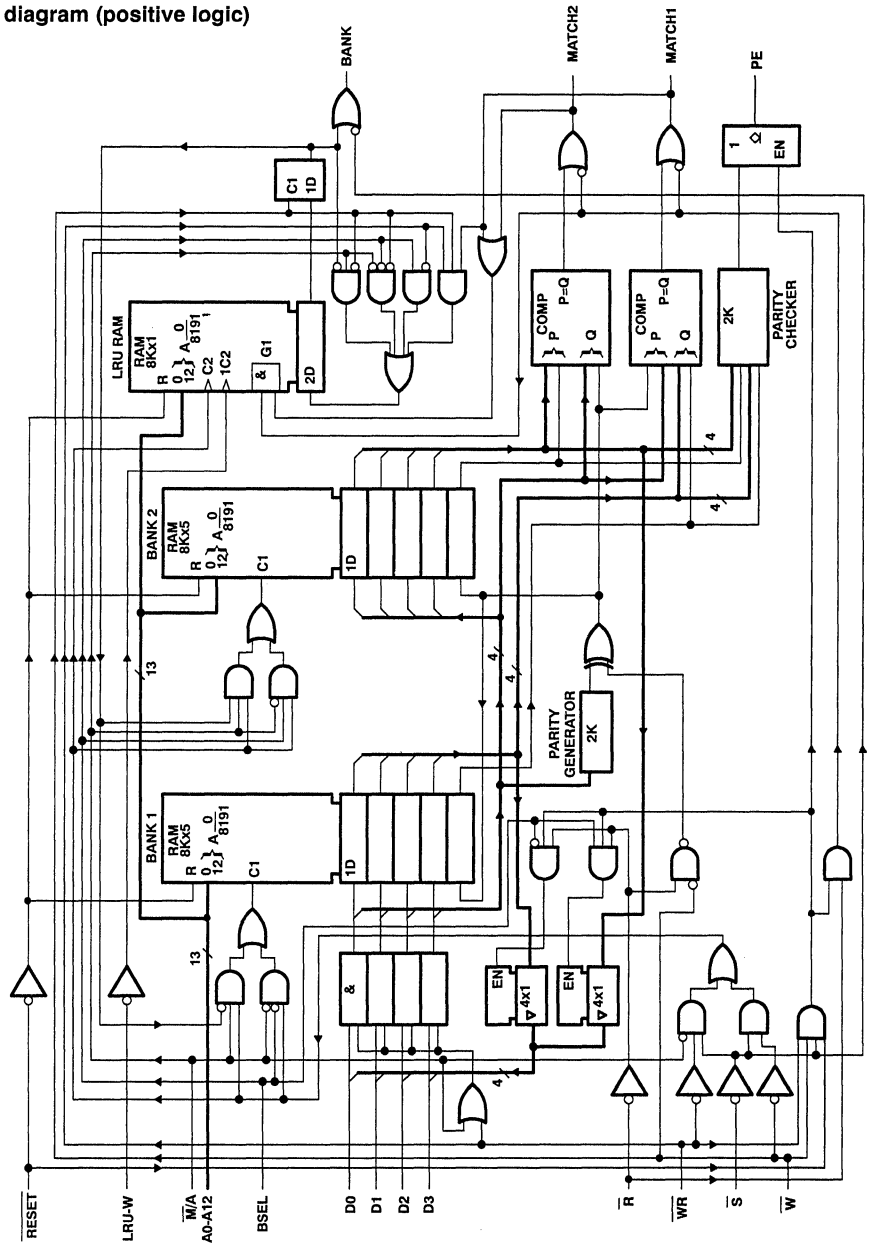
logic diagram (positive logic)



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Terminal Functions

PIN NAME	DESCRIPTION
A0-A12	Address inputs. Addresses a memory location in each of the three 8K RAM arrays. Address must be stable for the duration of the write cycle.
BSEL	Bank Select input. This input is used in conjunction with the manual/auto, read and word reset functions. When BSEL is low, bank 1 is selected. When BSEL is taken high, bank 2 is selected. When $\overline{M}$/A is high, the BSEL input does not affect writing.
BANK	Bank output. The BANK output is used during a write to indicate which bank D0-D3 is being written into when $\overline{M}$/A is high. BANK is low for bank 1 and high for bank 2. BANK is forced high during reset and deselect. BANK is used to indicate which cache SRAM bank the system data should be written into. When $\overline{W}$ is taken low, the output of the LRU RAM is latched causing BANK to remain stable. When $\overline{W}$ returns high, the latch returns transparent and the BANK output will switch if the LRU bit was changed. BANK is a totem-pole output.
D0-D3	Data (tag) inputs and outputs. Provides input to RAM bank 1 or bank 2 depending on the state of the $\overline{S}$, $\overline{W}$, BSEL, $\overline{M}$/A, and $\overline{WR}$ pins. When in the compare mode, D0-D3 plus generated parity are compared to the addressed 5-bit memory location in bank 1 and bank 2. D0-D3 also function as outputs (see the $\overline{R}$ pin description).
LRU-W	Least Recently Used Write timing signal. In the compare mode, a falling edge on LRU-W will initiate an LRU write pulse if MATCH1 and/or MATCH2 are high. If a falling edge at LRU-W occurs before MATCH1 or MATCH2 are valid based on t_{pd1} and t_{su1}, the LRU write may not occur or a false LRU write could occur. LRU-W will only initiate a LRU write pulse on a falling edge. LRU-W has no effect during any other mode of operation.
$\overline{M}$/A	Manual/Auto input. The $\overline{M}$/A input determines the bank select mode for writing data. When $\overline{M}$/A is low, the bank to be written into is selected manually via the BSEL input. When the $\overline{M}$/A input is high, the bank selection is done automatically. An internal 8K x 1 RAM is used to keep track of the bank to be written into using the least recently used (LRU) replacement algorithm. After the device is reset, the first write is into bank 1. The next time data is written to the same address, it will be stored in bank 2. Successive writes to the same address automatically alternate between bank 1 and bank 2. $\overline{M}$/A can also be used to perform the word reset function. With $\overline{WR}$ low, the addressed location in the selected bank will be reset when $\overline{M}$/A is taken low.
MATCH1 MATCH2	Match outputs. When MATCH1 or MATCH2 are high during a compare cycle, D0-D3 plus generated parity equal the contents of one of two memory locations addressed by A0-A12. MATCH1 is high when D0-D3 matches D0-D3 stored in bank 1. MATCH2 is high when D0-D3 matches D0-D3 stored in bank 2. The match outputs are high during deselect, write, read, word reset, and reset. The logic level at the match outputs is fed back to the internal LRU circuitry. If a match output is high indicating a match when LRU-W is taken low, the LRU bit is adjusted so that the next write into that address will be into the other bank (LRU concept). If a match occurs with both banks (MATCH1 and MATCH2 high) and LRU-W is taken low, bank 2 will be written into when $\overline{M}$/A is low and bank 1 will be written into when $\overline{M}$/A is high. Since this device features open-drain match outputs, an external pullup resistor of 180 Ω minimum is required. If a parity error is present in bank 1 or bank 2 during compare, the corresponding match output will be forced low.
$\overline{PE}$	Parity Error output. During compare cycles, a low level at $\overline{PE}$ indicates a parity error in one of the 8K X 5 RAMs. A parity error will force the corresponding match output low. $\overline{PE}$ is an open-drain output and an external pullup resistor is required. $\overline{PE}$ is disabled during write, reset, word reset, and deselect.
$\overline{R}$	Read input. When $\overline{R}$ is low and the device is selected, D0-D3 are enabled as outputs. The output data (tag) is determined by A0-A12 and the BSEL input. Outputs D0-D3 are disabled during write, word reset, reset, deselect, and when $\overline{R}$ is high. During write cycles, a parity error can be forced into the memory location addressed by A0-A12 of the selected bank when $\overline{R}$ is taken low.
$\overline{RESET}$	Reset input. Asynchronously clears all three RAM arrays to zero with valid parity independent of the select pin when $\overline{RESET}$ is low. By tying a single data input high, a false match will not occur when a tag of zero is applied after initialization.
$\overline{S}$	Chip select input. Enables device when $\overline{S}$ is low. When $\overline{S}$ is high, MATCH1 and MATCH2 are forced high. $\overline{PE}$ and D0-D3 are disabled when $\overline{S}$ is high and BANK is forced high.
$\overline{WR}$	Word Reset input. The $\overline{WR}$ input allows any addressed memory location to be cleared to zero with valid parity. This is achieved by taking $\overline{WR}$ low while in the manual mode ($\overline{M}$/A low). The desired bank is selected using the BSEL input. When $\overline{WR}$ is asserted, the addressed LRU bit is adjusted so that the next write to that address (with $\overline{M}$/A high) is into the reset memory location. By tying a single D0-D3 input high, this bit will act as a valid bit assuring that a false match will not occur with a reset memory location.
$\overline{W}$	Write control input. When the device is selected and $\overline{W}$ is low, D0-D3 and generated parity are written into the addressed memory location in either bank 1 or bank 2. The RAM bank to be written into can be selected automatically or manually depending on the $\overline{M}$/A input.

FUNCTION TABLES

write mode

INPUTS							OUTPUTS				I/O	FUNCTION
$\overline{W}$	$\overline{R}$	$\overline{S}$	$\overline{M}$/A	BSEL	$\overline{RESET}$	$\overline{WR}$	MATCH1	MATCH2	$\overline{PE}$	BANK†	D0-D3	
L	H	L	L	L	H	H	H	H	H	L‡	Input	Write into bank 1
L	H	L	L	H	H	H	H	H	H	L‡	Input	Write into bank 2
L	H	L	H	X	H	X	H	H	H	H or L‡	Input	LRU write (bank 1 or 2)
L	L	L	L	L	H	H	H	H	H	L‡	Input	Write parity error into bank 1
L	L	L	L	H	H	H	H	H	H	L‡	Input	Write parity error into bank 2
L	L	L	H	X	H	H	H	H	H	H or L‡	Input	Write parity error (LRU)
L	H	L	L	X	H	L§	H	H	H	L§	Hi-Z	Write zero into selected bank

read mode

INPUTS							OUTPUTS				I/O	FUNCTION
$\overline{W}$	$\overline{R}$	$\overline{S}$	$\overline{M}$/A	BSEL	$\overline{RESET}$	$\overline{WR}$	MATCH1	MATCH2	$\overline{PE}$	BANK	D0-D3	
H	L	L	X	L	H	H	H	H	H	H or L	Output	Read bank 1
H	L	L	X	H	H	H	H	H	H	H or L	Output	Read bank 2
H	L	L	X	X	H	H	H	H	L	H or L	Output	Parity error in bank 1 or 2
H	H	L	X	X	H	H	H or L	H or L	EN	H or L	Hi-Z	Disable/compare

compare mode

INPUTS							OUTPUTS				I/O	FUNCTION
$\overline{W}$	$\overline{R}$	$\overline{S}$	$\overline{M}$/A	BSEL	$\overline{RESET}$	$\overline{WR}$	MATCH1	MATCH2	$\overline{PE}$	BANK	D0-D3	
							H	L	H	H or L		Match bank 1, miss bank 2
							L	H	H	H or L		Match bank 2, miss bank 1
H	H	L	X	X	H	H	H	H	H	H or L		Match bank 1 and 2
				or			L	L	H	H or L	Input	Miss bank 1 and 2
H	H	L	H	X	H	X	L	L	L	H or L		Parity error bank unknown
							L	H	L	H or L		Parity error bank 1, match bank 2
							H	L	L	H or L		Parity error bank 2, match bank 1

reset, word reset, and deselect mode

INPUTS							OUTPUTS				I/O	FUNCTION
$\overline{W}$	$\overline{R}$	$\overline{S}$	$\overline{M}$/A	BSEL	$\overline{RESET}$	$\overline{WR}$	MATCH1	MATCH2	$\overline{PE}$	BANK	D0-D3	
H	X	L	X	X	L	X	H	H	H	L	Hi-Z	Memory reset-selected
H	X	H	X	X	L	X	H	H	H	H	Hi-Z	Memory reset-deselect
H	X	L	L	L	H	L	H	H	H	L¶	Hi-Z	Word reset in bank 1
H	X	L	L	H	H	L	H	H	H	L¶	Hi-Z	Word reset in bank 2
H	X	L	H	X	H	L	H or L	H or L	EN	H or L	Hi-Z	Word reset disabled/compare mode
X	X	H	X	X	H	X	H	H	H	H	Hi-Z	Device disabled

EN denotes enabled, H denotes a high level, L denotes a low level, X denotes a don't care level, – denotes an undetermined output

† The BANK output is transparent when $\overline{W}$ is high and latched when $\overline{W}$ is low.

‡ When writing with $\overline{M}$/A high, the BANK output indicates which bank D0-D3 is being written into. When writing with $\overline{M}$/A low, the BANK output will be forced low and will not indicate which bank is being written into. After writing with $\overline{M}$/A low, the BANK output will indicate the correct LRU bit state.

§ The state of BANK after $\overline{W}$ and $\overline{M}$/A or $\overline{W}$ and $\overline{WR}$ return high is indeterminate. This operation is not recommended.

¶ The BANK output is forced low during word reset. After a word reset in bank 2, the BANK output will be high.

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FUNCTION TABLES (continued)

LRU write

$\overline{S}$	$\overline{WR}$	$\overline{W}$	LRU-W†	MATCH1	MATCH2	QI‡	LRU WRITE	QN§	FUNCTION
L	H	↓	X	H	H	L	YES	H	Write to bank 1, selected by LRU circuitry
L	H	↓	X	H	H	H	YES	L	Write to bank 2, selected by LRU circuitry
↓	H	L	X	H	H	X	NO	–	No write occurs
L	H	H	↓	H	L	X	YES	H	Match bank 1
L	H	H	↓	L	H	X	YES	L	Match bank 2
L	H	H	↓	H	H	X	YES	L	Match bank 1 and 2
L	↓	H	X	H	L	X	YES	L	Word reset bank 1
L	↓	H	X	L	H	X	YES	H	Word reset bank 2
L	↓	H	X	H	H	X	YES	L	Word reset bank 1 and bank 2
L	↓	H	X	L	L	X	NO	–	No word reset
↓	L	H	X	H	H	X	NO	–	No word reset
H	X	X	X	H	H	X	NO	–	Device disabled

H denotes a high level, L denotes a low level, X denotes a don't care level, – denotes an undetermined level, ↓ denotes the falling edge of the signal.
† LRU-W is falling-edge-triggered and has effect only during the compare mode.
‡ QI is the state of the LRU RAM output before a LRU write occurs.
§ QN is the state of the LRU RAM output after a LRU write occurs.

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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, V_{CC} (see Note 1) ..... – 1.5 V to 7 V
Input voltage range, any input ..... – 1.5 V to 7 V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$) ..... ± 25 mA
Output clamp current, I_{OK} ($V_I < 0$ or $V_I > V_{CC}$) ..... ± 25 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) : D0-D3, BANK ..... ± 25 mA
MATCH1, MATCH2, PE ..... ± 50 mA
Continuous current through V_{CC} or GND pins ..... ± 200 mA
Operating free-air temperature range ..... 0°C to 70°C
Storage temperature range ..... – 65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds ..... 260°C

‡ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
NOTE 1: All voltage values are with respect to GND.

recommended operating conditions (see important notice)

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage		4.75	5	5.25	V
V_{IH}	High-level input voltage		2.2		V_{CC}+0.5	V
V_{IL}	Low-level input voltage (see Note 2)		– 0.5		0.8	V
V_{OH}	High-level output voltage, MATCH1, MATCH2, and $\overline{PE}$				5.25	V
I_{OH}	High-level output current, D0-D3 and BANK				– 8	mA
I_{OL}	Low-level output current	D0-D3, BANK			8	mA
		MATCH1, MATCH2, $\overline{PE}$			27	
T_A	Operating free-air temperature		0		70	°C

NOTE 2: The algebraic convention, where the more negative (less positive) limit is designated as minimum, is used in this data sheet for logic voltage levels only.

important notice

Due to the high-performance characteristics of this device and to ensure the integrity of stored data (or tag), the address inputs must not be allowed to float through the input threshold region (1.5 V). Rise and fall times at the threshold region of the address inputs must not exceed 20 ns/V. Slow rise and fall times through the threshold region may be eliminated by not using pullup resistors on the address lines and minimizing the high-impedance time when switching between bus drivers. An alternate approach is to use latches or registers in front of the cache tag address inputs to eliminate floating-address conditions. Ground bounce, due to simultaneous switching, into the threshold region of the address inputs should be avoided in order to ensure that a slow rise/fall condition does not occur.

Negative undershoot at the address or data inputs could cause this device to reset if the V_{IH} level at the $\overline{RESET}$ pin is at its minimum high level (2.2 V). In systems with – 1.5 V or more of undershoot at the address and data inputs, it is recommended that the minimum V_{IH} level at the $\overline{RESET}$ pin be 4 V. As with all designs, proper termination and capacitive bypass techniques should be employed. Unused inputs should be tied to either V_{CC} or GND.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS	SN74ACT2160-17			UNIT
				MIN	TYP†	MAX	
V_{OH}	High-level output voltage	D0-D3, BANK	V_{CC} = 4.75 V, I_{OH} = – 8 mA	3.7			V
V_{OL}	Low-level output voltage	D0-D3, BANK	V_{CC} = 4.75 V, I_{OL} = 8 mA			0.4	V
		MATCH1, MATCH2, $\overline{PE}$	V_{CC} = 4.75 V, I_{OL} = 27 mA			0.4	
I_{OH}	High-level output current	MATCH1, MATCH2, $\overline{PE}$	V_{CC} = 4.75 V, V_{OH} = 5.25 V			10	µA
I_I	Input current		V_{CC} = 5.25 V, V_I = 0 to V_{CC}			±5	µA
I_{OZ}	Off-state output current		V_{CC} = 5.25 V, V_O = 0 to V_{CC}, $\overline{S}$ at V_{IH}			±10	µA
I_{CC1}	Supply current (operating)		V_{CC} = 5.25 V, $\overline{RESET}$ at V_{CC}, $\overline{S}$ at 0 V		130	180	mA
I_{CC2}	Supply current (reset)		V_{CC} = 5.25 V, $\overline{RESET}$ at 0 V, $\overline{S}$ at 0 V		30	75	mA
I_{CC3}	Supply current (deselected)		V_{CC} = 5.25 V, $\overline{RESET}$ at V_{CC}, $\overline{S}$ at V_{CC}		80	150	mA
C_I	Input capacitance‡		f = 1 MHz			5	pF
C_O	Output capacitance‡		f = 1 MHz			5	pF

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ This is the capacitance at an input, output, or I/O pin.

ADVANCE INFORMATION

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		SN74ACT2160-17			UNIT
		MIN	TYP†	MAX	
t_{pd1}	Propagation time from address to MATCH1 and MATCH2		15	17	ns
t_{pd2}	Propagation time from D0-D3 to MATCH1 and MATCH2		9	15	ns
t_{pd3}	Propagation time from $\overline{S}$ low to MATCH1 and MATCH2		7	12	ns
t_{pd4}	Propagation time from $\overline{S}$ high to MATCH1 and MATCH2 high		7	10	ns
t_{pd5}	Propagation time from address to $\overline{PE}$		20	25	ns
t_{pd6}	Propagation time from $\overline{S}$ to $\overline{PE}$		15	20	ns
t_{pd7}	Propagation time from $\overline{S}$ to BANK		7	15	ns
t_{pd8}	Propagation time from address to BANK		15	22	ns
t_{pd9}	Propagation time from LRU-W↓ to BANK		12	18	ns
t_{pd10}	Propagation time from address to D0-D3		17	25	ns
t_{pd11}	Propagation time from BSEL to D0-D3		7	12	ns
t_{pd12}	Propagation time from $\overline{W}$ high to BANK		7	12	ns
t_{pd13}	Propagation time from $\overline{W}$ low to MATCH1 and MATCH2 high		6	10	ns
t_{pd14}	Propagation time from $\overline{W}$ low to $\overline{PE}$ high		7	11	ns
t_{pd15}	Propagation time from $\overline{RESET}$ low to MATCH1 and MATCH2 high		6	10	ns
t_{pd16}	Propagation time from word reset to MATCH1 and MATCH2 high		6	10	ns
t_{pd17}	Propagation delay, $\overline{W}$ high to MATCH‡		14	20	ns
t_{pd18}	Propagation delay, $\overline{W}$ high to $\overline{PE}$‡		14	20	ns
t_{pd19}	Propagation delay, $\overline{RESET}$ high to MATCH‡		14	20	ns
t_{pd20}	Propagation delay, $\overline{RESET}$ high to $\overline{PE}$‡		60	100	ns
t_{en1}	Enable time from $\overline{S}$ low to D0-D3		9	14	ns
t_{en2}	Enable time from $\overline{R}$ low to D0-D3		7	12	ns
t_{en3}	Enable time from $\overline{RESET}$ high to D0-D3		9	14	ns
t_{dis1}	Disable time from $\overline{R}$ high to D0-D3		7	12	ns
t_{dis2}	Disable time from $\overline{S}$ high to D0-D3		7	12	ns
t_{dis3}	Disable time from $\overline{RESET}$ low to D0-D3		9	14	ns
t_{v1}	Valid time, MATCH1 and MATCH2 after change of data	2			ns
t_{v2}	Valid time, MATCH1 and MATCH2 after change of address	1			ns
t_{v3}	Valid time, MATCH1 and MATCH2 low after $\overline{S}$ high	0			ns
t_{v4}	Valid time, $\overline{PE}$ after change of address	2			ns
t_{v5}	Valid time, $\overline{PE}$ low after $\overline{S}$ high	0			ns
t_{v6}	Valid time, D0-D3 after change of address	1			ns

† All typical values are at V_{CC} = 5 V, T_A = 25°C.

‡ The MATCH and $\overline{PE}$ outputs will glitch at the end of a write or reset cycle after $\overline{W}$ or $\overline{RESET}$ returns high. These specs indicate when the MATCH and $\overline{PE}$ outputs are stable after $\overline{W}$ returns high. This specification assumes that the address and/or data inputs are not changed immediately after $\overline{W}$ or $\overline{RESET}$ high.

timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER			SN74ACT2160-17			UNIT
			MIN	TYP†	MAX	
t_{w1}	Pulse duration, LRU-W	High	10			ns
		Low	10			
t_{w2}	Pulse duration, $\overline{W}$ low		12			ns
t_{w3}	Pulse duration, $\overline{RESET}$ low		60			ns
t_{w4}	Pulse duration, word reset	$\overline{WR}$ low with $\overline{M}$/A low	12			ns
		$\overline{M}$/A low with $\overline{WR}$ low	12			
t_{su1}	Setup time, MATCH1 and MATCH2 valid before LRU-W↓		5			ns
t_{su2}	Setup time, address valid before $\overline{W}$ high	$\overline{M}$/A high	27			ns
		$\overline{M}$/A low	12			
t_{su3}	Setup time, $\overline{S}$ low before $\overline{W}$	$\overline{W}$ high, $\overline{M}$/A = L	12			ns
		$\overline{W}$ low, $\overline{M}$/A = H	8			
t_{su4}	Setup time, address before $\overline{W}$ low	$\overline{M}$/A high	15			ns
		$\overline{M}$/A low	0			
t_{su5}	Setup time, BSEL before $\overline{W}$ low with $\overline{M}$/A low		0			ns
t_{su6}	Setup time, $\overline{M}$/A before $\overline{W}$ low		2			ns
t_{su7}	Setup time, D0-D3 before $\overline{W}$ high		10			ns
t_{su8}	Setup time, $\overline{R}$ low before $\overline{W}$ high (see Note 3)		10			ns
t_{su9}	Setup time, $\overline{RESET}$ inactive before $\overline{W}$ high		30			ns
t_{su10}	Setup time, address before word reset	$\overline{WR}$ and $\overline{M}$/A low	0			ns
t_{su11}	Setup time, BSEL before word reset	$\overline{WR}$ and $\overline{M}$/A low	2			ns
t_{su12}	Setup time, $\overline{S}$ low before word reset	$\overline{WR}$ and $\overline{M}$/A low	0			ns
t_{su13}	Setup time, word reset	$\overline{M}$/A low before $\overline{WR}$ low	0			ns
		$\overline{WR}$ low before $\overline{M}$/A low	0			
t_{h1}	Hold time, address after LRU-W↓ (see Note 4)		9			ns
t_{h2}	Hold time, $\overline{S}$ low after LRU-W↓		5			ns
t_{h3}	Hold time, address after $\overline{W}$ high		2			ns
t_{h4}	Hold time, $\overline{S}$ low after $\overline{W}$ high		0			ns
t_{h5}	Hold time, BSEL after $\overline{W}$ high		2			ns
t_{h6}	Hold time, $\overline{M}$/A after $\overline{W}$ high		2			ns
t_{h7}	Hold time, D0-D3 after $\overline{W}$ high		5			ns
t_{h8}	Hold time, $\overline{R}$ low after $\overline{W}$ high (see Note 3)		1			ns
t_{h9}	Hold time, address after word reset	$\overline{WR}$ or $\overline{M}$/A high	2			ns
t_{h10}	Hold time, BSEL after word reset	$\overline{WR}$ or $\overline{M}$/A high	2			ns
t_{h11}	Hold time, $\overline{S}$ low after word reset	$\overline{WR}$ or $\overline{M}$/A high	0			ns
t_{h12}	Hold time, word reset	$\overline{M}$/A low after $\overline{WR}$ high	0			ns
		$\overline{WR}$ low after $\overline{M}$/A high	0			

† All typical values are at V_{CC} = 5 V, T_A = 25°C.

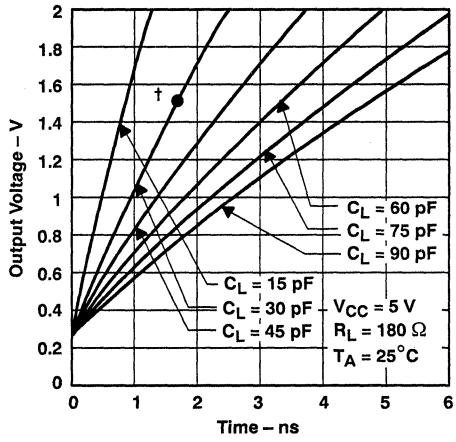
NOTES: 3. Parameters t_{su8} and t_{h8} apply only during the write cycle timing when writing a parity error. It should be noted that if $\overline{R}$ is low when $\overline{W}$ is high, D0-D3 are enabled as outputs.

4. Minimum t_{h1} is the time interval after LRU-W goes low during which the address must remain valid to ensure that an internal LRU write occurs.

ADVANCE INFORMATION

TYPICAL CHARACTERISTICS

LOW-TO-HIGH TRANSITION
OF MATCH1, MATCH2, AND $\overline{PE}$ OUTPUTS
FOR VARIOUS LOADS
OUTPUT VOLTAGE vs TIME

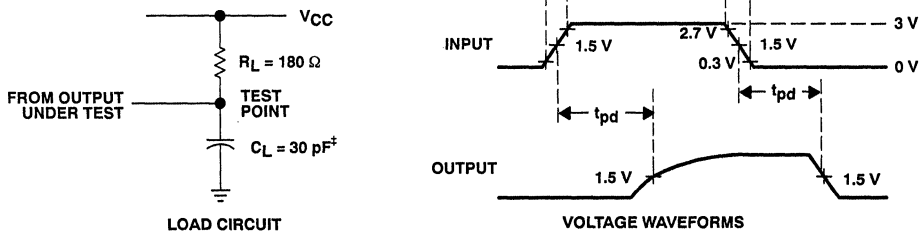


† Specified switching characteristics for open-drain outputs are specified at V_O = 1.5 V with C_L = 30 pF.

FIGURE 1

Figure 1 is provided as a tool to determine how propagation delay specifications for a 27-mA open-drain output will change with different load capacitance. For example from Figure 1, it can be seen that a 15-pF load will cause about a 1-ns decrease in specified propagation delay while a 60-pF load will cause a 1.7-ns increase in a specified propagation delay.

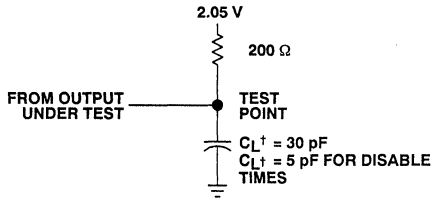
PARAMETER MEASUREMENT INFORMATION



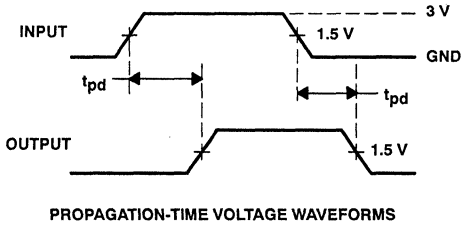
‡ C_L includes probe and test fixture capacitance.

FIGURE 2. OPEN-DRAIN OUTPUTS

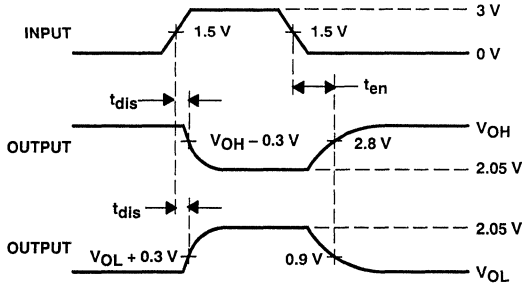
PARAMETER MEASUREMENT INFORMATION



LOAD CIRCUIT



PROPAGATION-TIME VOLTAGE WAVEFORMS



ENABLE/DISABLE VOLTAGE WAVEFORMS

† C_L includes probe and test fixture capacitance.

FIGURE 3. ALL OTHER OUTPUTS

ADVANCE INFORMATION

PARAMETER MEASUREMENT INFORMATION

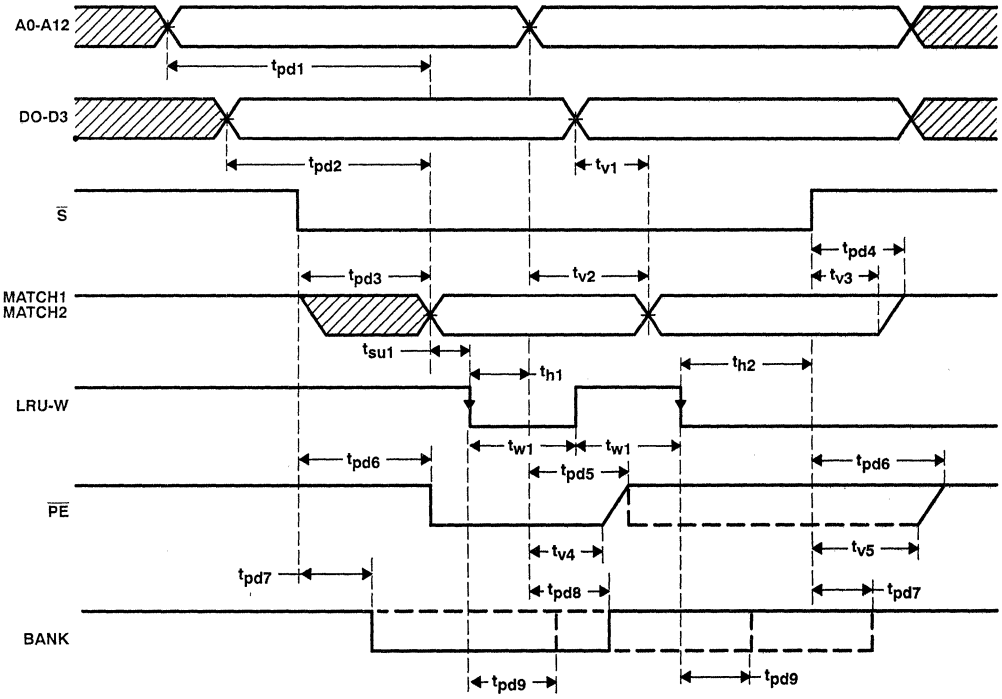


FIGURE 4. COMPARE CYCLE TIMING

PARAMETER MEASUREMENT INFORMATION

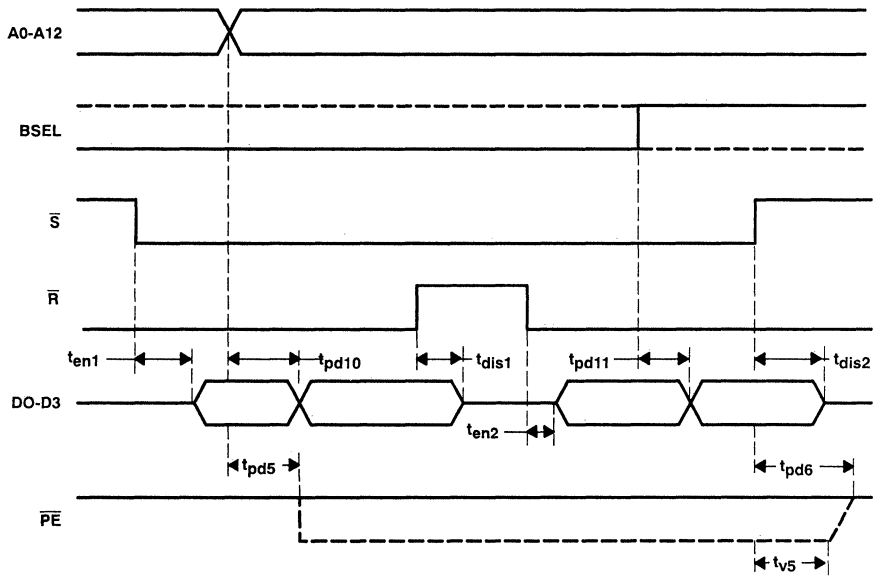


FIGURE 5. READ CYCLE TIMING

ADVANCE INFORMATION

PARAMETER MEASUREMENT INFORMATION

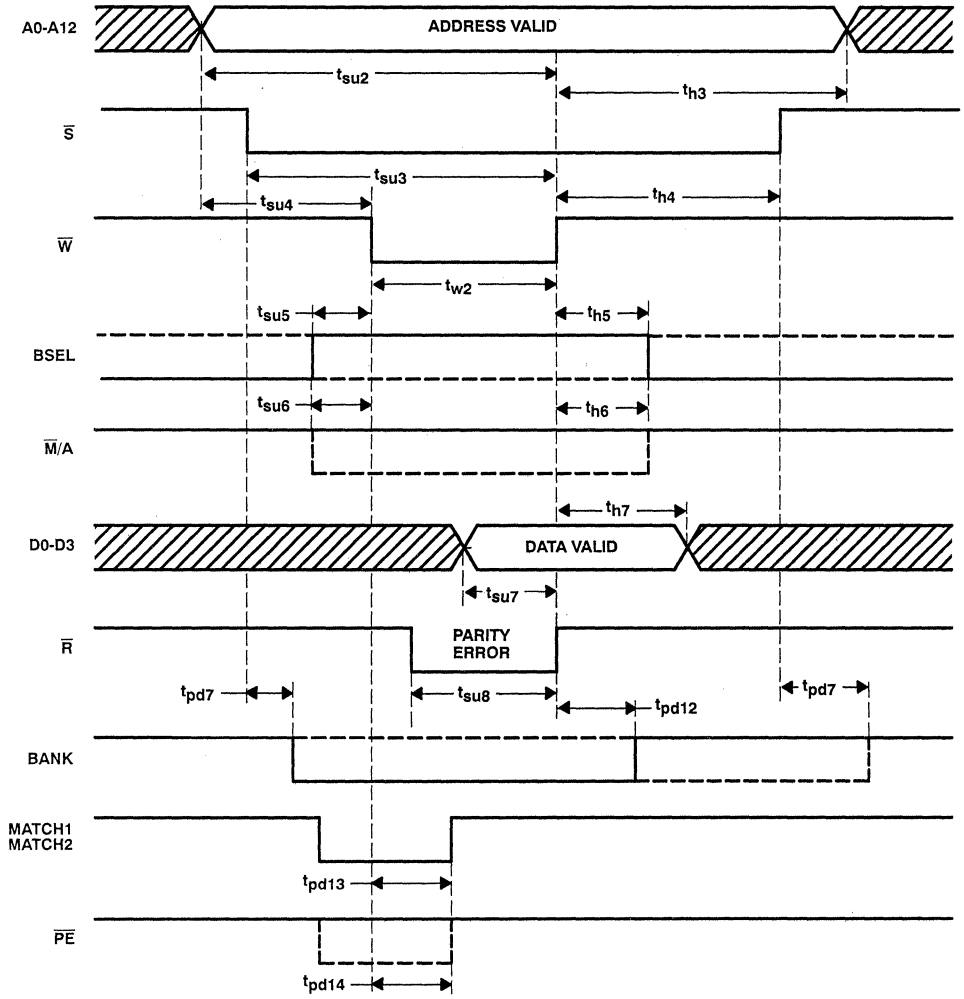


FIGURE 6. WRITE CYCLE TIMING

PARAMETER MEASUREMENT INFORMATION

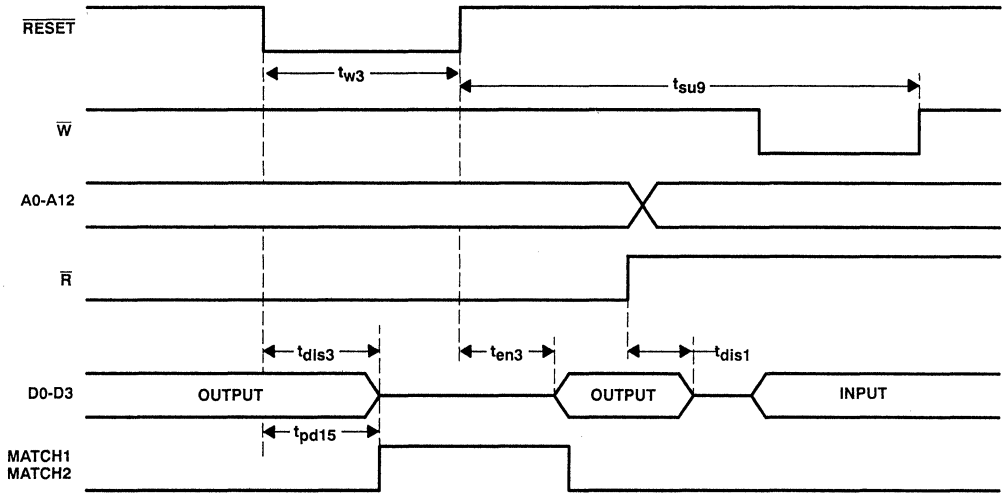


FIGURE 7. RESET CYCLE TIMING

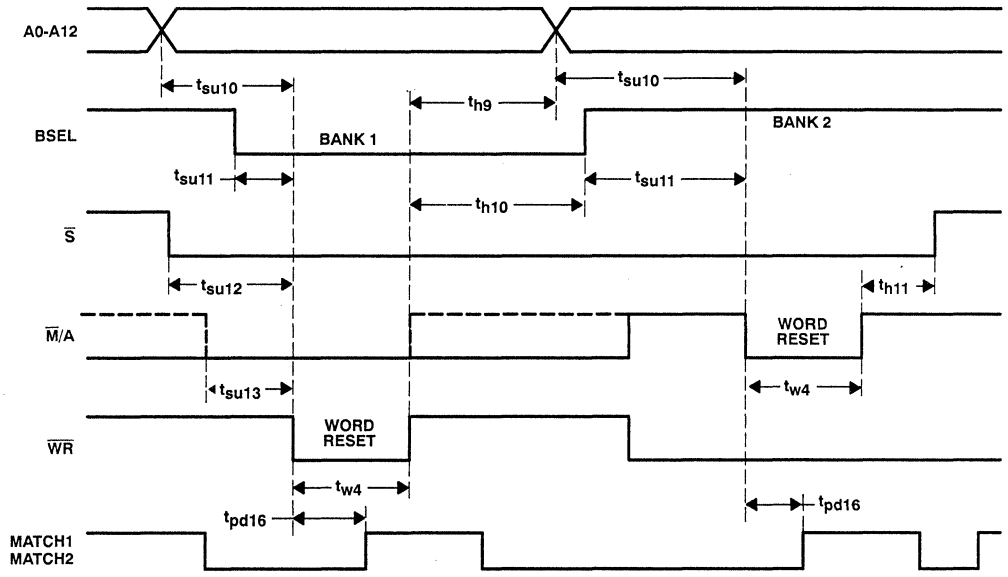


FIGURE 8. WORD RESET TIMING

ADVANCE INFORMATION

PARAMETER MEASUREMENT INFORMATION

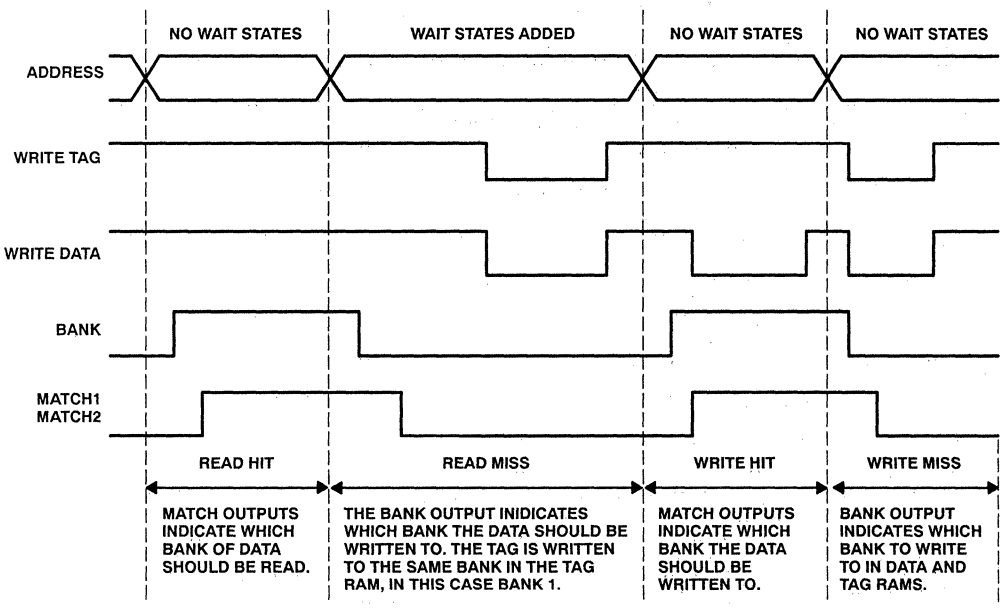


FIGURE 9. CACHE CYCLES

PARAMETER MEASUREMENT INFORMATION

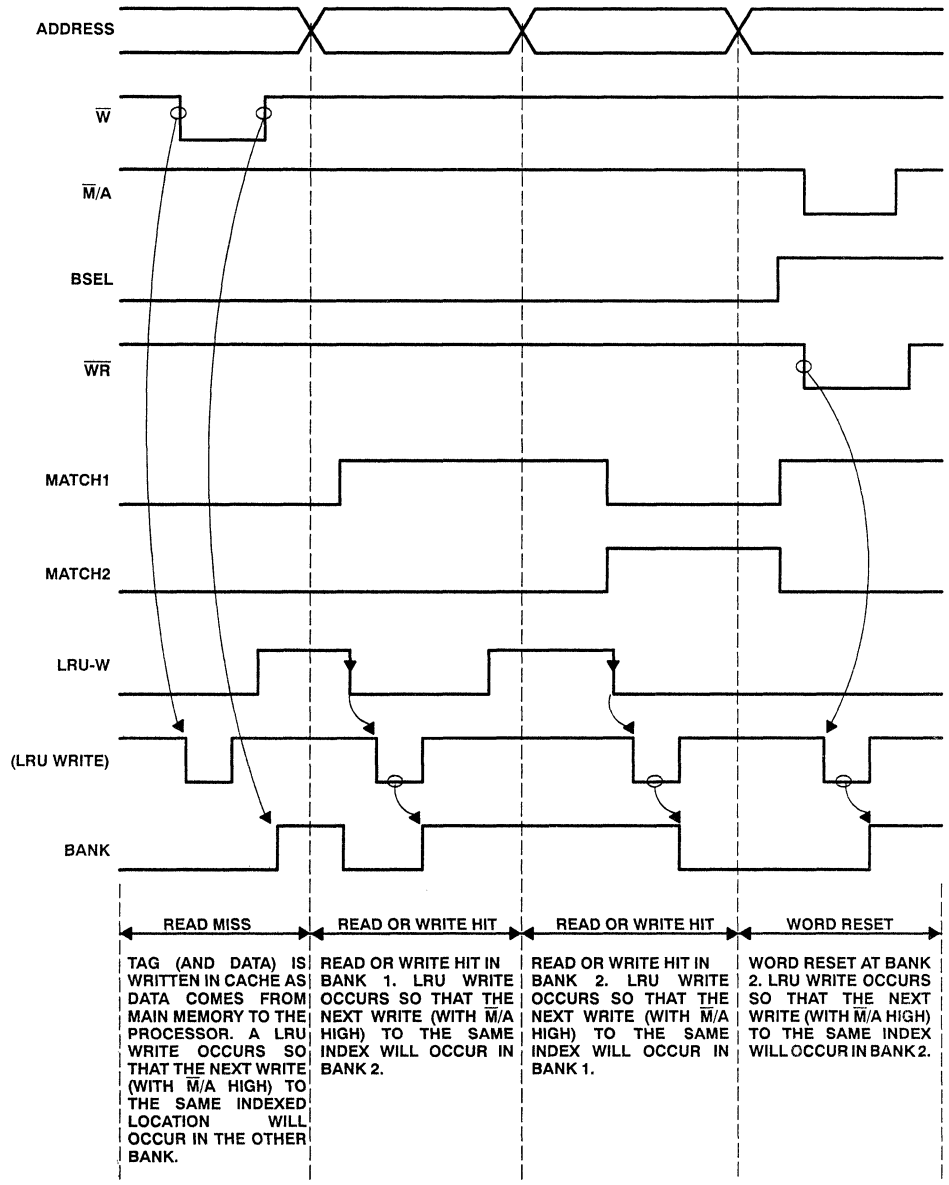
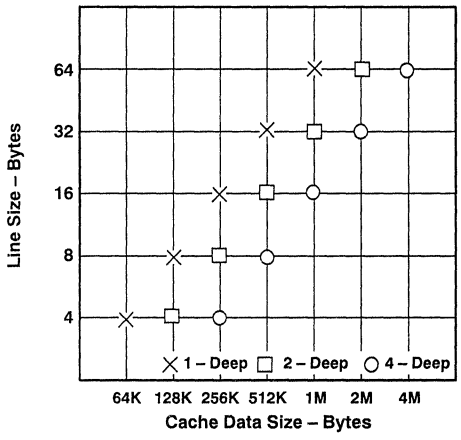


FIGURE 10. LRU WRITE TIMING DIAGRAM

ADVANCE INFORMATION

APPLICATION INFORMATION

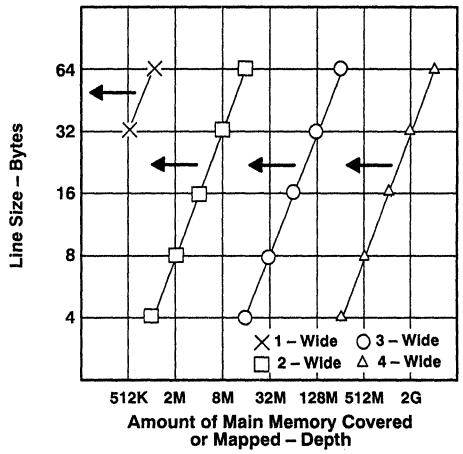
DEPTH CASCADING
NUMBER OF DEVICES
CACHE SIZE
vs
LINE SIZE†



† Direct-mapped caches

FIGURE 11

WIDTH CASCADING
NUMBER OF DEVICES
MAIN MEMORY COVERAGE
vs
LINE SIZE‡



‡ One tag/line. Assumes a word length of 32 bits.

FIGURE 12

depth cascading

For four-way caches, each solution shown in Figure 11 is moved to the right one increment doubling the cache size and the number of devices used.

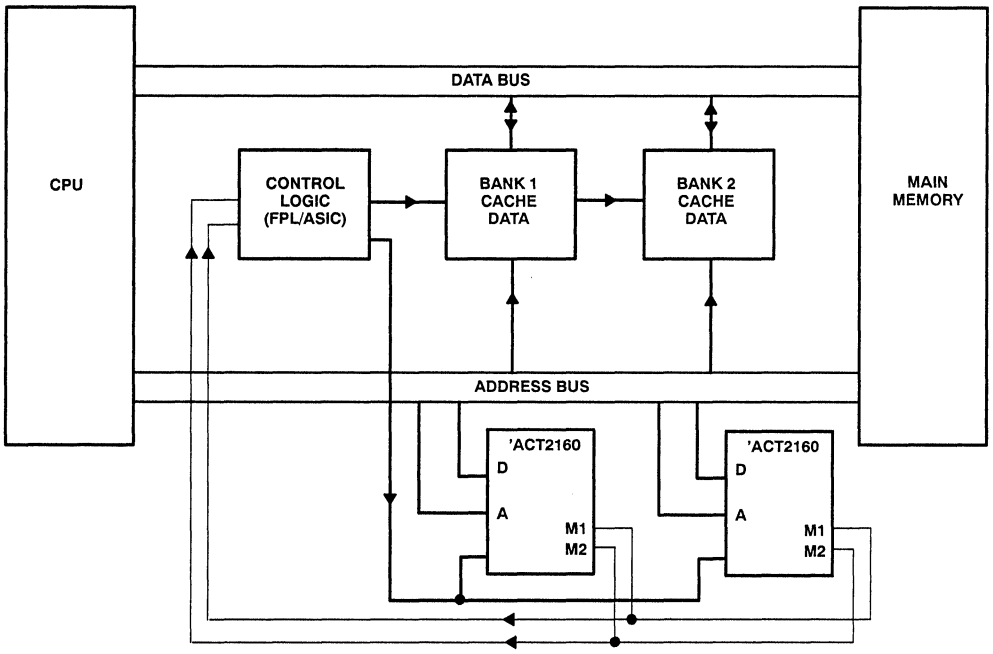
width cascading

Memory coverage assumes one bit used as a valid bit (See Figure 12). Each solution for a given line size can be moved to the left covering smaller amounts of memory. Each increment moved represents an unused tag bit. When cascading in depth memory coverage increases, i.e., two deep — twice as much memory.

usage explanation and example

Figures 11 and 12 provide a quick means for determining if the 'ACT2160 will provide a good solution and the number of devices needed for implementation. For example, a design requires 256K bytes of two-way cache, memory coverage of 256M, and a line size of 16 bytes (a 16-byte line size means each tag location maps four 32-bit words of cached data). From Figure 11, it is determined that one 'ACT2160 deep will provide a 256K byte cache with a 16-byte line size. From Figure 12, it is determined that four 'ACT2160s cascaded in width will map 256M of memory (or as much as 1G). Therefore, one deep by four wide (four 'ACT2160s) are needed to meet the design's requirements.

APPLICATION INFORMATION



CACHE SIZE† (BYTES)	LINE SIZE† (BYTES)
64K	4
128K	8
256K	16
512K	32
1M	64

† Assumes 1 tag per line & 8K of tag depth. The cache size line size relationship shown can be changed by cascading the 'ACT2160 in depth.

FIGURE 13. TWO-WAY CACHE USING THE 'ACT2160

ADVANCE INFORMATION

APPLICATION INFORMATION

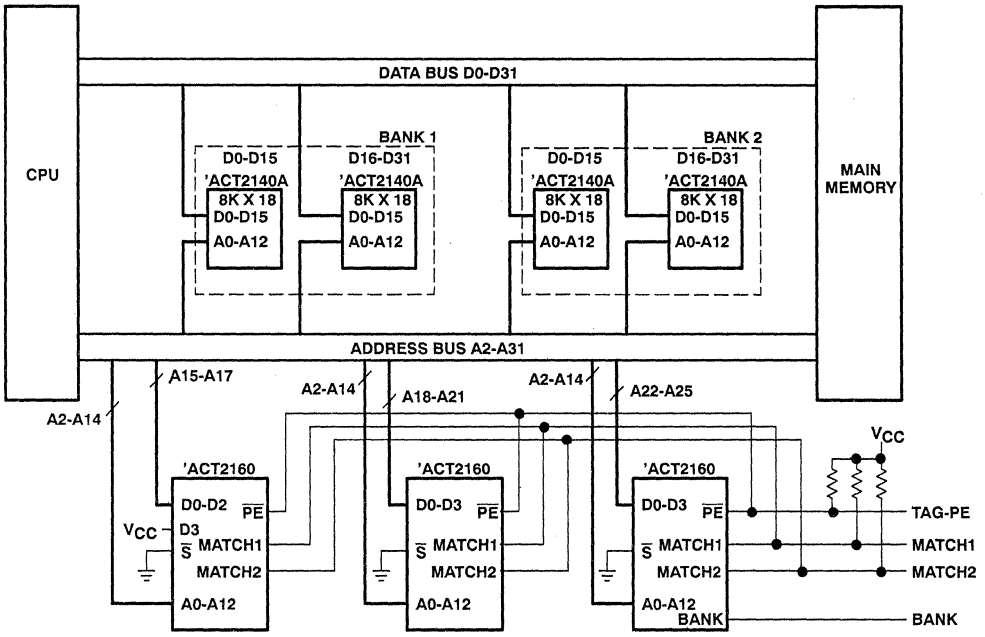


FIGURE 14. 64K BYTE TWO-WAY SET ASSOCIATIVE CACHE, LINE SIZE = 4 BYTES

APPLICATION INFORMATION

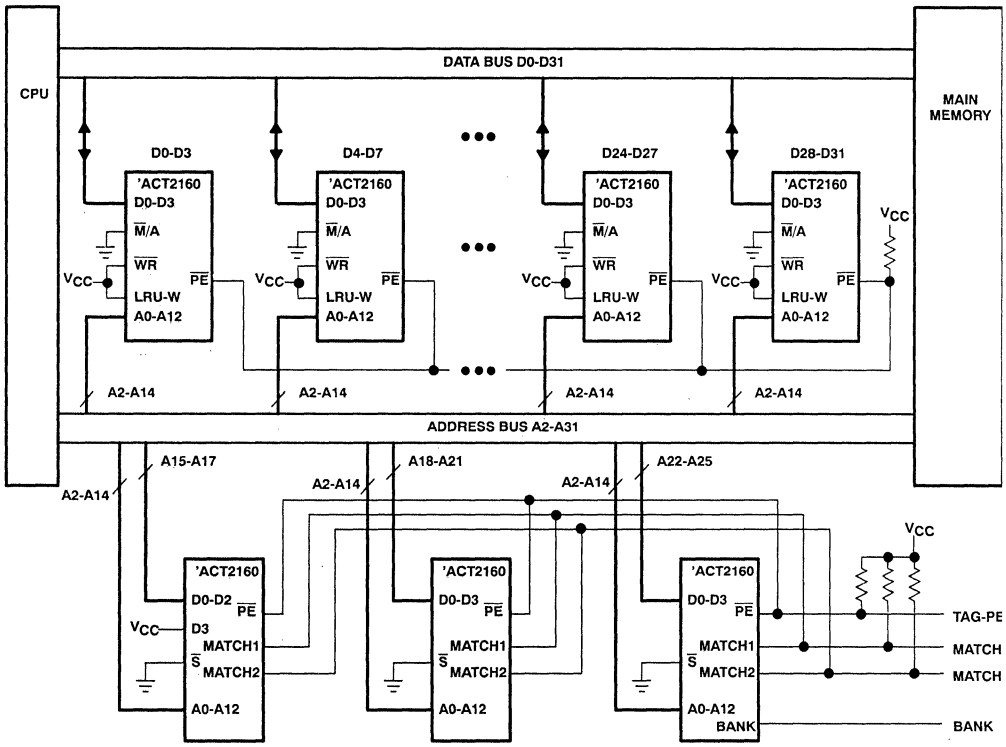


FIGURE 15. 64K BYTE TWO-WAY ASSOCIATIVE CACHE, LINE SIZE = 4 BYTES

ADVANCE INFORMATION

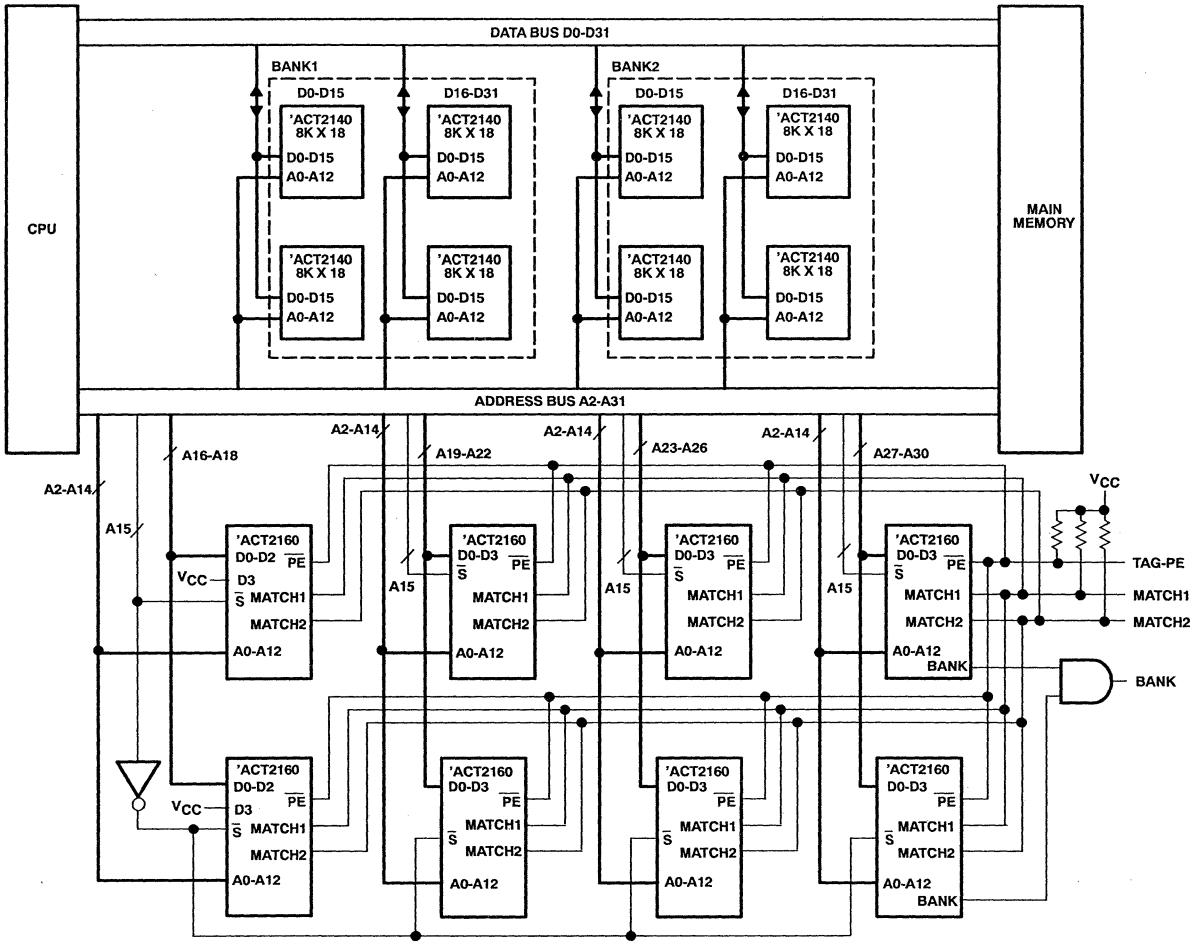


FIGURE 16. 128K BYTE CACHE, LINE SIZE = 4 BYTES

APPLICATION INFORMATION

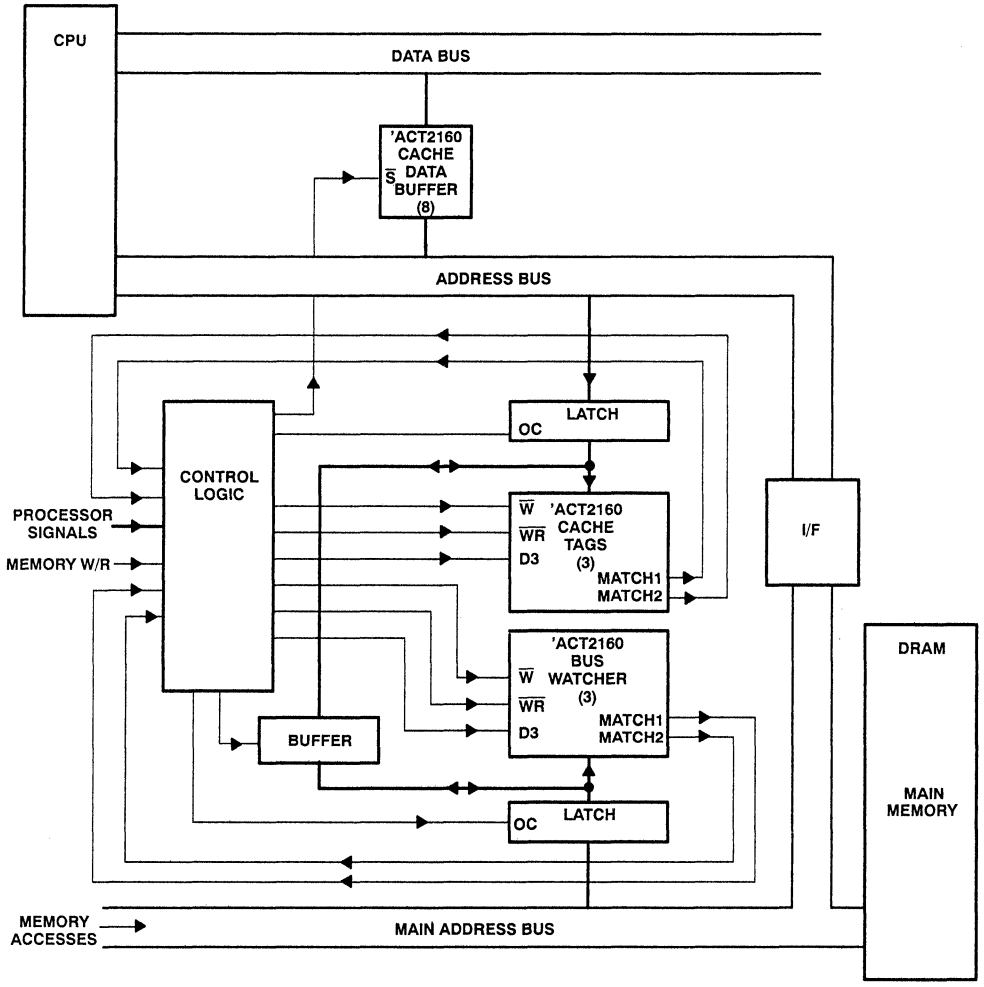


FIGURE 17. BUS WATCHING WITH THE 'ACT2160

ADVANCE INFORMATION