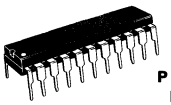
MCM6270

Advance Information

4K x 4 Bit Static RAM



P PACKAGE
PLASTIC
CASE 736A

J PACKAGE
300 MIL SOJ
CASE 810A

The MCM6270 is a 16,384-bit static random access memory organized as 4096 words of 4 bits, fabricated using Motorola's high-performance silicon-gate CMOS technology. Static design eliminates the need for external clocks or timing strobes, while CMOS circuitry reduces power consumption for greater reliability.

The MCM6270 is equipped with both chip enable ($\overline{E}$) and output enable ($\overline{G}$) inputs, allowing for greater system flexibility. Either input, when high, will force the outputs to high impedance.

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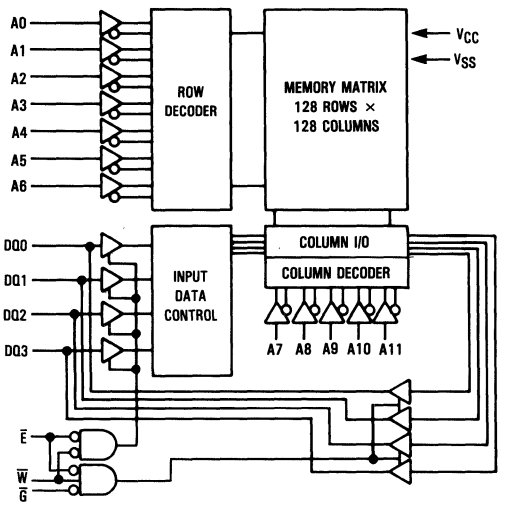
- Single 5 V Supply, ±10%
- Fully Static—No Clock or Timing Strobes Necessary
- Three-State Outputs
- Fully TTL Compatible
- Fast Access Time (Maximum):

	Address	Chip Enable	Output Enable
MCM6270-20	20 ns	20 ns	10 ns
MCM6270-25	25 ns	25 ns	12 ns
MCM6270-35	35 ns	35 ns	14 ns

- Low Power Operation: 110 mA Maximum, Active AC
- Output Enable ($\overline{G}$) Feature for Increased System Flexibility and to Eliminate Bus Contention Problems

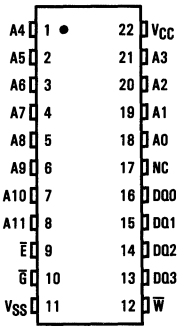
BLOCK DIAGRAM



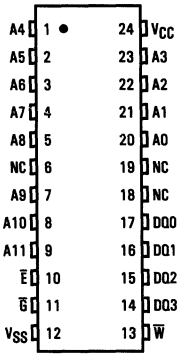
PIN NAMES	
A0-A11 . . . . . Address Input	$\overline{E}$ . . . . . Chip Enable
DQ0-DQ3 . Data Input/Output	V_{CC} . . . +5 V Power Supply
$\overline{W}$ . . . . . Write Enable	V_{SS} . . . . . Ground
$\overline{G}$ . . . . . Output Enable	NC . . . . . No Connection

PIN ASSIGNMENT

DUAL-IN-LINE



SMALL OUTLINE



This document contains information on a new product. Specifications and information herein are subject to change without notice.

TRUTH TABLE

$\overline{E}$	$\overline{G}$	$\overline{W}$	Mode	V_{CC} Current	I/O Pin	Cycle
H	X	X	Not Selected	I_{SB}	High-Z	—
L	H	H	Read	I_{CCA}	High-Z	—
L	L	H	Read	I_{CCA}	D_{out}	Read Cycle
L	X	L	Write	I_{CCA}	D_{in}	Write Cycle

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high-impedance circuit.

ABSOLUTE MAXIMUM RATINGS (See Note)

Rating	Symbol	Value	Unit
Power Supply Voltage (V_{CC})	V_{CC}	−0.5 to +7.0	V
Voltage Relative to V_{SS} for Any Pin Except V_{CC}	V_{in}, V_{out}	−0.5 to V_{CC}+0.5	V
Output Current (per I/O)	I_{out}	±20	mA
Power Dissipation (+25°C)	P_D	1.0	W
Temperature Under Bias	T_{bias}	−10 to +85	°C
Operating Temperature	T_A	0 to +70	°C
Storage Temperature	T_{stg}	−55 to +125	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

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DC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ±10%, T_A = 0 to 70°C, Unless Otherwise Noted)

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage (Operating Voltage Range)	V_{CC}	4.5	5.0	5.5	V
Input High Voltage	V_{IH}	2.0	—	V_{CC}+0.3	V
Input Low Voltage	V_{IL}	−0.5*	—	0.8	V

*V_{IL} (min) = −0.5 V dc; V_{IL} (min) = −3.0 V ac (pulse width ≤20 ns)

DC CHARACTERISTICS

Parameter	Symbol	Min	Max	Unit
Input Leakage Current (All Inputs, V_{in} = 0 to V_{CC})	$I_{lkg(I)}$	—	±1.0	μA
Output Leakage Current ($\overline{E}$ = V_{IH} or $\overline{G}$ = V_{IH} or $\overline{W}$ = V_{IL}, V_{out} = 0 to V_{CC})	$I_{lkg(O)}$	—	±1.0	μA
AC Supply Current (I_{out} = 0 mA)	I_{CCA}	—	110	mA
TTL Standby Current ($\overline{E}$ = V_{IH}, No Restrictions on Other Inputs)	I_{SB1}	—	20	mA
CMOS Standby Current ($\overline{E}$ ≥ V_{CC} − 0.2 V, No Restrictions on Other Inputs)	I_{SB2}	—	15	mA
Output Low Voltage (I_{OL} = 8.0 mA)	V_{OL}	—	0.4	V
Output High Voltage (I_{OH} = −4.0 mA)	V_{OH}	2.4	—	V

CAPACITANCE (f = 1.0 MHz, dV = 3.0 V, T_A = 25°C, Periodically Sampled Rather Than 100% Tested)

Characteristic		Symbol	Typ	Max	Unit
Input Capacitance	All Inputs Except $\overline{E}$	C_{in}	4	6	pF
	$\overline{E}$		5	7	
I/O Capacitance	DQ	$C_{I/O}$	5	7	pF

AC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC}=5 V ±10%, T_A=0 to +70°C, Unless Otherwise Noted)

Input Timing Measurement Reference Level . . . . . 1.5 V
Input Pulse Levels . . . . . .0 to 3.0 V
Input Rise/Fall Time . . . . . 5 ns

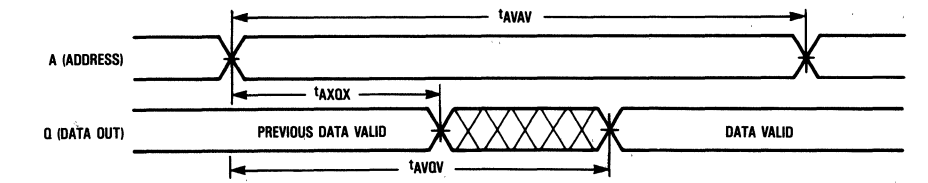
Output Timing Measurement Reference Level . . . . . 1.5 V
Output Load . . . . . Figure 1A Unless Otherwise Noted

READ CYCLE (See Note 1)

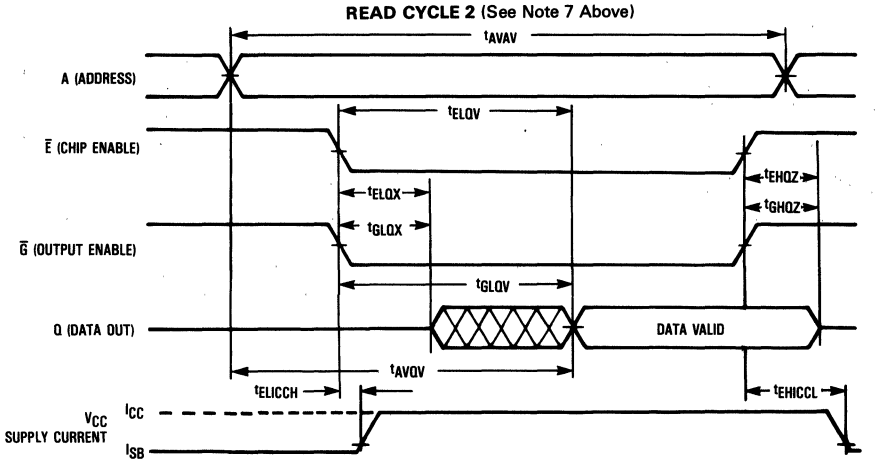
Parameter	Symbol		MCM6270-20		MCM6270-25		MCM6270-35		Unit	Notes
	Standard	Alternate	Min	Max	Min	Max	Min	Max		
Read Cycle Time	t_{AVAV}	t_{RC}	20	–	25	–	35	–	ns	2
Address Access Time	t_{AVQV}	t_{AA}	–	20	–	25	–	35	ns	
Chip Enable Access Time	t_{ELQV}	t_{ACS}	–	20	–	25	–	35	ns	
Output Enable Access Time	t_{GLQV}	t_{OE}	–	10	–	12	–	14	ns	
Output Hold from Address Change	t_{AXQX}	t_{OH}	4	–	5	–	5	–	ns	
Chip Enable Low to Output Active	t_{ELQX}	t_{LZ}	4	–	5	–	5	–	ns	3,4,5
Chip Enable High to Output High-Z	t_{EHQZ}	t_{HZ}	0	8	0	10	0	15	ns	3,4,5
Output Enable Low to Output Active	t_{GLQX}	t_{LZ}	0	–	0	–	0	–	ns	3,4,5
Output Enable High to Output High-Z	t_{GHQZ}	t_{HZ}	0	8	0	10	0	15	ns	3,4,5
Power Up Time	t_{ELICCH}	t_{PU}	0	–	0	–	0	–	ns	
Power Down Time	t_{EHICCL}	t_{PD}	–	20	–	20	–	30	ns	

NOTES: 1. $\overline{W}$ is high for read cycle.
2. All read cycle timing is referenced from the last valid address to the first transitioning address.
3. At any given voltage and temperature, t_{EHQZ} max is less than t_{ELQX} min, and t_{GHQZ} max is less than t_{GLQX} min, both for a given device and from device to device.
4. Transition is measured ±500 mV from steady-state voltage with load of Figure 1B.
5. This parameter is sampled and not 100% tested.
6. Device is continuously selected ($\overline{E}$=V_{IL}, $\overline{G}$=V_{IL}).
7. Addresses valid prior to or coincident with $\overline{E}$ going low.

READ CYCLE 1 (See Note 6 Above)



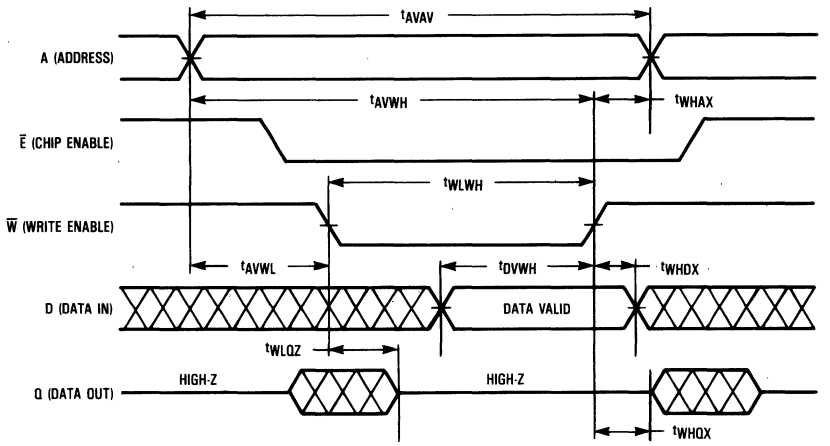
READ CYCLE 2 (See Note 7 Above)



WRITE CYCLE 1 ($\overline{W}$ Controlled, See Notes 1 and 2)

Parameter	Symbol		MCM6270-20		MCM6270-25		MCM6270-35		Unit	Notes
	Standard	Alternate	Min	Max	Min	Max	Min	Max		
Write Cycle Time	t_{AVAV}	t_{WC}	20	–	25	–	35	–	ns	3
Address Setup Time	t_{AVWL}	t_{AS}	0	–	0	–	0	–	ns	
Address Valid to End of Write	t_{AVWH}	t_{AW}	15	–	20	–	30	–	ns	
Write Pulse Width	t_{WLWH}	t_{WP}	15	–	20	–	25	–	ns	
Data Valid to End of Write	t_{DVWH}	t_{DW}	10	–	10	–	15	–	ns	
Data Hold Time	t_{WHDX}	t_{DH}	0	–	0	–	0	–	ns	
Write Low to Output High-Z	t_{WLQZ}	t_{WZ}	0	8	0	10	0	15	ns	4,5,6
Write High to Output Active	t_{WHQX}	t_{OW}	4	–	5	–	5	–	ns	4,5,6
Write Recovery Time	t_{WHAX}	t_{WR}	0	–	0	–	0	–	ns	

NOTES:
1. A write occurs during the overlap of $\overline{E}$ low and $\overline{W}$ low.
2. If $\overline{G}$ goes low coincident with or after $\overline{W}$ goes low, the output will remain in a high impedance state.
3. All write cycle timing is referenced from the last valid address to the first transitioning address.
4. Transition is measured ±500 mV from steady-state voltage with load in Figure 1B.
5. Parameter is sampled and not 100% tested.
6. At any given voltage and temperature, t_{WLQZ} max, is less than t_{WHQX} min, both for a given device and from device to device.



AC TEST LOADS

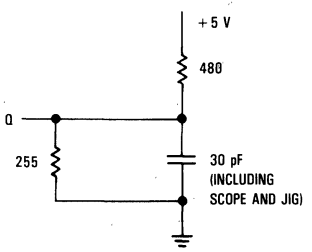


Figure 1A

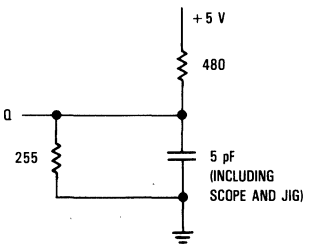
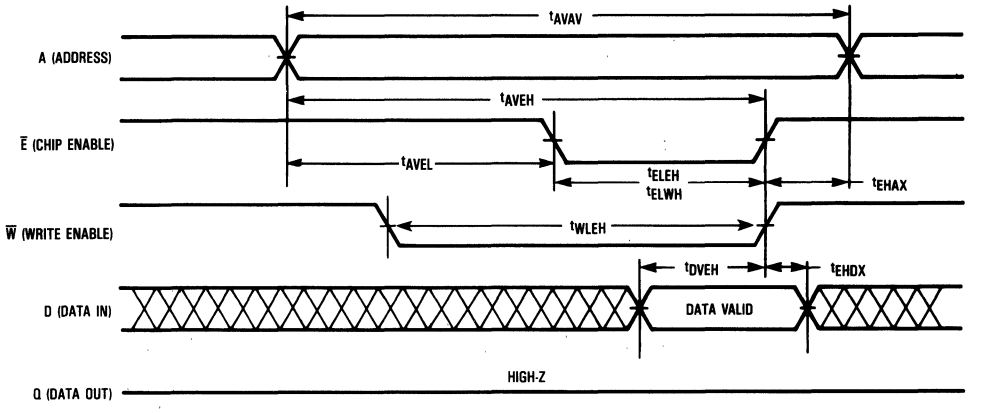


Figure 1B

WRITE CYCLE 2 ($\overline{E}$ Controlled; See Notes 1 and 2)

Parameter	Symbol		MCM6270-20		MCM6270-25		MCM6270-35		Unit	Notes
	Standard	Alternate	Min	Max	Min	Max	Min	Max		
Write Cycle Time	t_{AVAV}	t_{WC}	20	–	25	–	35	–	ns	3
Address Setup Time	t_{AVEL}	t_{AS}	0	–	0	–	0	–	ns	
Address Valid to End of Write	t_{AVEH}	t_{AW}	15	–	20	–	30	–	ns	
Chip Enable to End of Write	t_{ELEH}	t_{CW}	15	–	20	–	30	–	ns	4,5
Chip Enable to End of Write	t_{ELWH}	t_{CW}	15	–	20	–	30	–	ns	4,5
Write Pulse Width	t_{WLEH}	t_{WP}	15	–	20	–	25	–	ns	
Data Valid to End of Write	t_{DVEH}	t_{DW}	10	–	10	–	15	–	ns	
Data Hold Time	t_{EHDX}	t_{DH}	0	–	0	–	0	–	ns	
Write Recovery Time	t_{EHAX}	t_{WR}	0	–	0	–	0	–	ns	

NOTES:
1. A write occurs during the overlap of $\overline{E}$ low and $\overline{W}$ low.
2. If $\overline{G}$ goes low coincident with or after $\overline{W}$ goes low, the output will remain in a high impedance state.
3. All write cycle timing is referenced from the last valid address to the first transitioning address.
4. If $\overline{E}$ goes low coincident with or after $\overline{W}$ goes low, the output will remain in a high impedance condition.
5. If $\overline{E}$ goes high coincident with or before $\overline{W}$ goes high, the output will remain in a high impedance condition.



ORDERING INFORMATION
(Order by Full Part Number)

MCM 6270 X XX XX

- MCM — Motorola Memory Prefix
- 6270 — Part Number
- X — Package (P = Plastic DIP, J = Plastic SOJ)
- XX — Speed (20 = 20 ns, 25 = 25 ns, 35 = 35 ns)
- XX — Shipping Method (R2 = Tape & Reel, Blank = Rails)

Full Part Numbers—

MCM6270P20	MCM6270P25	MCM6270P35
MCM6270J20	MCM6270J25	MCM6270J35
MCM6270J20R2	MCM6270J25R2	MCM6270J35R2