82310/11
Micro Channel* Compatible Peripheral Family

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November 1988
Order Number: 290167-002

Micro Channel COMPATIBLE PERIPHERALS FAMILY

High Performance/High Integration/100% Compatibility

- **Total Solution ... High Integration VLSI Components Implement Complete Micro Channel Compatible Motherboards**
- **Single Architectural Solution for 80386 and 80386SX Systems**
- **High Performance**
  - **— 80386 Systems to 25 MHz**
  - **— Up to 16 MB of Zero Wait State Page-Interleaved DRAM**
  - **— Interface to Industry Standard 82385 Cache Controller for Maximum Performance Memory Design**
- **100% Compatible at All Levels**
  - **— Architecture Compatible**
  - **— Register Level Compatible**
  - **— Compatible with All Micro Channel Bus Timing and Drive Characteristics**
- **High Integration ... Two Chip Sets to Choose from, 82310 and More Highly Integrated 82311**
- **82310 Chip Set Includes:**
  - **— 82306 Local Channel Support Chip**
  - **— 82307 DMA Controller/Central Arbiter**
  - **— 82308 Micro Channel Bus Controller**
  - **— 82309 Address Bus Controller**
  - **— 82706 VGA Graphics Controller**
- **82311 Chip Set Includes:**
  - **— 82303 and 82304 Local I/O Channel Support Chips**
  - **— 82307 DMA Controller/Central Arbiter**
  - **— 82308 Micro Channel Bus Controller**
  - **— 82309 Address Bus Controller**
  - **— 82706 VGA Graphics Controller**
  - **— 82077 Floppy Disk Controller**

Intel's Micro Channel Peripheral Family consists of two chip sets, either of which can be used to build a high performance, 100% Micro Channel compatible motherboard. The two chip sets differ primarily in their implementation of the motherboard peripheral bus. The 82310 Chip Set supports either the 8272A or 82072 Floppy Disk Controller. The 82311 Chip Set features a more highly integrated peripheral bus, and includes the 82077 Single Chip Floppy Disk Controller. (The 82311 chip set does not support the 8272A or 82072.) Both chip sets support 80386 systems up to 25 MHz and 80386SX 16 MHz systems.

The following pages describe Intel's Micro Channel Peripheral Family. The first section presents an overview of the 82310 and 82311 chip sets, and discusses system issues such as clock requirements and Micro Channel interface logic. Following this are the individual component descriptions and specifications.

		82310 Chip Set	82311 Chip Set
82303	Local I/O Support Chip		✓
82304	Local I/O Support Chip		✓
82306	Local Channel Support Chip	✓	
82307	DMA/Micro Channel Arbitration Controller	✓	✓
82308	Micro Channel Bus Controller	✓	✓
82309	Address Bus Controller	✓	✓
82706	VGA Graphics Controller	✓	✓
82077	Floppy Disk Controller		✓

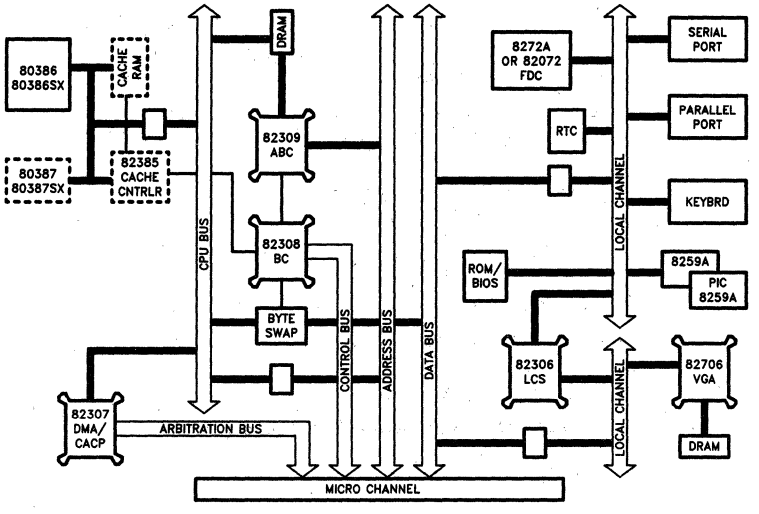
Figure 1. Micro Channel Peripheral Family

82310
Micro Channel COMPATIBLE PERIPHERAL CHIP SET

- **Highly Integrated VLSI Components to Implement Micro Channel™ Compatible Motherboard**
- **Single Architectural Solution for 80386 16 MHz, 20 MHz and 25 MHz systems, and 80386SX 16 MHz Systems**
- **Full Compatibility with IBM Micro Channel Architecture**
- **Zero-Wait State Performance**
- **Cache Interface (82385) for Highest Performance Compatible System Implementation with 80386**
- **Supports up to 16 MB of Memory on Motherboard**
  — Extended Memory for OS/2 Support
- **100% IBM Compatible VGA Graphics**
- **Flexible Memory Architecture Support**
  — Up to 4 Banks of Interleaved Page Memory
  — 256K, 1M, 4M DRAM Support
- **Multiple Floppy Disk Controller Interface to Support 3½" and 5¼" Disk Drives**
- **Keyboard and BIOS Support from 3rd Party**
- **Numeric Coprocessor(s) Interface (80387, 80387SX)**
- **Surface Mount Packaging for Small Footprint Design (0.025" Pitch)**
- **Low Power CHMOS Technology**
- **Available in 100 & 132-Pin Plastic Quad Flat Pack Packages.**
  (See Packaging Spec. # 231369)

Intel's peripheral chip family is designed to support the new generation of Micro Channel compatible systems. Intel's Micro Channel compatible peripheral solution consists of highly integrated VLSI components designed to support 80386 systems up to 25 MHz, as well as 16 MHz 80386SX systems.

The Intel solution is based on the high performance IBM Model 80 register model but it is highly integrated to provide full compatibility across all models. The specifications for 82310 VLSI components conform to architectural specifications defined for the Micro Channel Bus Architecture. The VLSI components are implemented in 1.5 micron CHMOS technology and packaged in space saving surface mount JEDEC flat pack packages.



290167-1

INTRODUCTION

The new generation of Personal Computer systems from IBM offers significant technological advantages over the PC/AT and XT systems. The most significant advancement is in the *Architectural* definition of the bus—Micro Channel Bus. Unlike the AT bus, the Micro Channel is well defined in terms of bus protocol timings. To create a compatible Micro Channel system requires adherence to the Micro Channel timings and electrical drive characteristics.

All IBM Micro Channel models have increased system functionality included on the motherboard. In the older PC/AT architecture, such functionality required the addition of peripheral cards. Specific features added to the motherboard include the Serial Port, Bi-directional Parallel Port and Video Graphics Control.

Micro Channel ARCHITECTURE

The Micro Channel Bus is defined to support an open architecture providing Multi-Master capability, Multi-Device arbitration with fairness, arbitration capability and easy configurability of the total system (Programmable Option Select-POS). Providing full details about the Micro Channel Bus Architecture is beyond the scope of this document. Please refer to IBM Technical Reference Manuals on Micro Channel systems.

To provide Multi-Master capability as defined in the Micro Channel Architecture, each Master device is responsible for driving the Address, Data, arbitration and control signals. For operation reliability and compatibility there are significant constraints in terms of timing and drive levels. These constraints are well documented in IBM's Technical Reference Manual for Micro Channel systems. Intel's chip set is designed to meet the Micro Channel timings.

The Micro Channel has four modes of Memory and I/O Bus cycles. These are Default cycle, Synchronous Extended cycle, Asynchronous Extended cycle and Matched Memory cycle. Each of these bus cycles is supported by the Intel Peripheral chip set.

COMPATIBILITY METRICS

The Intel chip set provides full compatibility with the IBM Micro Channel solution. All Bus cycles comply with the Micro Channel timings. Selection of buffers for drive level with minimum delays to meet Micro Channel timings are specified in the Intel *Designers Guide for Micro Channel Compatible Implementation.*

MEMORY PERFORMANCE

With the Intel chip set, Micro Channel compatible motherboards can be designed to provide zero-wait performance. Performance is predicated on memory design and DRAM speed selection. The Intel chip set offers flexible memory design support to meet various cost/performance goals.

SYSTEM CONSIDERATIONS

System Components

82306	Local Channel Support Chip
82307	DMA/CACP Controller
82308	Micro Channel Bus Controller
82309	Address Bus Controller
82706	VGA Graphics Controller

Note that the above part names/numbers are frequency independent; i.e., they refer to a generic functional VLSI device. To actually implement for example, a 20 MHz system, however requires an 82310-20 Chip Set as opposed to an 82310-16 Chip Set. The 25 MHz version of the 82308 (dubbed the 82308HS-25) cannot be used at 16 MHz or 20 MHz.

To implement a minimum configuration Micro Channel compatible motherboard, each of the five system components listed above are required in addition to the following components:

- 80386 or 80386SX Microprocessor
- TTL/CMOS Buffers for Various Buses in the System
- 8742 Keyboard Controller with Firmware for 101 and 102 Keyboard Interface
- 8272A or 82072 for Floppy Disk Controller
- — 8272A Required to Maintain IBM Look-Alike Motherboard with 3½" Drive Support
- — 82072 for PS/2 Compatible 3½" and AT Compatible 5¼" Disk Drive Interface
- Battery-Backed Real Time Clock with CMOS RAM
- Serial Port
- Parallel Port
- Programmable Interrupt Controllers (Two 8259s)
- Memory
- — ROM BIOS
- — DRAMs for Main Memory
- — DRAMs for VGA
- System Clock Sources
- Mechanical Connectors/Components

The Intel solution is supported by a fully compatible BIOS firmware from a third-party vendor.

82310 CHIP SET SYSTEM CLOCK REQUIREMENTS

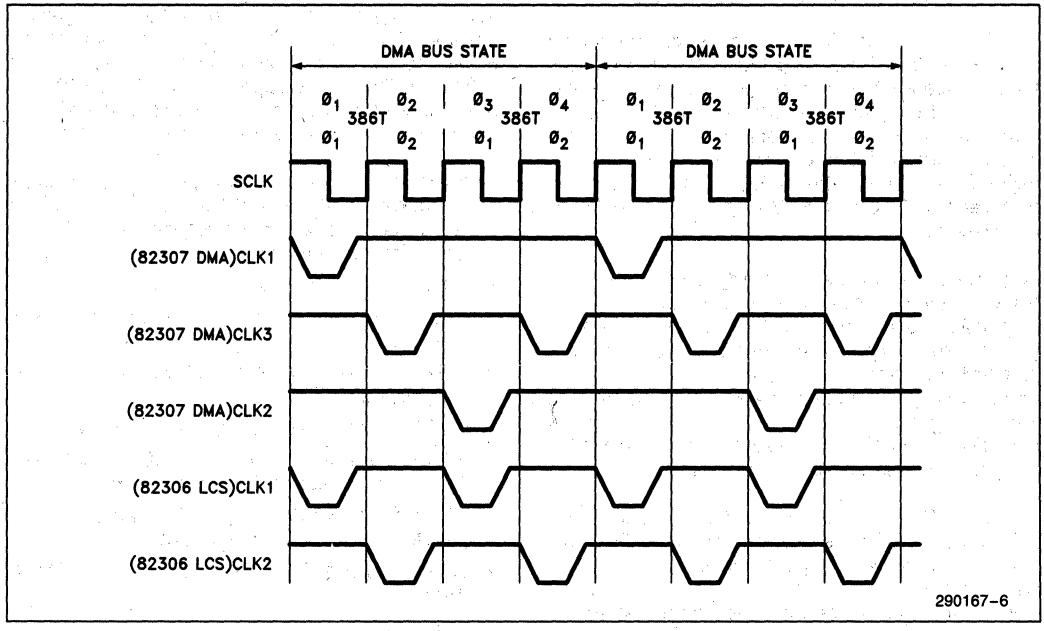
- **Introduction**
- **Clock Definitions**
- **Clock Requirements**

INTRODUCTION

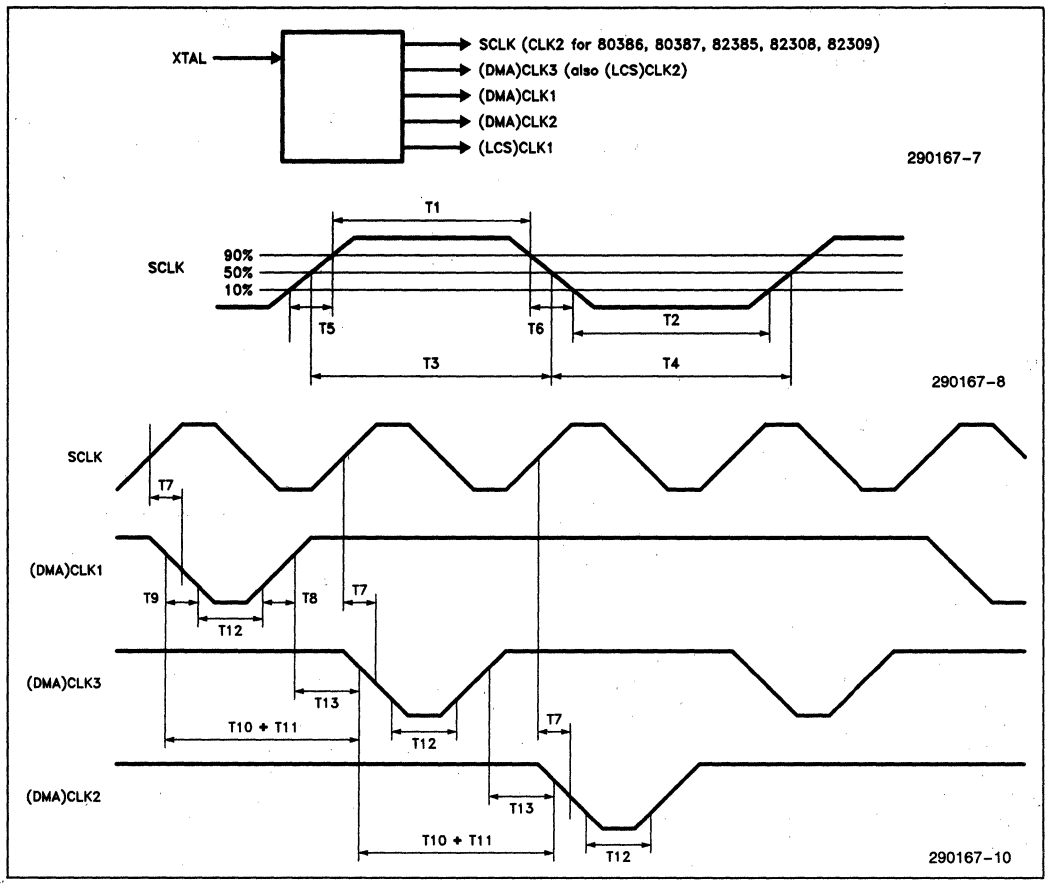
This section describes the basic clocking scheme of the host CPU (80386 or 80386SX), LCS (82306), DMA (82307), BC (82308) and ABC (82309). Although each component spec individually describes its own clock requirements, this section describes the synchronous relationship that exists between them. (Note that several other clocks exist in a Micro Channel system. However, this section describes only those clocks that are synchronously related to the CPU clock.)

The clocking scheme essentially divides the DMA bus state into four phases as depicted in the figure. Note that there is a direct 2-to-1 mapping of 80386 state to DMA state. The DMA (82307) and LCS (82306) comprehend phases by inputting distinct, active low, non-overlapping clock phases. The Address Bus Controller and Bus Controller learn the system phase by synchronously sampling the falling edge of RESET, as described in the component specifications.

BASIC FOUR-PHASE CLOCKING REQUIREMENT



CLOCK CIRCUIT DEFINITION



SYSTEM CLOCK REQUIREMENTS

Symbol	Parameter	Kit 16 MHz		Kit 20 MHz		Kit 25 MHz		Notes
		Min	Max	Min	Max	Min	Max	
T1	SCLK High Time (90%)	8		6.5		5.5		
T2	SCLK Low Time (10%)	8		6.5		5.5		
T3	SCLK High Time (50%)	12		10		9		1
T4	SCLK Low Time (50%)	12		10		9		1
T5	SCLK Rise Time		3.5		3.5		3.5	
T6	SCLK Fall Time		3.5		3.5		3.5	
T7	SCLK-To-DMACLK(N) Skew	−2	3	−2	3	−2	3	2
T8	DMACLK(N) Rise Time		2		2		2	
T9	DMACLK(N) Fall Time		2		2		2	
T10	SCLK Period							
T11	DMACLK-To-DMACLK Skew	−2	2	−2	2	−2	2	2
T12	DMACLK Low Time	15		15		12		
T13	DMACLK Non-Overlap Time	4		4		2		

NOTES:
1. Needed to enforce a duty cycle between 40% and 60%. (45% and 55% at 25 MHz.)
2. Limiting skew to this level is recommended.

82311
HIGH INTEGRATION Micro Channel COMPATIBLE PERIPHERAL CHIP SET

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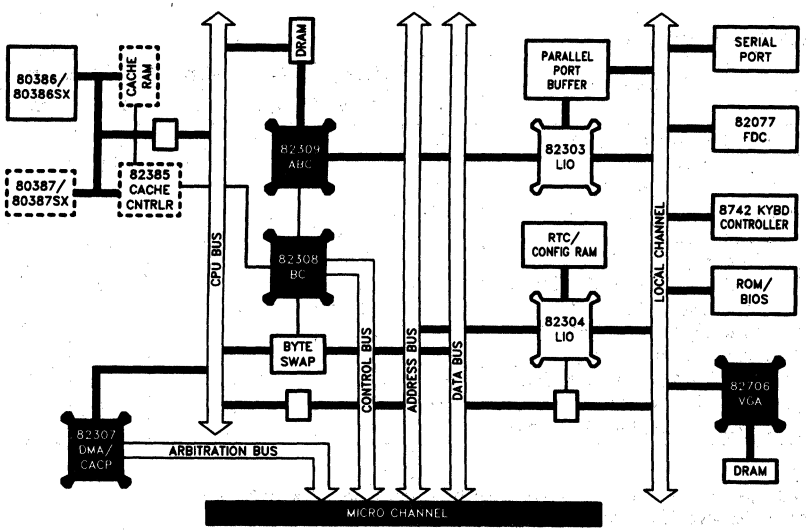

290167-82

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82309	Address Bus Controller
82706	VGA Graphics Controller
82077	Floppy Disk Controller

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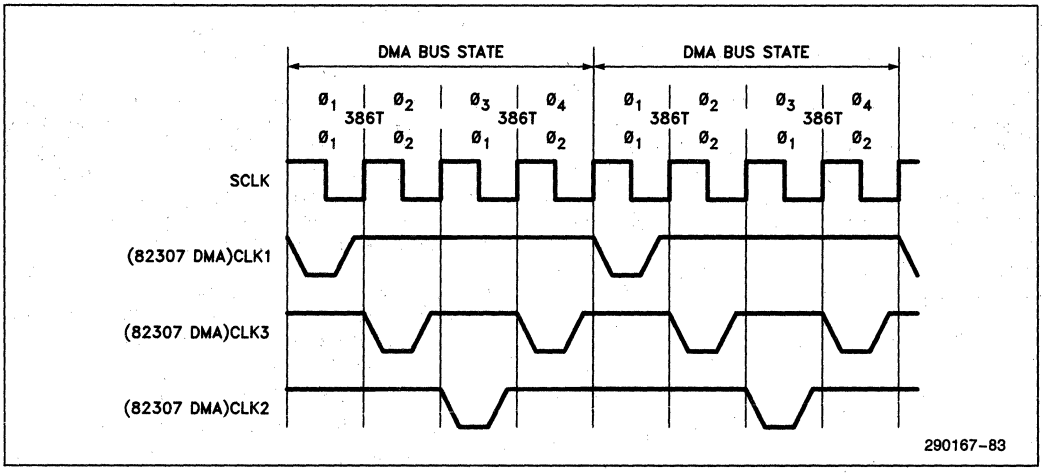
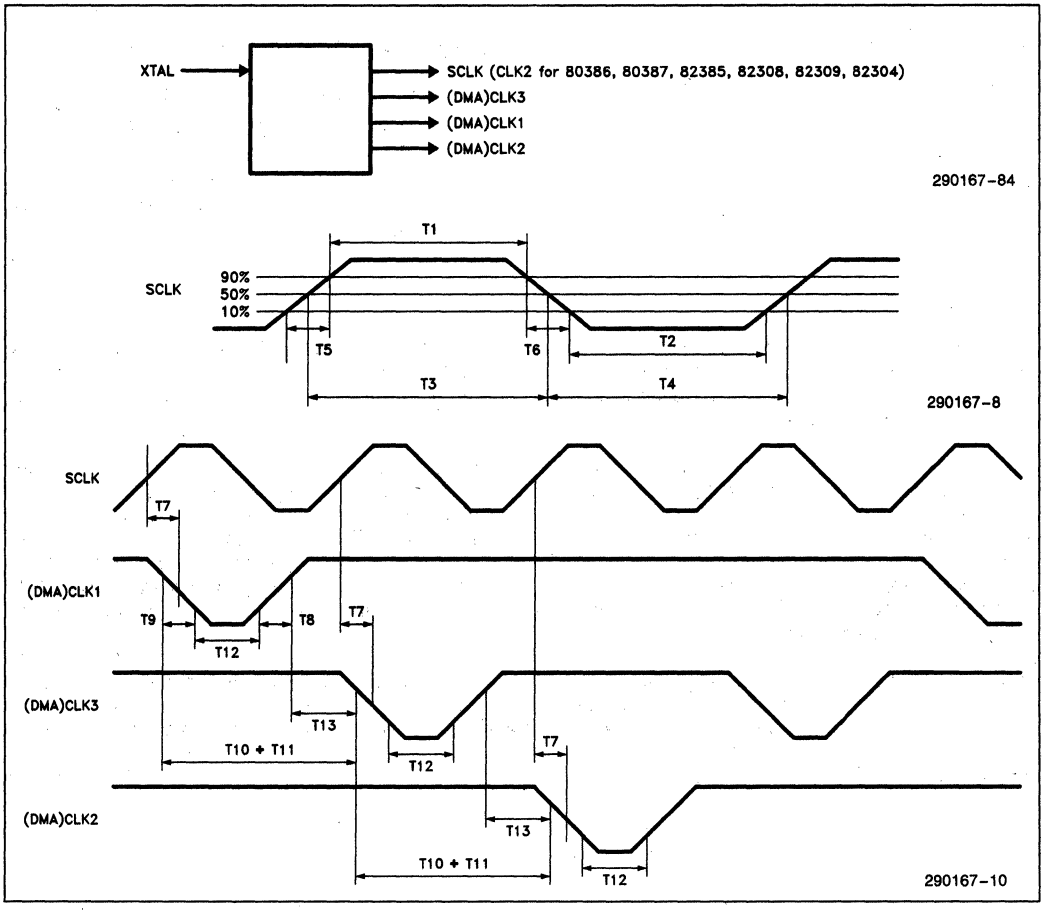


CLOCK CIRCUIT DEFINITION



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T3	SCLK High Time (50%)	12		10		9		1
T4	SCLK Low Time (50%)	12		10		9		1
T5	SCLK Rise Time		3.5		3.5		3.5	
T6	SCLK Fall Time		3.5		3.5		3.5	
T7	SCLK-To-DMACLK(N) Skew	−2	3	−2	3	−2	3	2
T8	DMACLK(N) Rise Time		2		2		2	
T9	DMACLK(N) Fall Time		2		2		2	
T10	SCLK Period							
T11	DMACLK-To-DMACLK Skew	−2	2	−2	2	−2	2	2
T12	DMACLK Low Time	15		15		12		
T13	DMACLK Non-Overlap Time	4		4		2		

NOTES:
1. Needed to enforce a duty cycle between 40% and 60% (45% and 55% at 25 MHz).
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Micro Channel INTERFACE AND SPECIFICATIONS

- **Introduction**
- **Micro Channel Specifications**
- **Micro Channel Interface Logic Requirements**
  - **— 80386 System Data Path**
  - **— 80386 System Address/Command Path**
  - **— 80386SX System Data Path**
  - **— 80386SX System Address Command Path**

INTRODUCTION

This section describes the interface between the host CPU (80386, 80386SX), DMA (82307), Bus Controller (82308) and Micro Channel Bus. This interface provides 100% compliance to published Micro Channel timings, driver type requirements, drive levels, and drive current capability. Timings meet the full capacitive load allowed on the Micro Channel.

The Micro Channel Specifications included in this section assume the specific TTL Data, Address, and Command Path interfaces depicted in the accompanying figures. Timing analysis was based on the Bus Controller AC specifications included in the 82308 Bus Controller section. Worst case TTL analysis was used, except when two related signals share a path through the same physical chip. (For example, since MMCCMD#, S0#, and S1# propagate through the same 74F241 package in an 80386 system, one signal will not experience a worst case delay while the other sees a best case. Rather, it is assumed that the signals will track within 2 ns of each other.) For this reason, it is important to follow the recommendations detailed at the end of this section in the Interface Logic Notes.

The F and AS TTL logic is typically specified into a 50 pF load, worst case delays were derated at 1 ns per 50 pF for loads greater than 50 pF. As an example, the 74F241 published maximum delay is specified as 7 ns. To meet Micro Channel bus loading of 250 pF, a 4 ns derating factor was added, resulting in an effective worst case delay of 11 ns.

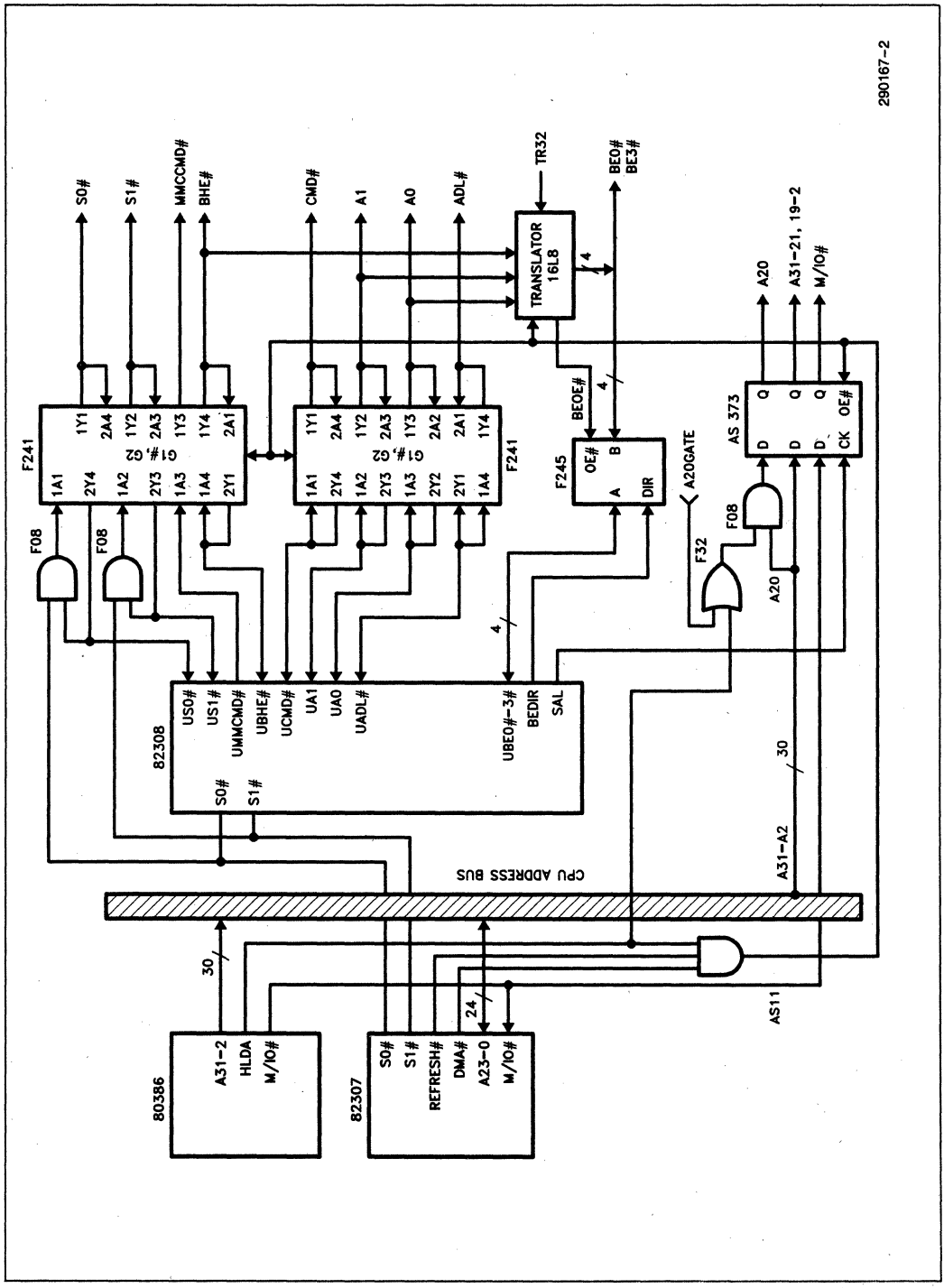
DEFAULT CYCLE SPECIFICATIONS — ALL KITS

Symbol	Parameter	Min	Max
T1	Status active from ADDR,M/IO#,REFRESH#	10	
T2	CMD# active from Status active	55	
T3	ADL# active from ADDR,M/IO#,REFRESH#	45	
T4	ADL# active to CMD# active	40	
T5	ADL# active from Status active	12	
T6	ADL# pulse width	40	
T7	Status hold from ADL# inactive	25	
T8	ADDR,M/IO#,REFRESH#,SBHE# hold frm ADL# INACTIVE	25	
T9	ADDR,M/IO#,REFRESH#,SBHE# hold frm CMD# ACTIVE	30	
T10	Status hold from CMD# active	30	
T11	SBHE# setup to ADL# inactive	40	
T12	SBHE# setup to CMD# active	40	
T13	CDDS16/32 active from ADDR,M/IO#,REFRESH#		55
T14	CDSFDBK# active from ADDR,M/IO#,REFRESH#		60
T15	CMD# active from ADDRESS valid	85	
T16	CMD# pulse width	90	
T17	Write data setup to CMD# active	0	
T18	Write data hold from CMD# inactive	30	
T19	Status to Read Data valid (Access Time)		125
T20	Read Data valid from CMD# active		60
T21	Read Data hold from CMD# inactive	0	
T22	Read Data bus tri-state from CMD# INACTIVE		40
T23	CMD# active to next CMD# active	190	
T23A	CMD# inactive to next CMD# active	80	
T23B	CMD# inactive to next ADL# active	40	
T24	Next Status active from Status Inactive	30	
T25	Next Status active to CMD# Inactive		20
T26	CHRDY INACTIVE FROM ADDR VALID		60
T27	CHRDY INACTIVE FROM STATUS ACTIVE		30
T28	CHRDY RELEASE FROM CMD# ACTIVE		30
T28D	READ DATA VALID FROM CMD# ACTIVE		160
T29S	READ DATA VALID FROM CHRDY RELEASE		60
T31	BE#(0–3) from Addr valid (32-Bit Masters Only)		40
T32	BE#(0–3) active from SBHE#,A0,A1 active		30
T33	BE#(0–3) active to CMD# active	10	

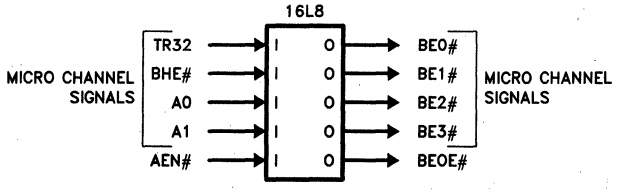
MATCHED MEMORY CYCLE SPECIFICATIONS — ALL KITS

Symbol	Parameter	Min	Max
T1	ADDR VALID TO STATUS ACTIVE	10	
T2	Status valid to MMCCMD# active	82	
T3	ADDR hold from MMCCMD# active	20	
T4	Status hold from MMCCMD# active	25	
T5	CDDS16/32 active from ADDR valid		55
T6	MMCR# active from ADDR valid		55
T7	CDSFDBK# active from ADDR valid		60
T8	ADDR valid to MMCCMD# active	100	
T9	MMCCMD# pulse width	85	
T10	Write Data valid to MMCCMD# active	0	
T11	Write Data hold from MMCCMD# inactive	30	
T12A	Read Data valid from Status active		145
T12B	for non-aligned xfers (16b < = = > 32b)		145
T13A	Read Data valid from MMCCMD# active		60
T13B	for non-aligned xfers (16b < = = > 32b)		60
T14	Read Data hold from MMCCMD# inactive	0	
T15	Read Data off dly from MMCCMD# inactive		40
T16	MMCCMD# active to next MMCCMD# active	180	
T17	CDCHRDY valid from ADDR valid		70
T18	CDCHRDY valid from Status active		30
T23	Status inactive pulse width	30	
T24	MMCCMD# inactive to Status active	5	
T25	MMCCMD# inactive pulse width	85	
T26	MMCCMD# ACTIVE TO NEXT STATUS ACTIVE	90	

80386 SYSTEM ADDRESS/COMMAND PATH



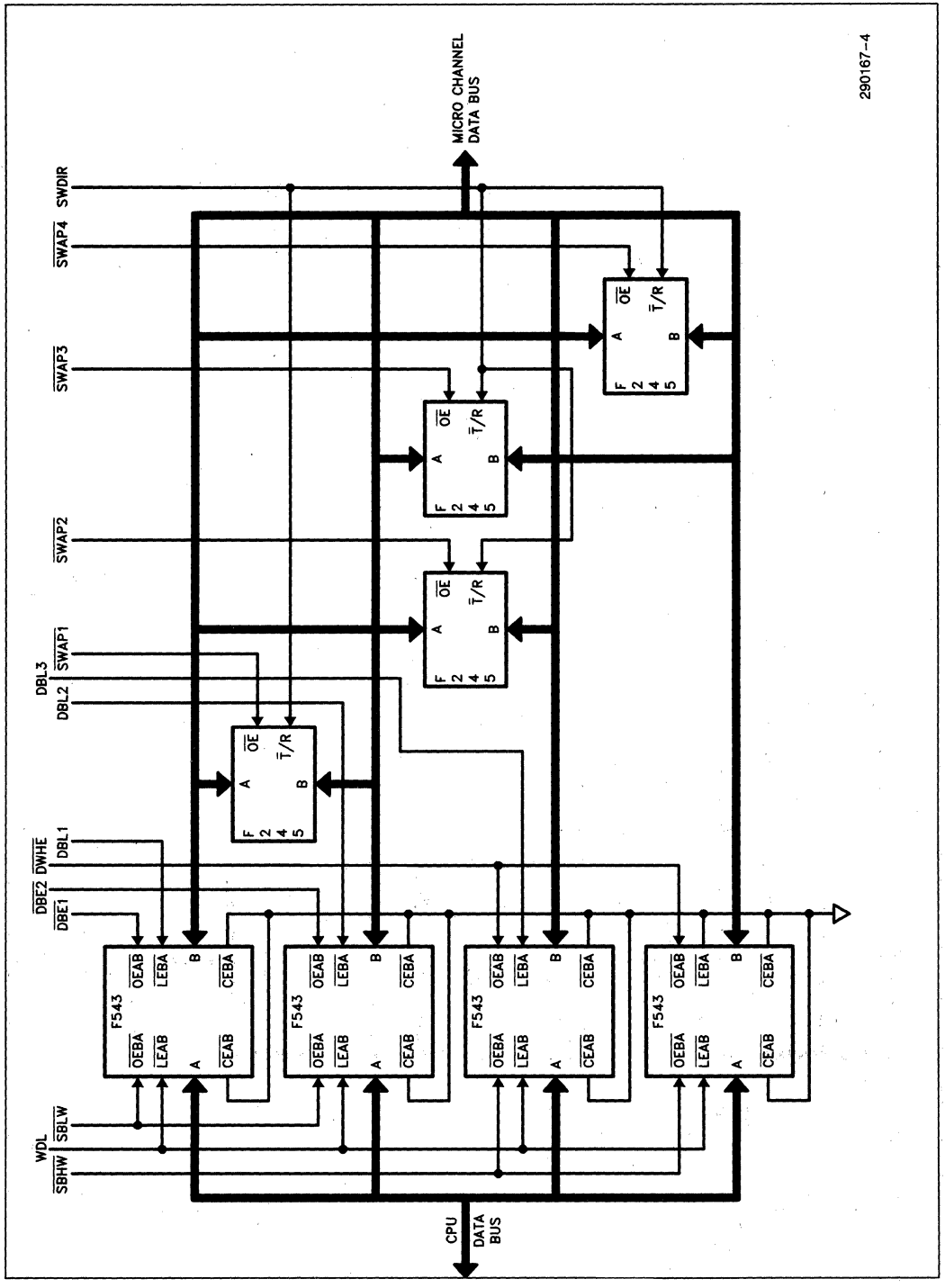
80386 SYSTEM BYTE ENABLE TRANSLATOR PAL



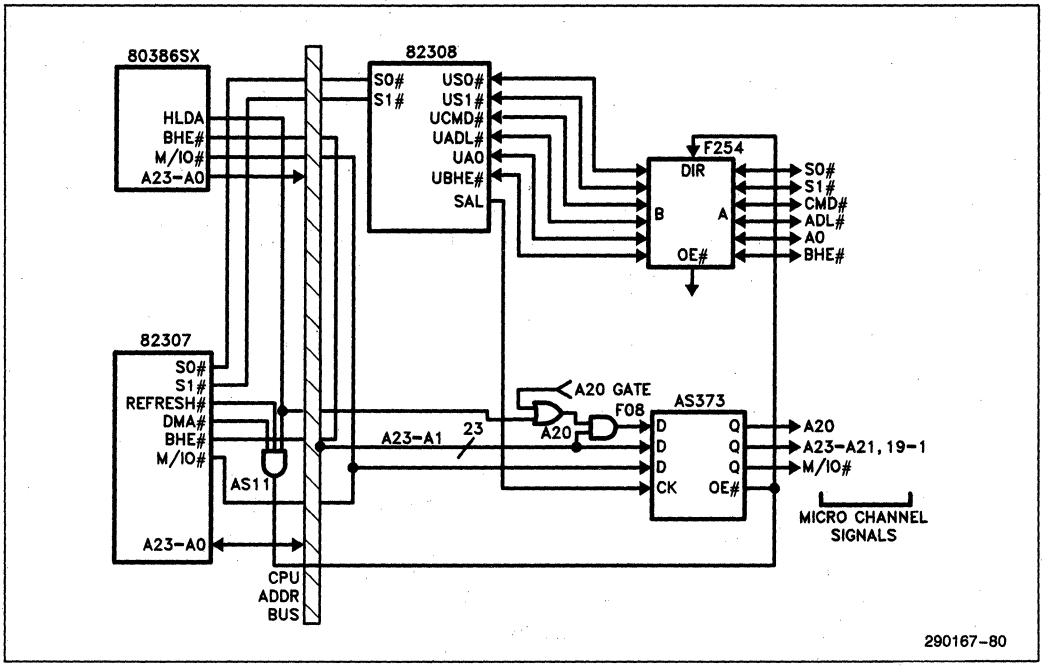
TR32	AEN#	BHE#	A1	A0	BE3#	BE2#	BE1#	BE0#	BEOE#
1	1	0	0	0	1	1	0	0	1
1	1	0	0	1	1	1	0	1	1
1	1	0	1	0	0	0	1	1	1
1	1	0	1	1	0	1	1	1	1
1	1	1	0	0	1	1	1	0	1
1	1	1	0	1	1	1	0	1	1
1	1	1	1	0	1	0	1	1	1
1	1	1	1	1	0	1	1	1	1
0	X	X	X	X	TS	TS	TS	TS	0
X	0	X	X	X	TS	TS	TS	TS	0

TS = TRISTATE

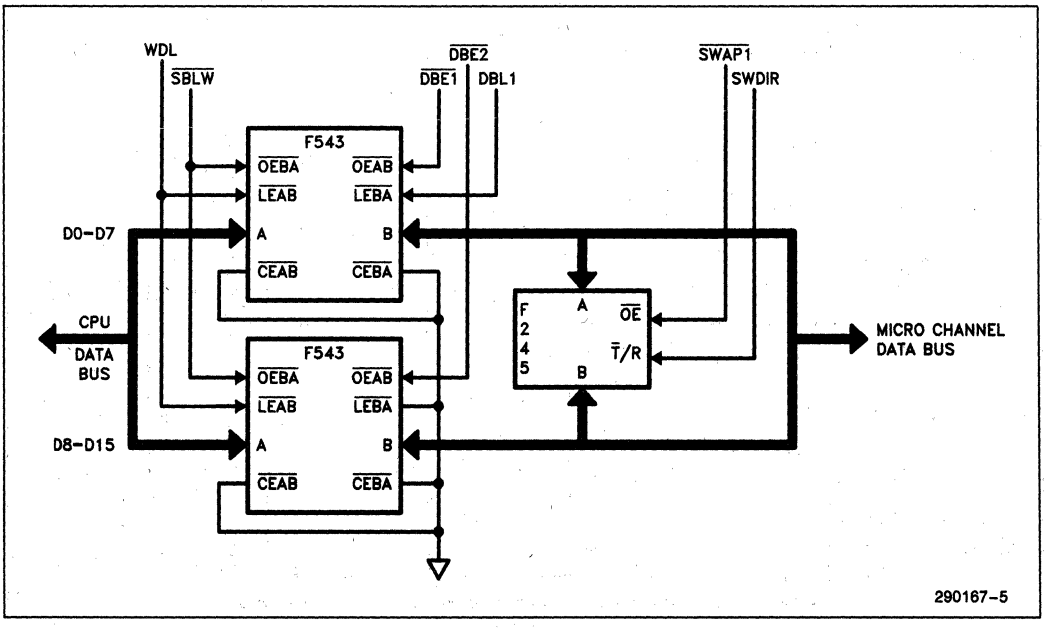
80386 SYSTEM DATA PATH



80386SX SYSTEM ADDRESS/COMMAND PATH



80386SX SYSTEM DATA PATH



Micro Channel Interface Logic Notes

80386 SYSTEM

1. The F08 gates in the S0#, S1# path are required at 20 MHz and at 25 MHz. They should not be used at 16 MHz.
2. In an 82385 system, the A20 gate logic is on the 80386 local bus, and is thus not required on the 82385 local bus as shown in the diagram.
3. The F08 gates in the S0#, S1# path and the F08 in the A20 path should all be from the same TTL package.
4. It is important that S0#, S1#, BHE#, and MMCCMD# go through the same F241 package, and that CMD#, ADL#, A0, and A1 go through the same package.

80386SX SYSTEM

1. The F08 gates in the S0#, S1# path and in the A20 path should all be from the same package.

PLASTIC PACKAGING INFORMATION

(See Packaging Spec. Order # 231369)

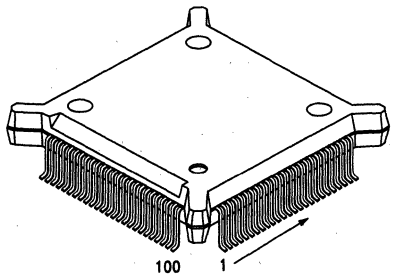
Introduction

The individual components of Intel's Micro Channel Compatible Peripheral Chip Sets come in JEDEC standard Gull Wing packages (25 MIL pitch), with "bumpers" on the corners for ease of handling. Please refer to the accompanying table for the package associated with each device, and to the individual component specifications for pinouts. (Note that the individual pinouts are numbered consistently with the numbering scheme depicted in the accompanying figures.)

MICRO CHANNEL COMPATIBLE PERIPHERAL FAMILY COMPONENT PACKAGES

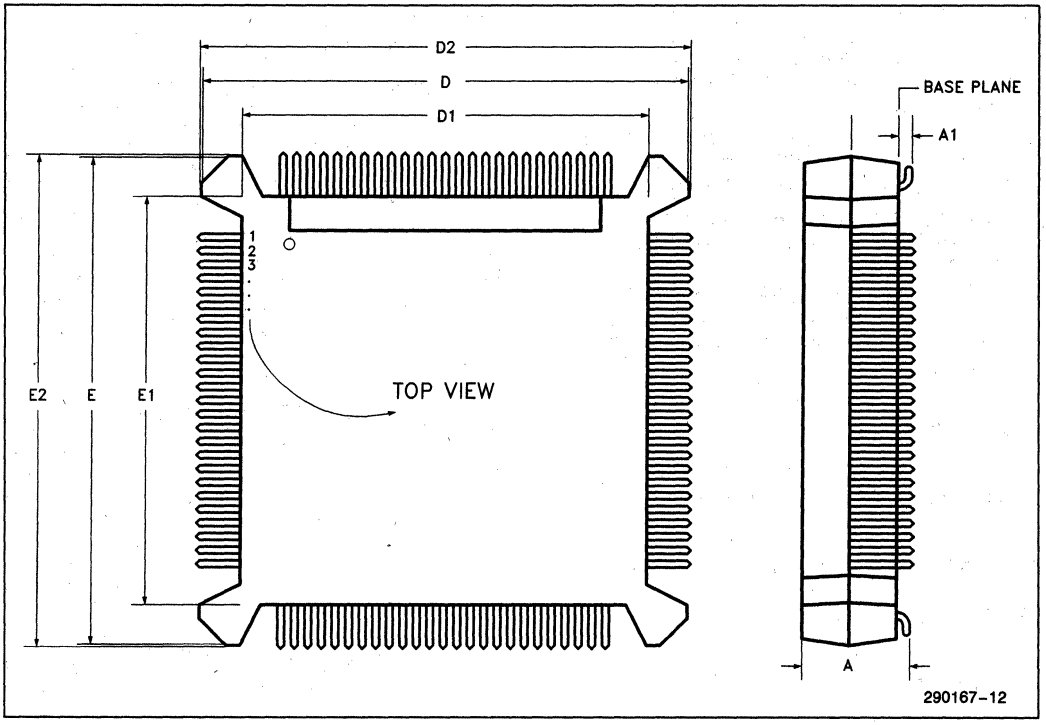
Component	Package
82303	100 Pin PQFP
82304	132 Pin PQFP
82306	100 Pin PQFP
82307	132 Pin PQFP
82308	100 Pin PQFP
82309	100 Pin PQFP
82706	132 Pin PQFP
82077	68-Pin PLCC, See Component Data Sheet

PLASTIC QUAD FLAT PACK (PQFP)

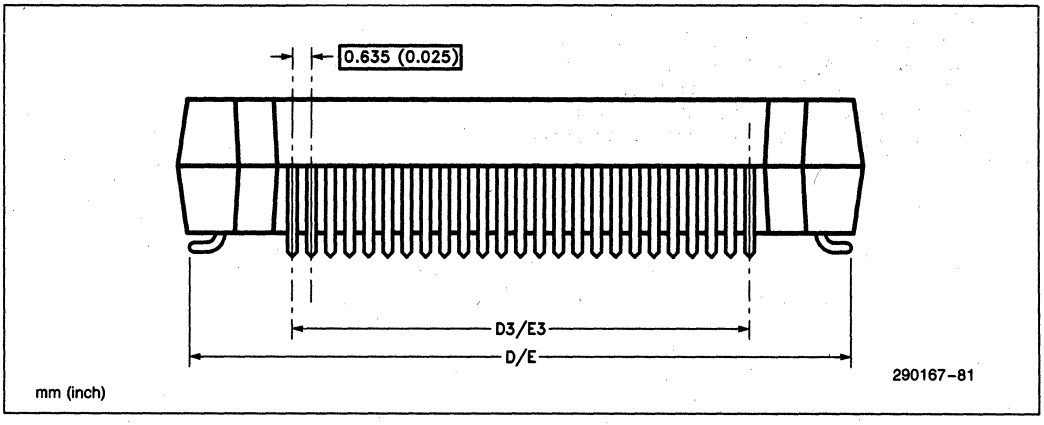


290167-11

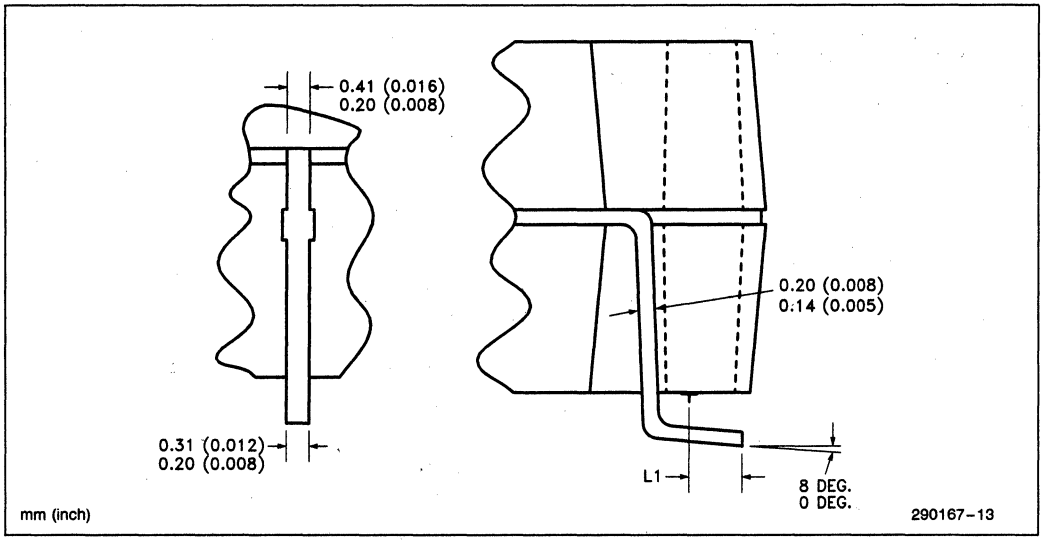
PRINCIPAL DIMENSIONS & DATUMS



TERMINAL DETALS



TYPICAL LEAD



Case Outline Drawings
Plastic Fine Pitch Chip Carrier

		0.025 inch Pitch				0.84 mm Pitch			
Symbol	**Description**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**
N	Lead Count	100		132		100		132	
A	Package Height	0.160	0.170	0.160	0.170	4.06	4.32	4.06	4.32
A1	Standoff	0.020	0.030	0.020	0.030	0.51	0.76	0.51	0.76
D, E	Terminal Dimension	0.875	0.885	1.075	1.085	22.23	22.48	27.31	27.56
D1, E1	Package Body	0.747	0.753	0.947	0.953	18.97	19.13	24.05	24.21
D2, E2	Bumper Distance	0.897	0.903	1.097	1.103	22.78	22.94	27.86	28.02
D3, E3	Lead Dimension	0.600 Ref		0.800 Ref		15.24 Ref		20.32 Ref	
L1	Foot Length	0.020	0.030	0.020	0.030	0.51	0.76	0.51	0.76
		Inch				mm			

REVISION HISTORY

The A.C. Specifications of the 82306, 82307, 82308 and 82309 chips have been modified with respect to the 82310 Data Sheet Order Number 290167-001. These modifications apply to the 16 MHz and 20 MHz kits only.

82306 Spec Revisions

— T1 changed from 14 ns to 15 ns at 16 MHz ... from 12 ns to 15 ns at 20 MHz

— T2 changed from 10 ns to 4 ns at 16 MHz ... from 7 ns to 4 ns at 20 MHz

— T16 changed from 180 ns to 230 ns at 16 MHz and 20 MHz

— T20 changed from 200 ns to 120 ns at 16 MHz and 20 MHz

82307 Spec Revisions

— T1 changed from 14 ns to 15 ns at 16 MHz ... from 12 ns to 15 ns at 20 MHz

— T2 changed from 10 ns to 4 ns at 16 MHz ... from 7 ns to 4 ns at 20 MHz

— T33 cap load C(L) changed from 50 pF to 25 pF

82308 Spec Revisions

— T5A changed from 37 ns to 30 ns at 16 MHz and 20 MHz

— T6A broken into two specs ... T6A for FLUSH, and T6C for SNOOP#

— T44 broken into two specs ... T44A for Setup to SCLK and T44B for Setup to UCMD# ... T44A left at 0 ns, but T44B changed to 3 ns

— T47C changed from 35 ns to 40 ns

82309 Spec Revisions

— T18A changed from 45 ns to 30 ns at 16 MHz

— T18B changed from 50 ns to 38 ns at 16 MHz

— T18C changed from 50 ns to 35 ns at 16 MHz

— T27B changed from 30 ns to 33 ns

— T32B changed from 50 ns to 55 ns

— T32E (Min) changed from 8 ns to 4 ns

— T32E (Max) changed from 30 ns to 27 ns

— T32G (Min) changed from 6 ns to 4 ns

— T32I changed from 50 ns to 40 ns

— T33 (Min) changed from 8 ns to 5 ns

— T34 (Min) changed from 6 ns to 3 ns

— T34 (Max) changed from 26 ns to 27 ns

— T35 changed to 115 ns to 100 ns at 16 MHz and from 90 ns at 20 MHz

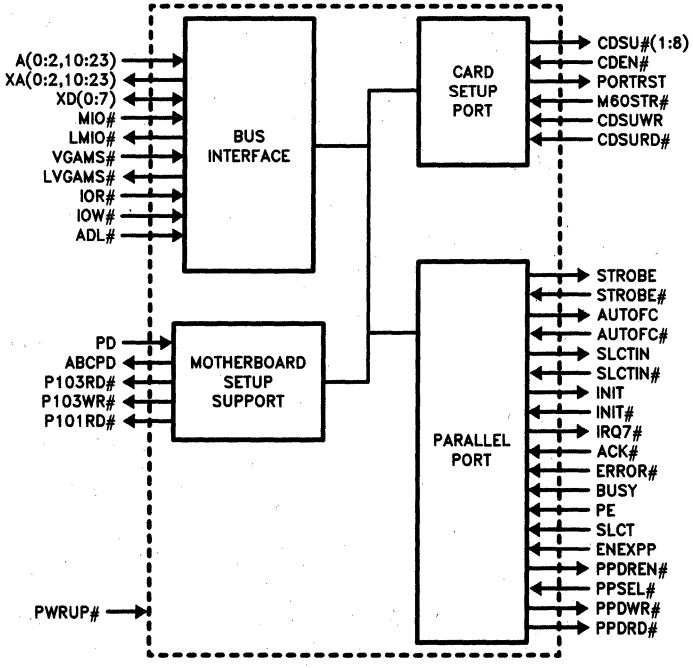
— T45 changed from 26 ns to 32 ns

82303
LOCAL I/O SUPPORT CHIP

- **High Integration—The 82304, 82303 and 82077 Floppy Disk Controller Replace 50 IC's in IBM Design**
- **Integrated Parallel Port**
- **Integrated Card Setup Port (96H)**
- **Supports System Board Setup**
- **Integrated Peripheral Bus Address Latches**
- **Low Power CHMOS Technology**
- **100-Pin Plastic Quad Flat Package**

The 82303 Local Channel Support Chip, along with its companion chip (the 82304) and the 82077 Floppy Disk Controller, significantly reduce system cost, design effort, and form factor constraints by replacing 50 IC devices in an equivalent IBM system.

The 82303 integrates most all logic required to implement a parallel port. This port operates either as a standard parallel port or as a Microchannel architecture compatible "extended mode" (bi-directional) port. The 82303 also integrates the Card Setup Port (96H) and several peripheral bus address latches, and provides signals in support of system setup functions.



290184-1

November 1988
Order Number: 290184-001

Introduction

The 82303 is a high integration device intended for Microchannel compatible system designs. It integrates the Microchannel Card Setup Port, a parallel port, several peripheral bus address latches, and a variety of system board setup functions. The 82303, in conjunction with its sister chip the 82304 and the 82077 Floppy Disk Controller, replaces approximately 50 IC devices in an equivalent IBM system. Included as an appendix to this data sheet is a functional logic diagram of the 82303 that will facilitate understanding of the part. Note that the 82304 and 82303 integrate a variety of system ports. For programming and register level details, please refer to the IBM Technical Reference Manual.

Bus Interface

The Bus Interface unit interfaces the 82303 to the Microchannel and peripheral busses. It inputs the unlatched Microchannel address, latches it for internal use, and makes the latched version available externally for other peripheral bus resources. It also provides additional latches for decodes generated from the Microchannel address.

Parallel Port

The 82303 integrates most all logic required to implement a standard or "extended-mode" parallel port. The only logic not integrated is that which directly drives the physical parallel port connector, specifically one '05 (open collector) inverter package and one '652 data buffer. (This allows the system design to stay clear of directly exposing a VLSI component to an external connector.) The parallel port can serve as LPT1, LPT2, or LPT3, as dictated by the decode received via the input parallel port decode PPSEL#.

Card Setup Port

The 82303 integrates the Card Setup Port (96H), which generates the card setup lines to the individual Microchannel connectors. This port also features a software generated reset capability that resets the Microchannel, serial port, and parallel port independently of the rest of the system.

Motherboard Setup Support

The 82303 generates decoded read/write strobes for system board setup port 103H, and a read strobe for setup port 101H. It also generates a version of the system board POS decode (ABCPD) that is then forwarded to the 82309 Address Bus Controller. Note that other system board setup ports can be easily implemented externally using the same PD (POS Decode) that the 82303 uses.

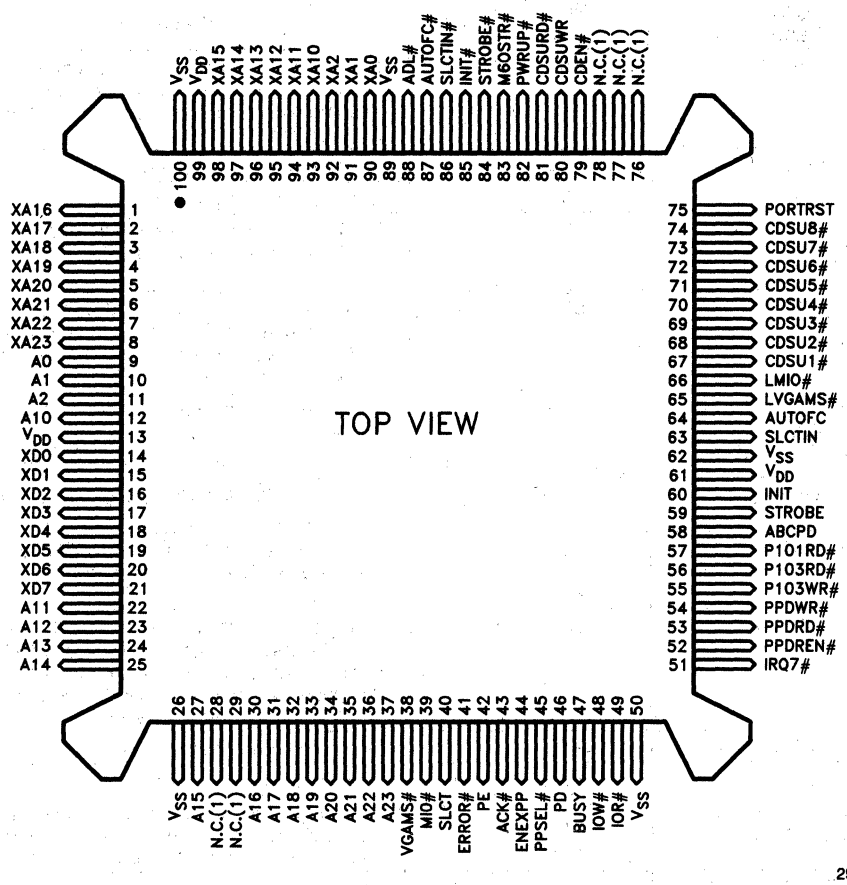
82303 Local Channel Support Chip Pin Definitions

Signal Name	Pin Number	I/O	Description
PWRUP#	82	I	Power-up reset input. Brings 82303 to initial known state.
A[0:2, 10:23]	9–12, 22–25, 27, 30–37	I	Microchannel address inputs. These signals are internally latched. (Note that in systems in which a full 24-bit peripheral address is not required, the upper significant address latches may be used as general purpose decode latches.)
XA[0:2, 10:23]	90–98, 1–8	O	Peripheral Bus Address. These outputs are latched versions of the Microchannel address inputs.
XD[0:7]	14–21	I/O	Bi-directional peripheral data bus.
MIO#	39	I	Microchannel MIO# indicator.
LMIO#	66	O	Latched Microchannel MIO# indicator. The MIO#/LMIO# pin combination may be used as a general purpose latch if LMIO# is not required.
VGAMS#	38	I	VGA memory buffer decode.

82303 Local Channel Support Chip Pin Definitions (Continued)

Signal Name	Pin Number	I/O	Description
LVGAMS#	65	O	Latched VGA memory buffer decode. The VGAMS#/LVGAMS# pin combination may be used as a general purpose latch if LVGAMS# is not required.
IOR#, IOW#	49, 48	I	82303 read/write strobes.
ADL#	88	I	Microchannel ADL# input.
PD	46	I	POS decode. Decode driven in response to accesses to system board setup Ports 100, 101, 103–107H.
ABCPD	58	O	Address Bus Controller (82309) POS decode. This is simply the PD input gated by an active IOW# signal, and insures that the 82309 does not see a decoding glitch.
P101RD#, P103RD#, P103WR#	57, 56, 55	O	Various system board setup port read/write strobes.
CDSU#[1:8]	67–74	O	Card setup signals to the Microchannel slots.
CDEN#	79	I	Port 100-107H decode used as qualifier for card setup signals.
PORTRST	75	O	Microchannel reset signal. The "OR" of the power-up reset and the reset function built into Port 96H.
M60STR#	83	I	Model 60 strap. When low, the 82303 will drive Port 96H data in either a Port 96 or 97H read. (This is in keeping with the Model 50/60 definition.) When high, the 82303 will remain tri-stated during a Port 97H read.
CDSUWR	80	I	Port 96–97H write strobe.
CDSURD#	81	I	Port 96–97H read strobe.
STROBE, AUTOFC, SLCTIN, INIT	59, 64, 63, 60	O	Parallel port control outputs. These signals are externally buffered with open collector inverters before driving the parallel port connector.
STROBE#, AUTOFC#, SLCTIN#, INIT#	84, 87, 86, 85	I	Parallel port control inputs.
IRQ7#	51	O	Parallel port interrupt request.
ACK#, ERROR#, BUSY, PE, SLCT	43, 41, 47, 42, 40	I	Parallel port status inputs.
ENEXPP	44	I	Enable parallel port extended mode. Allows parallel port to operate bi-directionally.
PPSEL#	45	I	Parallel port chip select.
PPDREN#	52	O	Enables the external '652 parallel port data buffer to be used bi-directionally. This signal is a function of the Control port direction bit (bit 5) and the ENEXPP input.
PPDWR#, PPRD#	54, 53	O	Parallel port data buffer write/read strobes.
V_{DD}	13, 61, 99		Power.
V_{SS}	26, 50, 62, 89, 100		Ground.
N.C.	28, 29, 76, 77, 78		No Connect.

82303 100-Pin PQFP Pinout



290184-2

NOTE:
1. N.C. pins must be left not connected.

82303 PARAMETRICS ABSOLUTE MAXIMUM RATINGS*

Case Temperature Under Bias .... −40°C to +85°C
Storage Temperature ..... −65°C to +150°C
Voltage to any Pin
with Respect to Ground −0.3V to +(V_{CC} +0.3)V
DC Supply Voltage (V_{CC}) ..... −0.3V to +7.0V
DC Input Current ..... ±10 mA

**Notice: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

D.C. CHARACTERISTICS T_C = 0°C to +70°C, V_{CC} = 5V ±10%

Symbol	Parameter	Min	Max	Units	Notes
V_{IL}	Input Low Voltage		0.8	V	
V_{IH}	Input High Voltage	2.0		V	
V_{OL}	Output Low Voltage		0.4	V	I_{OL} = 4 mA (Note 1)
V_{OH}	Output High Voltage	2.4		V	I_{OH} = 4 mA (Note 1)
V_{OL}	Output Low Voltage		0.4	V	I_{OL} = 2 mA (Note 2)
V_{OH}	Output High Voltage	2.4		V	I_{OH} = 2 mA (Note 2)
I_{CC}	Power Supply Current		180	mA	No DC Loads
I_{LI}	Input Leakage Current		±10	μA	$V_{SS} < V_{IN} < V_{CC}$
I_{OZ}	TRI-STATE Output Leakage Current		±10	μA	$V_{SS} < V_{OUT} < V_{CC}$

NOTES:
1. CDSU# [1:8], XA [0:2, 10:23], XD[0:7].
2. All outputs other than those listed in Note 1.

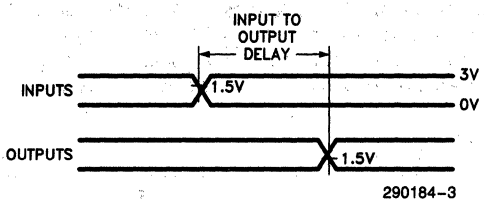
82303 A.C. SPECIFICATIONS T_C = 0°C to +70°C, V_{CC} = 5V ±10%

Symbol	Parameter	Min	Max	C_L (pF)	Notes
T_1	PWRUP#, Pulse Width	500			
T_2	IOR#, IOW#, CDSURD#, CDSUWR Pulse Width	170			
T_3	Write Data Setup	25			(Note 1)
T_4	Write Data Hold	10			(Note 2)
T_5	Read Data Valid Delay		60	100	(Note 3)
T_6	Read Data Float Delay		40	100	(Note 5)
T_7	Status Inputs to XD[0:7]		35	100	(Note 6)
T_8	Write Strobe Delays		35	50	(Note 7)
T_9	Read Strobe Delays		40	50	(Note 8)
T_{11}	PPSEL#, PD Setup to IOR#, IOW# ↓	20			
T_{12}	PPSEL#, PD Hold from IOR#, IOW# ↑	5			
T_{13}	XA[0:2, 10:23] DLY from ADL# ↓		35	100	
T_{14}	A[0:2, 10:23], VGAMS#, MIO# Setup to ADL# ↑	30			
T_{17}	CDSU# [1:8] Delay from CDEN#		28	75	
T_{18}	IOR# ↑ to ADL# ↓	30			
T_{19}	LVGAMS#, LMIO# Delay from ADL# ↓		35	50	

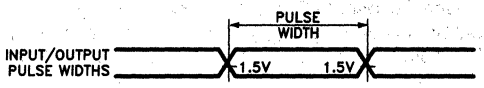
NOTES:
1. To IOW# or CDSUWR active, whichever is appropriate.
2. From IOW# or CDSUWR inactive, whichever is appropriate.
3. From IOR# or CDSURD# active, whichever is appropriate.
5. From IOR# or CDSURD# inactive, whichever is appropriate.
6. Parallel port status inputs include SLCT, PE, BUSY, ERROR#, and ACK#.
7. Write strobes include P103WR# and PPDWR#.
8. Read strobes include P103RD#, P101RD#, and PPDRD#.

82303 Drive Levels/Measurement Points for A.C. Specifications

Input/Output Pulse Widths

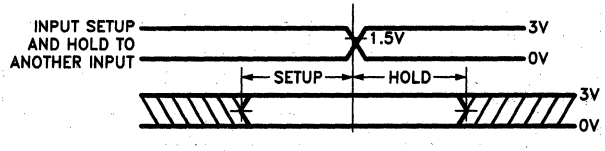


290184-3



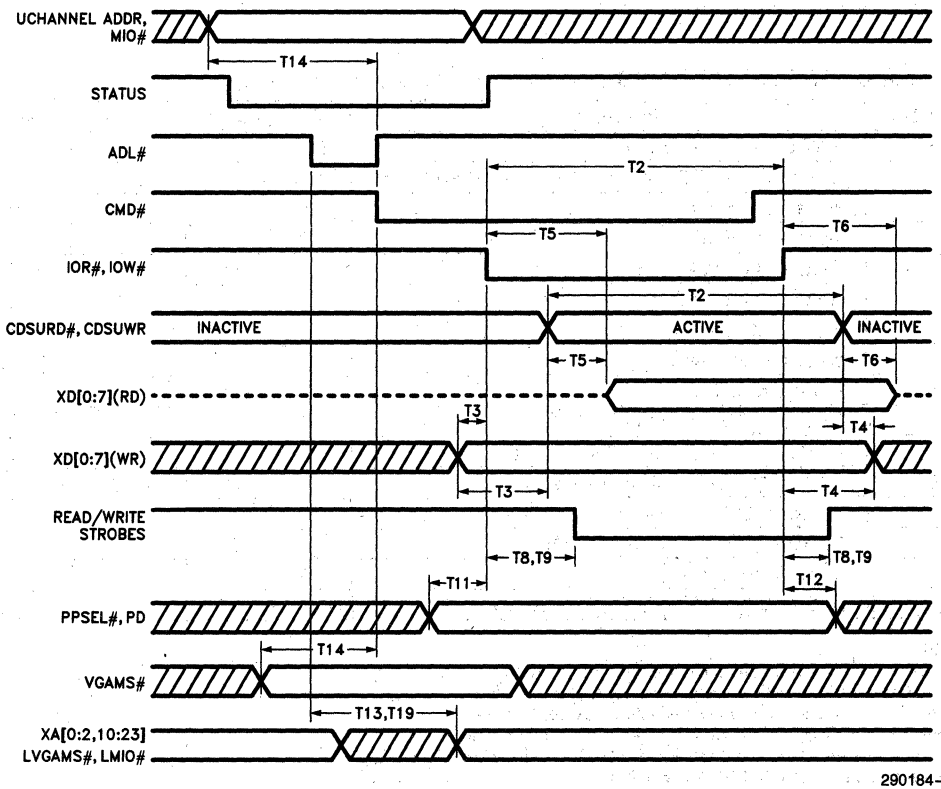
290184-4

Input Setup and Hold to another Input

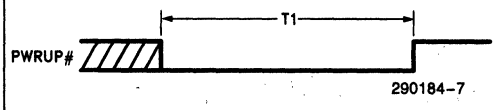


290184-5

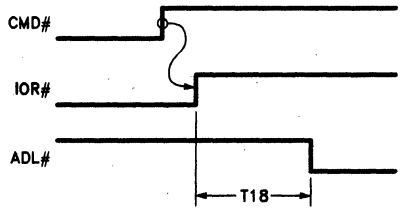
NOTE:
Input Waveforms have $T_R \leq 2.0$ ns from 0.8V to 2.0V.



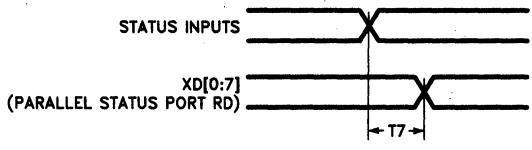
290184-6



290184-7

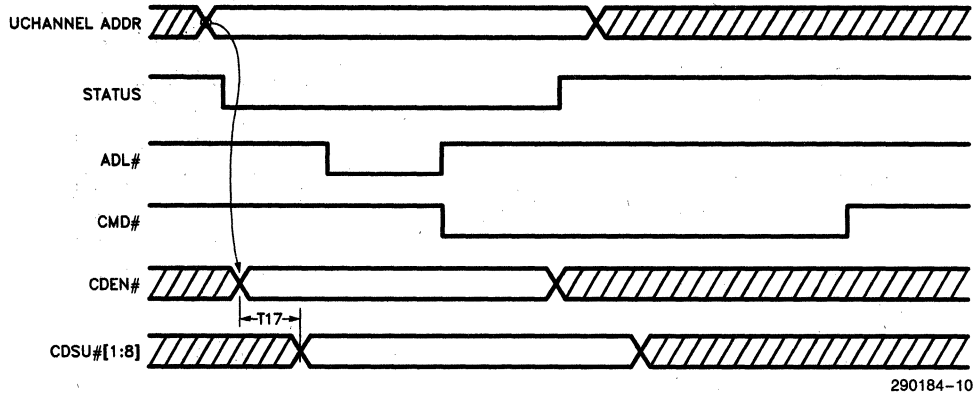


290184-8



290184-9

NOTE:
T7 is the flow through propagation delay, and thus assumes T5A, is not the limiting parameter.



290184-10

APPENDIX
82303 INTERNAL LOGIC DIAGRAMS

These logic diagrams are provided to aid in understanding the basic functionality of the 82303, and should not be used to estimate signal loading, propagation delays, or any other timing behavior.

The clocked latches in the diagrams are functionally equivalent to 7474 type TTL latches. The transparent latches are equivalent to 74373 type TTL latches except that the gate input is active low rather than active high.

The truth table for the combinatorial PAL is as follows:

RD

PPSEL#	IOR#	XA0	XA1	PPDR#	PPCR#	PSRD#
0	0	0	0	0	1	1
0	0	0	1	1	0	1
0	0	1	0	1	1	0

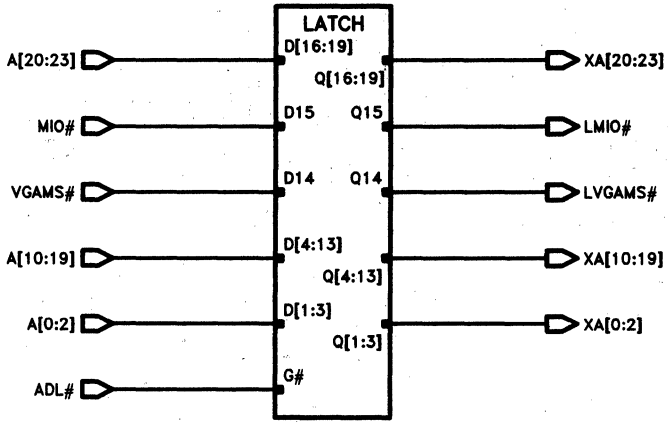
SELPOS	IOR#	XA2	XA1	XA0	PPOS1D#	PPOS13R#
1	0	0	0	1	0	1
1	0	0	1	1	1	0

WR

PPSEL#	IOW#	XA0	XA1	PPDW#	PCWR#
0	0	0	0	0	1
0	0	0	1	1	0

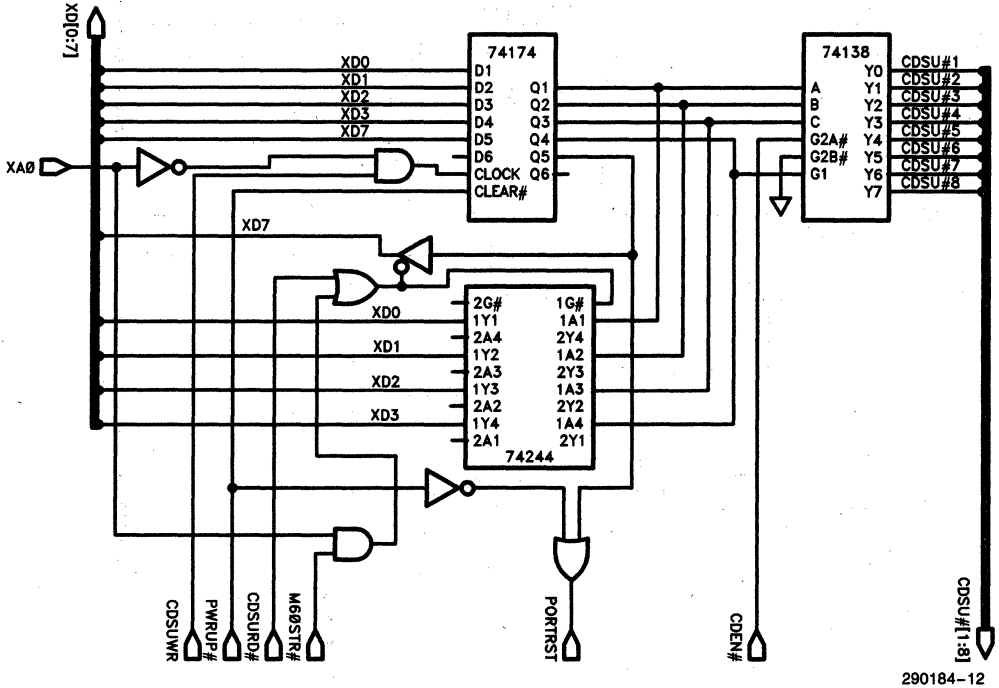
SELPOS	IOW#	XA2	XA1	XA0	POS103WR#
1	0	0	1	1	0

Address Latch
Transparent Latch × 19

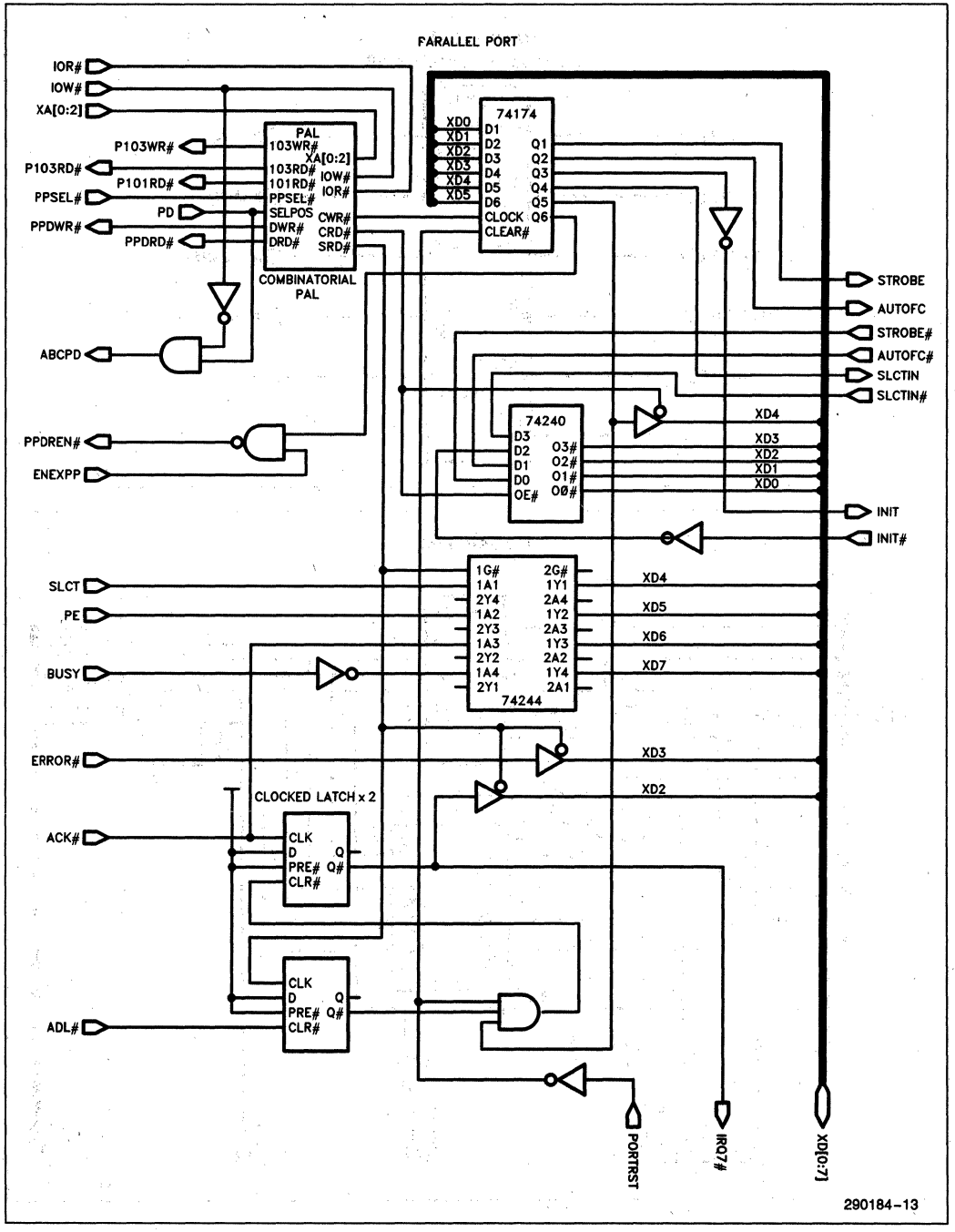


290184-11

Card Setup Port



290184-12

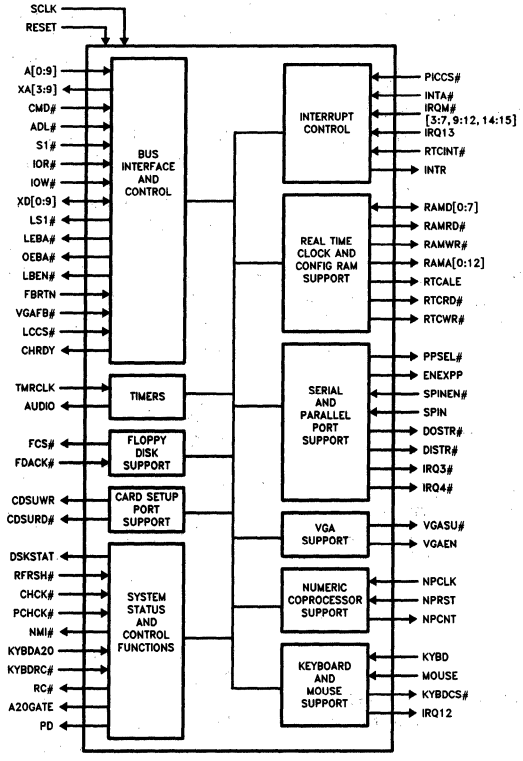

PARALLEL PORT
IOR#
IOW#
XA[0:2]
P103WR#
P103RD#
P101RD#
PPSEL#
PD
PPDWR#
PPDRD#
PAL
103WR#
XA[0:2]
103RD#
IOW#
101RD#
IOR#
PPSEL#
SELPOS
CWR#
DWR#
CRD#
DRD#
SRD#
COMBINATORIAL PAL
ABCPD
PPDREN#
ENEXPP
74174
XD0
XD1
XD2
XD3
XD4
XD5
D1
D2
D3
D4
D5
D6
CLOCK
CLEAR#
Q1
Q2
Q3
Q4
Q5
Q6
74240
D3
D2
D1
D0
OE#
O3#
O2#
O1#
O0#
1G#
1A1
2Y4
1A2
2Y3
1A3
2Y2
1A4
2Y1
2G#
1Y1
2A4
1Y2
2A3
1Y3
2A2
1Y4
2A1
74244
SLCT
PE
BUSY
ERROR#
ACK#
ADL#
CLOCKED LATCH x 2
CLK
D
PRE#
CLR#
Q
Q#
STROBE
AUTOFC
STROBE#
AUTOFC#
SLCTIN
SLCTIN#
INIT
INIT#
PORTRST
IRQ7#
XD[0:7]
290184-13

82304
LOCAL I/O SUPPORT CHIP

- **High-Integration—The 82304, 82303 and 82077 Floppy Disk Controller Replace 50 IC's in IBM Design**
- **Supports I/O Peripherals . . . Keyboard/ Mouse Controller, Serial/Parallel Ports, Configuration RAM, and Real Time Clock**
- **Integrates Two 8259 PIC's and All Associated Logic**
- **Integrates Programmable Timer Counters 0, 2 and 3**
- **Supports VGA Controller on the Local Channel**
- **Integrates the OS/2 Optimized HOT A20 and HOT RESET Functions**
- **Integrates Variety of System Status/ Control Ports and Functions**
- **Low Power CHMOS Technology/132-Pin PQFP Package**

The 82304 Local Channel Support Chip, along with its companion chip (the 82303) and the 82077 Floppy Disk Controller, significantly reduce system cost, design effort, and form factor constraints by replacing 50 IC devices in an equivalent IBM system.

The 82304 integrates logic to support local bus I/O peripherals and the VGA Controller. Also integrated are three programmable timer/counters, two "8259-like" programmable interrupt controllers, and a variety of system status/control ports and functions. Integrated along with the 8259 PIC's is all logic required to make the PIC's Microchannel architecture compatible.



290185-1

November 1988
Order Number: 290185-001

INTRODUCTION

The 82304 is a high integration device intended for Microchannel compatible system designs. It essentially integrates the 82306 Local Channel Support chip, two 8259 Programmable Interrupt Controllers, and a wide assortment of TTL circuitry. The 82304, in conjunction with its sister chip the 82303 and the 82077 Floppy Disk Controller, replaces approximately 50 IC devices in an equivalent IBM system. Included as an appendix to this data sheet is a functional logic diagram of the 82304 that should facilitate understanding of the part. Note that the 82304, 82303 and 82077 integrate a variety of system ports. For programming and register level details, please refer to the IBM Technical Reference Manual, 82077 data sheet, and 8259A data sheet.

BUS INTERFACE AND CONTROL

The Bus Interface and Control unit interfaces the 82304 to the Microchannel and peripheral busses. It inputs the unlatched Microchannel address, latches it for internal use, and makes the latched version available externally for other peripheral bus resources. It also provides signals to control an external 74F543 latching data transceiver that sits between the Microchannel and peripheral data busses. The bus interface unit also provides functions such as cycle extension on behalf of slower peripherals, and support of the Microchannel architecture's system feedback function.

SYSTEM TIMERS

The 82304 integrates the timers required for multitask time slice interrupt (timer 0), audio tone generation (timer 2), and "watch-dog" function (timer 3). These timers are accessed via ports 40, 42, 43, 44, and 47H.

FLOPPY DISK SUPPORT

The 82304 provides the decode signal required by the 82077 Floppy Disk Controller. The decode addresses ports 3F0–3F7H. The 82304 also inputs the 82077's DMA acknowledge in support of the system feedback function.

VGA SUPPORT

The 82304 supports the VGA setup and enable/disable functions. Specifically, bit 5 of integrated port 94H is used to put the VGA into setup mode, and this mode is reflected to the VGA on the 82304's VGASU# pin. Also, the 82304 integrates bit 0 of port 3C3H, which is used to enable/disable the system board VGA subsystem as indicated by the 82304's VGAEN output.

CARD SETUP PORT SUPPORT

The 82304 provides decoded read/write strobes for ports 96–97H. Port 96H is the card setup port, which is integrated on the 82303 chip. Port 97H is currently reserved by IBM.

INTERRUPT CONTROL

The 82304 integrates two 8259 Programmable Interrupt Controllers, and all additional logic required to make these interrupt controllers Microchannel architecture compatible. Specifically, the Microchannel definition requires that interrupts be active low and level sensitive. This allows a wire-OR system implementation. Integrated logic includes inverters for incoming interrupts, as the 8259 treats level sensitive interrupts as active high. Additionally, logic to inhibit the 8259's from being programmed in edge-triggered mode is integrated.

REAL TIME CLOCK AND CONFIGURATION RAM SUPPORT

The 82304 integrates all logic required to support an external battery backed up real time clock chip and static RAM. Note that while the IBM implementation supports a 2K RAM, the 82304 makes provision to support either a 2K or 8K RAM. The real time clock is accessed via ports 70–71H, while the RAM is accessed via ports 74–76H. (RAM data is accessed via port 76H, while ports 74H and 75H serve as an indirect address latch for the RAM.) The 82304 also integrates the logic required to enforce the Microchannel architecture's password security function. Specifically, writes to port 70H are monitored. If a write to 70H is attempting to access offsets 38–3FH in the real time clock chip's onboard RAM, and if the security bit in 92H indicates that these offsets are off limits, then no address latch signal is generated to the real time clock chip.

SERIAL AND PARALLEL PORT SUPPORT

The 82304 provides various functions in support of an external serial port chip (the 16550A), and a par-

allel port (integrated on the 82303 chip). The 82304 provides decoded read/writes strobes for the serial port chip, as well as converting a serial port interrupt into either IRQ3# or IRQ4#, depending on whether the serial port is configured as COMM1 or COMM2. When configured as COMM1, the serial port is decoded at ports 3F8–3FFH. As COMM2, the port is decoded from 2F8–2FFH. Configuration is done via the integrated system setup port 102H.

The 82304 generates a parallel port chip select that maps to LPT1, LPT2, or LPT3, depending on how system setup port 102H is programmed. As LPT1, the parallel port is decoded at ports 3BC, 3BD, 3BE, and 3BFH. LPT2 maps to ports 378, 379, 37A, and 37BH. LPT3 maps to 278, 279, 27A, and 27BH. The 82304 also generates a signal that indicates whether the parallel port is to operate in its normal output-only mode, or its "extended" bi-directional mode. The mode is selected via system setup port 102H.

NUMERIC COPROCESSOR SUPPORT

The 82307 DMA Controller, in response to a software command, issues a pulse to reset the 80387 or 80387SX Numeric Coprocessor. The 82304 inputs this pulse and effectively stretches it out to insure that the 80387 reset input pulse is long enough to meet its internal reset requirements. (Note that the 80387 reset pulse out of the 82304 must be externally synchronized to the 80387 clock so as to convey the system phase to the 80387.) The 82304 also manipulates CHRDY to extend the bus cycle that initiates the reset so as to tie up the CPU until the 80387's reset and initialization requirements are met.

KEYBOARD AND MOUSE SUPPORT

The 82304 provides a chip select for the 8742 Keyboard Controller. This decode maps to ports 60 and 64H. The 82304 also integrates the logic required to both latch and subsequently clear keyboard and mouse interrupts.

SYSTEM STATUS AND CONTROL FUNCTIONS

The 82304 integrates a variety of system status and control functions and ports. Integrated ports include:

Port 61H System Control Port B
Port 92H System Control Port A
Port 91H Card Selected Feedback Register
Port 94H System Board Setup Port
Port 102H System Board POS Port
Port 70H NMI Enable (Write Only)

The functions and register level details of these ports are documented in the IBM Technical Reference.

82304 LOCAL CHANNEL SUPPORT CHIP PIN DEFINITIONS

Symbol	Pin No.	Type	Description
SCLK	50	I	**INPUT CLOCK:** Tied to same clock as host CPU.
RESET	64	I	**SYNCHRONIZED POWER-UP RESET:** Resets 82304 and synchronizes internal clock to system phase.
A[0:9]	85–81, 78–74	I	**MICROCHANNEL ADDRESS:** Address Lines are internally latched.
XA[3:9]	73–67	O	**PERIPHERAL BUS ADDRESS:** These are latched versions of the Microchannel address.
CMD#	97	I	**MICROCHANNEL CMD# INPUT**
ADL#	100	I	**MICROCHANNEL ADL# INPUT**
S1#	1	I	**MICROCHANNEL S1# INPUT**
IOR#, IOW#	96, 95	I	**82304 READ AND WRITE STROBES**
XD[0:7]	94–90, 88–86	I/O	**BI-DIRECTIONAL DATA BUS**
LS1#	131	O	**LATCHED VERSION OF MICROCHANNEL S1# INPUT**
LEBA#, OEBA#	130, 129	O	**EXTERNAL 74543 DATA BUFFER CONTROL SIGNALS:** These signals control data timing on the peripheral data bus.
LBEN#	52	O	**LOCAL (PERIPHERAL) BUS ENABLE:** The 82304 generates this in response to address decodes of peripheral bus ports. It is typically "OR"ed with other system qualifiers to enable the peripheral bus data buffer.

82304 LOCAL CHANNEL SUPPORT CHIP PIN DEFINITIONS (Continued)

Signal Name	Pin No.	I/O	Description
FBRTN	41	I	**SYSTEM FEEDBACK:** This input receives the OR of the system feedback signals of the Microchannel slots. It is internally latched and "OR"ed with other feedback sources, and the result made available via a Port 91H read (Bit 0).
VGAFB#	42	I	**VGA FEEDBACK.**
LCCS#	37	I	**LOCAL CHANNEL CHIP SELECT:** Activated for the I/O address range 0–3FFH (CPU or DMA master) or 100–3FFH (Microchannel Master). LCCS# is internally latched.
CHRDY	5	O	**CHANNEL READY:** The 82304 deasserts CHRDY to extend accesses to certain peripheral bus resources, specifically the keyboard controller, real time clock and serial port. Also, CHRDY is used to tie up the CPU during numeric coprocessor resets.
TMRCLK	45	I	**1.193 MHz CLOCK INPUT:** Drives clock inputs of system timers 0 and 2.
AUDIO	128	O	**OUTPUT OF SYSTEM TIMER 2 GATED BY BIT 1 OF PORT 61H:** It drives the Microchannel audio sum node.
FCS#	46	O	**FLOPPY DISK CONTROLLER (82077) CHIP SELECT:** Responds to I/O range 3F0–3F7H.
FDACK#	49	I	**FLOPPY DISK CONTROL DMA ACKNOWLEDGE:** Internally latched and "OR"ed with other system feedback sources.
VGASU#	44	O	**VGA SETUP:** Puts the VGA into setup mode when active, according to Bit 5 of Port 94H.
VGAEN	43	O	**VGA ENABLE:** Enables/Disables motherboard VGA according to Bit 0 of Port 3C3H.
CDSUWR	126	O	**CARD SETUP WRITE STROBE:** Active High command generated during writes to Port 96–97H.
CDSURD#	125	O	**CARD SETUP READ STROBE:** Active low command generated during reads from Port 96–97H.
DSKSTAT	127	O	**FIXED DISK STATUS:** Controls the fixed disk activity light. It is active when either Bit 6 or Bit 7 of Port 92H is set.
RFRSH#	51	I	**REFRESH CYCLE INDICATOR:** Diagnostics can monitor refresh activity via Bit 4 of Port 61H.
CHCK#	54	I	**MICROCHANNEL CHECK INDICATOR:** Used to report adapter errors.
PCHCK#	55	I	**DRAM PARITY ERROR:** Driven in response to motherboard memory parity errors.
NMI#	53	O	**NON-MASKABLE INTERRUPT REQUEST TO CPU:** This acts as an open drain output that allows for an external wire "OR" with other NMI sources.
KYBDA20	60	I	**A20 GATE SIGNAL OUT OF THE KEYBOARD CONTROLLER:** Internally "OR"ed with the alternate A20 switch incorporated in Bit 1 of Port 92H.
KYBDRC#	58	I	**CPU RESET SIGNAL OUT OF THE KEYBOARD CONTROLLER:** It is internally "OR"ed with the alternate reset function of Bit 0 of Port 92H.
RC#	59	O	**RESET CPU:** Resets CPU via Port 92H (Bit 0) or the KYBDRC# input.
A20GATE	57	O	**A20 GATE SIGNAL:** The "OR" of Bit 1 of Port 92H and the KYBDA20 input.

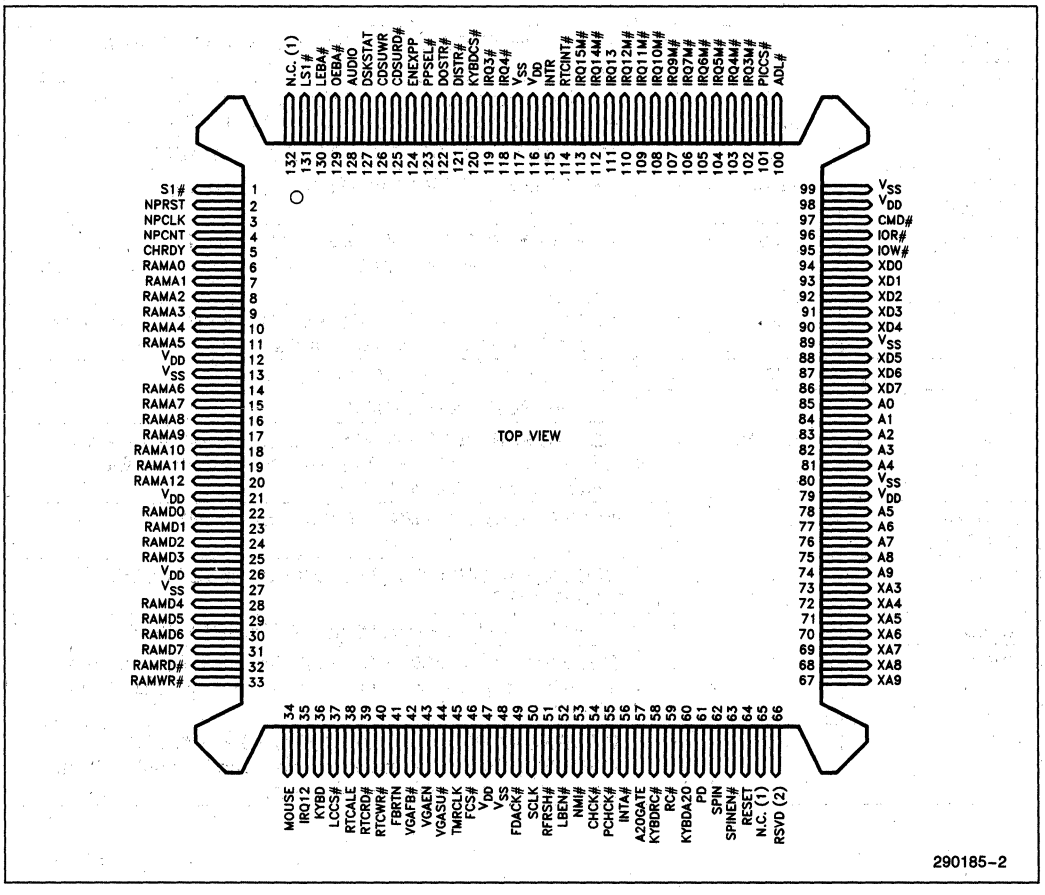
82304 LOCAL CHANNEL SUPPORT CHIP PIN DEFINITIONS (Continued)

Signal Name	Pin No.	I/O	Description
PD	61	O	**POS DECODE:** An active high decode of system board setup ports 100, 101, 103–107H. (Port 102H is integrated on the 82304.)
PICCS#	101	I	**CHIP SELECT FOR THE INTEGRATED 8259 PROGRAMMABLE INTERRUPT CONTROLLERS (PIC)**
INTA#	56	I	**INTERRUPT ACKNOWLEDGE:** Generated by the bus controller during interrupt acknowledge cycles.
IRQM# [3:7, 9:12, 14:15]	102–110, 112–113	I	**MICROCHANNEL INTERRUPT INPUTS.**
IRQ13	111	I	**INTERRUPT INPUT USED TO REPORT NUMERIC COPROCESSOR ERRORS.**
RTCINT#	114	I	**INTERRUPT INPUT FROM REAL TIME CLOCK.**
INTR	115	O	**MASKABLE INTERRUPT REQUEST TO CPU.**
RAMD[0:7]	22–25, 28–31	I/O	**REAL TIME CLOCK AND CONFIGURATION RAM DATA BUS.**
RAMRD#, RAMWR#	32, 33	O	**READ/WRITE STROBES TO CONFIGURATION RAM:** Generated during accesses to Port 76H.
RAMA[0:12]	6–11, 14–20	O	**CONFIGURATION RAM ADDRESS BUS:** Internal RAM address latches are written to via Ports 74–75H.
RTCALE	38	O	**REAL TIME CLOCK ADDRESS LATCH ENABLE.**
RTCRD#, RTCWR#	39, 40	O	**REAL TIME CLOCK READ/WRITE STROBES.**
PPSEL#	123	O	**PARALLEL PORT CHIP SELECT:** Maps to LPT1, LPT2, or LPT3 as controlled by Bits 5 and 6 of system board setup Port 102H.
ENEXPP	124	O	**PARALLEL PORT EXTENDED MODE ENABLE:** This mode is controlled via bit 7 of system board setup Port 102H.
SPINEN#	63	I	**SERIAL PORT INTERRUPT ENABLE.**
SPIN	62	I	**SERIAL PORT INTERRUPT.**
IRQ3#, IRQ4#	119, 118	O	**SERIAL PORT INTERRUPT:** Configured to either COMM1 (IRQ4#) or COMM2 (IRQ3#). Selection is done via Bit 3 of system board setup Port 102H.
DOSTR#, DISTR#	122, 121	O	**WRITE/READ STROBES FOR SERIAL PORT.**
NPCLK	3	I	**CLOCK FOR NUMERIC PROCESSOR RESET PULSE STRETCHER.**
NPRST	2	I	**NUMERIC PROCESSOR RESET REQUEST INPUT**
NPCNT	4	O	**NUMERIC PROCESSOR COUNT:** Numeric processor reset signal typically synchronized externally and fed to 80387 or 80387SX.
KYBD	36	I	**INTERRUPT REQUEST INPUT FROM KEYBOARD CONTROLLER:** It is internally latched, and then subsequently cleared by a keyboard controller read.

82304 LOCAL CHANNEL SUPPORT CHIP PIN DEFINITIONS (Continued)

Signal Name	Pin No.	I/O	Description
MOUSE	34	I	**INTERRUPT REQUEST INPUT FROM KEYBOARD CONTROLLER'S MOUSE PORT:** It is internally latched and subsequently cleared by a keyboard controller read.
KYBDCS#	120	O	**KEYBOARD CONTROLLER CHIP SELECT.**
IRQ12	35	O	**LATCHED VERSION OF MOUSE INPUT INTERRUPT REQUEST.**
V_{DD}	12, 21, 26, 47, 79, 98, 116		**POWER.**
V_{SS}	13, 27, 48, 80, 89, 99, 117		**GROUND.**
NC	65, 132		**NO CONNECT.**
RSVD	66		**RESERVED.**

82304 132-Pin PQFP Pinout



NOTES:
1. N.C. pins must be left not connected.
2. This pin is reserved . . . must be tied to ground in system.

82304 Parametrics

Absolute Maximum Ratings*

Case Temperature Under Bias .... −40°C to +85°C
Storage Temperature ..... −65°C to +150°C
Voltage to any Pin with
Respect to Ground .... −0.3V to +(V_{CC} +0.3)V
DC Supply Voltage (V_{CC}) ..... −0.3V to +7.0V
DC Input Current ..... ±10 mA

**Notice: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

D.C. Electrical Characteristics T_C = 0°C to +70°C, V_{CC} = 5V ±10%

Symbol	Parameter	Min	Max	Units	Notes
V_{IL}	Input Low Voltage		0.8	V	
V_{IH}	Input High Voltage	2.0		V	
V_{IL}	Input Low Voltage		0.8	V	SCLK
V_{IH}	Input High Voltage	V_{CC}−0.8		V	SCLK
V_{OL}	Output Low Voltage		0.4	V	I_{OL} = 4 mA (Note 1)
V_{OH}	Output High Voltage	2.4		V	I_{OH} = 4 mA (Note 1)
V_{OL}	Output Low Voltage		0.4	V	I_{OL} = 2 mA (Note 2)
V_{OH}	Output High Voltage	2.4		V	I_{OH} = 2 mA (Note 2)
I_{CC}	Power Supply Current		180	mA	No DC Loads
I_{LI}	Input Leakage Current		±10	μA	$V_{SS} < V_{IN} < V_{CC}$
I_{OZ}	TRI-STATE Output Leakage Current		±10	μA	$V_{SS} < V_{OUT} < V_{CC}$

NOTES:
1. DSKSTAT, XA[3:9], XD[0:7].
2. All outputs other than those listed in Note 1.

82304 A.C. Electrical Specifications T_C = 0°C to +70°C, V_{CC} = 5V ±10%

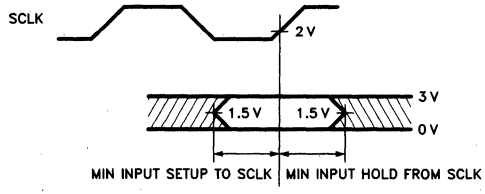
Symbol	Parameter	KIT-16		KIT-20		KIT-25		C_L (pF)	Notes
		Min	Max	Min	Max	Min	Max		
T_1	SCLK Period	31.25		25		20			
T_{2A}	SCLK High/Low Time	12		10		8			
T_{2B}	SCLK High/Low Time	8		6.5		6			
T_3	Reset Setup	10		10		10			
T_4	Reset Hold	3		3		3			
T_5	Reset Pulse Width	500		500		500			
T_6	RC# Pulse Width	75	150	75	150	75	150	50	
T_7	TMRCLK High/Low Time	300		300		300			
T_8	PICCS#, FDACK# Setup	30		30		30			
T_9	PICCS#, FDACK# Hold	0		0		0			
T_{10}	IOR#, IOW#, INTA# Pulse Width	170		170		170			

82304 A.C. Electrical Specifications T_C = 0°C to +70°C, V_{CC} = 5V ±10% (Continued)

Symbol	Parameter	KIT-16		KIT-20		KIT-25		C_L (pF)	Notes
		Min	Max	Min	Max	Min	Max		
T_{11}	Write Data Setup	25		25		25			
T_{12}	Write Data Hold	10		10		10			
T_{13}	Read Data Valid Delay	0	90	0	90	0	90	100	
T_{14}	Read Data Float Delay	0		0		0		100	
T_{15}	RAMD[0:7] to XD[0:7] Delay		36		36		36	100	
T_{17}	CHRDY Delay	0	80	0	80	0	80	25	
T_{18}	CHRDY Inactive Pulse Width	280		280		230		25	5
T_{19}	Address Decode Delays from ADL# ↓	0	62	0	62	0	62	50	1
T_{20A}	Write Strobe Delays from IOW# ↓	0	40	0	40	0	40	50	2
T_{20B}	CDSUWR, DOSTR# Delays from IOW# ↑	0	35	0	35	0	35	50	
T_{20C}	RTCWR#, RAMWR# Delay from CMD# ↑	0	33	0	33	0	33	50	
T_{21}	Read Strobe Delays	0	40	0	40	0	40	50	6
T_{22}	RTCALE Min Pulse Width	120		120		110		50	3
T_{23}	XA[3:9] Delay from ADL# ↓		35		35		35	100	5
T_{24}	S1#, LCCS#, A[0:9] Setup to ADL# ↑	30		30		30			
T_{25}	FBRTN Setup to CMD# ↓	15		15		15			
T_{26}	VGAFB# Setup to CMD# ↑	15		15		15			
T_{27}	LEBA# Delay from CMD#		26		26		26	25	
T_{28}	OEBA# Delay from CMD# ↓		30		30		30	25	
T_{30}	CHRDY ↓ Delay		38		38		38	25	4
T_{31}	NPCNT ↑ Delay	128 NPCLKS		128 NPCLKS		128 NPCLKS		50	5
T_{32}	CHRDY ↑ Delay	192 NPCLKS		192 NPCLKS		192 NPCLKS		25	5
T_{33}	NPCLK High/Low Time	12		12		12			
T_{34}	LS1# Delay from ADL# ↓		35		35		35	50	

NOTES:
1. Address decodes include FCS#, PPSEL#, KYBDCS#, PD and LBEN#.
2. Write strobes include RTCWR#, COSUWR#, DOSTR#, and RAMWR#.
3. Read strobes include RTCRD#, CDSURD#, DISTR# and RAMRD#.
4. From later or NPRST ↑ or CMD# ↓.
5. Functional Specification . . . Not tested.
6. CMD# ↑ causes RTCWR# ↑ and RAMWR# ↑, while IOW# ↑ causes RAMD[0:7] to float. The 82304 insures that CMD#-to-RAMWR#/RTCWR# is at least 5 ns faster than IOW# to RAMD[0:7] float, assuming loading on RAMD[0:7] is greater than or equal to loading on RAMWR# or RTCWR#. This provides a minimum of 5 ns data hold time for the real time clock and SRAM, assuming CMD# and IOW# reach the 82304 at the same instant. Typically, more than 5 ns is provided, since IOW# is generated from, and thus delayed from CMD#.
7. Specification applies to software reset generated via port 92H.

82304 DRIVE LEVELS/MEASUREMENT POINTS FOR A.C. SPECIFICATIONS



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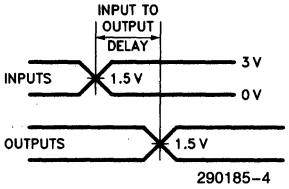

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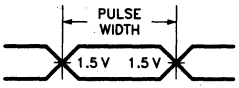

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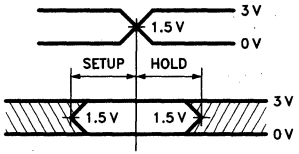
Input/Output Pulse Widths,
Input Clock (Other than SCLK)
HIGH/LOW Times



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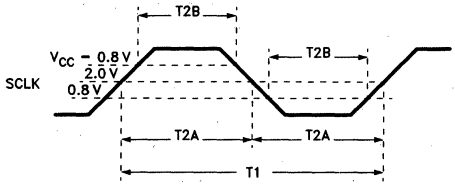
Input Setup and Hold to
another Input (Other than SCLK)



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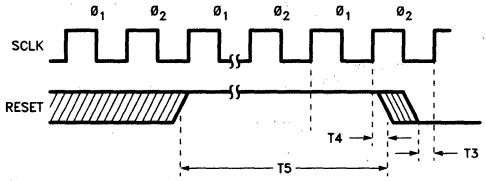
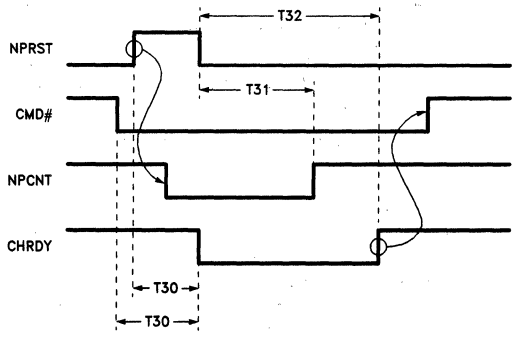


290185-8



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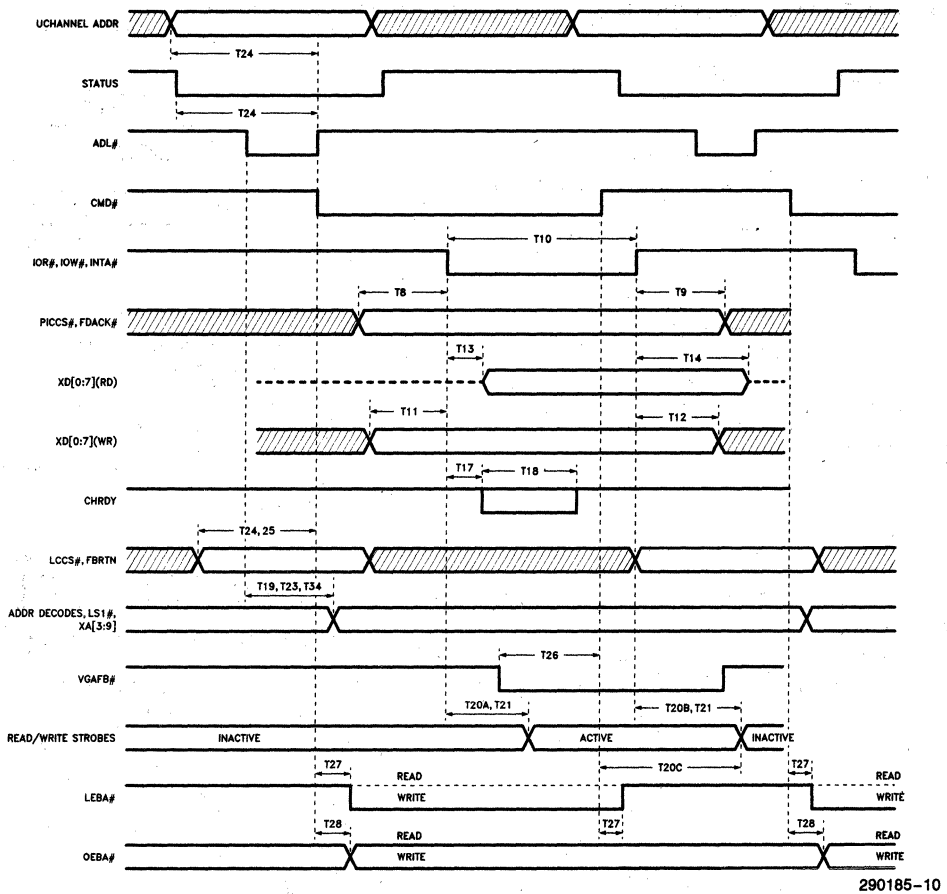
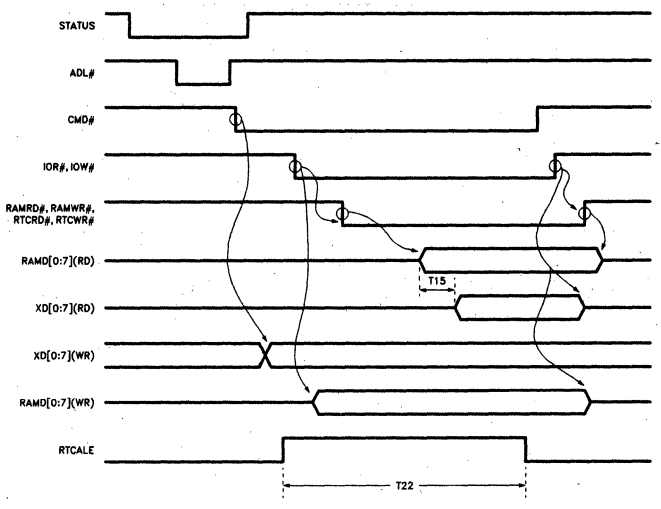
NOTE:
Input Waveforms have $T_R \leq 2.0$ ns from 0.8V to 2.0V.



290185-10



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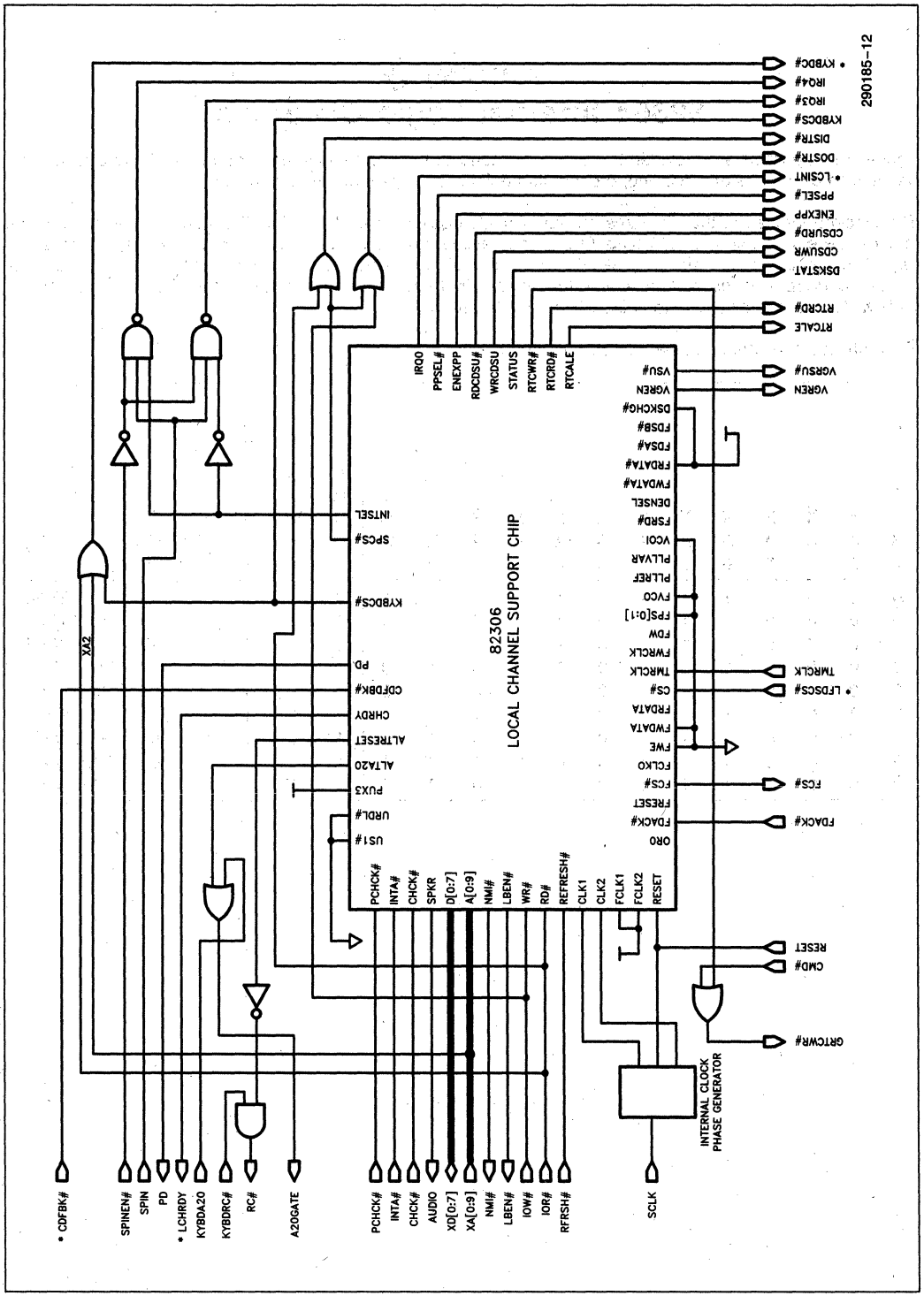
APPENDIX
82304 Internal Logic Diagrams

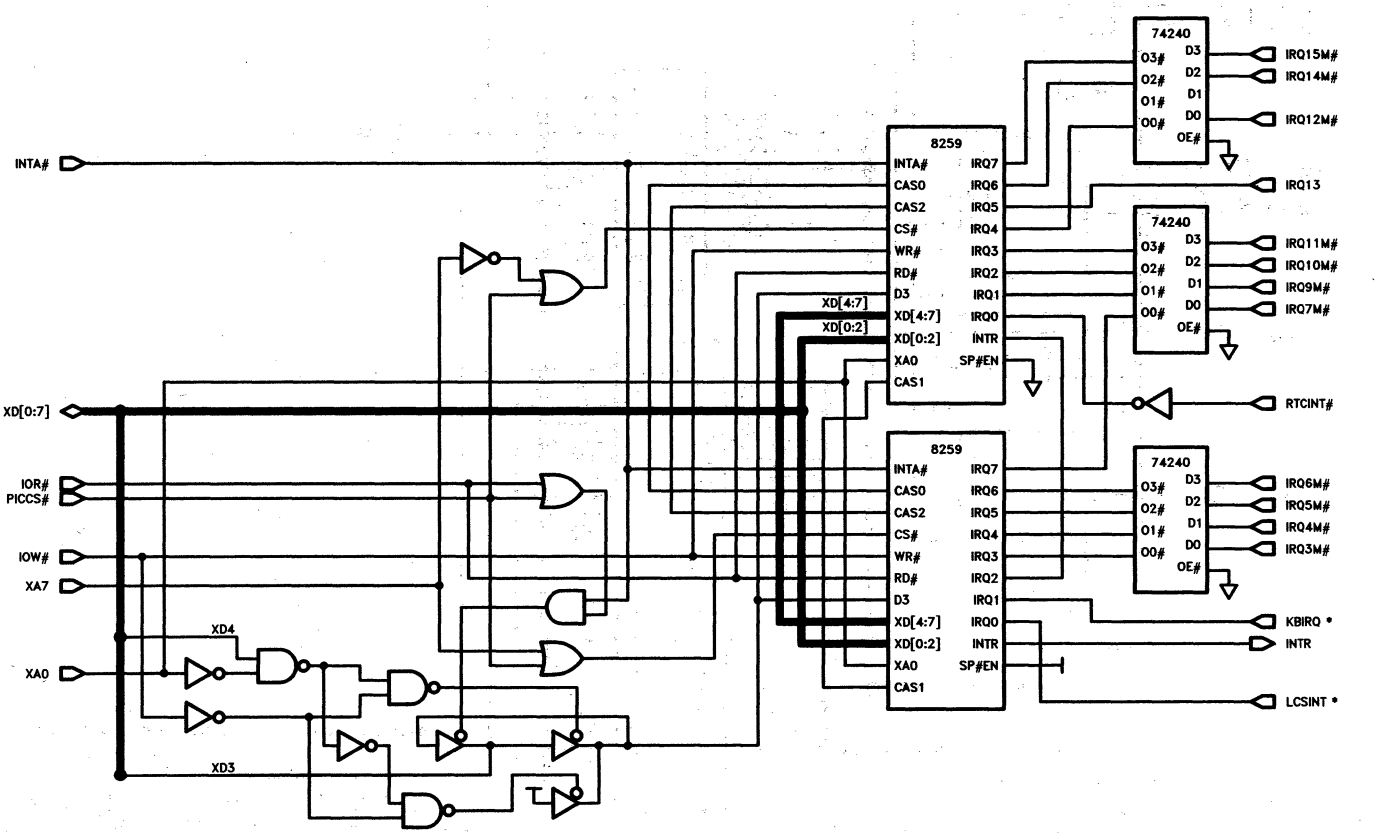
These logic diagrams are provided to aid in understanding the basic functionality of the 82304, and should not be used to estimate signal loading, propagation delays, or any other timing behavior.

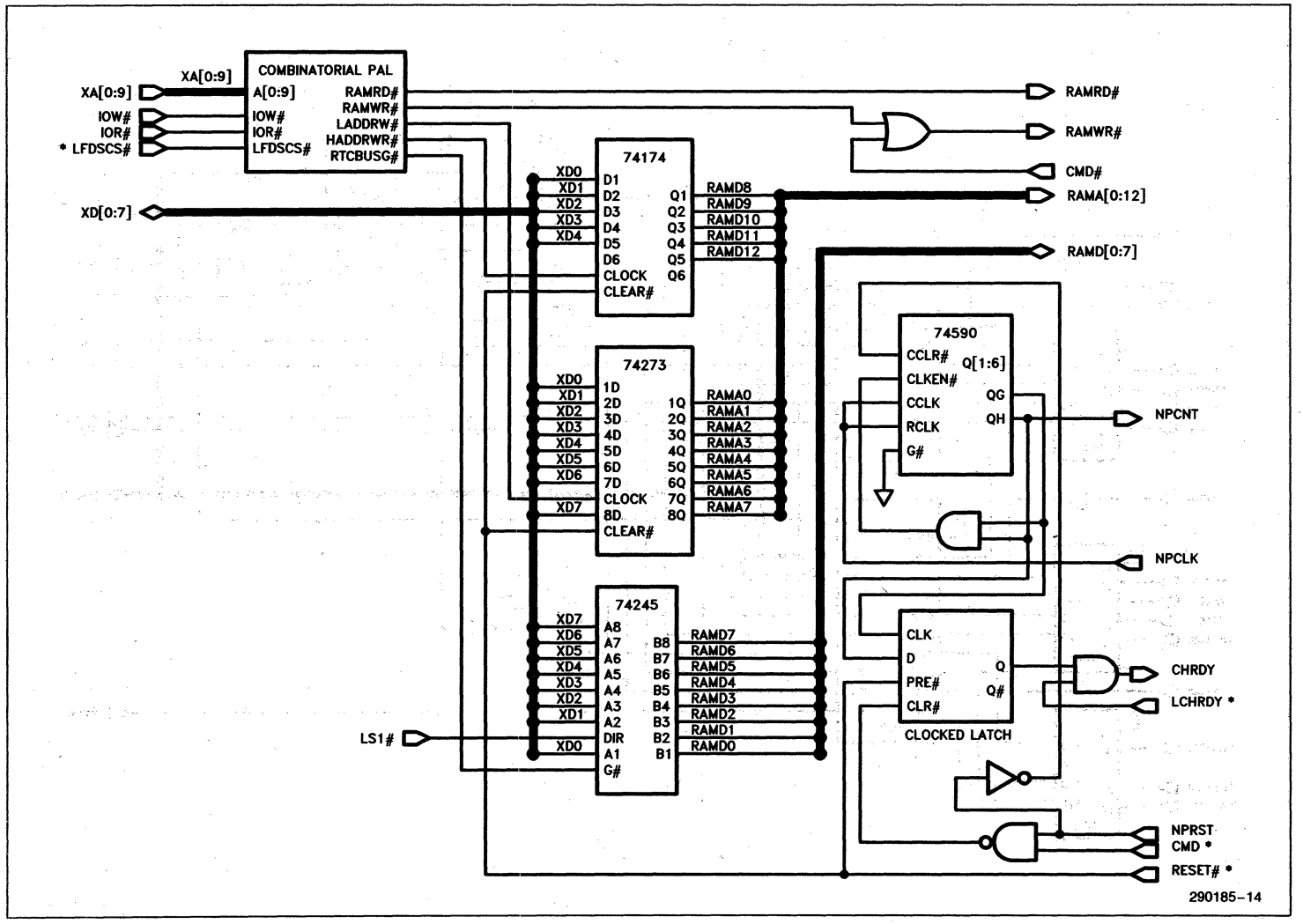
The clocked latches in the diagrams are functionally equivalent to 7474 type TTL latches. The transparent latches are equivalent to 74373 type TTL latches except that the gate input is active low rather than active high. The signals marked with asterisks (*) are not actually available external to the 82304, but simply serve as page-to-page references. Note however, that the XA[0:9] internal address bus is not marked with an asterisk. Only XA[3:9] are available externally, while XA[0:2] are not.

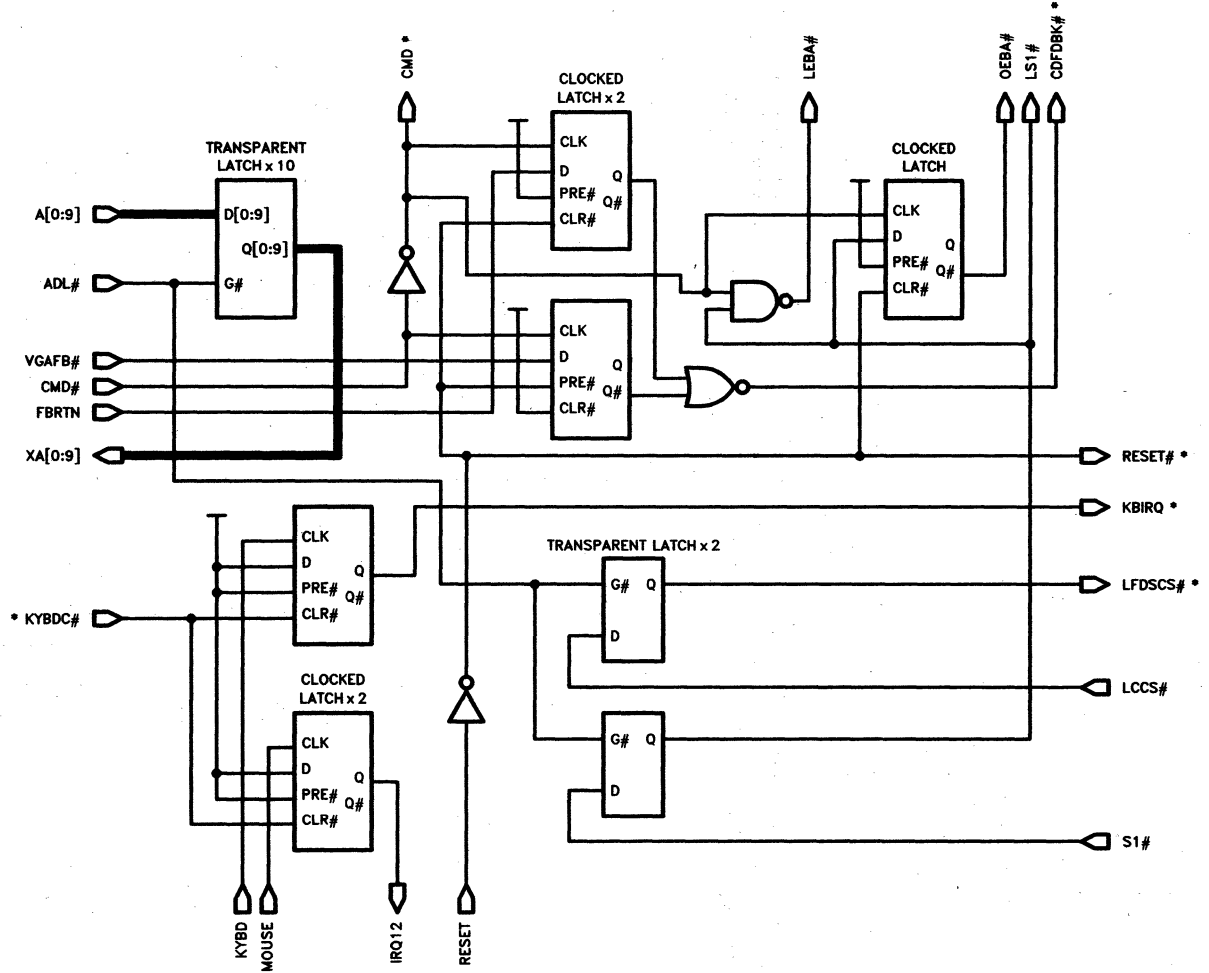
The truth table for the combinatorial PAL is as follows:

LFDSCS#	XA9	XA8	XA7	XA6	XA5	XA4	XA3	XA2	XA1	XA0	IORC#	IOWC#	RAMRD#	RAMWR#	HADDRWR#	LADDRWR#	RTCBUSG#	
0	0	0	0	1	1	1	0	1	1	0	0	1	0	1	1	1	1	76H READ
0	0	0	0	1	1	1	0	1	1	0	1	0	1	0	1	1	1	76H WRITE
0	0	0	0	1	1	1	0	1	0	1	1	0	1	1	0	1	1	75H WRITE
0	0	0	0	1	1	1	0	1	0	0	1	0	1	1	1	0	1	74H WRITE
0	0	0	0	1	1	1	0	0	0	0	1	0	1	1	1	1	0	70H WRITE
0	0	0	0	1	1	1	0	0	0	1	1	0	1	1	1	1	0	71H WRITE
0	0	0	0	1	1	1	0	1	1	0	1	0	1	1	1	1	0	76H WRITE
0	0	0	0	1	1	1	0	0	0	1	0	1	1	1	1	1	0	71H READ
0	0	0	0	1	1	1	0	1	1	0	0	1	1	1	1	1	0	76H READ


290185-12
82306
LOCAL CHANNEL SUPPORT CHIP
INTERNAL CLOCK
PHASE GENERATOR
XA2
* KYBDC#
IR04#
IR03#
KYBDCS#
DISTR#
DOSTR#
* LCSINT
PPSEL#
ENEXPP
CDSURD#
CDSUWR
DSKSTAT
RTCRD#
RTCALE
VGRSU#
VGREN
TMRCLK
* LFDSCS#
FCS#
FDACK#
RESET
CMD#
GRTCWR#
IRQ0
PPSEL#
ENEXPP
RDCDSU#
WRCDSU
STATUS
RTCWR#
RTCRD#
RTCALE
VSU#
VGREN
DSKCHG#
FDSB#
FDSA#
FRDATA#
FWDATA#
DENSEL
FSRD#
VCOI
PLLVAR
PLLREF
FVCO
FPS[0:1]
FDW
FWRCLK
TMRCLK
CS#
FRDATA
FWDATA
FWE
FCLKO
FCS#
FRESET
FDACK#
ORO
INTSEL
SPCS#
KYBDCS#
PD
CDFDBK#
CHRDY
ALTRESET
ALTA20
PUX3
URDL#
US1#
PCHCK#
INTA#
CHCK#
SPKR
D[0:7]
A[0:9]
NMI#
LBEN#
WR#
RD#
REFRESH#
CLK1
CLK2
FCLK1
FCLK2
RESET
* CDFBK#
SPINEN#
SPIN
PD
* LCHRDY
KYBDA20
KYBDRC#
RC#
A20GATE
PCHCK#
INTA#
CHCK#
AUDIO
XD[0:7]
XA[0:9]
NMI#
LBEN#
IOW#
IOR#
RFRSH#
SCLK


INTA#
XD[0:7]
IOR#
PICCS#
IOW#
XA7
XA0
XD4
XD3
8259
INTA#
CAS0
CAS2
CS#
WR#
RD#
D3
XD[4:7]
XD[0:2]
XA0
CAS1
IRQ7
IRQ6
IRQ5
IRQ4
IRQ3
IRQ2
IRQ1
IRQ0
INTR
SP#EN
XD[4:7]
XD[0:2]
74240
O3#
O2#
O1#
O0#
D3
D2
D1
D0
OE#
IRQ15M#
IRQ14M#
IRQ12M#
IRQ13
IRQ11M#
IRQ10M#
IRQ9M#
IRQ7M#
RTCINT#
IRQ6M#
IRQ5M#
IRQ4M#
IRQ3M#
KBIRQ *
INTR
LCSINT *
290185-13


COMBINATORIAL PAL
XA[0:9]
A[0:9]
IOW#
IOR#
LFDSCS#
RAMRD#
RAMWR#
LADDRW#
HADDRWR#
RTCBUSG#
* LFDSCS#
XD[0:7]
74174
D1
D2
D3
D4
D5
D6
CLOCK
CLEAR#
Q1
Q2
Q3
Q4
Q5
Q6
RAMD8
RAMD9
RAMD10
RAMD11
RAMD12
74273
1D
2D
3D
4D
5D
6D
7D
8D
1Q
2Q
3Q
4Q
5Q
6Q
7Q
8Q
RAMA0
RAMA1
RAMA2
RAMA3
RAMA4
RAMA5
RAMA6
RAMA7
74245
A8
A7
A6
A5
A4
A3
A2
DIR
A1
G#
B8
B7
B6
B5
B4
B3
B2
B1
RAMD7
RAMD6
RAMD5
RAMD4
RAMD3
RAMD2
RAMD1
RAMD0
LS1#
RAMD[0:7]
74590
CCLR#
CLKEN#
CCLK
RCLK
G#
Q[1:6]
QG
QH
NPCNT
NPCLK
CLK
D
PRE#
CLR#
Q
Q#
CLOCKED LATCH
CHRDY
LCHRDY *
NPRST
CMD *
RESET# *
RAMRD#
RAMWR#
CMD#
RAMA[0:12]
290185-14


CMD *
CLOCKED LATCH x 2
LEBA#
OEBA#
LS1#
CDFDBK# *
TRANSPARENT LATCH x 10
CLOCKED LATCH
A[0:9]
D[0:9]
Q[0:9]
ADL#
G#
CLK
D
PRE#
CLR#
Q
Q#
VGAFB#
CMD#
FBRTN
XA[0:9]
RESET# *
KBIRQ *
TRANSPARENT LATCH x 2
LFDSCS# *
* KYBDC#
LCCS#
CLOCKED LATCH x 2
S1#
KYBD
MOUSE
IRQ12
RESET

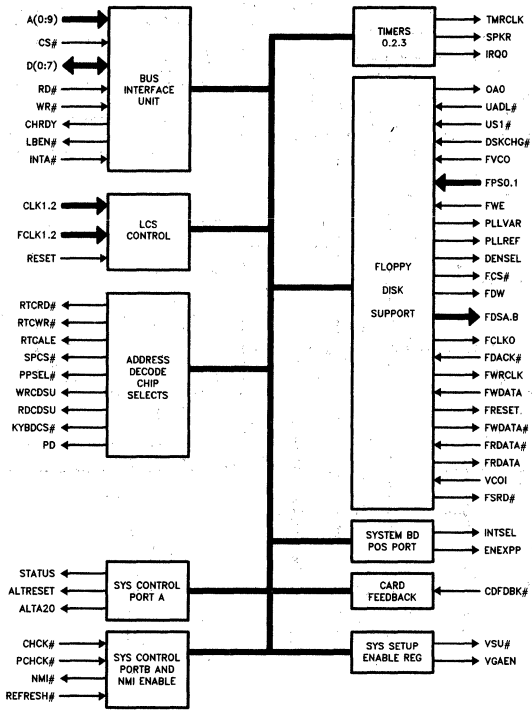
290185-15

82306
LOCAL CHANNEL SUPPORT CHIP

- **Supports I/O Peripherals on the Local Channel**
- **Supports VGA Controller on the VGA Graphics Channel**
- **Floppy Disk Sub-System Support**
  - **— 8272A Interface for IBM Micro Channel Compatible 3½" Drives (Dual Speed Drives −250/500 Kbps)**
  - **— 82072 Interface for IBM Micro Channel Compatible 3½" Drives (250/500 Kbps) and AT Compatible 5¼" Drive (250/300/500 Kbps)**
- **Integrated Programmable Timer/ Counters (0, 2, 3)**
- **Integrates System Registers and Ports**
- **Low Power CHMOS Technology**
- **100-Pin Plastic Quad Flat Pack Packaging**
  (See Packaging Guide Order # 231369)

The 82306 Local Channel Support chip is the register level implementation of the equivalent VLSI device in the IBM Micro Channel systems. It provides FDC interface to support IBM compatible 3½" disk drives when used with 8272A FDA and 3½" & 5¼" (AT Compatible) disk drives when used with the 82072 FDC.

The 82306 also has integrated I/O ports and registers for miscellaneous system board functions, Integrated Address decoder for generaing chip selects for the I/O devices on the Local Channel and 8254 like programmable timers (0, 2, 3) to support speaker tone generation, watch-dog timer and periodic interrupts.



290183-1

October 1988
Order Number: 290183-001

FLOPPY DISK CONTROLLER INTERFACE

The Floppy Disk Controller (FDC) function of the 82306 Local Channel Support chip has two FDC interfaces: 8272A FDC interface as used in IBM Micro Channel systems Model 50/60 and 80, and 82072 FDC interface for value-added performance and compatibility.

The 82306 Local Channel Support chip integrates glue logic required to support the 8272A and the 82072 Floppy Disk Controllers. The FDC interface includes the pre-compensation logic, digital portion of the read data separator logic, and status registers (03F1H, 03F2H, 03F7 ports). The integrated prescaler supports 250 Kbits/sec and 500 Kbits/sec as required in the IBM Micro Channel compatible system. With the 82072 FDC, however, an additional 300 Kbits/sec data stream is supported for interfacing to a standard AT 5¼" drive.

The Floppy Disk subsystem support includes generation of the chip select for the FDC when ports 03F4H or 03F5H are referenced. The Floppy status register (Read only) is implemented externally on the motherboard. To read this register, the 82306 generates the decoded read signal for address 03F0H.

The clock for 8272A is generated by the 82306 Local Channel Support chip, from an external 16 MHz frequency source. The 82072 utilizes its own fixed clock source of 24 MHz.

LOCAL CHANNEL ADDRESS DECODER

The 82306 Local Channel Support provides the Address decoding for the following devices and addresses.

- 8742 Keyboard Interface Chip
- Serial Port
- Parallel Port
- Ports 096H and 097H
- Real-Time Clock (Read, Write and Address Latch Enable)

SYSTEM TIMERS 0, 2, 3

The timers used for periodic interrupt (timer 0), tone generation for audio (timer 2) and watch-dog function (timer 3) are integrated on the 82306 Local Channel Support chip. Timer 0 and 2 are identical in their functionality as the timers in IBM PC/AT, XT and PC systems. The watch-dog timer 3 provides error detection capability and via BIOS, the watch-dog function can be enabled and disabled.

These timers can be programmed via ports 40, 42, 43, 44 and 47.

INTEGRATED SYSTEM REGISTER AND PORTS

The 82306 Local Channel Support chip has the following registers and ports integrated on the chip:

- System Control Port A & B (092H and 061H)
- Card Selected Feedback Register (091H)
- System Board POS Port (102H)
- Port 070H (Write Only)
- System Board Set Up (094H)

The POS register space as defined in the Micro Channel architecture is 100H to 107H. The 82306 integrates 102H on chip and generates PD signal during set-up mode for external implementation of POS ports 100, 101 and 103–107H. POS port 102H is programmed during set-up to enable serial, parallel port and the Floppy Disk Controller.

VGA ENABLE PORT 3C3H

When bit 0 of port 3C3H is programmed as 1, the VGA sub-system is enabled. The chip enable VGAEN is deactivated when a zero is written to the bit. On power up or reset, the VGA sub-system is enabled.

I/O DEVICE MAP

The following table lists the ports and registers integrated on the 82306 Local Channel Support chip.

I/O Register Address	Function
03F1H	Floppy Status Register B
03F2H	Floppy Digital Output Register
03F7H	Digital Input/Config. Register
061H	System Control Port B
092H	System Control Port A
091H	Card Selected Feedback Register
102H	System Board POS Port
070H	NMI Enable (Write Only)
094H	System Board Set-Up
3C3H	VGA Enable Port
40H, 42H, 43H, 44H, 47H	System Timer Ports

For programming and register level details, please refer to IBM technical reference manual.

82306 Local Channel Support Chip Pin Definitions

Signal Name	Pin Number	I/O	Description
A<0:9>	98–89	I	Address inputs.
D<0:7>	86–79	B	Bi-directional data bus.
CS#	78	I	Device chip select.
RD#, WR#	70, 69	I	I/O read and write command inputs.
REFRESH#	67	I	Refresh request generated by the DMA Controller.
RESET	5	I	System power-up reset.
CHRDY	6	O	Channel Ready signal. Driven low (not ready) by the Local Channel Support to extend accesses to its internal ports and to other local I/O bus devices that require a longer cycle time.
CDFDBK#	7	I	Latched card feedback signal.
TMRCLK	9	I	1.193 MHz clock input generated by the Address Bus Controller. It drives the clock inputs of system timers 0 and 2.
SPKR	10	O	Output of system timer 2 gated by bit 1 of Port 61H. It drives the Micro Channel audio sum node.
CLK1, CLK2	72, 3	I	Clock inputs.
FCLK1, FCLK2	71, 4	I	16 MHz (tied high for 82072 interface), clock inputs for 8272A interface.
VSU#	23	O	VGA Setup. It puts the VGA into set-up mode when low.
VGAEN	8	O	VGA chip enable. (Active High) A low level disables the VGA subsystem.
ENEXPP	22	O	Parallel port "extended mode" enable. When high, the parallel port can function bi-directionally. When low, the port is in "compatible mode" i.e., write only.
SPCS#	31	O	Serial port chip select. Can be mapped to COMM1 or COMM2.
INTSEL	32	O	Selects either IRQ3# (COMM2) or IRQ4# (COMM1) to serve as the interrupt request for the serial port.
STATUS	33	O	Floppy Disk Active Status
RTCWR# RTCRD# RTCALE	34 36 35	O	Write, Read and Address latch enable signal to the real time clock chip.
FSRD#	37	O	Read command for the Read-only floppy status port 3F0H.
WRCDSU	40	O	Write CD Setup Register. Active high write command generated on writes to port 96H (adapter enable setup register).
RDCDSU#	49	O	Read CD setup register. Active low signal reads port 96H.
LBEN#	42	O	Local Bus Engage. It is "OR"ed with the LBEN# output of the DMA/CACP to become one of the qualifiers that enable the data buffer between Micro Channel Bus and motherboard I/O bus. The LCS enable this buffer for accesses to the local I/O bus.
KYBDCS#	43	O	8742 keyboard controller chip select.
ALTRESET	44	O	Processor reset under software control. Except for a shorter reset pulse width, it is identical in function to the reset generated under software control by the 8742. (Optimized for switching between Real-mode and Protected-mode tasks.)

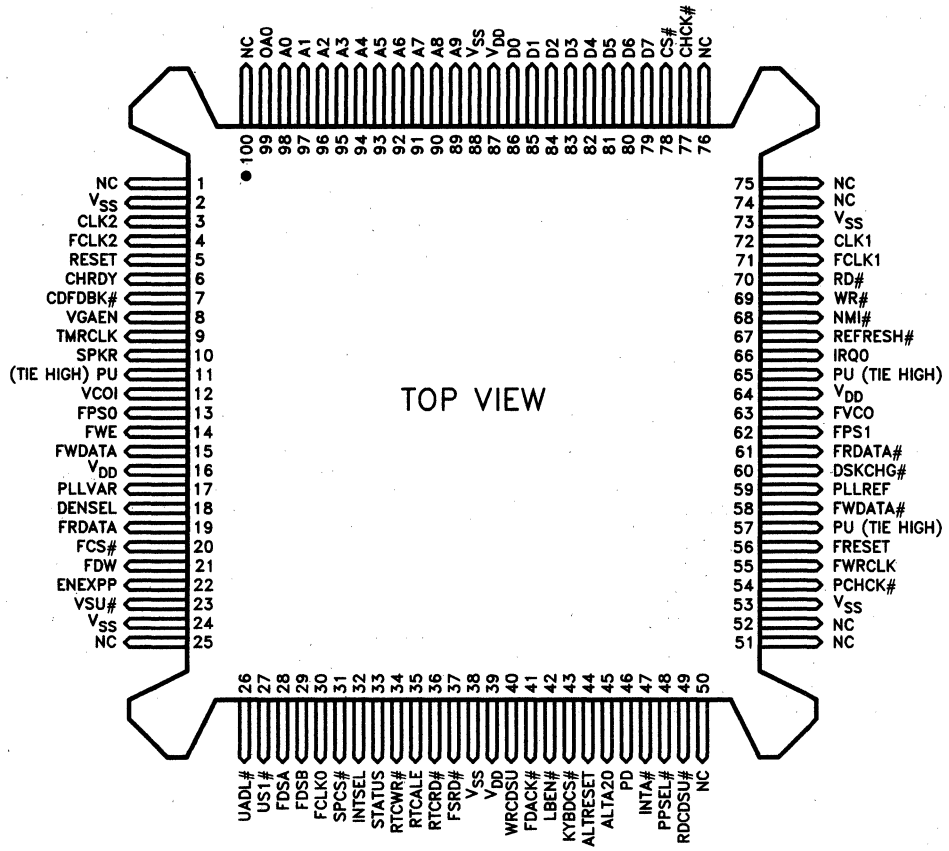
82306 Local Channel Support Chip Pin Definitions (Continued)

Signal Name	Pin Number	I/O	Description
ALTA20	45	O	Alternate A20 bit-Controls address bit A20 in a manner similar to the way it is controlled by the 8742. (Optimized for switching between Real-mode and Protected-mode tasks).
PD	46	O	POS Decode output. When the system board is in setup mode, this output acts as an (active high) chip select for system board POS ports 100H, 101H, and 103H through 107H. (POS port 102H is integrated on the Local Channel Support.)
INTA#	47	I	Interrupt acknowledge generated by the Bus controller.
PPSEL#	48	O	Parallel port chip select. Can be programmed to map the parallel port to LPT1, LPT2, or LPT3.
PCHCK#	54	I	DRAM Parity Error. It is driven by the Bus Controller upon detection of a motherboard DRAM parity error.
IRQ0	66	O	System Timer 0 timeout Interrupt Request.
NMI#	68	O	NMI request to the CPU. This is an open drain output that allows for an external wire "OR" with other NMI sources.
CHCK#	77	I	Micro Channel channel check indicator, for reporting adapter errors.
FPS0, FPS1	13, 62	I	Low and high order pre-compensation select bits. They are driven by the 8272A floppy disk controller. (Note that the pre-compensation logic is integrated on the Local Channel Support). Tied to GND when using 82072.
FWE	14	I	Write Enable for floppy. Generated by the FDC to enable the write data stream to disk.
FWDATA	15	I	FDC output write data stream. It goes through the LCS integrated pre-compensation logic, and then is fed to the drive over the LCS WRDATA# output. In 82072, the FWDATA is inverted and fed into the drive controller.
FWDATA#	58	O	Pre-compensated write data stream to disk for 8272. For 82072 it is simply an inverted output of FWDATA
FRDATA#	61	I	Read data stream from disk.
FRDATA	19	O	Buffered read data output to the FDC. No connect for 82072.
FDSA, FDSB	28, 29	O	Drive select/motor enable outputs.
DENSEL	18	O	Density Select.
FCS#	20	O	Device select for the FDC.
FDACK#	41	I	DMA acknowledge to the FDC from the DMA/CACP.
FCLKO	30	O	8272A clock. It is 8 MHz for high density, or 4 MHz for low density. Not required for 82072.
FWRCLK	55	O	8272A write clock input. It oscillates at twice the data rate; i.e., 1 MHz for a rate of 500 Kbits/sec and 500 KHz for a rate of 250 Kbits/sec. No connect for 82072.
FRESET	56	O	FDC Reset.
DSKCHG#	60	I	Disk changed signal.
VCOI	12	I	Buffered output of the 4024 voltage controlled oscillator. Grounded for 82072.

82306 Local Channel Support Chip Pin Definitions (Continued)

Signal Name	Pin Number	I/O	Description
PLLVAR	17	O	Divided down version of VCOI. It is fed back and used for phase comparison against the PLLREF output. No connect for 82072.
PLLREF	59	O	Phase Lock Loop Reference Clock. No connect for 82072.
FVCO	63	I	Valid Read Data Stream Indicator. It is driven by the 8272A, and defines a valid read data stream. Grounded for 82072.
FDW	21	O	Data window input of 8272A. It defines the valid sample points in the read data stream. No connect for 82072.
OA0	99	O	Output A0 signal for use by the 82072 disk controller. No connect for 8272A.
UADL#	26	I	Micro Channel Address decode latch. An Active low signal used to latch US1# on the trailing edge for support of the OA0 signal. Grounded for 8272A.
US1#	27	I	Micro Channel status bit 1. Used to distinguish a write operation from a read operation for support of the OA0 signal. Grounded for 8272A.
PU	11, 57, 65	I	Pull Up
V_{DD}	16, 39, 64, 87		Power
V_{SS}	2, 24, 38, 53, 73, 88		Ground
NC	1, 25, 50, 51, 52, 74, 75, 76, 100		No Connect

82306 Local Channel Support Chip



290183-2

NOTES:
PU = Pull-Up
NC = No Connect
—Pull-Up Resistor Value = 2K to 10K
—No more than three nodes to a single pull-up resistor.

82306 PARAMETRICS

ABSOLUTE MAXIMUM RATINGS*

Case Temperature under Bias .... −40°C to +85°C
Storage Temperature ..... −65°C to +150°C
Voltage to Any Pin with Respect to Ground ..... −0.3V to (V_{CC}+0.3)V
DC Supply Voltage (V_{CC}) ..... −0.3V to +7.0V
DC Input Current ..... ±10 mA

**Notice: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

NOTICE: Specifications contained within the following tables are subject to change.

D.C. CHARACTERISTICS

T_C = 0°C to +70°C, V_{CC} = 5V ±10%

Symbol	Parameter	Min	Max	Units	Conditions
V_{IL}	Input Low Voltage		0.8	V	
V_{IH}	Input High Voltage	2.0		V	
V_{IL}	Input Low Voltage		0.8	V	CLK1, CLK2
V_{IH}	Input High Voltage	V_{CC} − 0.8		V	CLK1, CLK2
V_{OL}	Output Low Voltage		0.4	V	I_{OL} = 2 mA
V_{OH}	Output High Voltage	2.4		V	I_{OH} = 2 mA
I_{CC}	Power Supply Current		180	mA	No DC Loads
I_{LI}	Input Leakage Current		±10	μA	$V_{SS} < V_{IN} < V_{CC}$
I_{OZ}	Tri-State Output Leakage Current		±10	μA	$V_{SS} < V_{OUT} < V_{CC}$

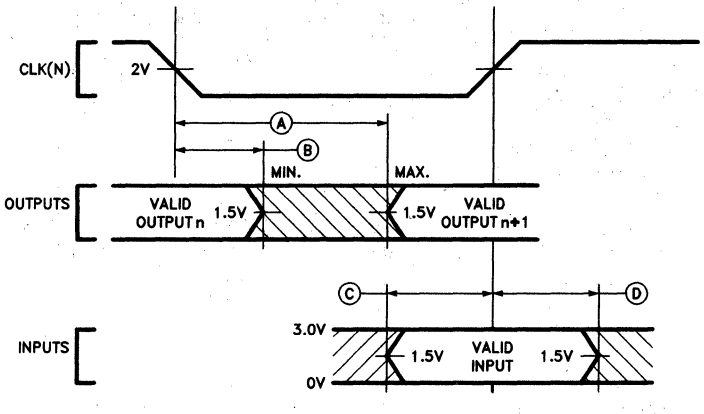
82306 LCS A.C. SPECS

T_C = 0°C to +70°C, V_{CC} = 5V ±10%

Symbol	Parameter	Kit 16 MHz		Kit 20 MHz		Kit 25 MHz		C_L	Notes
		Min	Max	Min	Max	Min	Max	(pF)	
T1	CLK1, CLK2 LOW TIME	15		15		14			
T2	CLK1, CLK2 NON-OVERLAP	4		4		0			
T3	FCLK1, FCLK2 LOW TIME	10		10		10			
T4	FCLK1, FCLK2 NON-OVERLAP	10		10		10			
T5	RESET PULSE WIDTH	500		500		500			
T6	ALTRESET PULSE WIDTH	75	150	75	150	75	150	75	
T7	TMRCLK HIGH/LOW TIME	300		300		300			
T8	A9–A0, CS#, FDACK# SETUP	30		30		30			
T9	A9–A0, CS#, FDACK# HOLD	10		10		10			
T10	RD#, WR#, INTA# PULSE WIDTH	170		170		170			
T11	WRITE DATA SETUP	25		25		25			
T12	WRITE DATA HOLD	0		0		0			
T13	READ DATA VALID DELAY	0	50	0	50	0	50	75	
T14	READ DATA FLOAT DELAY	0	35	0	35	0	35	75	
T15	CHRDY DELAY	0	80	0	80	0	80	75	5
T16	CHRDY INACTIVE PULSE WIDTH	230		230		180		75	5, 10
T17	ADDRESS DECODE DELAYS	0	50	0	50	0	50	75	1
T18	WRITE STROBE DELAYS	0	40	0	33	0	30	75	2
T19	READ STROBE DELAYS	0	40	0	40	0	40	75	3
T20	RTCALE MIN PULSE WIDTH	120		120		110		75	10
T21	DATA SETUP TO INTA#	25		25		25			
T22	DATA HOLD FROM INTA#	5		5		5			
T23A	FCLKO HIGH TIME	45	63	45	63	45	63	75	6
T23B	FCLKO HIGH TIME	90	150	90	150	90	150	75	6
T23C	FCLKO VALID DELAY		35		35		35	75	
T24A	FWRCLK HIGH TIME	200	300	200	300	200	300	75	
T24B	FWRCLK VALID DELAY		35		35		35	75	
T25	FWDATA# PULSE WIDTH	350		350		350		75	
T26	FRDATA# PULSE WIDTH	40		40		40		75	
T27	FRDTA PULSE WIDTH	125		125		125		75	
T28A	FDW SAMPLE PERIOD	1 µs		1 µs		1 µs		75	4, 7
T28B	FDW SAMPLE PERIOD	2 µs		2 µs		2 µs		75	4, 7
T29	VCOI FREQUENCY	4 MHz		4 MHz		4 MHz			4
T30A	PLLVAR,PLLREF FREQUENCY	1 MHz		1 MHz		1 MHz		75	4, 7, 8
T30B	PLLVAR,PLLREF FREQUENCY	500 KHz		500 KHz		500 KHz		75	4, 7, 8
T31	US1# SETUP TO UADL#	25		25		25			9

NOTES:
1. Address decode delays include SPCS#, LBEN#, KYBDCS#, FCS#, PD, PPSEL#, and OA0. (OA0 supports 82072 interface.)
2. Write Strobe delays include RTCWR# and WRCDSU.
3. Read Strobe delays include RTCRD#, FSRD#, and RDCDSU#.
4. Typical values . . . not tested.
5. LCS extends cycles to the 8242 keyboard controller, serial port, real time clock, and 8272 Floppy Disk Controller.
6. T23A applies to FCLKO = 8 MHz (500 KBPS Data Rate).
   T23B applies to FCLKO = 4 MHz (250 KBPS Data Rate).
7. T28A and T30A apply to 500 KBPS. The T28B and T30B apply to 250 KBPS.
8. VCOI/4 for 500 KBPS. VCOI/8 for 250 KBPS. PLLREF applies only when PLL is locked.
9. 82072 Support.
10. Functional Spec . . . not tested.

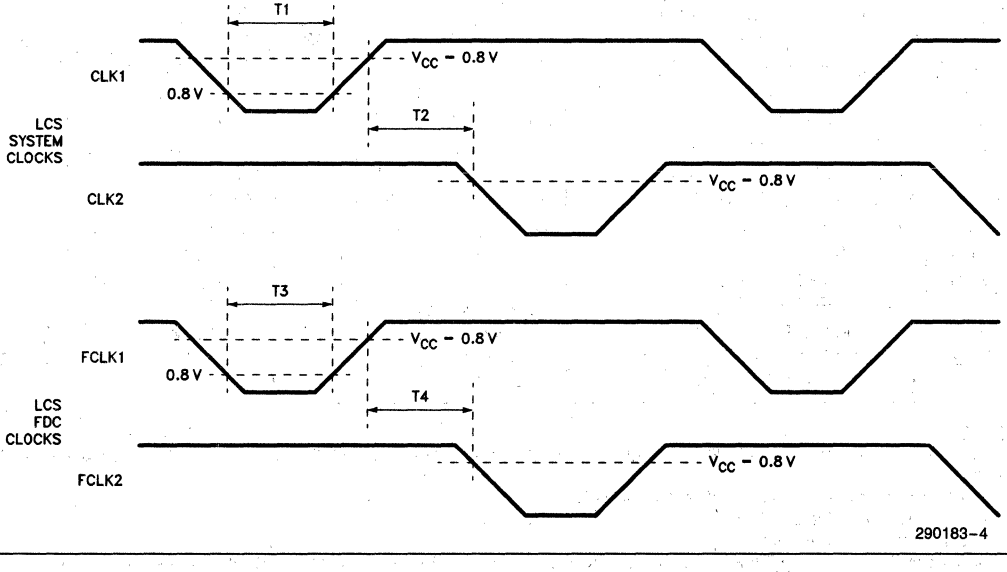
DRIVE LEVELS AND MEASUREMENT POINTS FOR A.C. SPECIFICATIONS



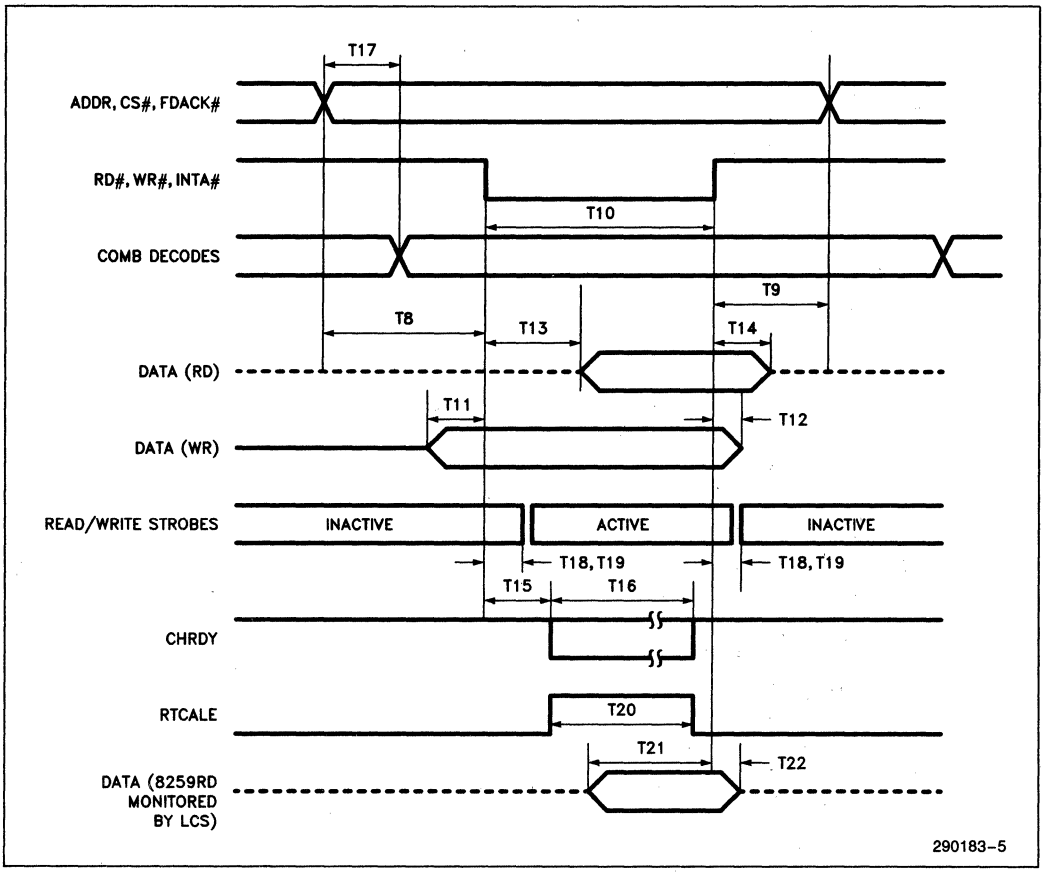
LEGEND:
A. Maximum Output Delay Specification.
B. Minimum Output Delay Specification.
C. Minimum Input Setup Specification.
D. Minimum Input Hold Specification.

Input waveforms have tr ≤ 2.0 ns from 0.8V to 2.0V.

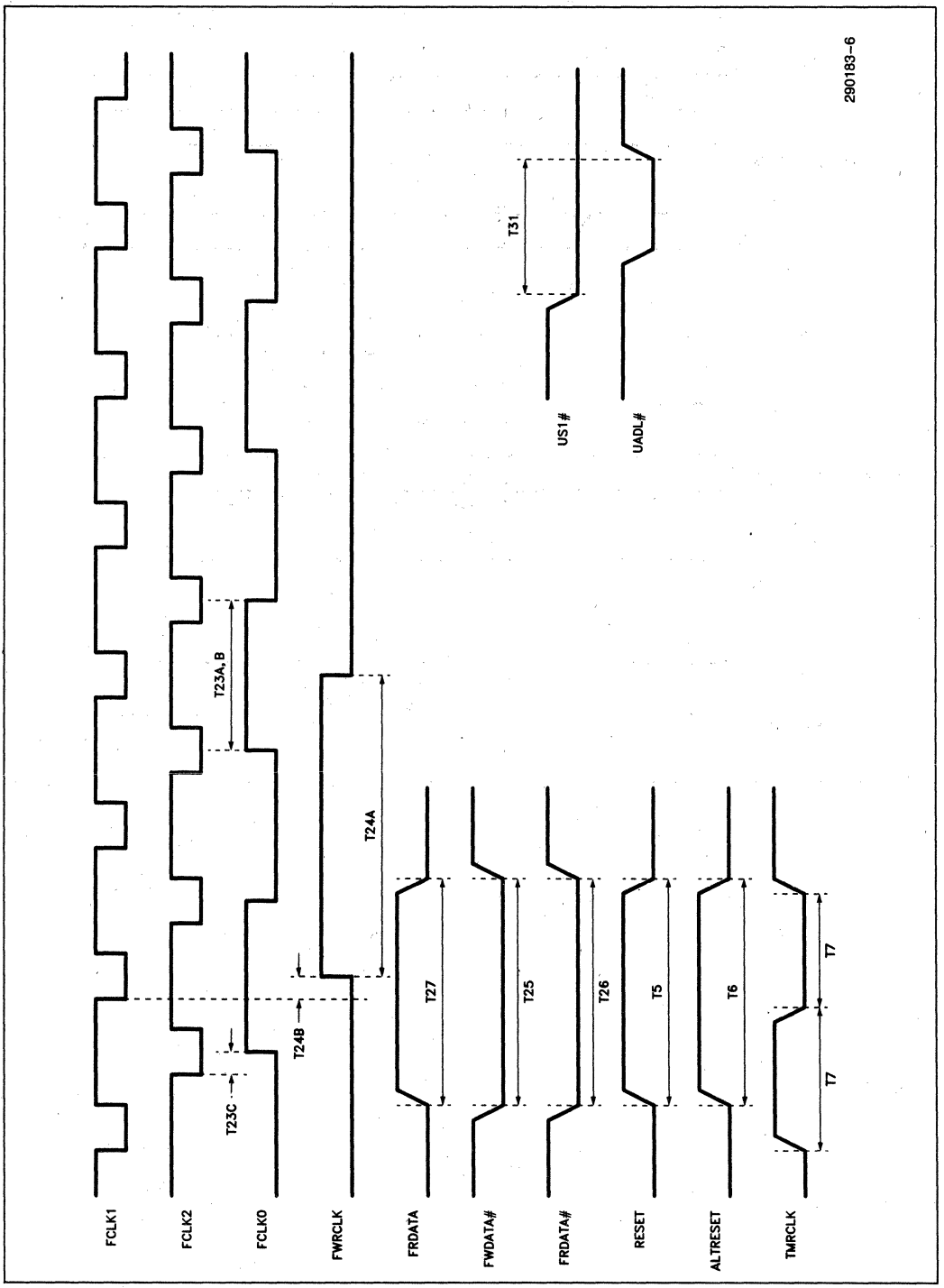
LCS CLOCKS



SYSTEM INTERFACE



MISCELLANEOUS TIMINGS



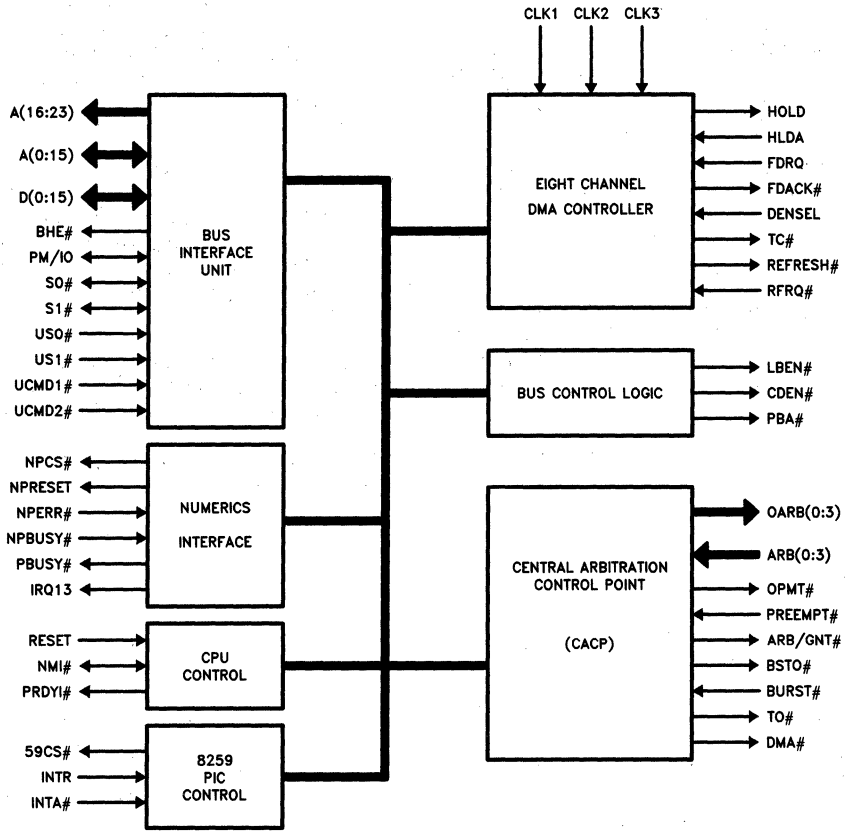
82307
DMA/Micro Channel ARBITRATION CONTROLLER

- **8 Channel DMA Controller (8/16-Bit)**
- **Integrated Central Arbitration Control Point**
- **Refresh Address Generation/Cycling**
- **Numerics Co-processor Interface**
- **Address Decoding**
  - **— Numeric Coprocessor**
  - **— Interrupt Controller**
  - **— POS Address Space for Expansion Slots**
- **Low Power CHMOS Technology**
- **132-Pin Plastic Quad Flat Pack Packaging**

  (See Packaging Spec., Order # 231369)

The 82307 DMA/Micro Channel Arbitration Controller is a register level implementation of the equivalent VLSI device in IBM Micro Channel systems. The Central Arbitration Control Point (CACP) as defined in the Micro Channel Architecture for bus arbitration is integrated in this VLSI device.

The 82307 also integrates the Address decoder logic for generating decodes for numeric coprocessor, Interrupt controllers and POS address space.



290186-1

November 1988
Order Number: 290186-001

DMA FUNCTION

The 82307 features eight 8/16-bit channels, 24-bit addressing capability, and operates in two-cycle transfer mode as defined in the Micro Channel architecture. The DMA controller owns the bus for both halves of the transfer cycle.

The DMA function in the 82307 also supports the motherboard Floppy Disk Controller. Upon receiving the DMA request from the FDC, the DMA controller arbitrates for the Micro Channel bus on behalf of the FDC. The FDC is acknowledged once the bus is granted to initiate the data transfer.

Micro Channel ARBITRATION

The other major function of the 82307 DMA controller is to provide Micro Channel Arbitration. It provides full Micro Channel bus arbitration capability according to the 18-level priority scheme. During normal operation priority 0–15 are assigned with 15 being the lowest priority for the CPU. Priority level −1 which has the higher priority than 0 is also assigned to CPU (switched from 15 to −1) during NMI error recovery. The highest priority −2 is used for refresh.

The bus arbitration priority is asserted via the ARB0–ARB3 signals by the requesting masters to gain control. Bus granting is assigned by the priority level. During an arbitration cycle no Micro Channel master is allowed to drive the bus.

The bus can be preempted by the 82307 when arbitrating on behalf of DMA, or when it is requested to run a refresh cycle, or to respond to NMI error recovery. The preempting of the bus can also be initiated by Micro Channel masters.

The CACP Control Port 090H is integrated on chip.

Micro Channel REFRESH ADDRESS GENERATION/CYCLING

The actual refresh request is generated by the 82309 Address Bus Controller. Upon receiving this request the 82307 DMA Controller gains bus control and executes the refresh cycle. Address generation for the Micro Channel refresh cycle is generated by the 82307 DMA controller.

NUMERICS COPROCESSOR INTERFACE

The 82307 DMA controller supports the numerics coprocessor interface. It provides software transparency required to interface an 80387 to 80386 processor. Ports F0H and F1H are integrated on the 82307.

The numerics coprocessor interface support includes the chip select decode for coprocessor internal register accesses of addresses F8H, FAH and FCH. The 82307 also alerts the CPU of any coprocessor error output generated by asserting the interrupt request IRQ13.

ADDRESS DECODER

The Address Decoder logic decodes the chip select for the 8259 Interrupt Controllers and generates POS Address Space output for addresses 100H through 107H to support the Card set-up signals for the expansion slots.

The chip select output is for both 8259s in the system, so it must be externally gated with local channel address bit A7 to select each actual device.

For programming and register level details, please refer to IBM PS/2 Technical Reference Manual.

82307 DMA/Micro Channel Arbitration Controller Pin Definitions

Signal Name	Pin Number	I/O	Description
A<0:23>	13-2, 130-124, 122-118	A0-A15 B A16-A23 O	Processor local address bus. A16-A23 are output only and are driven when the DMA controller is bus master. A0-A15 are bi-directional. They are inputs when the CPU is master, allowing the CPU access to the chip's internal ports. They are outputs when the DMA is master.
D<0:15>	18-21, 23-31, 35-37	B	Processor local data bus. When the DMA is master, it drives this bus in a write cycle, and samples it during a read cycle. When the CPU is master, the bus is used to access DMA's internal registers.
S0#, S1#	87, 85	B	CPU or DMA cycle status indicators. The DMA drives these signals when it is bus master. When a slave, the DMA inputs these signals to track CPU cycles.
BHE#	84	O	Byte high enable. It is driven when the DMA owns the bus and tristated otherwise. This signal ties directly to the CPU BHE# output in an 80386SX machine.
PM/IO#	81	B	CPU memory / I/O indicator. The DMA drives PM/IO# when bus master, and inputs it when it is slave.
US0#, US1#	43, 44	I	Micro Channel status pins. Generated by the Bus controller when the CPU or DMA is master. When a slot-resident master owns the bus, it generates US0M# and US1M#, and the DMA inputs these so as to recognize when the slot-resident master relinquishes the bus. (The slot-resident master end-of-transfer is recognized when US0M#, US1M#, the channel CMD# signal, and the channel BURST# signal are all negated.)
OARB0-OARB3	58-55	O	DMA/CACP arbitration bus outputs. These signals are driven by the DMA/CACP to arbitrate on behalf of a floppy disk service at priority level 2.
PBA#	107	O	Processor Bus Access. The signal indicates a CPU bus access to the numeric coprocessor or to one of the DMA/CACP registers.
ARB3-ARB0	59-62	I	DMA/CACP arbitration bus inputs. These signals tie directly to the Micro Channel. All competing masters including the DMA/CACP drive these during an arbitration cycle, and the master with the highest priority takes control of the Micro Channel after the arbitration cycle is complete.
OPMT#	92	O	Preempt Bus Master. DMA/CACP drives this output whenever it wishes to preempt the current bus master. This can occur when arbitrating on behalf of a DMA channel service or when arbitrating on behalf of a refresh request, or when arbitrating on behalf of the CPU so as to let it respond to a NMI (non-maskable interrupt) request.
PREEMPT#	45	I	Wired "OR" of the PREEMPT# signals from all Micro Channel masters, including the DMA/CACP (PMTO#). It signifies that a master wishes to force an arbitration cycle.
ARB/GNT#	63	O	Arbitration Cycle indicator. The DMA/CACP drives this Micro Channel signal high to signify an arbitration cycle. During the arbitration cycle, all competing masters drive their priorities onto the arbitration bus (ARB03-ARB00). The falling edge of ARBGNT# signifies the end of the arbitration cycle, at which time the master with the highest priority takes control of the bus. If no master competes for the bus, the pullups on ARB03-ARB00 will read binary 1111 by default, which is the normal operating priority of the CPU.

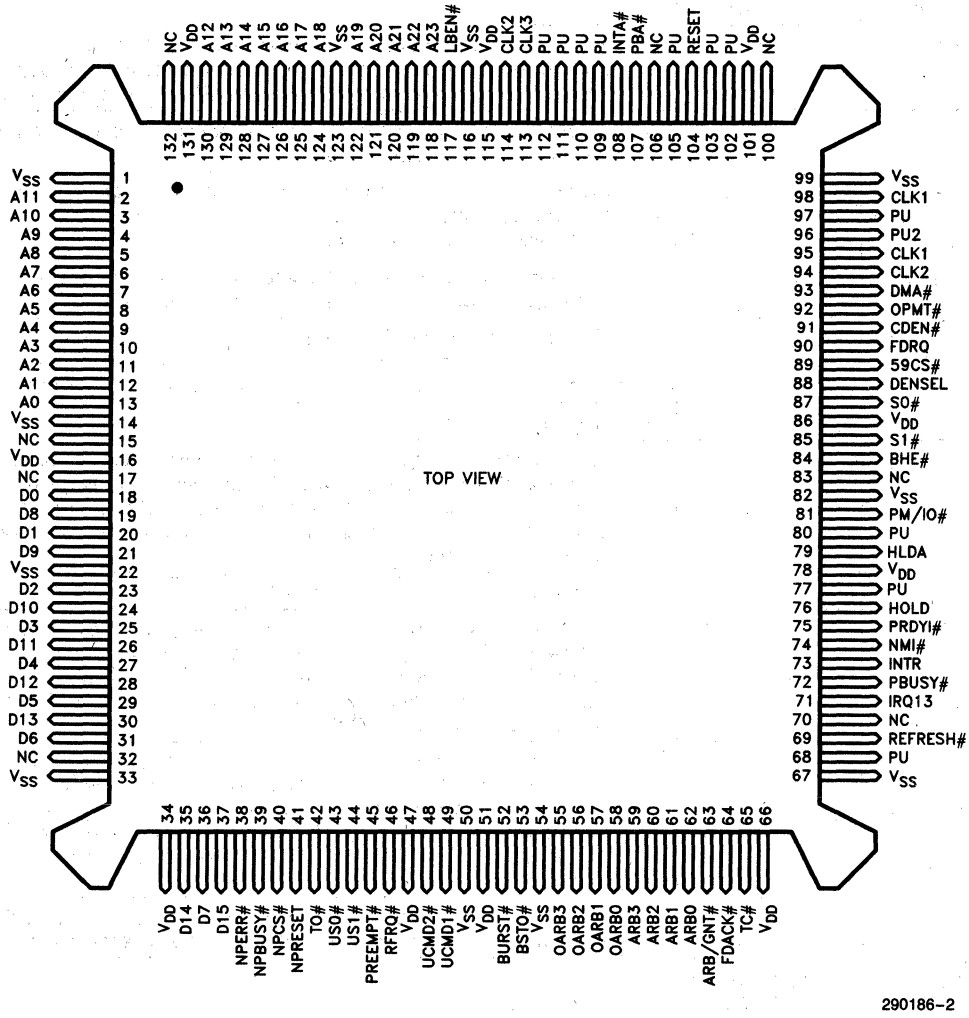
82307 DMA/Micro Channel Arbitration Controller Pin Definitions (Continued)

Signal Name	Pin Number	I/O	Description
BSTO#	53	O	Burst Output. The DMA/CACP drives this output in order to own the Micro Channel for multiple cycles. Specifically, since all PS/2 DMA cycles are two-cycle, BSTO# is driven to allow the DMA controller to own the bus for both halves of a two-cycle transfer.
BURST#	52	I	Burst Request Input. It is an input to the CACP from the current master wishing to own the bus for multiple cycles. It is derived by "OR"ing the Micro Channel BURST# signal with the DMA/CACP BSTO# signal.
HOLD, HLDA	76, 79	(HOLD = O) (HLDA = I)	Hold/Hold Acknowledge to the CPU.
FDRQ, FDACK#	90, 64	(FDRQ = I) (FDACK# = O)	Floppy DMA Request, Acknowledge signals. The motherboard FDC requests DMA service via FDRQ. In response, the DMA/CACP arbitrates for the Micro Channel on behalf of the floppy disk system. Once the DMA/CACP has gained control of the bus, it acknowledges the FDC via FDACK#.
TC#	65	O	DMA Transfer Complete.
UCMD1#, UCMD2#	49, 48	I	Micro Channel Command Inputs. These inputs are driven directly by the Micro Channel CMD# signal.
RFRQ#	46	I	Refresh Cycle Request from the Address Bus Controller.
REFRESH#	69	O	Refresh Cycle Signal. The DMA/CACP drives this output active during refresh cycles. This signal is buffered to become the Micro Channel REFRESH# signal.
59CS#	89	O	Interrupt Controller Chip Select (8259s). Note that this output is activated if either interrupt controller is selected. It is then externally gated with the local I/O channel address bit A7 to distinguish between controller 1 and controller 2.
DENSEL	88	I	Density Selected for the motherboard FDC
CDEN#	91	O	Card Setup Enable. During system setup, a bit pattern is written to port 96H to select a particular slot for configuration. CDEN# enables the decode of these bits to send an active CDSETUP# signal to the selected slot. CDEN# is simply a combinatorial (non-clocked) decode of ports 100H–107H.
CLK1, CLK2, CLK3	95, 98, 94, 114, 113	I	Clock Inputs
RESET	104	I	Power-up System Reset
INTR, INTA#	73, 108	I	Interrupt Request/Acknowledge. The PS/2's 8259 based interrupt system generates interrupt requests to the CPU via INTR. In response, the CPU fetches the appropriate interrupt vector from the interrupt controller in an interrupt acknowledge cycle. The Bus controller decodes the CPU status outputs, and drives INTA# to identify a CPU interrupt acknowledge cycle. The DMA/CACP monitors this activity via its INTR and INTA# inputs. In response to INTA#, the DMA/CACP drives LBEN# so as to enable the 8259 vector onto the Micro Channel. The CACP uses INTR to ensure that the CPU has an opportunity to service an interrupt within one "fairness" cycle; i.e., it prevents the CPU from being totally locked out by higher priority arbiters.

82307 DMA/Micro Channel Arbitration Controller Pin Definitions (Continued)

Signal Name	Pin Number	I/O	Description
NMI#	74	B	Non-Maskable Interrupt to force arbitration cycle to allow CPU bus ownership. As an output, this appears to the system as an open drain, which allows for an external wire "OR" with other NMI sources.
PRDYI#	75	I	Processor Ready Input. The Bus controller generates this signal to terminate CPU and DMA cycles.
NPCS#	40	O	Chip select for the Numeric Coprocessor. It is an unlatched decode that acts as a chip select for CPU accesses to the numeric coprocessor's internal registers.
NPRESET	41	O	Numeric Coprocessor Reset. It resets the numeric coprocessor either upon a system reset or under software control.
NPERR#	38	I	Numeric Coprocessor Error Input. It is an input from the numeric coprocessor error output. The DMA/CACP uses it to generate an interrupt request (IRQ13) to inform the CPU of a coprocessor error.
NPBUSY#	39	I	Numeric Coprocessor Busy
PBUSY#	72	O	Processor Busy Output. It drives the CPU numeric coprocessor busy input. It is activated normally when the coprocessor is busy executing an instruction, but is also activated when a coprocessor error is detected. The CPU will not attempt to utilize the coprocessor as long as PBUSY# is active.
IRQ13	71	O	Numeric Coprocessor Error Interrupt
LBEN#	117	O	Local Bus Enable. This signal is used to enable the data buffers between the Micro Channel and local I/O bus. It is activated for decoded accesses to the 8259 interrupt controllers, as well as for interrupt acknowledge cycles. It is also driven during the DMA acknowledge cycle to the FDC.
DMA#	93	O	DMA/CACP as the Bus Master. It is driven low at the end of an arbitration cycle (ARB/GNT# falling) to indicate that the DMA controller has gain control of the Micro Channel. It is negated during arbitration cycles, and is negated when either the CPU or slot-resident master owns the bus. It is also negated during refresh cycles.
TO#	42	O	Bus Timeout signal. The DMA/CACP also issues an NMI to the CPU in response to the Bus timeout, and forces an arbitration cycle.
V_{DD}	16, 34, 47, 51, 66, 78, 86, 101, 115, 131		Power
V_{SS}	1, 14, 22, 33, 50, 54, 67, 82, 99, 116, 123		Ground
NC	15, 17, 32, 70, 83, 100, 106, 132		No Connect
PU	68, 77, 80, 97, 102, 103, 105, 109–112	I	Pull Up
PU2	96	I	Pull Up. This input must have its own pullup.

82307 DMA/Micro Channel Arbitration Controller



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NOTES:
Important!! No other node allowed to share pull-up with PU2.
NC = No Connect
PU = Pull-Up
—Pull-Up Resistor Valve = 2K to 10K
—No more than three nodes to a single pull-up resistor.

82307 PARAMETRICS

ABSOLUTE MAXIMUM RATINGS*

Case Temperature under Bias .... −40°C to +85°C
Storage Temperature ..... −65°C to +150°C
Voltage to Any Pin with Respect to Ground ..... −0.3V to (V_{CC}+0.3)V
DC Supply Voltage (V_{CC}) ..... −0.3V to +7.0V
DC Input Current ..... ±10 mA

**Notice: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

NOTICE: Specifications contained within the following tables are subject to change.

D.C. CHARACTERISTICS

T_C = 0°C to +70°C, V_{CC} = 5V ±10%

Symbol	Parameter	Min	Max	Units	Conditions
V_{IL}	Input Low Voltage		0.8	V	
V_{IH}	Input High Voltage	2.0		V	
V_{IL}	Input Low Voltage		0.8	V	CLK1, CLK2, CLK3
V_{IH}	Input High Voltage	V_{CC} − 0.8		V	CLK1, CLK2, CLK3
V_{OL}	Output Low Voltage		0.4	V	I_{OL} = 2 mA
V_{OH}	Output High Voltage	2.4		V	I_{OH} = 2 mA
I_{CC}	Power Supply Current		180	mA	No DC Loads
I_{LI}	Input Leakage Current		±10	μA	$V_{SS} < V_{IN} < V_{CC}$
I_{OZ}	Tri-State Output Leakage Current		±10	μA	$V_{SS} < V_{OUT} < V_{CC}$

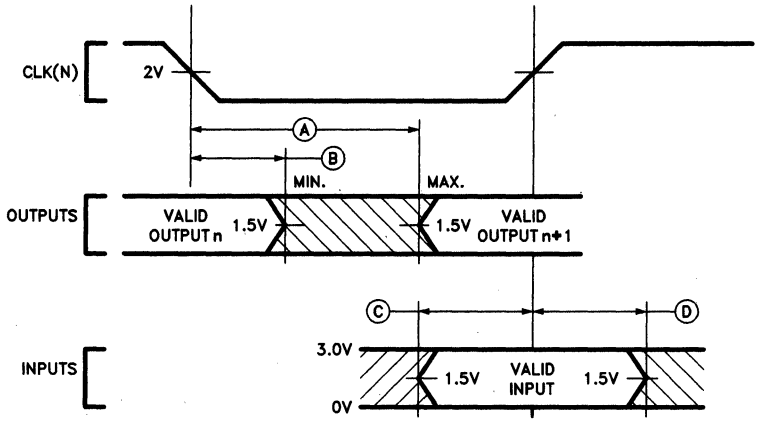
82307 DMA CONTROLLER A.C. SPECS

T_C = 0°C to +70°C, V_{CC} = 5V ±10%

Symbol	Parameter	Kit 16 MHz		Kit 20 MHz		Kit 25 MHz		C_L (pF)	Notes
		Min	Max	Min	Max	Min	Max		
T1	CLK1, CLK2, CLK3 LOW TIME	15		15		14			
T2	CLK(N) NON-OVERLAP TIME	4		4		0			
T3	RESET(IN), NPRESET(OUT) PULSE WIDTH	500		500		500		50	
T4	TO# PULSE WIDTH	60		60		60		50	
T5	A23–A0, PM/IO#, BHE#, REFRESH# DELAY	4	35	4	35	4	32	75	
T6	A23–A0, PM/IO#, BHE#, STATUS FLOAT DELAY	4	40	4	40	4	40	75	
T7	WRITE DATA VALID DELAY	2	35	2	35	2	28	75	
T8	WRITE DATA FLOAT DELAY	2	40	2	35	2	35	75	
T9	READ DATA SETUP TIME	15		13		11			
T10	READ DATA HOLD TIME	4		4		4			
T11A	STATUS VALID DELAY (TPHL)	4	25	4	25	4	20	75	
T11B	STATUS VALID DELAY (TPLH)	2	35	2	35	2	30	75	
T12	ADDR-TO-STATUS SETUP	35		27		22		75	
T13A	PRDYI# SETUP TIME	25		20		20			2
T13B	PRDYI# SETUP TIME	8		8		8			2
T14	PRDYI# HOLD TIME	5		5		5			2
T15	A15–A0, PM/IO# SETUP TIME	35		35		35			
T16	A15–A0, PM/IO# HOLD TIME	10		10		10			
T17	STATUS SETUP TIME	26		26		24			
T18	STATUS HOLD TIME	10		10		10			
T19	WRITE DATA SETUP TIME	25		25		25			1
T20	WRITE DATA HOLD TIME	25		25		25			1
T21	READ DATA VALID DELAY	2	100	2	100	2	100	75	
T22	READ DATA FLOAT DEALY	8	40	8	35	8	35	75	
T23	HOLD DELAY	2	35	2	32	2	32	50	
T24	ARB/GNT# DELAY FROM EOT	30		30		30		50	
T25	ARB/GNT# PULSE WIDTH	300		300		300		50	
T26	OARB3–OARB0 DELAY		32		32		32	50	
T27	OPMT# INACTIVE DELAY		35		35		35	50	
T28	BSTO# DELAY	2	40	2	40	2	40	50	
T29	TC# DELAY	2	36	2	33	2	33	50	
T30	FDACK#, DMA# DELAY	2	40	2	40	2	40	50	
T32	LBEN# VALID DELAY	0	30	0	25	0	22	50	
T33	CDEN# VALID DELAY	2	35	2	35	2	35	25	
T34	NPCS# DELAY	2	65	2	65	2	50	50	
T35	59CS# VALID DELAY	8	42	8	42	8	42	50	
T36	PBA# DELAY	2	34	2	34	2	30	50	

NOTE:
1. Write data is sampled on different clock edges by different DMA internal registers. T19 is speced relative to the earliest sampling edge, while T20 is relative to the latest edge.
2. PRDYI# must be inactive and stable according to these specs at all DMA state boundaries except at the end of the TC boundary at which the cycle is to be terminated.

DRIVE LEVELS AND MEASUREMENT POINTS FOR A.C. SPECIFICATIONS

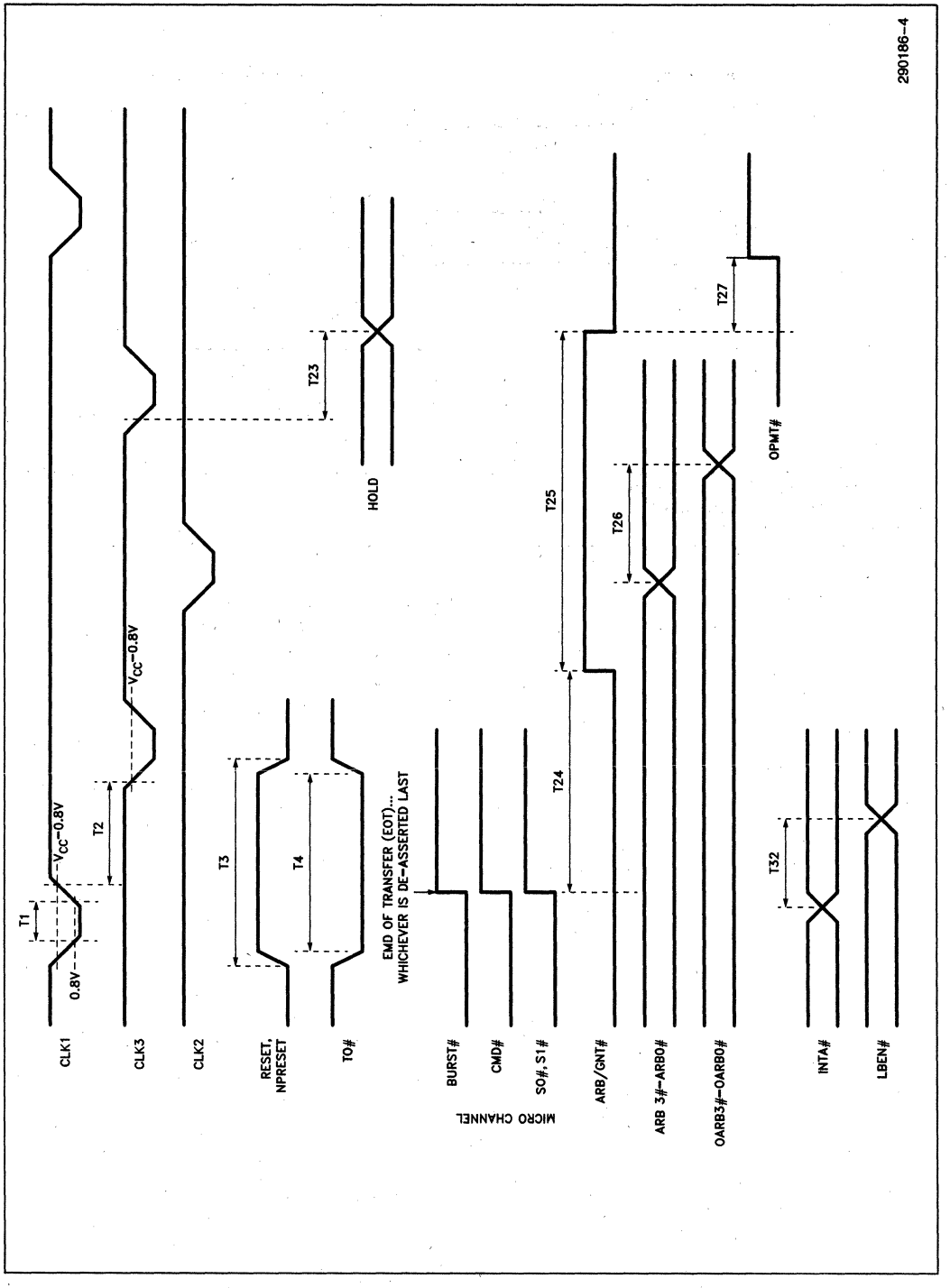


290186-3

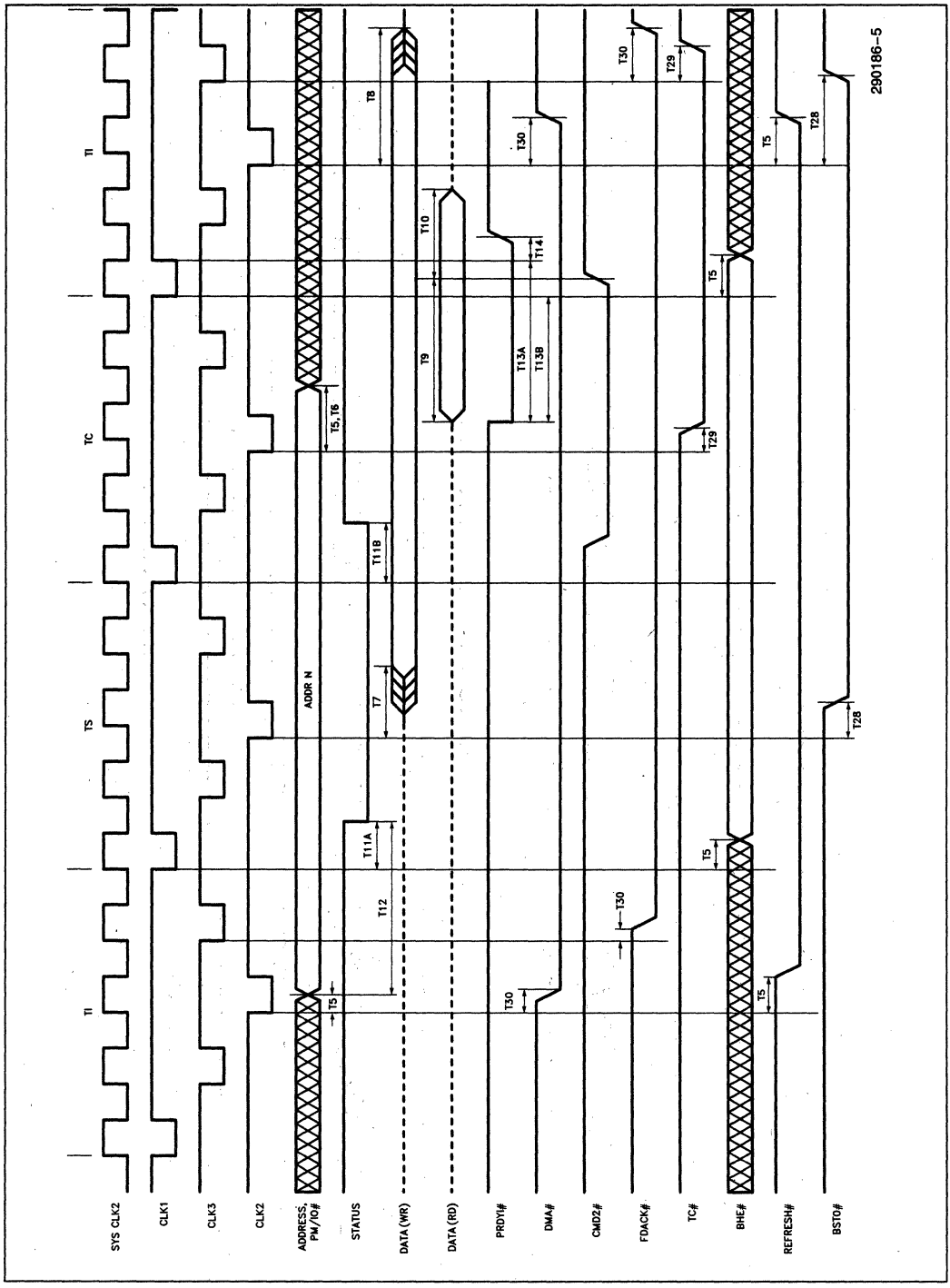
LEGEND:
A. Maximum Output Delay Specification.
B. Minimum Output Delay Specification.
C. Minimum Input Setup Specification.
D. Minimum Input Hold Specification.

Input waveforms have tr ≤ 2.0 ns from 0.8V to 2.0V.

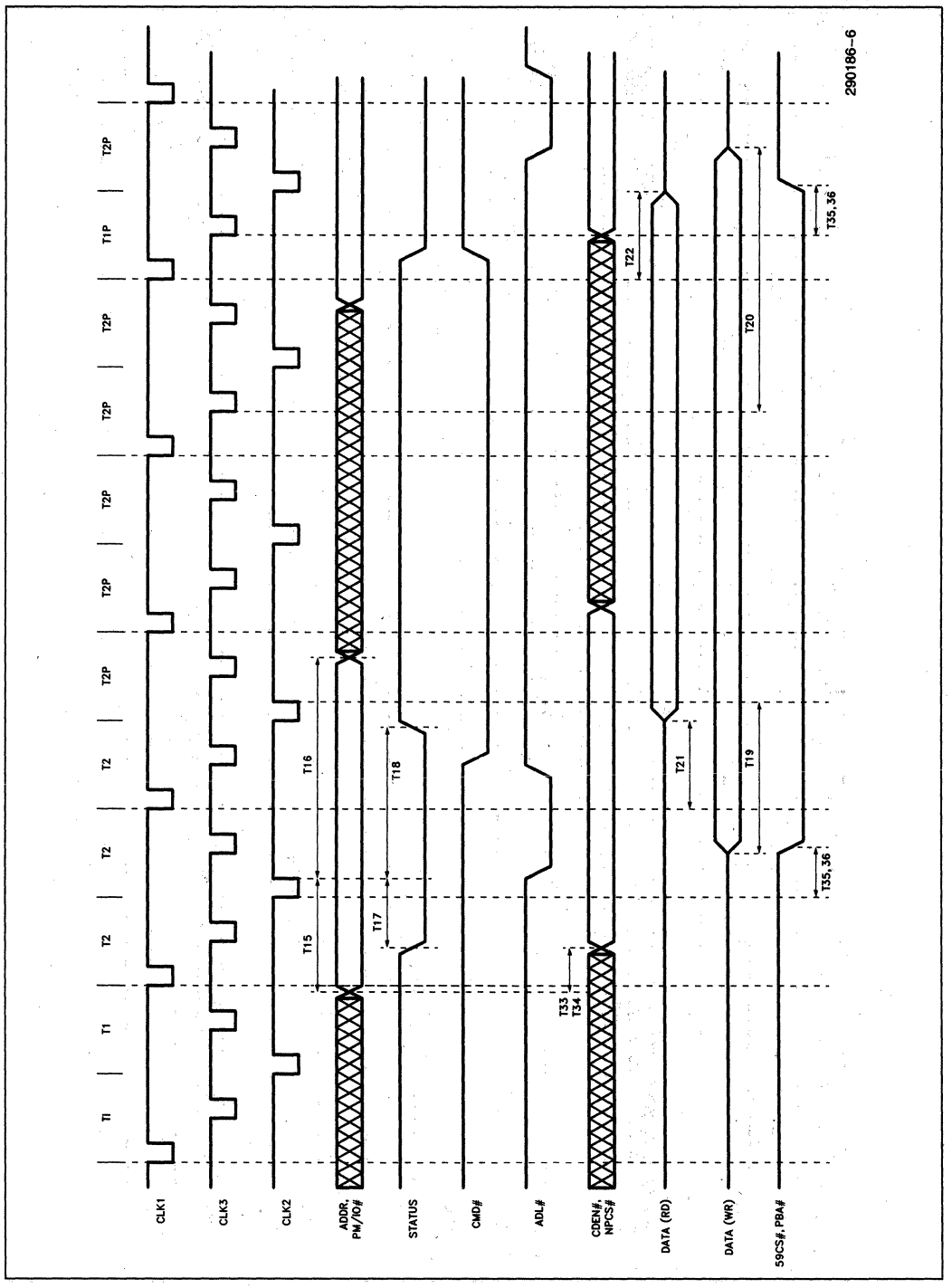
SYSTEM TIMINGS



DMA ... MASTER MODE



DMA . . . SLAVE MODE



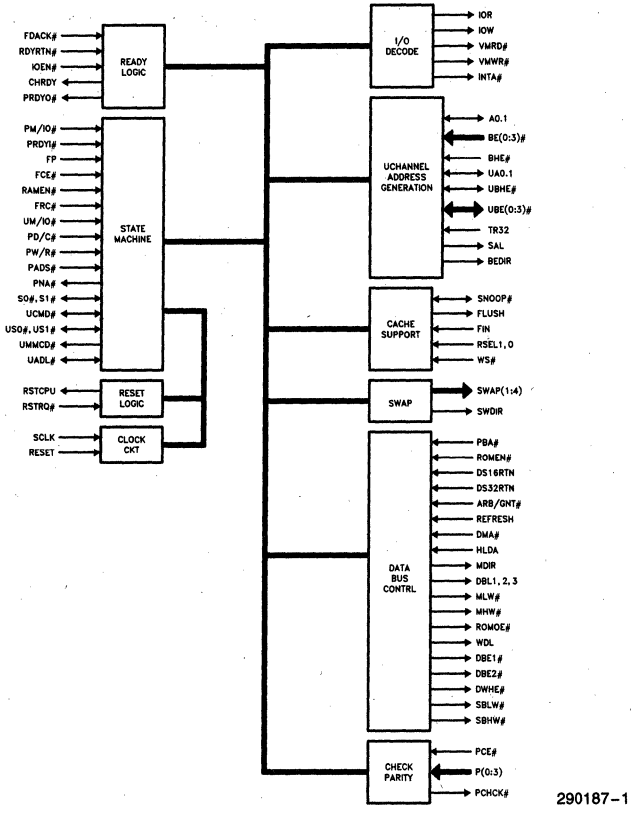
82308
Micro Channel BUS CONTROLLER

- **Micro Channel Compatible Bus Control**
- **Supports 8-, 16- or 32-Bit Data Transfers on the Micro Channel**
- **Optional Hardward Enforced I/O Recovery Mechanism**
- **Cache Controller (82385) Interface to Maximize Performance for 80386 Based Systems**
- **Low Power CHMOS Technology**
- **100-Pin Plastic Quad Flat Pack Packaging**
  (See Packaging Spec., Order # 231369)

The 82308 Micro Channel Bus Controller is the complementary device to the 82309 Address Bus Controller. It is designed to facilitate data transfers between the Microprocessor, DMA, Memory and Micro Channel bus. It generates the appropriate data conversion and alignment control signals to implement an external byte swap mechanism for transferring data of equal and different widths.

The 82308 Bus Controller generates all control signals necessary to run Micro Channel Memory and I/O Bus cycles for both 80386 and 80386SX processors.

To implement the highest performance 80386 based system with the 82385 cache controller, the Bus Controller features special cache hardware interface signals.



290187-1

October 1988
Order Number: 290187-001

STATE MACHINE

The primary purpose of the state machine is to generate the Micro Channel signals for processor and DMA cycles. These Micro Channel signals are: S0#, S1#, ADL#, MMCCMD# and CMD#. The state machine also generates the PNA# signal required by the 386 CPU and generates the DMA S0# and S1# based on the 386 processor status.

DATA TRANSFER

The 82308 Bus Controller directs the transfer of data between the 32-bit 80386 bus and 32-bit, 16-bit or 8-bit devices on the Micro Channel. For 16-bit transfers initiated by the 80386SX or DMA, the Bus Controller provides the control signals to facilitate transfers to 16-bit or 8-bit devices on the Micro Channel data bus and vice versa.

In addition to providing the transceiver direction, latch, and enable signals, the Bus Controller manipulates Address signals for the DMA and Micro Channel. For example, a 32-bit access to an 8-bit device is broken into four cycles, and the BC automatically sequences A1 and A0 in each cycle.

The 82308 Bus Controller also supports the ROM BIOS by providing the output enable for the BIOS based on the decoded BIOS address signal from the Address Bus Controller (ROMEN#).

RESET DETECT

The reset detect logic generates a synchronous CPU reset signal based on any of the following events:

— An active low-pulse on the RC# input to the Bus Controller

— Processor Shutdown Condition based on the Processors' status signals

— Power-up condition as determined by the RESET input.

I/O SUPPORT

The 82308 Bus Controller generates Memory and I/O Read and Write signals for devices on the motherboard. It also generates the Interrupt Acknowledge signal.

The Bus Controller extends motherboard device accesses by de-asserting CHRDY until a read or write strobe is generated. This gives the peripheral device an opportunity to extend the cycle even further if required by driving its own CHRDY inactive after it detects the read or write strobe. The motherboard device decode is performed by the 82309 Address Bus Controller.

CACHE SUPPORT

The 82308 Bus Controller supports 82385 Cache Controller interface signals to allow maximum system performance in cache based 386 systems.

CACHE FLUSH

The Bus Controller generates a synchronous flush output signal (FLUSH) to the cache controller whenever the flush request (FIN) is generated.

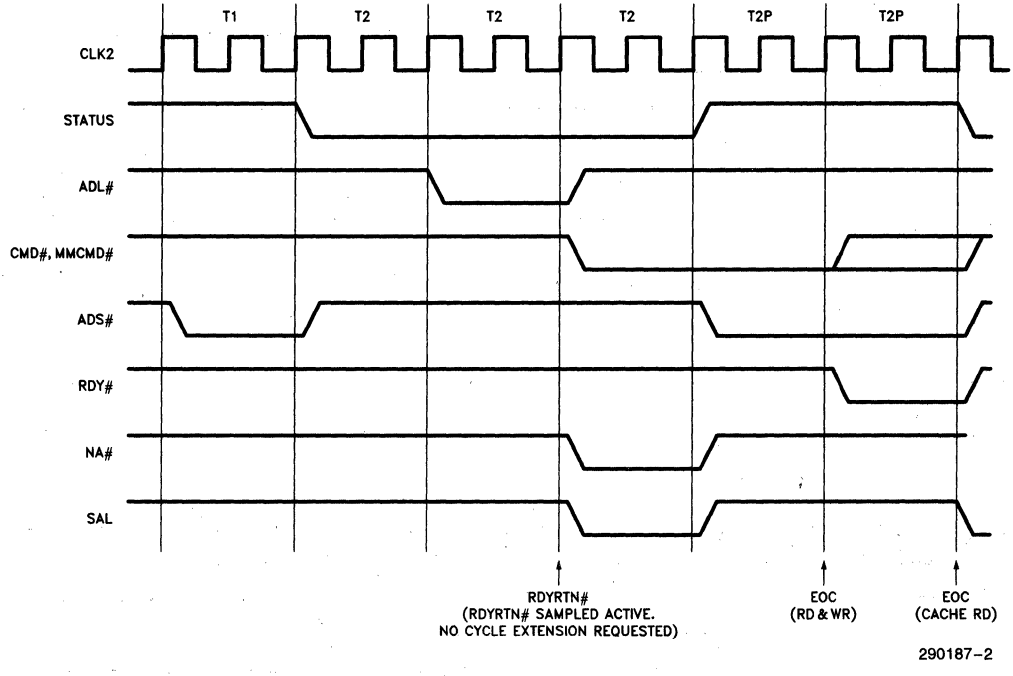
SNOOP STROBE

The Snoop Strobe output of the 82308 Bus Controller is a synchronized strobe indicating a valid address during non-processor write cycles. It is compatible with the 82385 cache controller's bus watching mechanism.

HARDWARE ENFORCED I/O RECOVERY

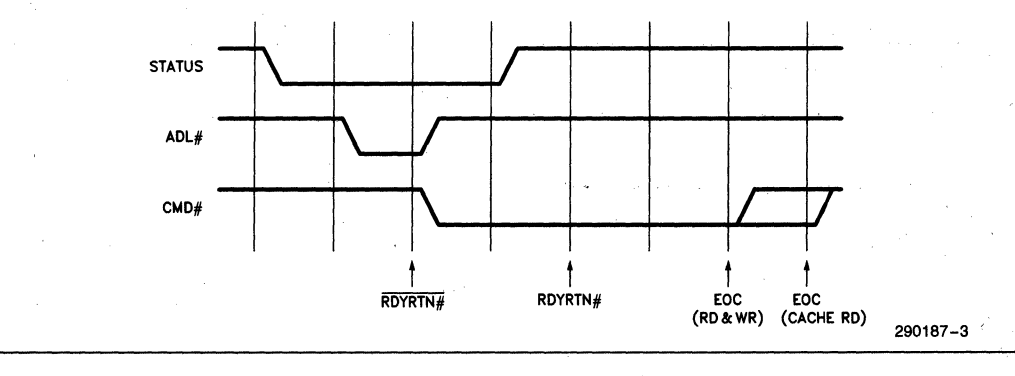
Certain I/O devices require a minimum delay between consecutive accesses. Typically, software loops are executed in the I/O routine to force the delay, but software loops cannot guarantee minimum delay times in all cases. The 82308 Bus Controller provides the option of enforcing I/O recovery in hardware. This mechanism is controlled by two inputs (RSEL1 and RSEL0), which select one of four possible minimum I/O recovery times. At the end of a CPU initiated I/O cycle, an internal timer is triggered, and the 82308 will not allow the next I/O access to proceed until the timer has timed out. The specific functioning of RSEL1 and RSEL0 is detailed in the pin definitions and A.C. Timing specifications.

16 MHz CPU DEFAULT CYCLE (FP = 0)

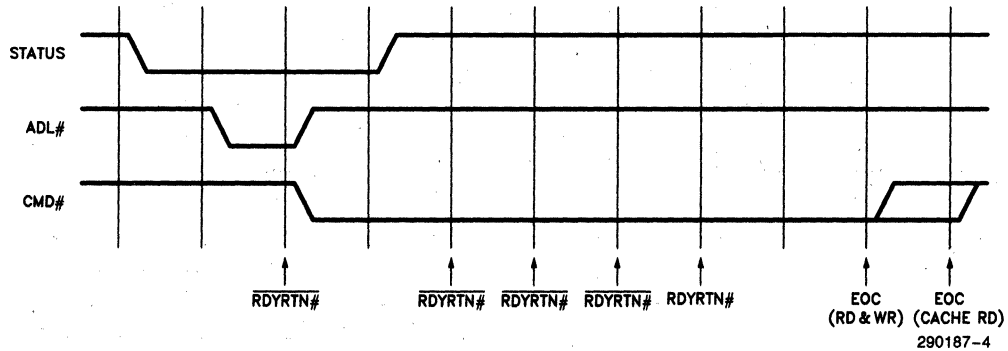


NOTE:
MMCCMD# only driven in CPU initiated cycles.
EOC = End Of Cycle.

16 MHz CPU SYNCHRONOUS EXTENDED

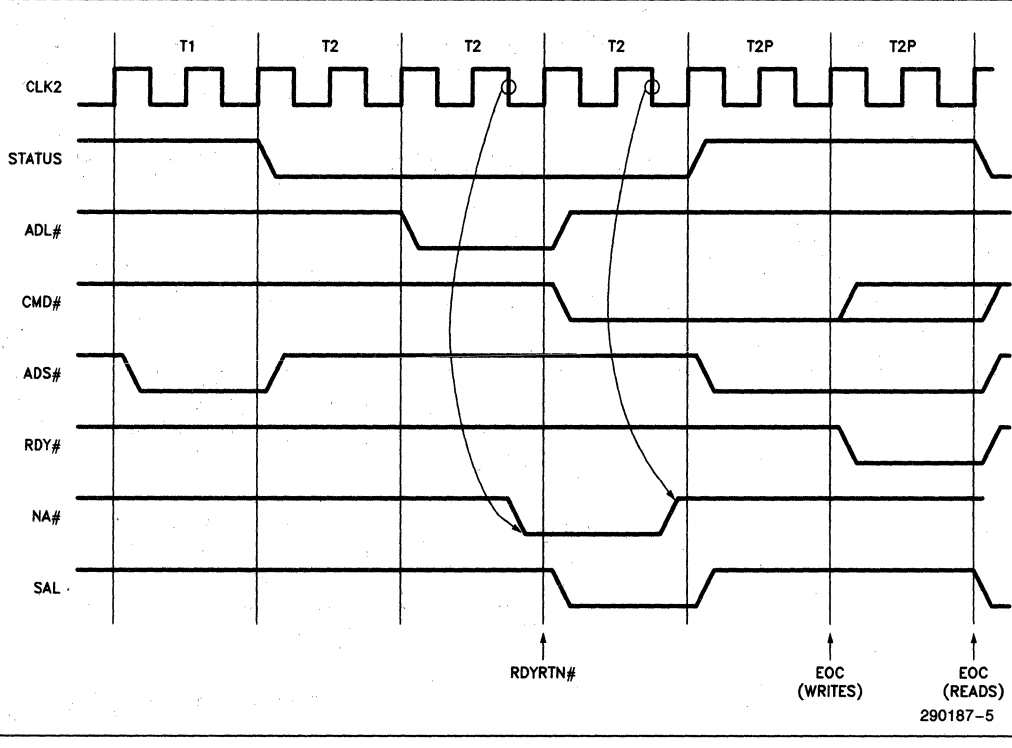


16 MHz CPU ASYNCHRONOUS EXTENDED

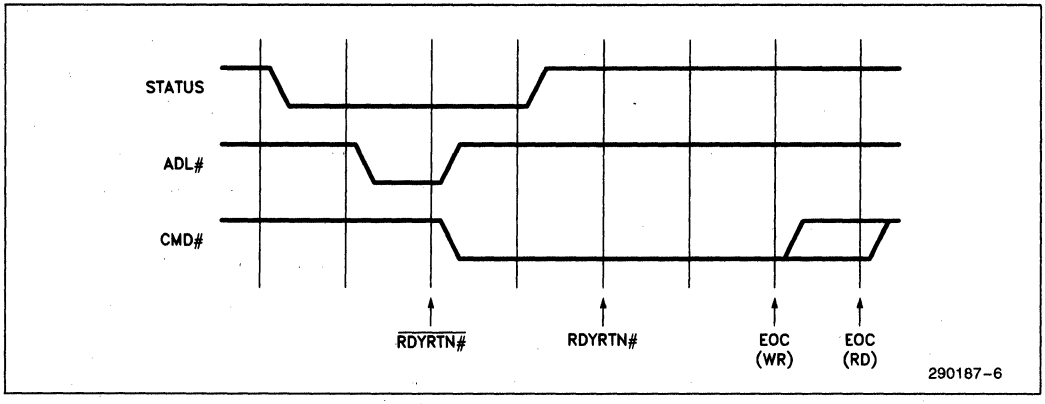


EOC = End Of Cycle

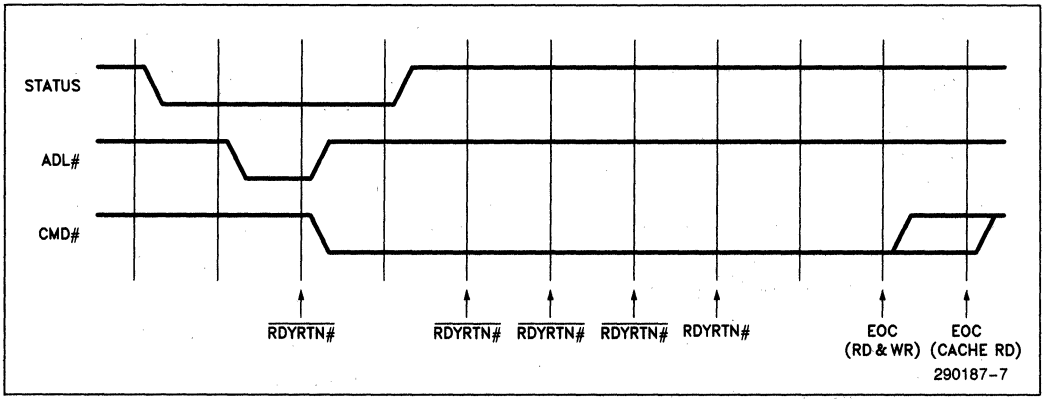
20 MHz CPU DEFAULT CYCLE (FP = 1)



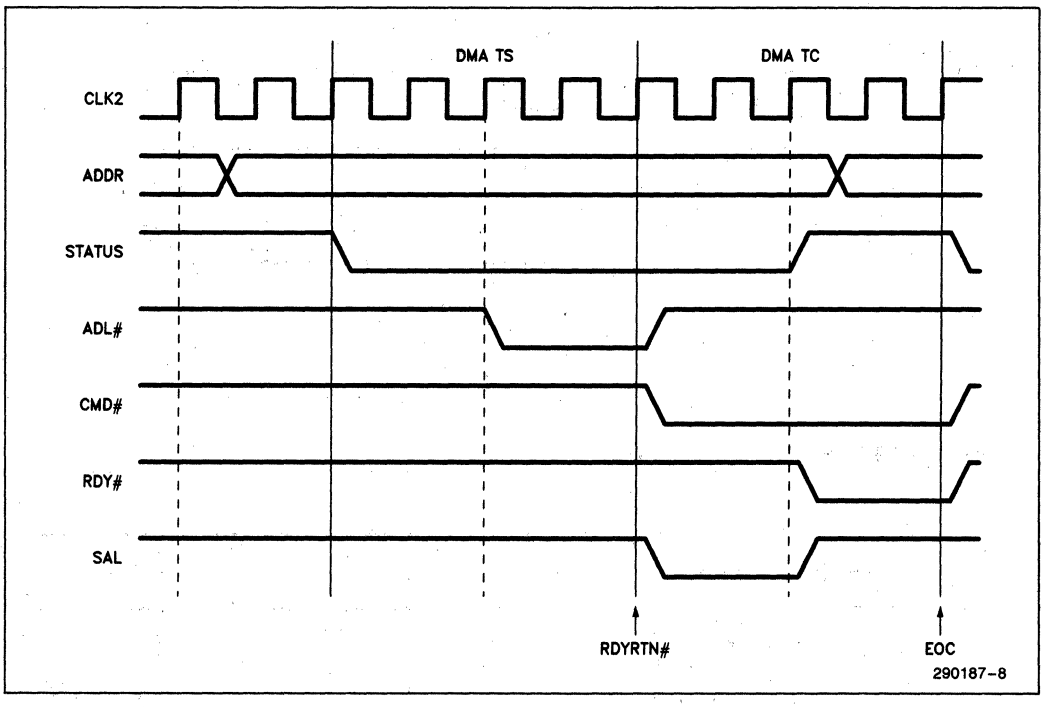
20 MHz CPU SYNCHRONOUS EXTENDED



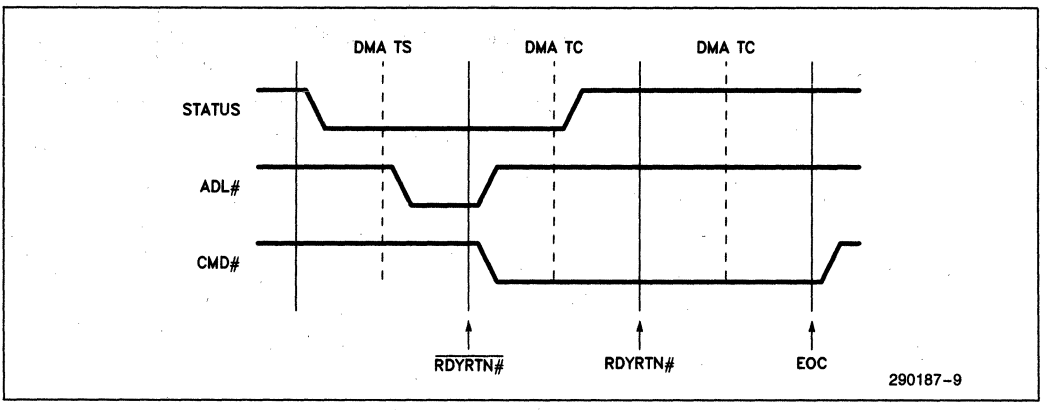
20 MHz CPU ASYNCHRONOUS EXTENDED



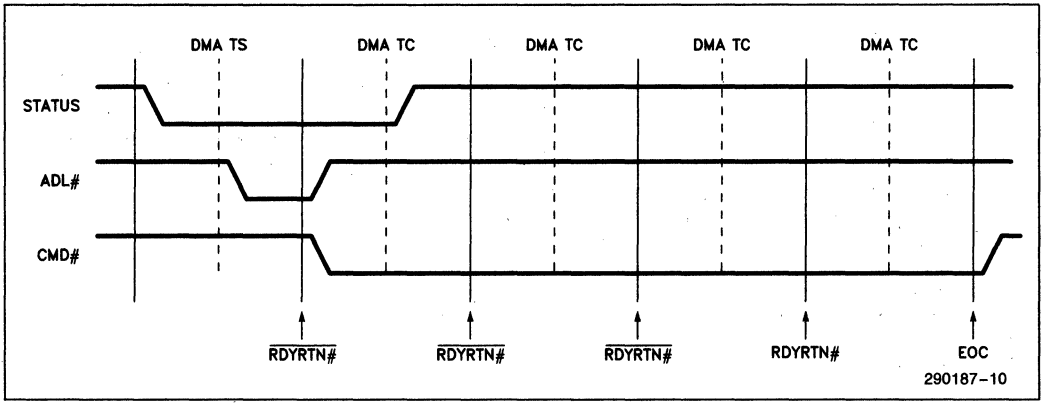
DMA DEFAULT CYCLE



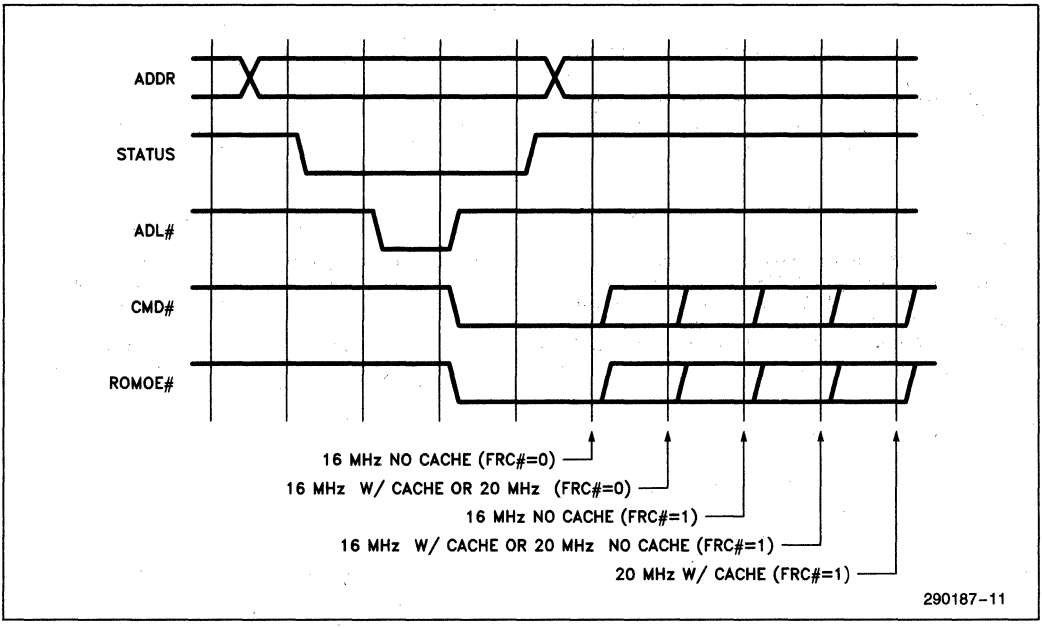
DMA SYNCHRONOUS EXTENDED



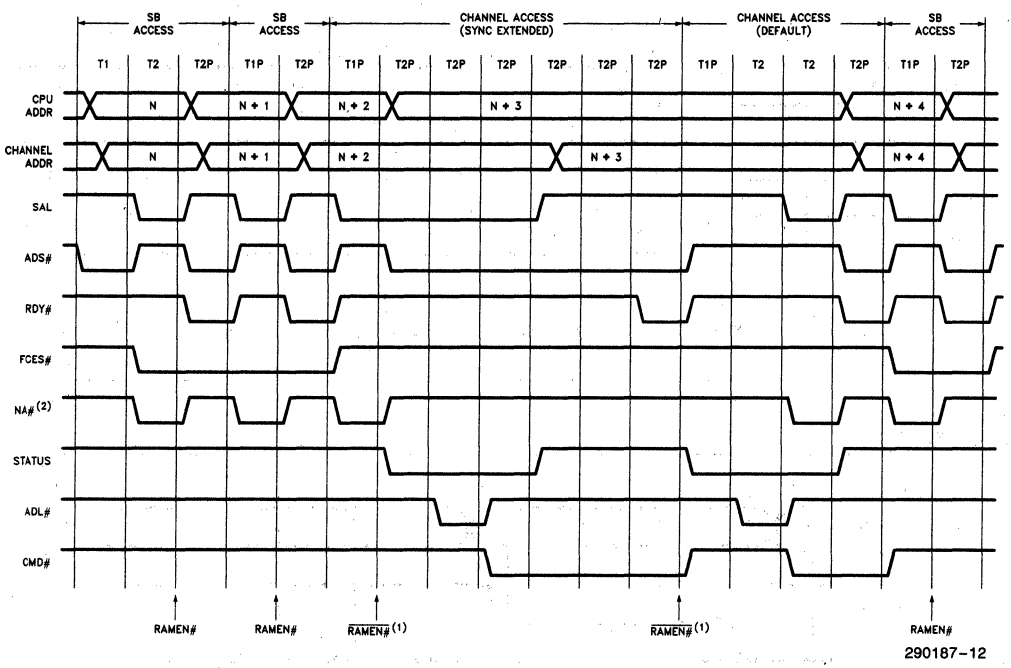
DMA ASYNCHRONOUS EXTENDED



ROM CYCLES



CPU SYSTEM BOARD MEMORY/Micro Channel MEMORY ACCESSES



290187-12

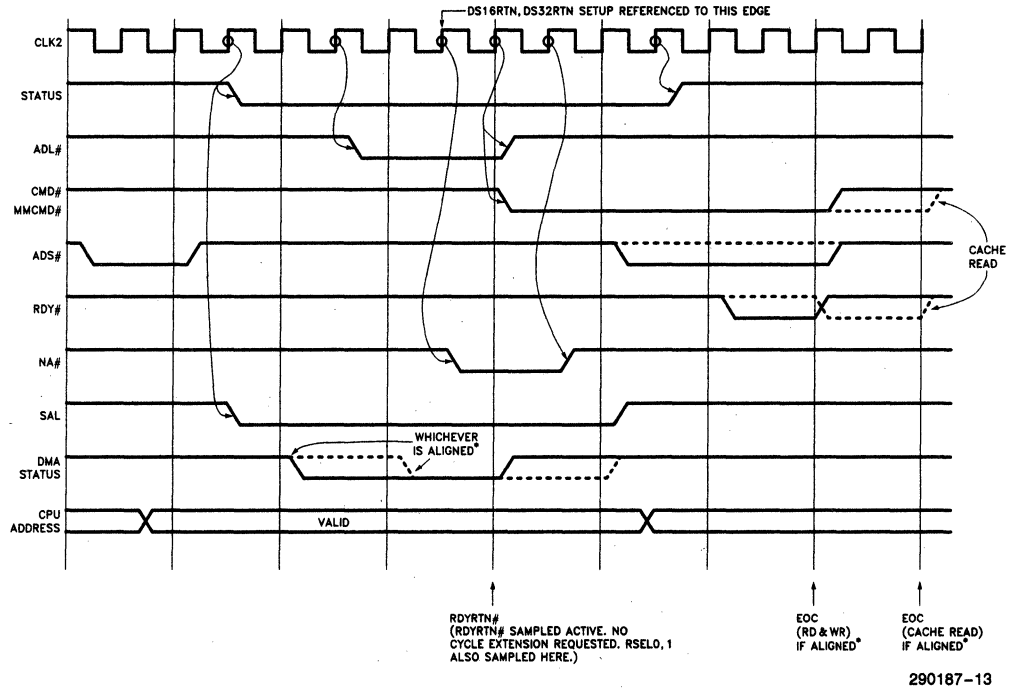
NOTES:

1. RAMEN# distinguishes between system board and channel memory accesses. The BC must wait for RAMEN# to resolve before driving STATUS in a channel access. Thus, in non-pipelined channel accesses or pipelined channel accesses in which the ABC sees only one state of pipelined address, the BC delays starting the channel access until the end of the T1P or first T2 state.
2. In memory cycles the BC must drive NA# before RAMEN# resolves in order to sustain 0WS pipelined page hits.

82308HS-25 MICROCHANNEL BUS CONTROLLER TIMING DIAGRAMS

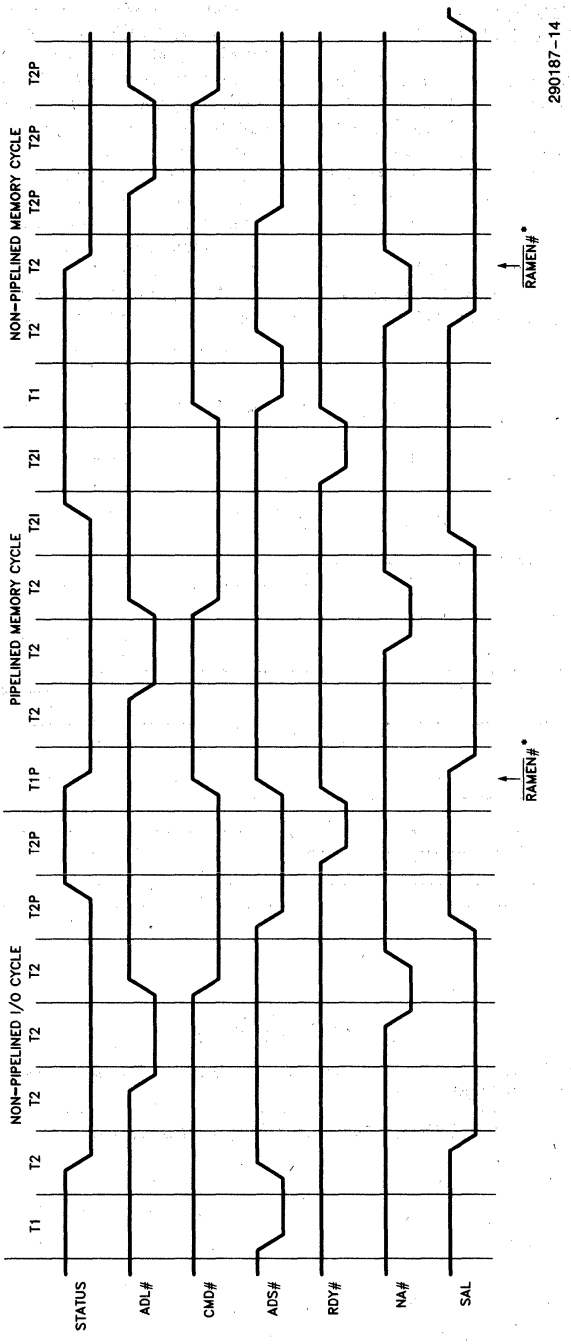
The 82308HS-25 provides Microchannel Bus Control for 25 MHz 80386 systems. It is 100% function and pin compatible with the 82308-16/20 Bus Controller, so minimal system re-design is required to upgrade current 16 MHz or 20 MHz systems to 25 MHz. (Note that the 82308HS-25 FP input must be tied high.)

Although the 82308HS-25 is functionally identical to the 82308-16/20, its internal state machine and external timing behavior are modified to insure full compatibility with published Microchannel timings at the increased CPU frequency, and to accommodate 25 MHz system and component specifications. This addendum to the 82308-16/20 data sheet provides the basic timing diagrams for the 82308HS-25, highlighting the specific clock edges that either sample specific inputs, or else trigger specific outputs. All AC specification output delays are referenced to the "causal" clock edge, and input setup/hold times are referenced to the sampling clock edge. Any signal not specifically addressed in these diagrams behaves just as it does in the 82308-16/20. (Note in the AC specifications that notes numbered 21 or greater apply only to the 82308HS-25.)



*If necessary, a wait state is added to CPU I/O cycles to align them with even DMA state boundaries. (Recall that DMA states are 4 clock phases wide while 80386 states are only 2 phases.)

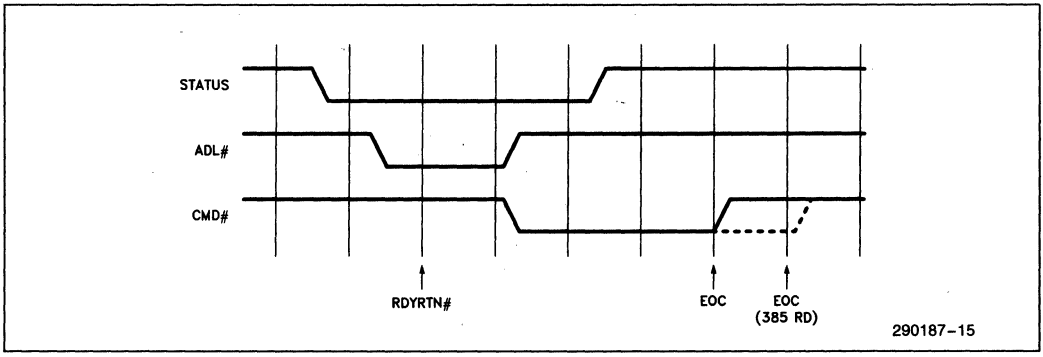
82308HS 25 MHz CPU Default I/O Cycle



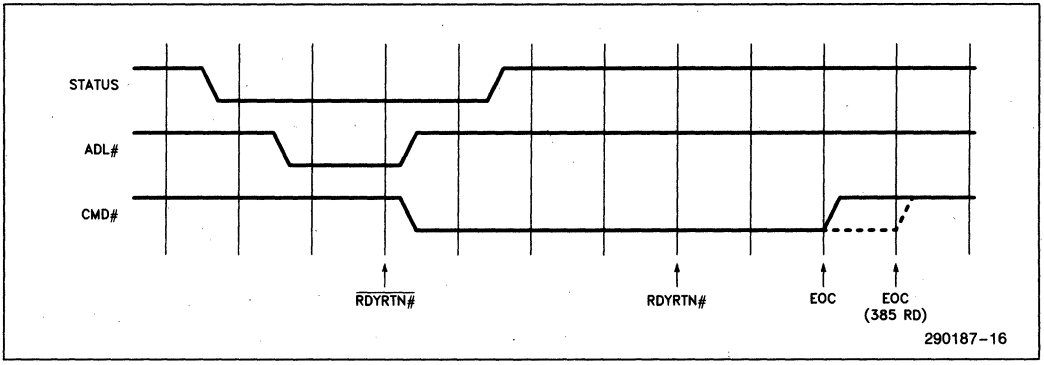
*Ramen# distinguishes between (non-broadcast) system board and channel memory accesses. (The 82308-25 samples Ramen# and Romen# on the phase 2 clock edge.) The BC must wait for Ramen# to resolve "not true" before driving status in a channel access. Thus, in a non-piplined channel memory access, the BC delays starting the channel cycle until after the first T2 state.

82308HS 25 MHz CPU Default Micro Channel Cycles

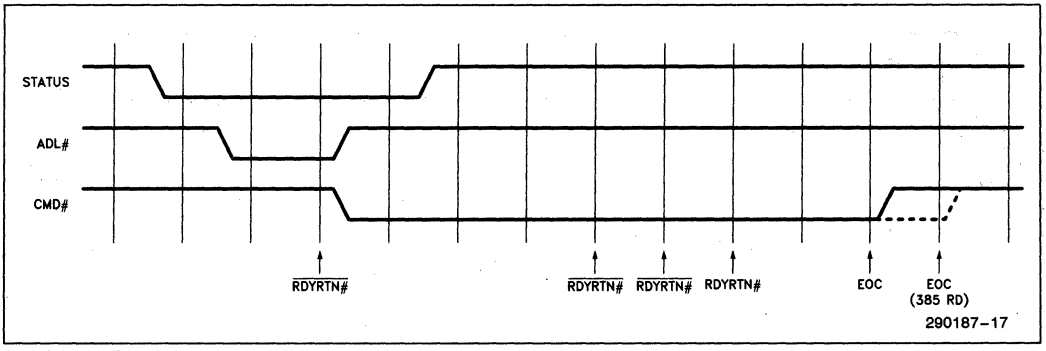
82308HS 25 MHz CPU EXTENDED CYCLES



Default

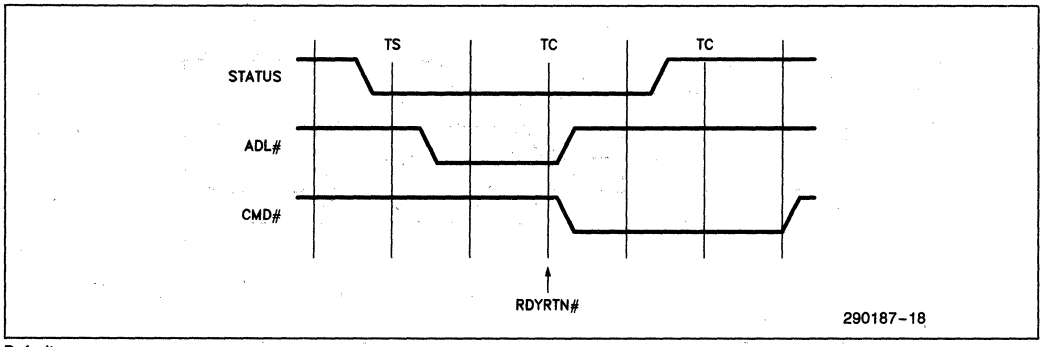


Synchronous Extended

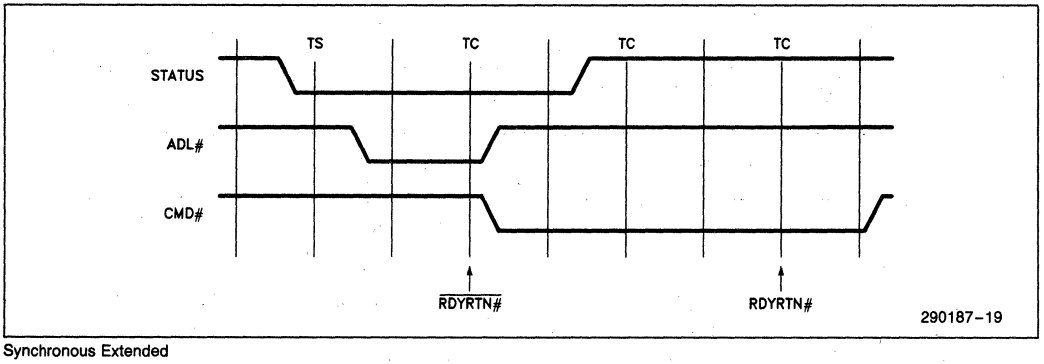


Asynchronous Extended

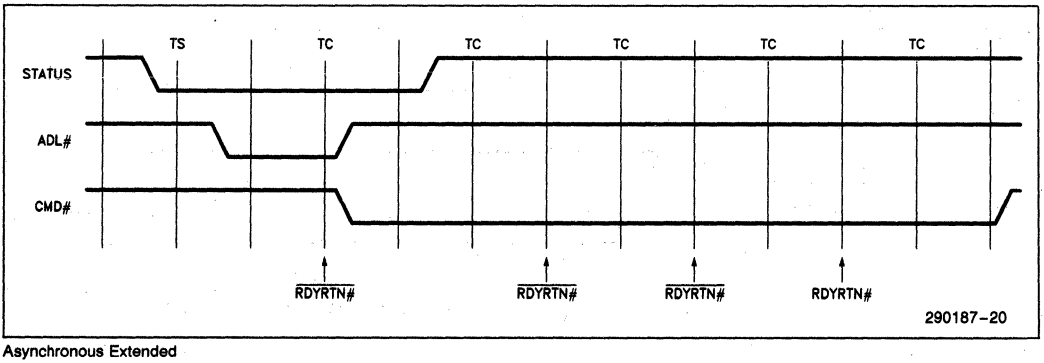
82308HS 25 MHz DMA EXTENDED CYCLES



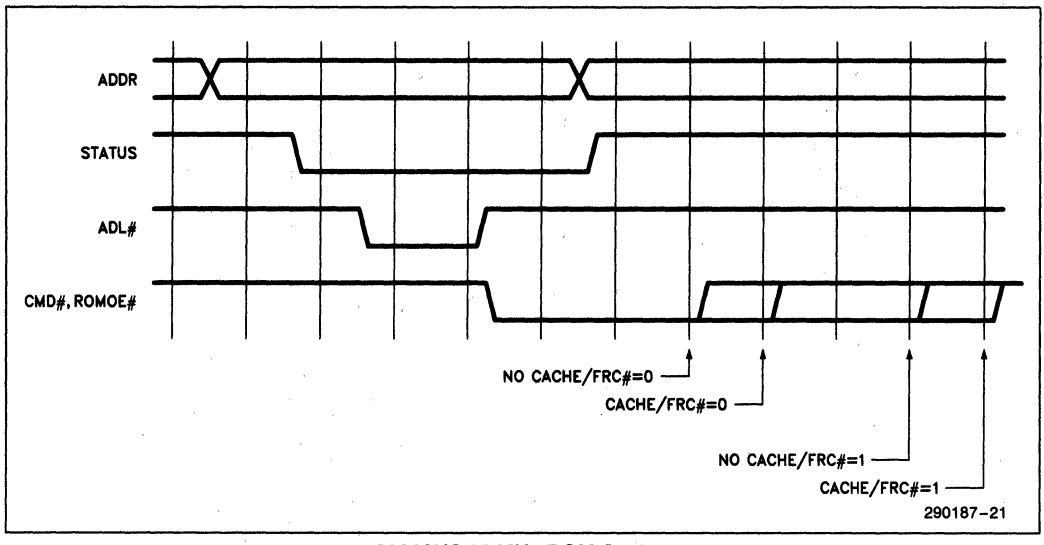
Default



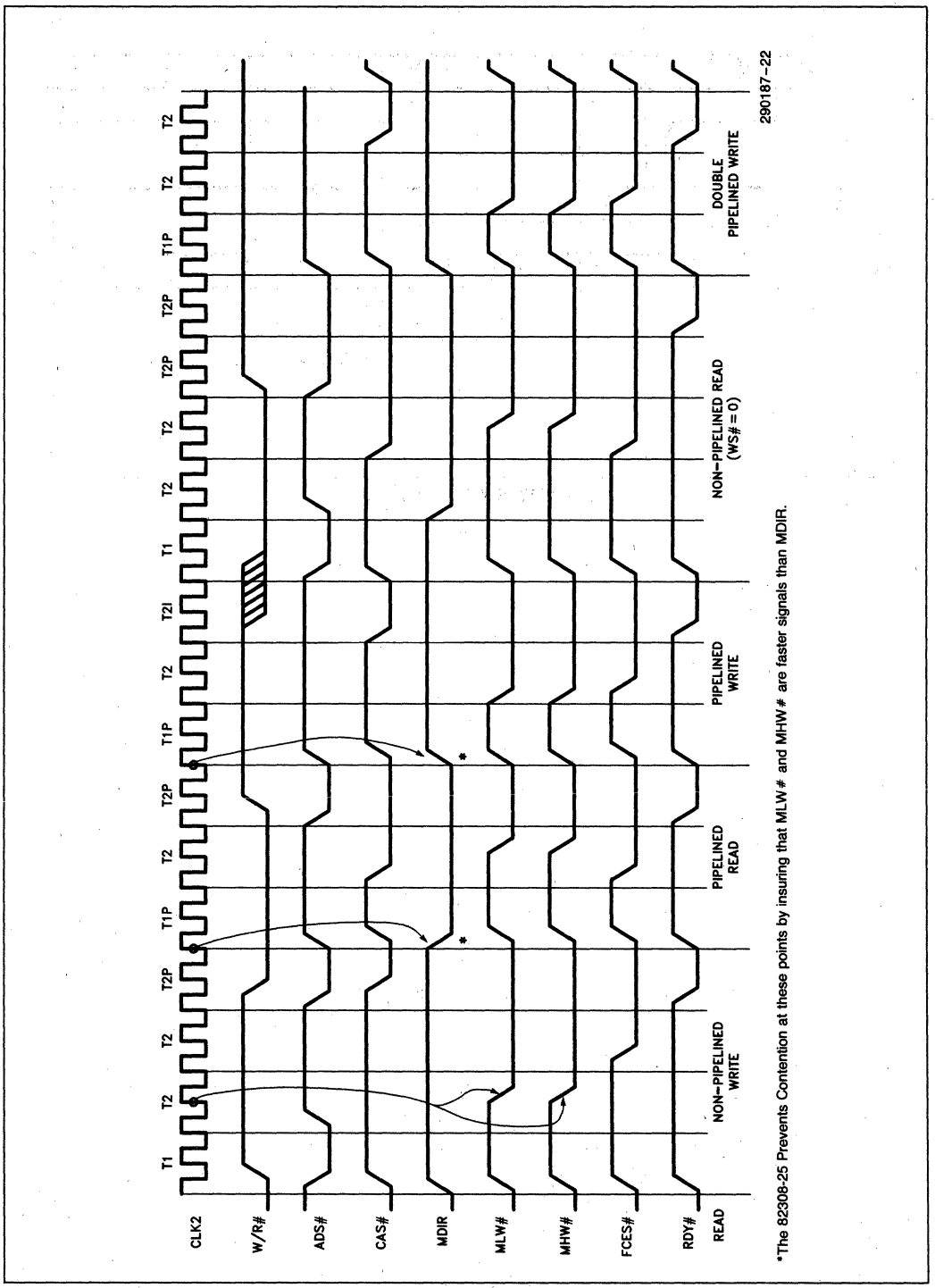
Synchronous Extended



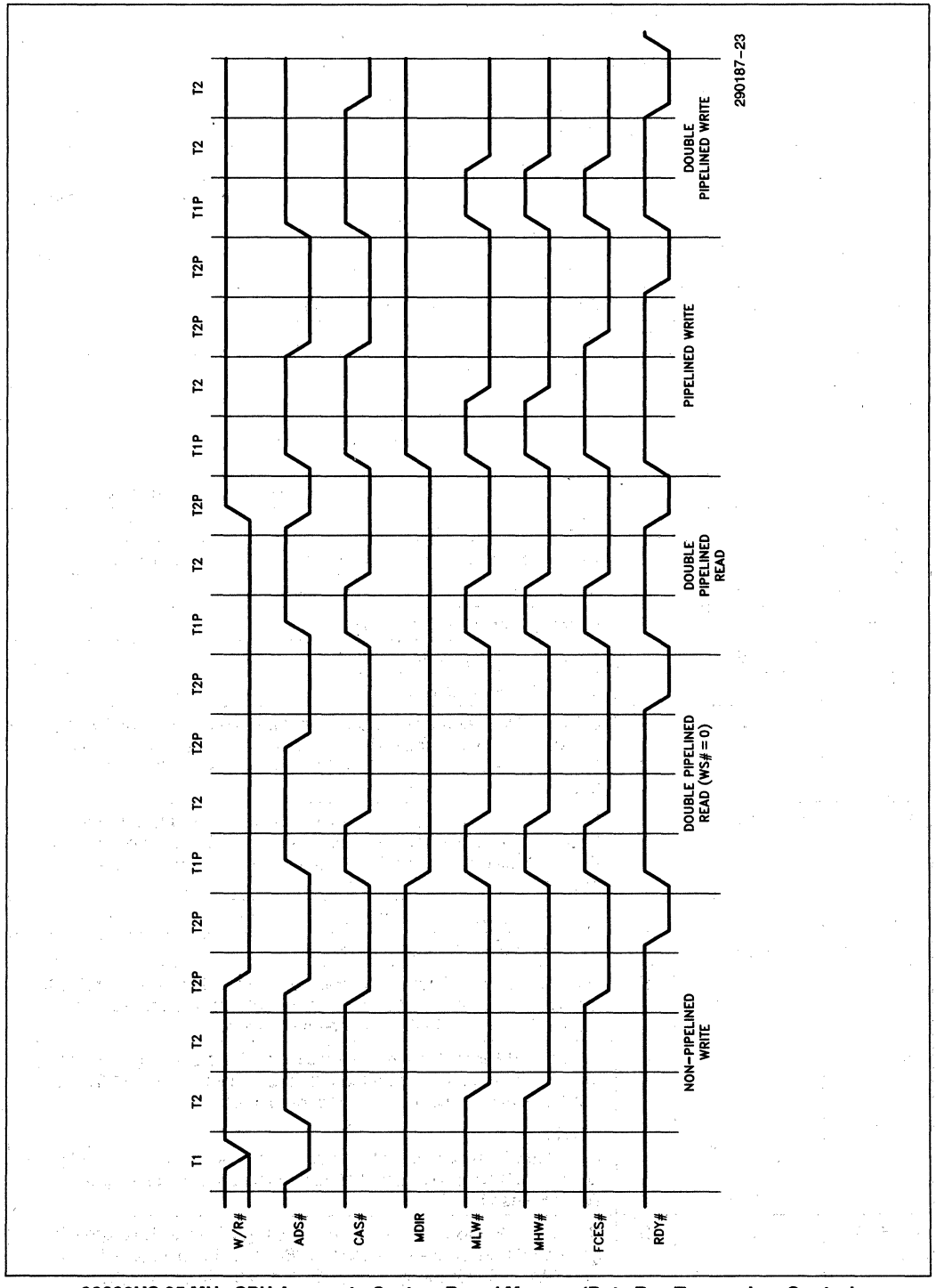
Asynchronous Extended



82308HS 25 MHz ROM Cycles



82308HS 25 MHz CPU Access to System Board Memory/Data Bus Transceiver Control



82308HS 25 MHz CPU Access to System Board Memory/Data Bus Transceiver Control

82308 Micro Channel Bus Controller Pin Definitions

Signal Name	Pin Number	I/O	Description
RSTRQ#	87	I	Logical NOR of 8042 pin 20 and LCS ALTRESET to initialize reset (Software reset).
RSTCPU	91	O	Microprocessor Reset.
PCE#	82	I	Enable Parity Check from Memory Encoding Register Bit 0. This input should be tied low for a model 60 system. (Parity check always enabled.)
PO	83	I	Parity Error from DRAM for bits 0–7.
P1	84	I	Parity Error from DRAM for bits 8–15.
P2	85	I	Parity Error from DRAM for bits 16–23.
P3	86	I	Parity Error from DRAM for bits 24–31.
PCHCK#	90	O	Parity Error Output.
IOEN#	79	I	Active low signal from the Address Bus controller indicating a motherboard I/O device address.
CHRDY	92	O	Input to the Channel Ready Return logic to extend the current cycle.
FDACK#	81	I	FDC DACK# signal.
IOR	97	O	I/O Read signal for motherboard devices (8042, 8259, etc.).
IOW	98	O	I/O Write signal for motherboard devices.
VMWR#	96	O	Memory write strobe to the VGA.
VMRD#	95	O	Memory read strobe to the VGA.
INTA#	94	O	INTA# Input to the 8259.
A0	9	B	CPU and DMA Address 0. A0 will be driven by the Bus controller based on the byte enable signals when the 386 owns the bus. It is a Bus controller input in an 80386SX system, or when the DMA is master.
A1	10	B	CPU and DMA Address 1. A1 will be driven by the Bus controller based on the byte enable signals when the 386 owns the bus. It is a Bus controller input in an 80386SX system, or when the DMA is master.
BHE#	100	I	Byte High Enable signal from the CPU and DMA.
BE0–3#	11–12, 14–15	I	Byte Enable bits 0–3 from the 80386.
UA0	3	B	Unbuffered Micro Channel Address bit 0. This signal is generated by the bus controller based on the byte enable signals and A0 from the DMA. It is also manipulated by the swap logic.
UA1	4	B	Unbuffered Micro Channel Address bit 1. This signal is generated by the bus controller based on the byte enable signals and A1 from the DMA. It is also manipulated by the swap logic. **NOTE:** For 80386SX systems, UA1 is unconnected, and should be lightly pulled up (10K). The channel A1 is latched along with the upper address lines.)
UBHE#	16	B	Unbuffered Micro Channel System Bus High Enable. This signal is generated from BE0–3# when the 386 owns the bus, or BHE# from the DMA. In 80386SX systems, UBHE# is a reflection of the 80386SX BHE# output.

82308 Micro Channel Bus Controller Pin Definitions (Continued)

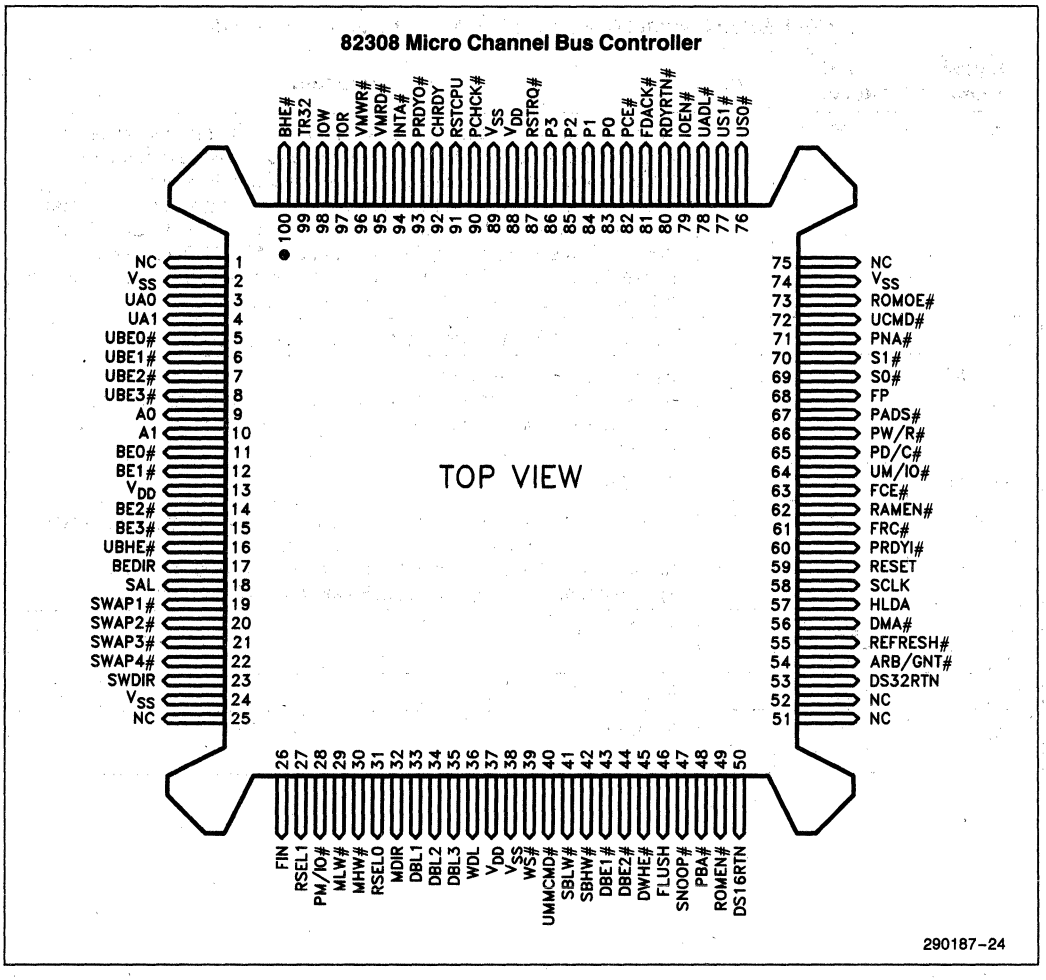
Signal Name	Pin Number	I/O	Description
UBE0–3#	5–8	B	Unbuffered Micro Channel Byte Enable bits 0–3. These byte enable signals are driven by the bus controller when the CPU or DMA is master. (An external PAL is required to generate the channel byte enables on behalf of a 16-bit channel master that requests translation.)
TR32	99	I	Translate 32 from the Micro Channel to indicate 32 bit masters driving BE0–3# (when inactive). (Tie high for 80386SX system.)
SAL	18	O	Latch enable for the system address bus. This signal controls the address latch between the CPU bus and channel.
BEDIR	17	O	Direction control for the UBE0–3# transceiver. It is high when the Bus controller is driving UBE0–3#.
PBA#	48	I	Indicates that the DMA or numeric coprocessor has been selected and is using the local data bus.
ROMEN#	49	I	Decode that inidicates that the BIOS ROM has been selected.
DS16RTN	50	I	Micro Channel Data Size 16 signal.
DS32RTN	53	I	Micro Channel Data Size 32 signal.
ARB/GNT#	54	I	Micro Channel ARB/-GNT status.
REFRESH#	55	I	Refresh Indicator.
DMA#	56	I	Indicates that the DMA owns the bus.
HLDA	57	I	CPU HLDA input. Indicates CPU controls local address and data bus if low.
WDL	36	O	Latch enable signal for latching data bus D0–31 for generating Micro Channel D0–31 signal. Insures Micro Channel write data hold time spec is met.
DBE1#	43	O	Output Enable for driving data on CPU D0–7 onto Micro Channel D0–7 during CPU or DMA writes or Micro Channel DRAM reads.
DBE2#	44	O	Output Enable for driving data on CPU D8–15 onto Micro Channel D8–15 during CPU or DMA writes or Micro Channel DRAM reads.
DWHE#	45	O	Output Enable for driving data on CPU D16–31 onto Micro Channel D16–31.
SBLW#	41	O	Output enable for driving data on Micro Channel D0–15 onto CPU D0–15.
SBHW#	42	O	Output enable for driving data on Micro Channel D16–31 onto CPU D16–31.
MDIR	32	O	Direction control for transferring data between the CPU Data Bus and the DRAM memory data bus.
MLW#	29	O	Output enable for the transceiver between the CPU data bus D0–15 and the DRAM memory data bus.
MHW#	30	O	Output enable for the transceiver between the CPU data bus D16–31 and the DRAM memory data bus.
ROMOE#	73	O	Output Enable signal for the BIOS ROMs.
SWAP1#	19	O	Transceiver enable for transferring data between Micro Channel Data Bus 0–7 and 8–15.

82308 Micro Channel Bus Controller Pin Definitions (Continued)

Signal Name	Pin Number	I/O	Description
SWAP2#	20	O	Transceiver enable for transferring data between Micro Channel Data Bus 0–7 and 16–23.
SWAP3#	21	O	Transceiver enable for transferring data between Micro Channel Data Bus 8–15 and 24–31.
SWAP4#	22	O	Transceiver enable for transferring data between Micro Channel Data Bus 0–7 and 24–31.
SWDIR	23	O	Direction control for Micro Channel Data Bus transceivers.
DBL1	33	O	Latch enable for latching Micro Channel Data Bus 0–7.
DBL2	34	O	Latch enable for latching Micro Channel Data Bus 8–15.
DBL3	35	O	Latch enable for latching Micro Channel Data Bus 16–23.
SCLK	58	I	Microprocessor Clock.
RESET	59	I	Synchronized reset input to synchronize the internal clock with the processor phase.
RDYRTN#	80	I	Channel Ready Return signal from Micro Channel (active low).
PRDYO#	93	O	Microprocessor ready signal.
FP	68	I	Processor Speed Select. (20 MHz = 1, 16 MHz = 0.)
PRDYI#	60	I	Synchronized microprocessor ready input.
FRC#	61	I	Fast ROM Cycle Select. When tied low, ROM cycles are run as Micro Channel default read cycles. When tied high, additional wait states are inserted to accommodate slower ROMs.
RAMEN#	62	I	Decode that indicates a system board DRAM access.
FCE#	63	I	Input that directs BC to terminate a CPU system board DRAM access.
UM/IO#	64	I	Micro Channel Memory/IO status.
PD/C#	65	I	CPU D/C# output.
PW/R#	66	I	CPU W/R# output.
PADS#	67	I	CPU ADS# output. (Indicates address valid.)
PNA#	71	O	Next Address Signal for address pipelining.
S0#, S1#	69, 70	B	DMA Status lines; input by the BC when DMA is master, and output by the BC when CPU is master.
UADL#	78	B	Micro Channel Address Latch Signal.
UMMCMD#	40	O	Micro Channel Matched Memory Command Signal.
UCMD#	72	B	Micro Channel Command Signal.
US0#, US1#	76, 77	B	Micro Channel Status.
RSEL1 RSEL0	27, 31	I I	These two signals are used for hardware enforced I/O recovery. They are sampled at the leading edge of UCMD# during CPU initiated I/O cycles, and are used to select one of four possible I/O recovery times. At the end of the I/O cycle, an internal timer is triggered, and then times out after the selected I/O recovery time. The next I/O cycle is not allowed to proceed into the active UCMD# phase until the internal timer times out. RSEL1,0 can be strapped for a particular time, or else driven from a combinatorial address decode.

82308 Micro Channel Bus Controller Pin Definitions (Continued)

Signal Name	Pin Number	I/O	Description
FIN	26	I	Asynchronous cache flush request input. A pulse on FIN causes a cache flush. Also, if FIN is left active for a long period of time, the 82385 will be kept in flush mode for as long as FIN is active. The exception to this is when the BC is directed to do a software initiated CPU reset when FIN is active. The BC will de-activate FLUSH for a period of time surrounding the falling edge of RSTCPU so as to prevent the 82385 from entering its self-test mode. If FIN is still active after the reset, then FLUSH will be re-activated.
FLUSH	46	O	Synchronous flush request to the 82385 Cache Controller.
SNOOP#	47	B	Synchronous strobe to the cache controller to indicate valid address during a non-processor memory write. SNOOP# is sampled at reset to indicate the presence of a cache. (1 = cache present, 0 = no cache.)
PM/IO#	28	I	CPU M/IO# output.
WS#	39	I	This input, if tied low, inserts an additional wait state into CPU reads from system board memory beyond the number of wait states requested via the FCE# input. It is primarily intended for cache applications, which typically require increased CPU data setup.
NC	1, 25, 51, 52, 75		No Connect
V_{DD}	13, 37, 88		Power
V_{SS}	2, 24, 38, 74, 89		Ground



NOTE:
NC = No Connect

82308 PARAMETRICS

ABSOLUTE MAXIMUM RATINGS*

Case Temperature under Bias .... −40°C to +85°C
Storage Temperature ..... −65°C to +150°C
Voltage to Any Pin with Respect to Ground ..... −0.3V to (V_{CC} + 0.3)V
DC Supply Voltage (V_{CC}) ..... −0.3V to +7.0V
DC Input Current ..... ±10 mA

**Notice: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

NOTICE: Specifications contained within the following tables are subject to change.

D.C. CHARACTERISTICS

T_C = 0°C to +70°C, V_{CC} = 5V ±10%

Symbol	Parameter	Min	Max	Units	Conditions
V_{IL}	Input Low Voltage		0.8	V	
V_{IH}	Input High Voltage	2.0		V	
V_{IL}	Input Low Voltage		0.8	V	SCLK
V_{IH}	Input High Voltage	V_{CC} − 0.8		V	SCLK
V_{OL}	Output Low Voltage		0.4	V	I_{OL} = 4 mA
V_{OH}	Output High Voltage	2.4		V	I_{OH} = 4 mA
I_{CC}	Power Supply Current		180	mA	No DC Loads
I_{LI}	Input Leakage Current		±10	μA	$V_{SS} < V_{IN} < V_{CC}$
I_{OZ}	Tri-State Output Leakage Current		±10	μA	$V_{SS} < V_{OUT} < V_{CC}$

82308 Micro Channel BUS CONTROLLER A.C. SPECS

T_C = 0°C to +70°C, V_{CC} = 5V ±10%

Symbol	Parameter	82308 Kit 16 MHz		82308 Kit 20 MHz		82308HS Kit 25 MHz		C_L (pF)	Notes	Conditions
		Min	Max	Min	Max	Min	Max			
T1	SCLK PERIOD	31.25		25		20				
T2A	SCLK HIGH/LOW TIME (50%)	12		10		8				
T2B	SCLK HIGH/LOW TIME (90%)	8		6.5		6				
T3	RESET SETUP	10		10		10				
T4	RESET HOLD	4		4		4				
T5A	RSTCPU DELAY	2	30	2	30	2	27	25		
T5B	RSTCPU PULSE WIDTH	1980		1580		1260		25	14, 20	
T6A	FLUSH DELAY	5	41	5	34	5	28	50		
T6B	FLUSH PULSE WIDTH	240		190		150		50	15, 20	
T6C	SNOOP# DELAY	5	41	5	34	5	34	50		
T7	FIN PULSE WIDTH	25		25		25				
T8A	COMMAND I/O RECOVERY PULSE WIDTH	600		600		600			20	RSEL1,0 = 01
T8B	COMMAND I/O RECOVERY PULSE WIDTH	2500		2500		2500			20	RSEL1,0 = 10
T8C	COMMAND I/O RECOVERY PULSE WIDTH	10000		10000		10000			20	RSEL1,0 = 00
T8D	COMMAND I/O RECOVERY PULSE WIDTH	0		0		0			20	RSEL1,0 = 11
T9	RSEL0,1 SETUP	15		15		15			4	
T10	RSEL0,1 HOLD	20		20		20			4	
T11A	PW/R#, PD/C#, PM/IO# SETUP	25		22		13				
T11B	PADS# SETUP	25		22		17				
T12	PADS#, PW/R#, PD/C#, PM/IO# HOLD	4		4		4				
T13A	UM/IO# SETUP TO UADL# ↓	20		20		20				
T13B	UM/IO# SETUP TO SCLK	20		20		20			8	
T14A	UM/IO# HOLD FROM UADL# ↑ OR UCMD# ↓	20		16		16			7	
T14B	UM/IO# HOLD FROM SCLK	20		16		16			8	
T15	PRDYO# DELAY	4	30	4	24	3	20	75		
T16	PRDYI# SETUP	18		18		15				
T17	PRDYI# HOLD	3		3		3				
T18	PNA# DELAY	0	25	0	25	3	28	25		
T19A	UADL# DELAY (TPHL)	2	24	2	24	2	22	25		
T19B	UADL# DELAY (TPLH)	2	24	2	24	2	22	25		
T20A	UCMD# DELAY (TPHL)	2	23	2	20	2	20	25	2	
T20B	UCMD# DELAY (TPLH)	2	25	2	23	2	20	25		
T21A	UMMCMD# DELAY (TPHL)	2	23	2	20	2	20	25	2, 5	
T21B	UMMCMD# DELAY (TPLH)	2	25	2	23	2	20	25		
T22A	US0#, US1# (TPHL) DELAY	2	27	2	26	2	24	25	2	
T22B	US0#, US1# (TPLH) DELAY	2	27	2	26	2	24	25		
T22C	US0#, US1# (TPHL) DELAY FROM S0#, S1#	0	27	0	30	0	30	25		
T23	S0#, S1# SETUP	20		20		15				
T24	S0#, S1# DELAY	2	35	2	30	2	22	50		
T25	A0, A1 DELAY FROM BE0-3#	2	35	2	30	2	25	25		
T26	UBE0-3#, UA0-1#, UBHE# DELAY FROM BE0-3#, A0-1, BHE#	2	30	2	28	2	28	25		
T28	SAL DELAY	2	36	2	30	2	27	100		
T30A	SBHW#, SBLW# INACTIVE DELAY FROM SCLK	2	30	2	25	2	32	50	11, 21	
T30B	SBHW#, SBLW# DELAY FROM UADL#	2	40	2	40	2	40	50	25	

82308 Micro Channel BUS CONTROLLER A.C. SPECS

T_C = 0°C to +70°C, V_{CC} = 5V ±10% (Continued)

Symbol	Parameter	82308 Kit 16 MHz		82308 Kit 20 MHz		82308HS Kit 25 MHz		C_L (pF)	Notes	Conditions
		Min	Max	Min	Max	Min	Max			
T30C	SBHW#, SBLW# DELAY FROM UCMD#	5	35	5	35	5	35	50	10, 25	
T30D	SWDIR DELAY FROM UADL#	2	40	2	40	2	40	100	12	
T30E	DWHE# DELAY FROM UADL#	2	40	2	40	2	40	50		
T30F	DWHE# DELAY FROM UCMD#	5	45	5	45	5	45	50	25	
T30G	DBE1#, DBE2# DELAY FROM UADL#	2	40	2	40	2	40	25		
T30H	DBE1#, DBE2# DELAY FROM UCMD#	5	45	5	45	5	45	25	25	
T30I	SWAP1-4# DELAY FROM UADL#	2	40	2	40	2	40	25	25	
T30J	SWAP1-4# DELAY FROM UCMD#	5	35	5	35	5	35	25	13, 25	
T30K	SBHW#, SBLW# ACTIVE DELAY FROM SCLK	2	40	2	40	2	40	50	11	
T30L	SWDIR DELAY FROM UCMD#	5	40	5	40	5	40	100	13, 25	
T30M	SWDIR DELAY FROM DS16RTN, DS32RTN	2	35	2	35	2	35	100	12, 25	
T30N	SWAP1-4# DELAY FROM UCMD#	2	35	2	35	2	35	25	11, 25	
T31	DBL1-3 SETUP TO UCMD#, UMMCMD#	−4		−4		−4		25		
T32	WDL DELAY	2	32	2	26	2	21	50		
T33	DBL1-3 DELAY ↑	2	27	2	25	2	22	25		
T34A	MHW#, MLW# ACTIVE DELAY FROM SCLK ↑	2	30	2	25	2	25	50	16	
T34B	MHW#, MLW# INACTIVE DELAY FROM SCLK ↑	2	30	2	25	2	32	50	17, 21, 24	
T34C	MDIR DELAY FROM SCLK	2	40	2	40	2	40	125	22, 24	
T34D	MHW#, MLW# DELAY FROM UADL#	2	45	2	45	2	45	50	25	
T34E	MHW#, MLW# DELAY FROM UCMD#	5	40	5	40	5	40	50	25	
T34F	MDIR DELAY FROM UADL#	2	45	2	45	2	45	125	25	
T34H	ROMOE# DELAY FROM SCLK	2	28	2	28	2	28	50		
T34I	MHW#, MLW# ACTIVE DELAY FROM SCLK ↓	2	35	2	35	2	35	50	18, 23, 25	
T34J	MHW#, MLW# INACTIVE DELAY FROM SCLK ↑	2	35	2	35	2	35	50	19, 24, 25	
T35	FCE# SETUP	15		15		10				
T36	FCE# HOLD	3		3		3				
T37	ROMEN#, RAMEN# SETUP	20		19		19				
T38A	DS16RTN, DS32RTN SETUP TO SCLK	30		30		25			6	
T38B	DS16RTN, DS32RTN SETUP TO UADL# ↑	15		15		15			3	
T41	RDYRTN# SETUP TO SCLK	10		10		10			9	
T42	RDYRTN# HOLD FROM SCLK	4		4		4				
T43	IOEN#, FDACK# SETUP TO UADL# ACTIVE	10		10		10			25	
T44A	P0-P3 SETUP TO SCLK	0		0		0			11	
T44B	P0-P3 SETUP TO UCMD#	3		3		3			13, 25	
T45	P0-P3 HOLD	12		12		12				
T46A	CHRDY DELAY FROM IOEN#	2	30	2	30	2	30	25		
T46B	CHRDY DELAY FROM STATUS	2	25	2	25	2	25	25	25	
T46C	CHRDY ACTIVE FROM MB COMMAND	100		90		70		25	1, 20	
T47A	MB COMMAND DELAY FROM UCMD# ACTIVE	75		75		75		100	1, 20	
T47C	MB COMMAND DELAY FROM UCMD# INACTIVE	3	40	3	40	3	40	100	1, 25	
T48	MB COMMAND PULSE WIDTH	250		225		190		100	1, 12, 20	

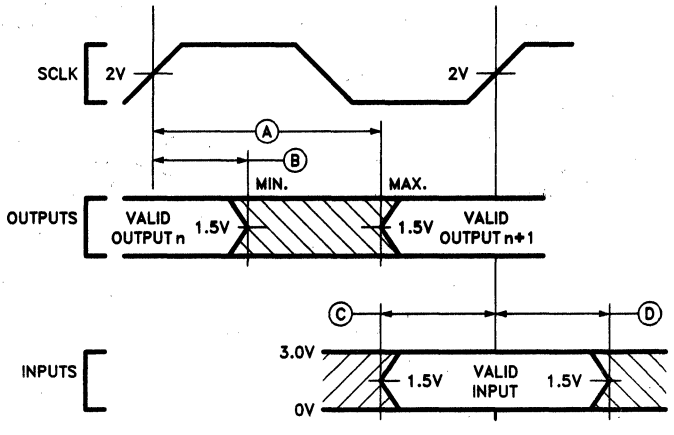
NOTES:

1. MB Commands include IOR, IOW, INTA#, VMRD# and VMWR#.
2. These specs and cycle edge definitions support a worst case "effective" data setup of 40 ns for a 385 system at 20 MHz. (Effective setup means setup to the "386-like" front end created by the 385.)
3. Spec applies only when master resides on Micro Channel.
4. RSEL0,1 should be tied high or low, or else driven from a combinatorial address decode.
5. UMMCMD# is only driven when the CPU is master.
6. Applies only when CPU is master.
7. T14A applies to the later of ADL# ↑ or CMD# ↓.
8. T13B, T14B apply to CPU or DMA master.
9. RDYRTN# is an asychronous input. Meeting T41 simply guarantees recognition at a particular clock edge.

NOTES:
10. Applies when DMA is master.
11. Applies when CPU is master.
12. Applies when CPU or DMA is master.
13. Applies when DMA or channel master is master.
14. Functional Spec . . . Not Tested (= 64 SCLK Periods).
15. Functional Spec . . . Not Tested (= 8 SCLK Periods).
16. READS AND PIPELINED WRITES
17. READS
18. NON-PIPELINED WRITES
19. WRITES
20. Functional Spec . . . Not Tested

NOTES (82308HS-25 ONLY):
21. Contention will not occur when a write immediately follows a read because the 82385 insures at least one BTI state between a read followed by write sequence during which the data bus remains tri-stated.
22. MDIR is generated and speced from SCLK ↑ instead of from SCLK ↓ at it is in the 82308-16/20.
23. In non-piped writes, MHW# and MLW# are generated from the phase 2 SCLK ↑ edge rather than from SCLK ↓ as in the 82308-16/20.
24. Since MDIR toggles from the same clock edge that MHW# and MLW# are de-asserted from, contention is prevented by 82308-25 internal design such that MDIR is guaranteed to be slower than MHW# or MLW#.
25. Only tested when UADL#, UCMD#, US0#, and US1# are inputs; i.e., when Microchannel is master.

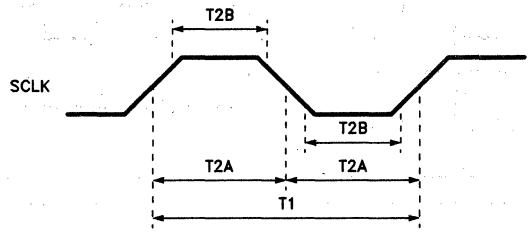
DRIVE LEVELS AND MEASUREMENT POINTS FOR A.C. SPECIFICATIONS



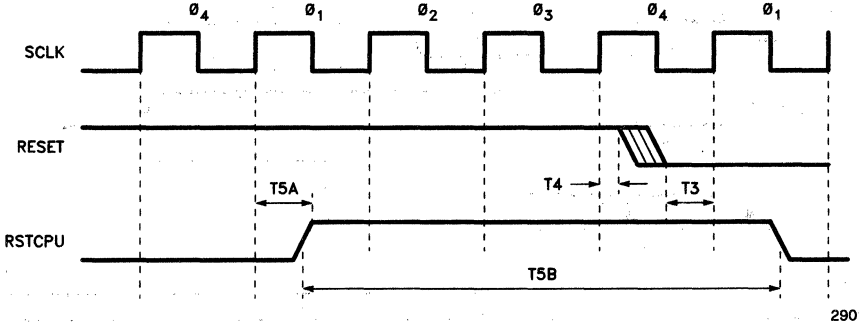
290187-25

LEGEND:
A. Maximum Output Delay Specification.
B. Minimum Output Delay Specification.
C. Minimum Input Setup Specification.
D. Minimum Input Hold Specification.

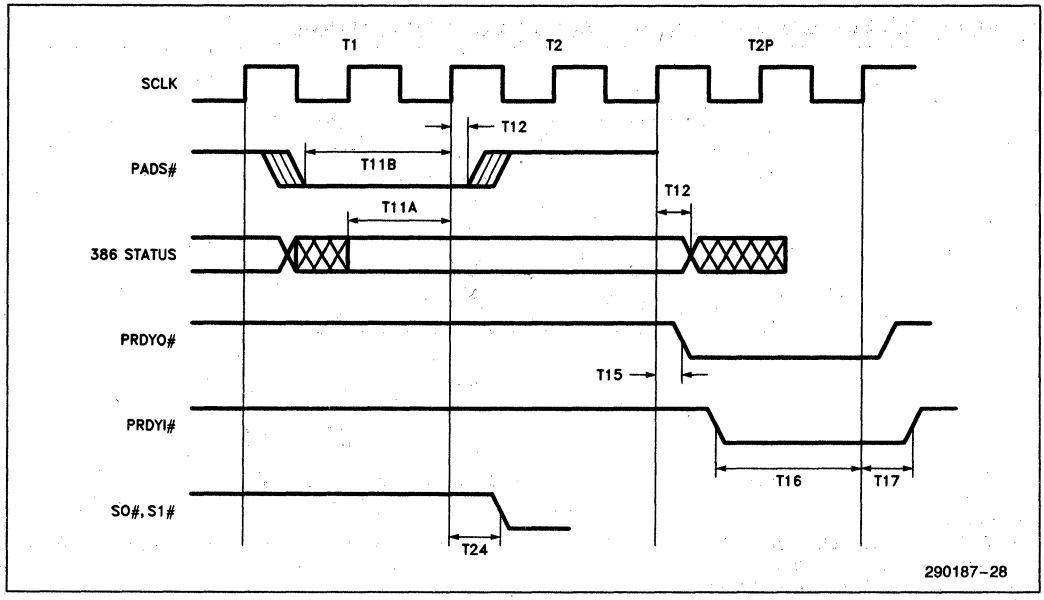
Input waveforms have tr ≤ 2.0 ns from 0.8V to 2.0V.

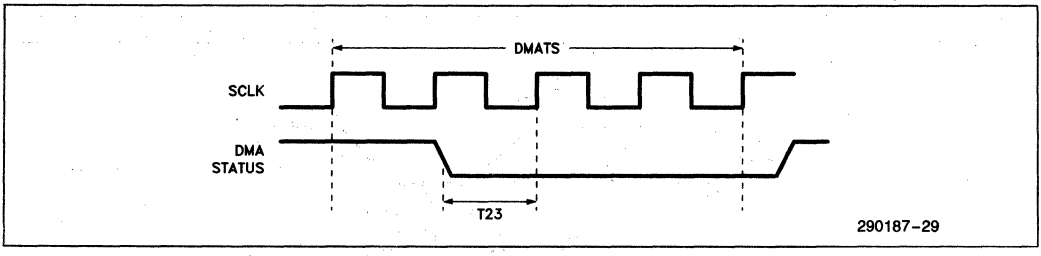


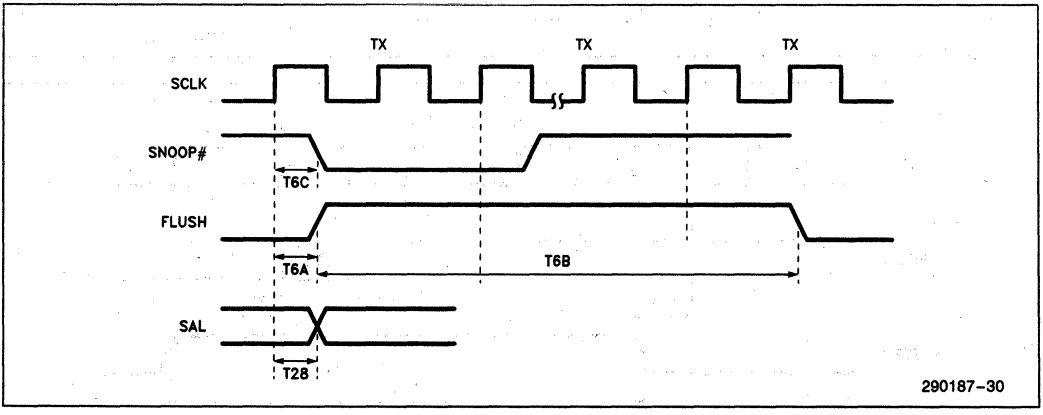
290187-26

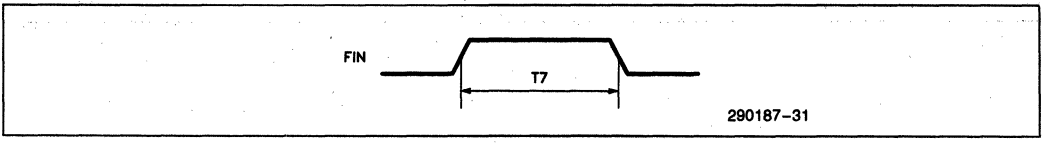


290187-27

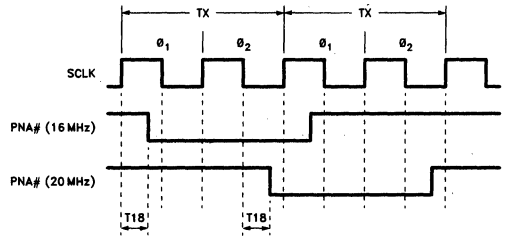

T1
T2
T2P
SCLK
T12
PADS#
T11B
T12
T11A
386 STATUS
PRDYO#
T15
PRDYI#
T16
T17
SO#, S1#
T24
290187-28


DMATS
SCLK
DMA STATUS
T23
290187-29

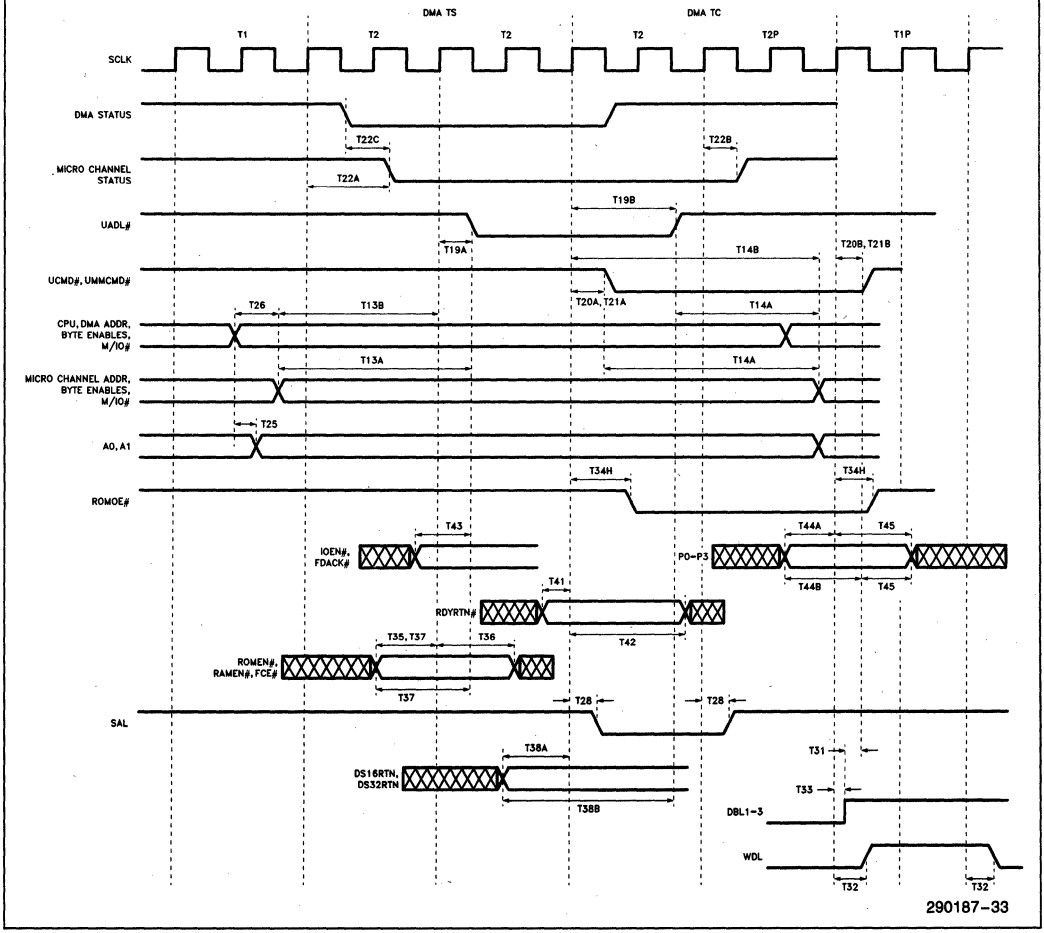

TX
TX
TX
SCLK
SNOOP#
T6C
FLUSH
T6A
T6B
SAL
T28
290187-30


FIN
T7
290187-31

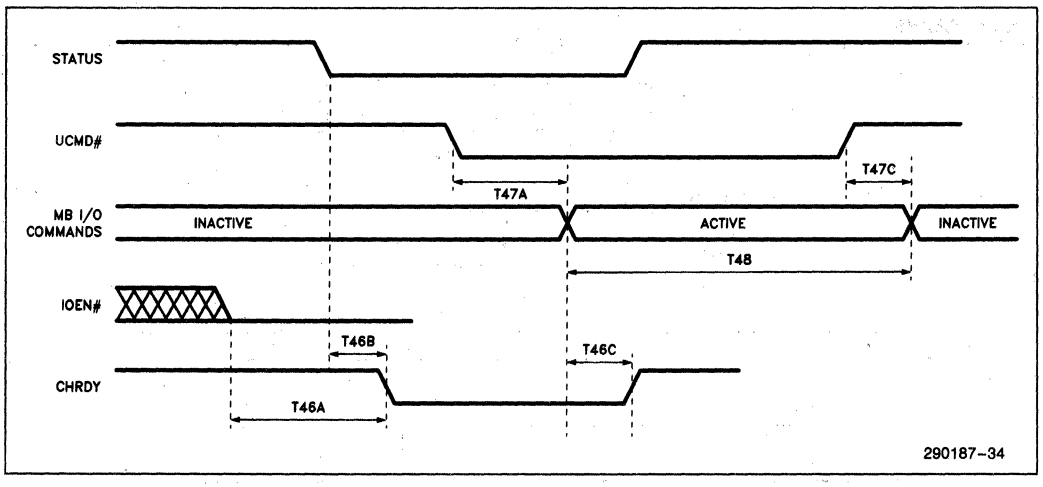
PNA# TIMING



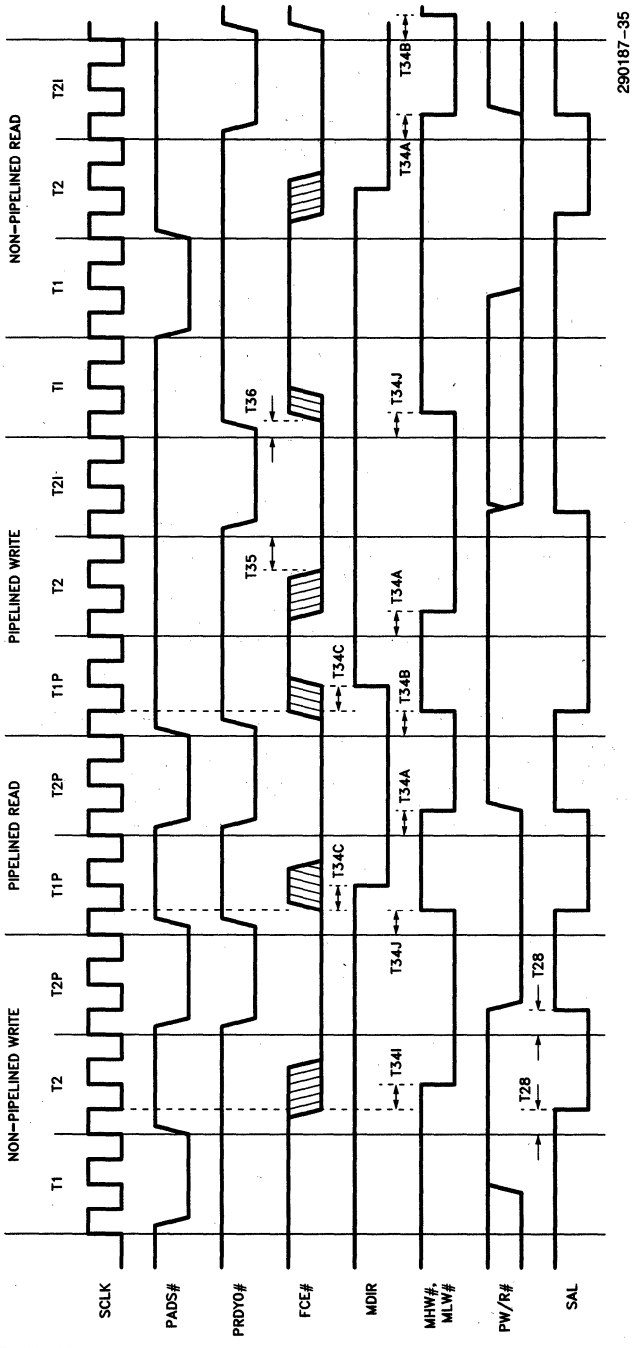
290187-32



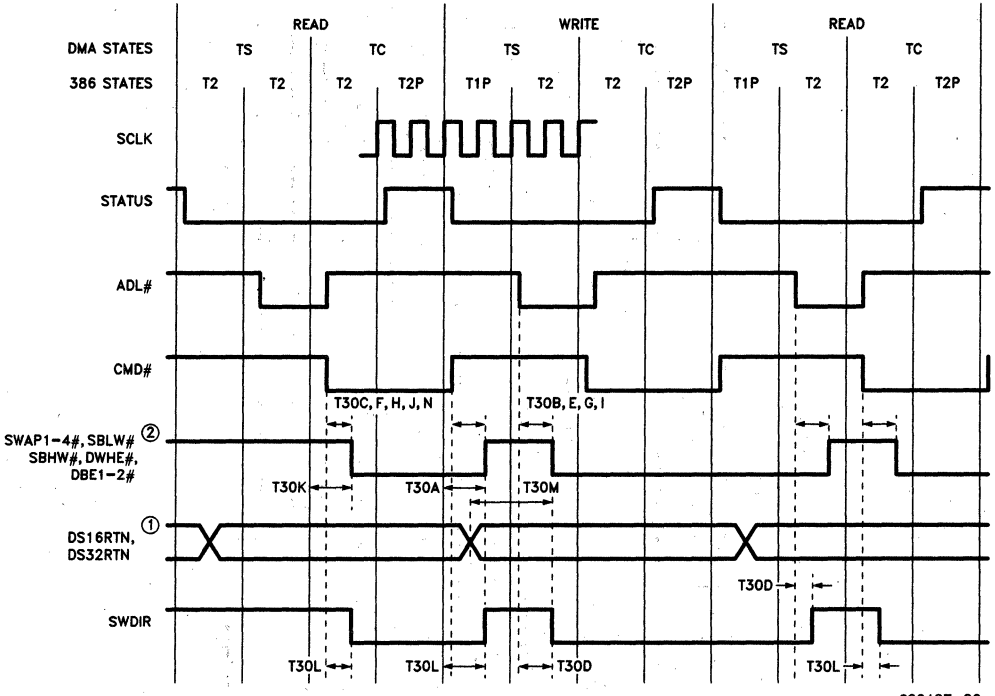
290187-33


STATUS
UCMD#
MB I/O COMMANDS
INACTIVE
ACTIVE
INACTIVE
T47A
T47C
T48
IOEN#
CHRDY
T46B
T46C
T46A
290187-34

MEMORY DATA BUFFER CONTROL
80386 ACCESSES TO MOTHERBOARD DRAM



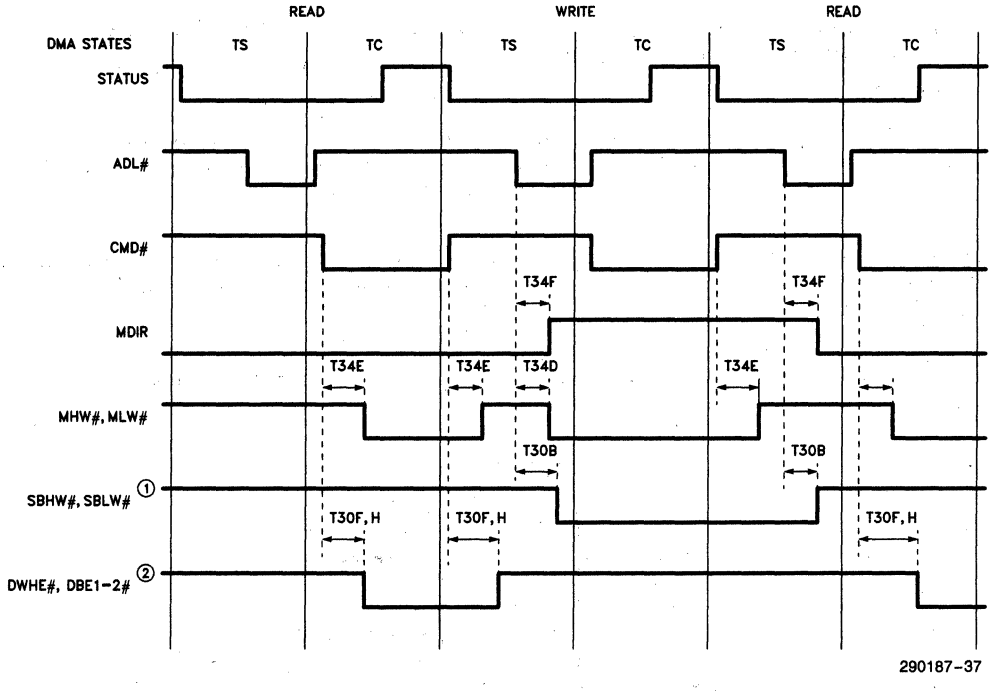
Micro Channel DATA BUFFER CONTROL 386/DMA MASTER, DATA STEERING FOR CHANNEL MASTER TO CHANNEL SLAVE



290187-36

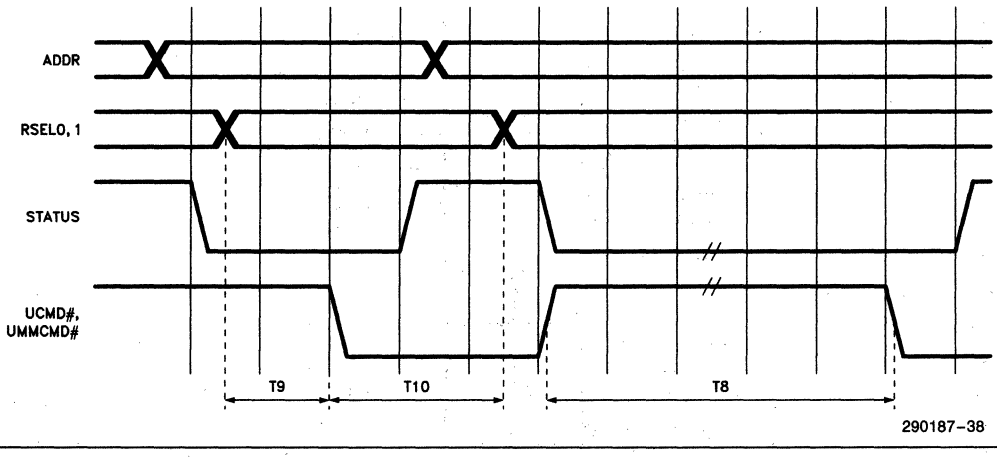
①T30D applies to SWDIR only when all involved combinatorial data size inputs (DS16RTN, DS32RTN) are available early enough not to delay SWDIR.
②T30A and T30K apply only to SBHW# and SBLW#, and only when the 386 is master.
③T30B applies here when DMA data is routed to system board memory from the lower half of the data bus (D0–D15) to the upper half (D16–D31).

MEMORY/Micro Channel DATA BUFFER CONTROL DMA/CHANNEL MASTER ACCESSES TO MB DRAM



①Channel Master writes to MB DRAM.
②Channel Master reads from MB DRAM.

(HARDWARE ENFORCED) I/O RECOVERY TIMING



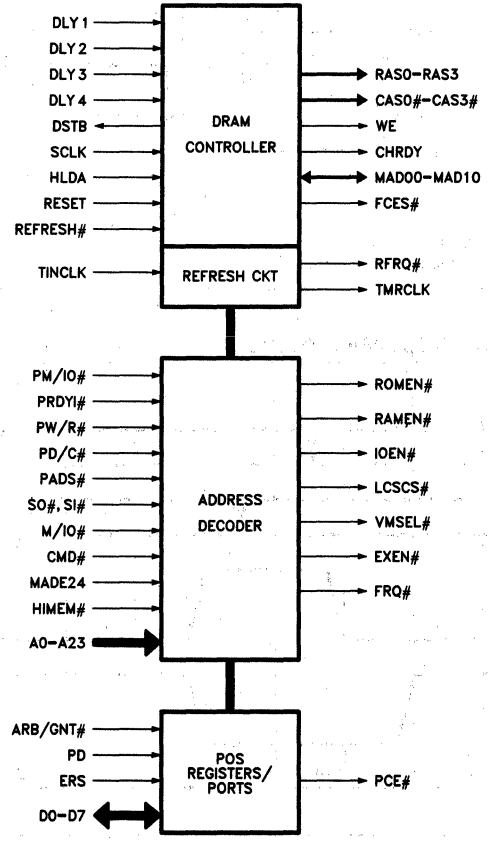
82309
ADDRESS BUS CONTROLLER

- **Address Decoder**
- **DRAM Controller ... Up to Four Banks of Page Interleaved Memory (Max 16M)**
- **Refresh Timer**
- **Integrated I/O Ports and Registers**
- **Low Power CHMOS Technology**
- **100-Pin Plastic Quad Flat Packaging**
  (See Packaging Spec., Order # 231369)

The 82309 Address Bus Controller provides Address decoding for devices on the motherboard, including the shadowed DRAM address of the ROM BIOS. The Address Bus Controller also has integrated DRAM controller, Refresh Timer and miscellaneous registers for memory control and error recovery, specifically ports E0, E1, E3, E4, E5, E7 and 103.

The 82309 Address Bus Controller provides the designer several price/performance choices for the configuration of up to 16 MBytes of Page Interleave DRAM memory on the motherboard. Up to four banks of 256K, 1M and 4M DRAMs are supported.

The 82309 Address Bus Controller generates periodic refresh requests to the 82307 DMA controller to run refresh cycles. The 82309 does not use the Refresh Address generated by the DMA controller but provides its own refresh address to the 256K, 1M and 4M DRAMs.



November 1988
Order Number: 290188-001

PORTS AND REGISTERS

Configuration bits SS1 and SS2 control the function of the Ports and Register Block. The Ports and Register Block, in turn, control the function of the Refresh Timer and the address mapping of the motherboard DRAMs and the BIOS EPROMs.

SS1 and SS2 essentially select one of four definitions of the memory encoding registers (E0, E1), error trace registers (E3, E4, E5, E7), and motherboard POS setup port (103). These defintions are depicted in Table 0, and go by the names System A, System B, System C and System D.

System A presents a Model 50/60 compatible definition of these ports. Specifically, Port 103 is defined as it is in the IBM PS/2 Model 50/60 Technical Reference and ports E0–E7 are non-existent. System B presents a Model 80 compatible definition of these ports, as detailed in the IBM PS/2 Model 80 Technical Reference.

System B has a limitation in that due to the definition of the card enable bits in ports E0 and E1 (described later), it is limited to 4 Mbytes of system board memory. System C overcomes this by making the card enable bits "free form"; i.e., accessible as read/write bits, but otherwise meaningless in terms of their effect on the system. System C allows a Model 80 type system to provide up to 16 Mbytes of system board memory.

System D provides a Model 50/60 compatible definition of port 103 and a Model 80 compatible definition of ports E0–E7. This system is targeted for designs that wish to present a Model 50/60 port definition, but wish to make use of features provided in the Model 80 register set, specifically the ability to copy ROM into RAM for increased performance. This system requires external logic (approx. ½ of a 16L8 PAL) that essentially makes E0–E7 disappear from a software point of view once the ROM has been copied into RAM. (Details will be provided in the forth coming Intel *Designers Guide for Micro Channel Compatible Implementation.*)

In systems A and D, bit 0 (the Memory Enable Bit) is the only accessible bit in Port 103. This bit can be accessed via channel I/O Read and/or Write operations. When Port 103 is read only bit 0 is driven, all other data bus bits remain tristated. This bit is set to a 1 by RESET. When the Memory Enable Bit = 0 all of the motherboard DRAM is disabled (but still refreshed). In both systems A and D, the refresh timer produces a 400 ns pulse every 15.12 μs. In system D, mapping is controlled by ports E0 and E1, as de-

Table 0. Configuration Bits SS1, SS2 Definition

Config Bits		System	Description
SS1	SS2		
0	0	A	Model 50/60 Compatible Port 103(1) Registers E0–E7 Non-Accessible
1	0	B	Model 80 Compatible Port 103 Error Trace Registers E3, E4, E5 and E7 Accessible Memory Encoding Registers E0 and E1 Accessible Compatible Card Enable Bits in E0 and E1
1	1	C	Model 80 Compatible Port 103 Error Trace Registers E3, E4, E5 and E7 Accessible Memory Encoding Registers E0 and E1 Accessible Free Form Card Enable Bits In E0 and E1
0	1	D	Model 50/60 Compatible Port 103 Error Trace Registers E3, E4, E5 and E7 Accessible (But Not Typically Used) Memory Encoding Registers E0 and E1 Accessible Free Form Card Enable Bits In E0 and E1

NOTES:
1. Port 103 is a motherboard POS port; i.e., accessible only when the motherboard is in Setup Mode.

scribed in a moment. In system A, the other functions of the ports and register block are as follows:

— The Split in the first megabyte is located at 640 Kbytes.

— If the motherboard DRAM space equals 16 Mbytes then the remaining DRAM is disabled, otherwise the remaining 384 Kbytes are remapped to the first 384 Kbytes past the end of the motherboard DRAM address space. (i.e., if there are 4 Mbytes of DRAM then the split is remapped to address 00400000 → 0045FFFF.)

— The BIOS EPROMs are mapped to both 000E0000 → 000FFFFF and FFFE0000 → FFFFFFFF.

In systems B and C, port 103 is defined as follows:

— Port 103 bit 0 (the Memory Enable Bit) is not accessible.

— Port 103 bit 1 (the Refresh Rate Bit) is accessible for write operations only. If this bit is a 1 then the Refresh Timer produces an approximately 400 ns long pulse once every 15.12 μs. If this bit is a 0 then the Refresh Timer produces a continuous stream of 400 ns pulses with a period of approximately 800 ns. This bit is set to a 1 by RESET.

In systems B, C and D, ports E0, E1, E3, E4, E5 and E7 are defined as follows:

— Four of the Read only Micro Channel Error Trace Registers (Ports 00E3, 00E4, 00E5 and 00E7) are accessible. (Typically, a system D design will not utilize these registers and will thus not require any external logic to implement any error register support.) These registers sample SA<02:23>, M/IO#, D/C# and ARB/GNT# on every rising edge of the ERS input pin. The bit assignments for these registers are as follows:

Bit	00E3	00E4	00E5	00E7
7	SA23	SA15	SA07	—
6	SA22	SA14	SA06	—
5	SA21	SA13	SA05	—
4	SA20	SA12	SA04	—
3	SA19	SA11	SA03	—
2	SA18	SA10	SA02	—
1	SA17	SA09	M/IO#	—
0	SA16	SA08	ARB/GNT#	D/C#

These four registers are all set to 00 by RESET. When Register E7 is read, only data bus bit 0 is driven by the ABC, data bus bit 1–7 remain tristated.

— Registers E0 and E1 are accessible via the channel for both I/O read and I/O write operations. These two registers control the address mapping of both the motherboard DRAMs and the BIOS EPROMs. (The reset state of E0 and E1 is FF.) The two most significant bits of both of these registers are free form register bits and have no effect on the functioning of the ABC. The functioning of the two next most significant bits (bits 5 & 4, the card enable bits) of both of these registers are controlled by configuration bits SS2 and SS1 as discussed in a moment.

— The four least significant bits (bits 3, 2, 1 & 0) of register E1 are defined as follows:

Bit 3	2	1	0	
0	.	.	.	- Memory beyond split Enabled
1	.	.	.	- Memory beyond split Disabled
.	0	.	.	- Split is at 640K (000A0000)
.	1	.	.	- Split is at 512K (00080000)
.	.	0	.	- BIOS ROMs deactivated in 000E0000 to 000FFFFF BIOS ROMs active in FFFE0000 to FFFFFFFF Shadow RAM Write Protected
.	.	1	.	- BIOS ROMs active in 000E0000 to 000FFFFF BIOS ROMs active in FFFE0000 to FFFFFFFF Shadow RAM Writeable.
.	.	.	0	- Parity Checking enabled
.	.	.	1	- Parity Checking disabled

If the memory beyond the Split is enabled by bit 3 then the four least significant bits (bits 3, 2, 1 & 0) of register 00E0 define the address range in memory where the portion of the first megabyte of system RAM beyond the split will be remapped. Bits 3, 2, 1 & 0 of this register correspond to address bits 23, 22, 21 & 20 of the remap location for this memory.

Bit 2 of register E1 defines the partitioning of the first megabyte of the motherboard DRAM. Figure 0 details the effect of this bit. The S in the remap addresses represents the value of the four least significant bits of register E0.

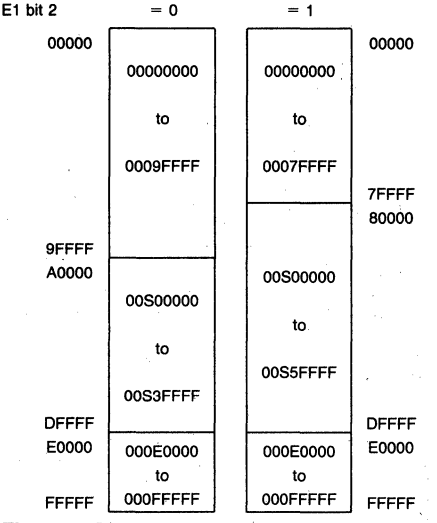


Figure 0. Partition of First Megabyte of DRAM

There is DRAM mapped in the address range 000E0000 to 000FFFFF. The function of this DRAM is controlled by bit 1 of register E1. If bit 1 = 1 then this RAM is writeable but not readable (thus the BIOS EPROMs can be Shadowed by Reading and Writing to the same address). If bit 1 = 0 then the BIOS EPROMs are disabed and this area of RAM is read enabled but write protected.

When bit 1 of register E1 is a 1 both the ROMEN# and the RAMEN# signals will respond to accesses in the range 000E0000 to 000FFFFF. In this way, the 82308 Bus Controller knows to direct reads to ROM and writes to RAM to allow shadowing. (In system D, if memory is disabled via bit 0 of port 103, then ROM is enabled in 000E0000 to 000FFFFF, regardless of the status of bit 1 in E1.)

Bit 0 of register E1 is output to the Bus Controller on the PCE# pin for use as an (active low) Parity Check Enable control bit.

— In system B, the amount of the physical motherboard DRAM that is accessable is controlled by the card enable bits (bits 5 and 4 of registers E0 and E1). These four bits act as enables (active low) for each of the first four megabytes of the physical motherboard DRAM space. Any additional DRAM controlled by the ABC will be refreshed but is otherwise disabled.

Register				Function
E0		E1		
Bit 5	Bit 4	Bit 5	Bit 4	
0	X	X	X	Megabyte #3 Enabled
1	X	X	X	Megabyte #3 Disabled
X	0	X	X	Megabyte #2 Enabled
X	1	X	X	Megabyte #2 Disabled
X	X	0	X	Megabyte #1 Enabled
X	X	1	X	Megabyte #1 Disabled
X	X	X	0	Megabyte #0 Enabled
X	X	X	1	Megabyte #0 Disabled

All megabytes that are enabled by these bits are mapped into one continuous block (with the exception of the Split from the first active megabyte) starting at address 00000000. (Thus if megabyte #0 is disabled, then the rest of the megabytes are remapped down to the range 00000000 to 002FFFFF, etc.)

In systems C and D, bits 5 and 4 of both registers E0 and E1 are free form register bits and have no effect on the functioning of the ABC.

DRAM CONTROLLER

The DRAM controller supports page interleaved memory designs in the configurations shown in Table 1. This table also details which channel address bits map to which DRAM address bits. Note that even though options D and G are two-bank options, the ABC thinks of these banks as 0 and 2, not banks 0 and 1, i.e., use RAS0, RAS2, CAS0# and CAS2#.

Table 1 describes the basic memory configurations A through N. However, a wide variety of additional options can be easily realized by building on A through N with minimal external address decode logic. These additional options include the ability to mix DRAM types (for example 256K and 1M DRAMs in the same system), and allow for a great deal of flexibility in memory upgrade paths. Examples of how to do this are included in the *Designer's Guide for Micro Channel Compatible Implementation.*

Table 1. Memory Configuration Options and Channel Address-To-DRAM Address Mapping

Opt	Size	Memory Configuration Options	Page Size
A	1M	1 Bank of 256K DRAMs (x 32) Page Mode	512
B	1M	2 Banks of 256K DRAMs (x 16) Page Mode	512
C	2M	1 Bank of 1M DRAMs (x 16) Page Mode	1024
D	2M	2 Banks of 256K DRAMs (x 32) Page Mode	512
E	2M	4 Banks of 256K DRAMs (x 16) Page Mode	512
F	4M	1 Bank of 1M DRAMs (x 32) Page Mode	1024
G	4M	2 Banks of 1M DRAMs (x 16) Page Mode	1024
H	4M	4 Banks of 256K DRAMs (x 32) Page Mode	512
I	8M	1 Bank of 4M DRAMs (x 16) Page Mode	2048
J	8M	2 Banks of 1M DRAMs (x 32) Page Mode	1024
K	8M	4 Banks of 1M DRAMs (x 16) Page Mode	1024
L	16M	1 Bank of 4M DRAMs (x 32) Page Mode	2048
M	16M	2 Banks of 4M DRAMs (x 16) Page Mode	2048
N	16M	4 Banks of 1M DRAMs (x 32) Page Mode	1024

Opt	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
A					Ps	Ps	Ps	Ps	Ps	Ps	Ps	Ps	Ps	Ws	Ws	Ws	Ws	Ws	Ws	Ws	Ws	Ws		
B					Ps	Ps	Ps	Ps	Ps	Ps	Ps	Ps	Bs	Ws	Ws	Ws	Ws	Ws	Ws	Ws	Ws	Ws	Ws	
C				Ps	Ps	Ps	Ps	Ps	Ps	Ps	Ps	Ps	Ps	Ws	Ws	Ws	Ws	Ws	Ws	Ws	Ws	Ws	Ws	
D				Ps	Ps	Ps	Ps	Ps	Ps	Ps	Ps	Ps	Bs	Ws	Ws	Ws	Ws	Ws	Ws	Ws	Ws	Ws		
E				Ps	Ps	Ps	Ps	Ps	Ps	Ps	Ps	Ps	Bs	Bs	Ws	Ws	Ws	Ws	Ws	Ws	Ws	Ws	Ws	
F			Ps	Ps	Ps	Ps	Ps	Ps	Ps	Ps	Ps	Ps	Ws	Ws	Ws	Ws	Ws	Ws	Ws	Ws	Ws	Ws		
G			Ps	Ps	Ps	Ps	Ps	Ps	Ps	Ps	Ps	Ps	Bs	Ws	Ws	Ws	Ws	Ws	Ws	Ws	Ws	Ws	Ws	
H			Ps	Ps	Ps	Ps	Ps	Ps	Ps	Ps	Ps	Bs	Bs	Ws	Ws	Ws	Ws	Ws	Ws	Ws	Ws	Ws		
I		Ps	Ps	Ps	Ps	Ps	Ps	Ps	Ps	Ps	Ps	Ps	Ws	Ws	Ws	Ws	Ws	Ws	Ws	Ws	Ws	Ws	Ws	
J		Ps	Ps	Ps	Ps	Ps	Ps	Ps	Ps	Ps	Ps	Bs	Ws	Ws	Ws	Ws	Ws	Ws	Ws	Ws	Ws	Ws		
K		Ps	Ps	Ps	Ps	Ps	Ps	Ps	Ps	Ps	Ps	Bs	Bs	Ws	Ws	Ws	Ws	Ws	Ws	Ws	Ws	Ws	Ws	
L	Ps	Ps	Ps	Ps	Ps	Ps	Ps	Ps	Ps	Ps	Ps	Ws	Ws	Ws	Ws	Ws	Ws	Ws	Ws	Ws	Ws	Ws		
M	Ps	Ps	Ps	Ps	Ps	Ps	Ps	Ps	Ps	Ps	Ps	Bs	Ws	Ws	Ws	Ws	Ws	Ws	Ws	Ws	Ws	Ws	Ws	
N	Ps	Ps	Ps	Ps	Ps	Ps	Ps	Ps	Ps	Ps	Bs	Bs	Ws	Ws	Ws	Ws	Ws	Ws	Ws	Ws	Ws	Ws		

Ps ≥ Page Select Ws ≥ Word Select Bs ≥ Bank Select

NOTE:
Options A, C, F, I & L use Bank 0
Options D & G use Bank 0 & 2
Options B, J & M use Bank 0 & 1
Options E, H, K & N use all Banks

Opt	Ps											Ws										Bs	
	10	09	08	07	06	05	04	03	02	01	00	10	09	08	07	06	05	04	03	02	01	00	01	00
A	><	><	11	12	13	19	18	17	16	15	14	><	><	02	10	03	09	08	07	06	05	04	><	><
B	><	><	11	12	13	19	18	17	16	15	14	><	><	02	01	03	09	08	07	06	05	04	><	10
C	><	11	20	12	13	19	18	17	16	15	14	><	01	02	10	03	09	08	07	06	05	04	><	><
D	><	><	20	12	13	19	18	17	16	15	14	><	><	02	10	03	09	08	07	06	05	04	11	><
E	><	><	20	12	13	19	18	17	16	15	14	><	><	02	01	03	09	08	07	06	05	04	11	10
F	><	21	20	12	13	19	18	17	16	15	14	><	11	02	10	03	09	08	07	06	05	04	><	><
G	><	21	20	12	13	19	18	17	16	15	14	><	01	02	10	03	09	08	07	06	05	04	11	><
H	><	><	20	21	13	19	18	17	16	15	14	><	><	02	10	03	09	08	07	06	05	04	11	12
I	22	21	20	12	13	19	18	17	16	15	14	01	11	02	10	03	09	08	07	06	05	04	><	><
J	><	21	20	22	13	19	18	17	16	15	14	><	11	02	10	03	09	08	07	06	05	04	><	12
K	><	21	20	22	13	19	18	17	16	15	14	><	01	02	10	03	09	08	07	06	05	04	11	12
L	23	21	20	22	13	19	18	17	16	15	14	12	11	02	10	03	09	08	07	06	05	04	><	><
M	23	21	20	22	13	19	18	17	16	15	14	01	11	02	10	03	09	08	07	06	05	04	><	12
N	><	21	20	22	23	19	18	17	16	15	14	><	11	02	10	03	09	08	07	06	05	04	13	12

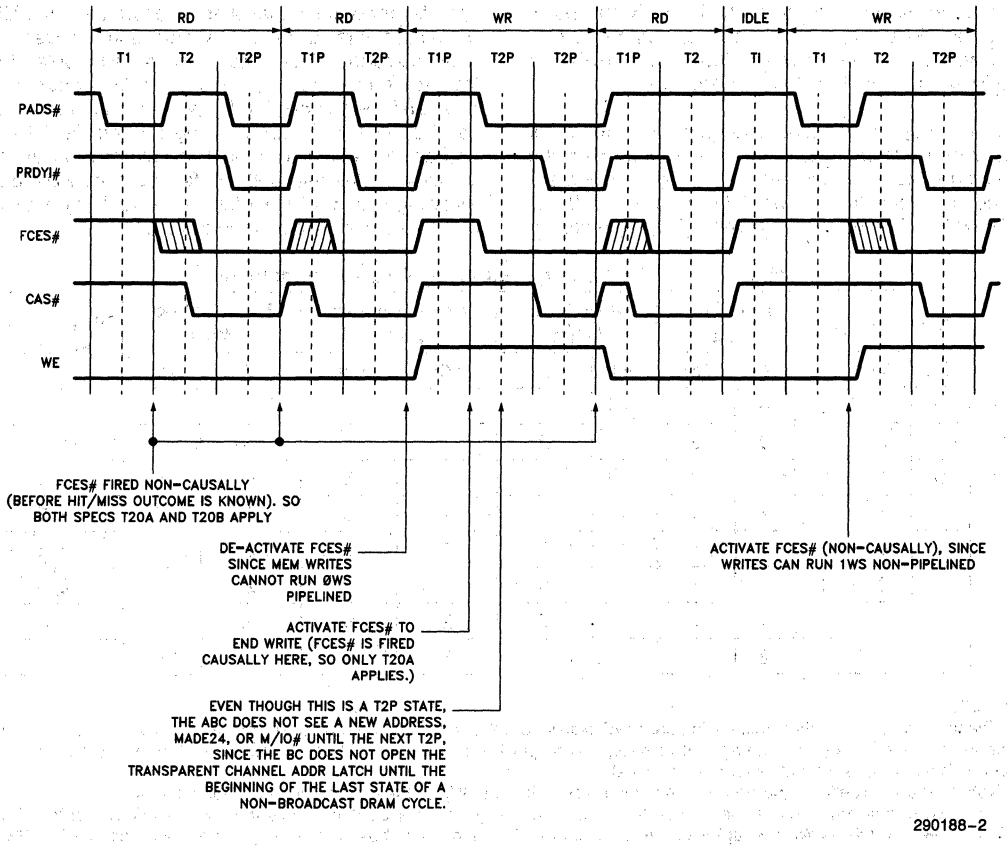
Typically, zero wait state pipelined page hit performance can be achieved at 16 MHz using 100 ns or 120 ns DRAMs, resulting in an aggregate of 0.5 to 0.8 wait states on average. The same DRAMs at 20 MHz will yield 1 wait state page hits.

At power-up, the 82309 Address Bus Controller samples its memory address bus to determine the desired system configuration. (This operation is described in detail later in the data sheet under "MAD BUS RESET CONFIGURATION".) The three configuration switches, C0, C1 and C2 are used to select a specific performance level as measured in page hit/page miss wait states. DRAM selection involves not only selecting a DRAM, but also choosing delay line taps to control the sequence of DRAM control signals, and then choosing the performance level that can be reliably supported using a particular DRAM and set of delay line taps. The next several pages describe all the available configuration options, and following this is a DRAM/Delay Tap selection guide along with some sample calculations.

Table 2. 82309 ABC Configuration and CPU Performance(3)

	Config Inputs			Pipelined Read		Pipelined Write		Non-Pipelined Read		Non-Pipelined Write		Reference Figures
	C0	C1	C2	Hit	Miss	Hit	Miss	Hit	Miss	Hit	Miss	
(1)	0	0	0	0	2	1(2)	2	1	3	1(2)	3	1, 4
(1)	0	0	1	0	3	1(2)	3	1	4	1(2)	4	1, 4
(1)	0	1	0	0	4	1(2)	4	1	5	1(2)	5	1, 4
	0	1	1	1	4	1	4	2	5	2	5	2, 5
	1	0	0	1	5	1	5	2	6	2	6	2, 5
	1	0	1	1	6	1	6	2	7	2	7	2, 5
	1	1	0	1	7	1	7	2	8	2	8	2, 5
	1	1	1	2	7	2	7	3	8	3	8	3, 5

NOTES:
1. These three configuration options feature 0WS pipelined page read hits. Strapping for one of these directs the ABC to determine whether a cycle is a page hit or miss, and to generate CAS# one SCLK phase earlier then the other options. Hence, these options are only supported at 16 MHz.
2. Note that both pipelined and non-pipelined write page hits run 1WS in these three configuration options.
3. The ABC completely controls the wait state counts in memory cycles according to this table via its FCES# output. The BC can however, (via its WS# strap) insert an additional wait state beyond those stated above in memory reads. (The WS# strap is intended for cache systems, which typically require additional data setup.)



NOTE:
Once the ABC fires FCES# to terminate a DRAM cycle, it remains active until the ABC detects the actual CPU end of cycle via the PRDYI# input. This allows the BC or any other external device to extend DRAM cycles if desired.

Figure 1. 0/2, 0/3, 0/4 Page Hits
(Cycles Named According to Pipelined Read Performance)

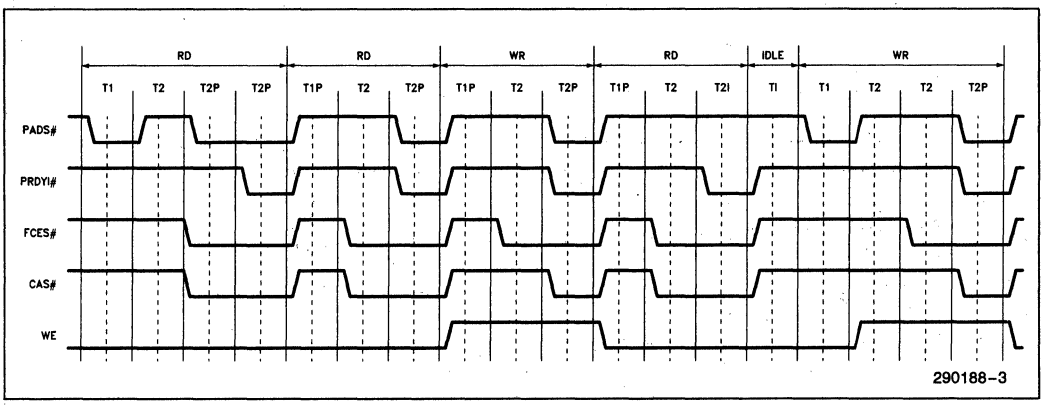


Figure 2. 1/4, 1/5, 1/6, 1/7 Page Hits (Cycles Named According to Pipelined Read Performance)

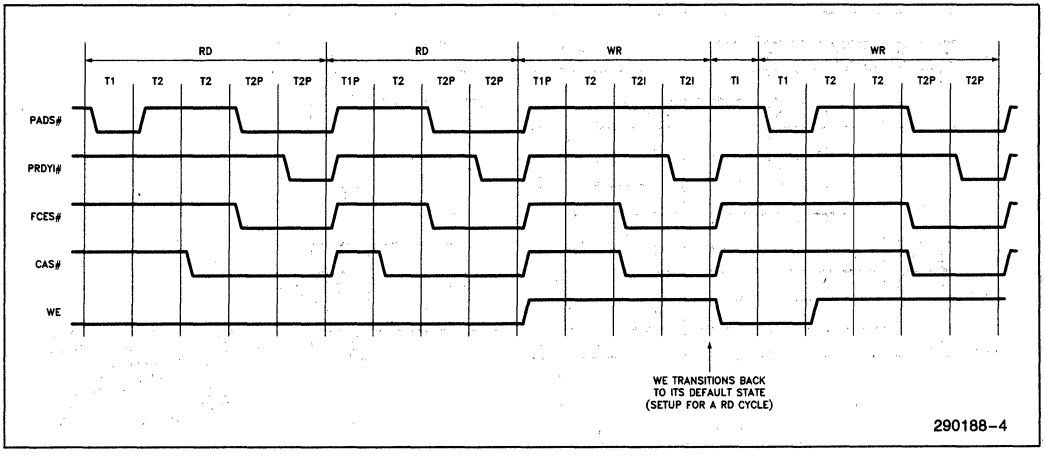


Figure 3. 2/7 Page Hit

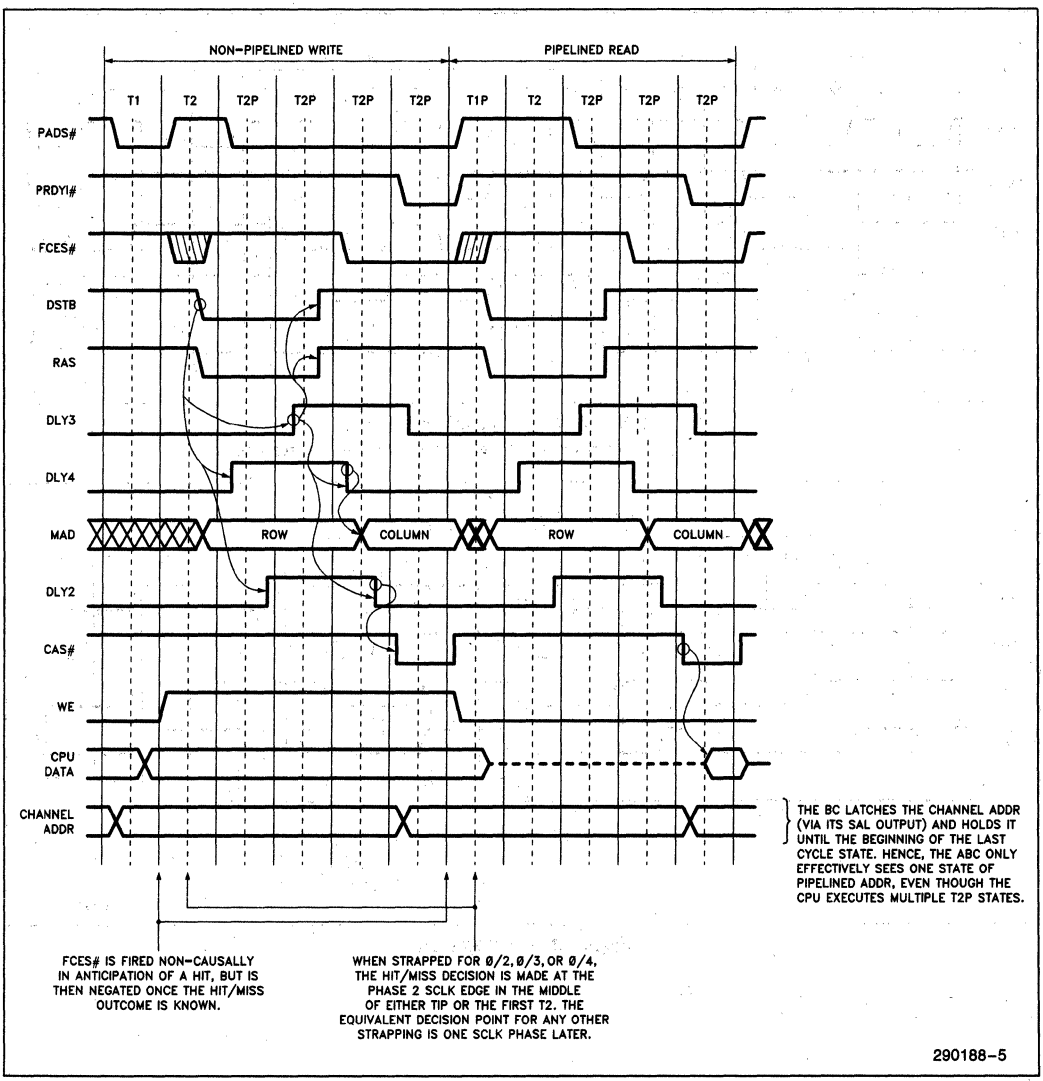


Figure 4. 0/2, 0/3, 0/4 Page Misses (Diagram Depicts 0/3 Operation. In 0/2, FCES# Fired One State Earlier. In 0/4, FCES# Fired One State Later.)

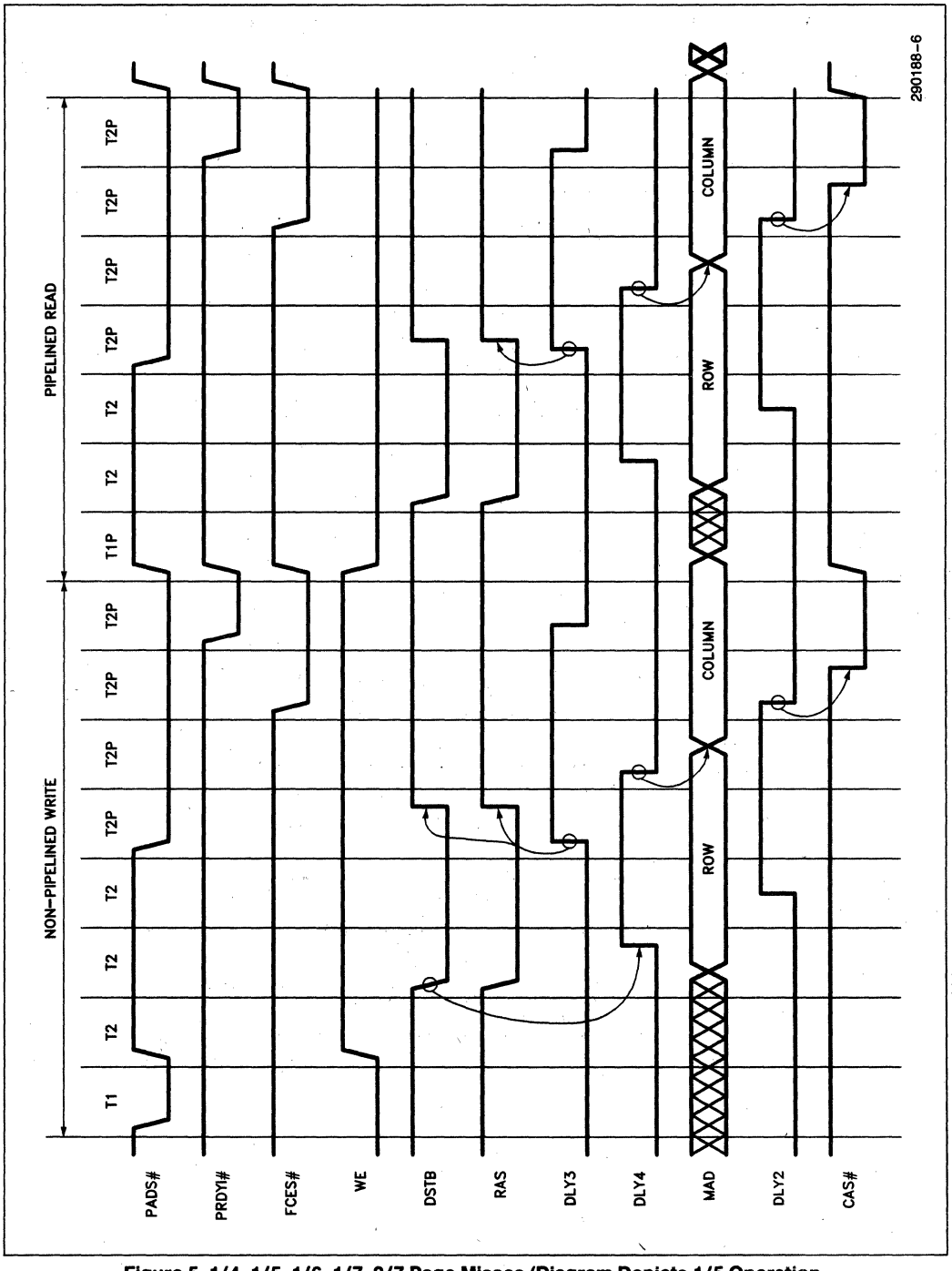
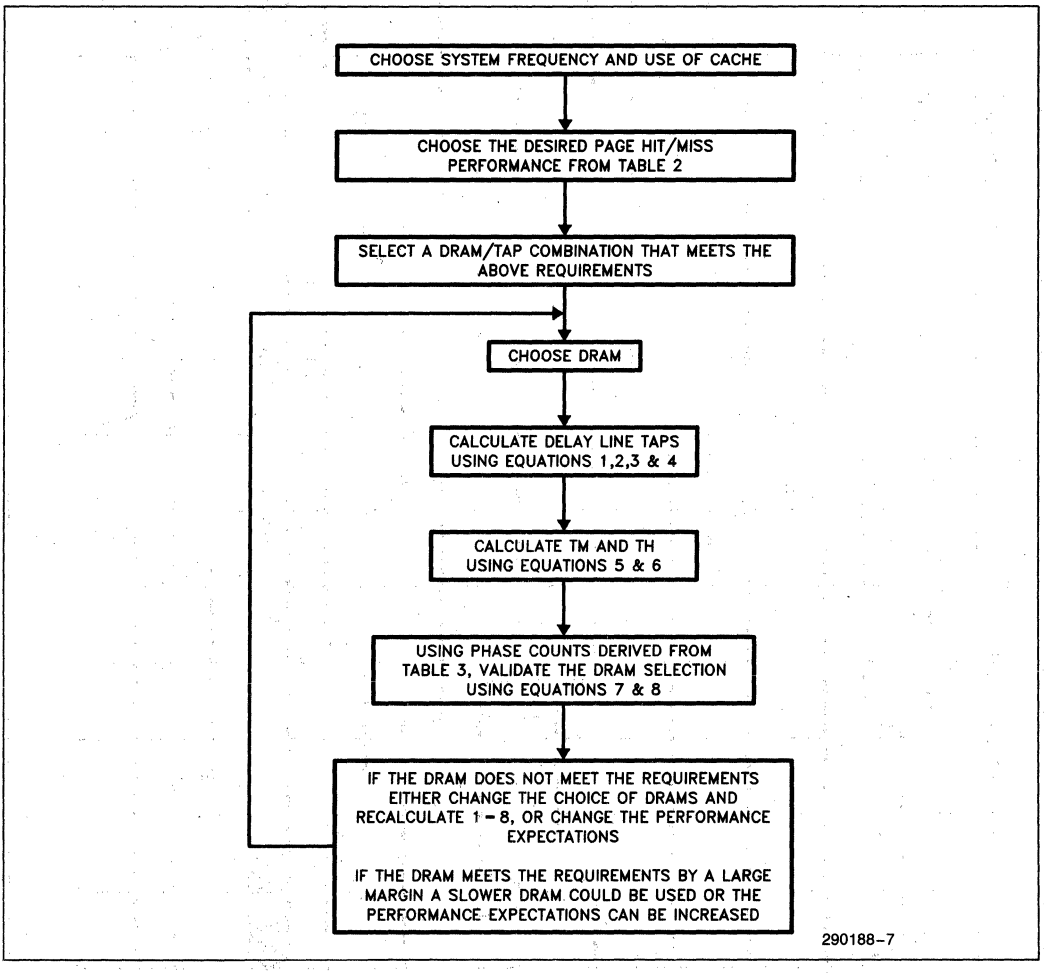


Figure 5. 1/4, 1/5, 1/6, 1/7, 2/7 Page Misses (Diagram Depicts 1/5 Operation. FCES# is Fired One State Earlier in 1/4 Operation, One State Later in 1/6 Operation, and Two States Later in Either 1/7 or 2/7 Operation.)

DRAM AND DELAY LINE TAP SELECTION

This chapter illustrates the methods that should be used to determine the delay line taps for a given DRAM, and the number of wait states a given DRAM will require.

The Flow Chart below should be used to select a DRAM/Delay line tap combination that meets the performance requirements of a system.



DELAY LINE TAP SELECTION

Function of the 4 Delay Line Taps

DLY1— Guarantees max. DRAM data from CHRDY on Micro Channel

DLY2— Guarantees the minimum RAS to CAS delay and DRAM address setup to CAS

DLY3— Guarantees min. RAS# precharge time

DLY4— Guarantees min. address hold to RAS#

Simplified DRAM Tap Selection Equations

DLY1 is the maximum of the following:

80386 System—

$$\text{Trac (Max)} - 10 \quad (1a)$$

$$\text{Trcd (Min)} + \text{Tcac (Max)} \quad (1b)$$

$$\text{Tasc (Min)} + \text{Trah (Min)} + \text{Tcac (Max)} + 20 \quad (1c)$$

80386SX System—

$$\text{Trac (Max)} - 25 \quad (1a)$$

$$\text{Trcd (Min)} + \text{Tcac (Max)} - 15 \quad (1b)$$

$$\text{Tasc (Min)} + \text{Trah (Min)} + \text{Tcac (Max)} + 5 \quad (1c)$$

DLY2 is the maximum of the following:

$$\text{Trcd (Min)} + 10 \quad (2a)$$

$$\text{Tasc (Min)} + \text{Trah (Min)} + 30 \quad (2b)$$

$$\text{DLY3} = \text{Trp (Min)} \quad (3)$$

$$\text{DLY4} = \text{Trah (Min)} + 10 \quad (4)$$

DRAM Access Time Calculations

Two access time parameters have been derived, one for hits (Th) and one for misses (Tm). These are the time from the decision to start a DRAM access to the time that data is available to the motherboard CPU.

$$\text{Th} = \text{Tcac (Max)} + \text{K1} \quad (5)$$

Tm is the maximum of the following:

$$\text{DLY3} + \text{Trac (Max)} + \text{K2} \quad \text{(RAS Path Limited)} \quad (6a)$$

$$\text{DLY3} + \text{DLY2} + \text{Tcac (Max)} + \text{K3} \quad \text{(CAS Path Limited)} \quad (6b)$$

The constants K1, K2 and K3 in equations 5 and 6 are simply a sum of all the propagation delay elements in the appropriate data access path including capacitive load derating:

$$\text{K1} = \underset{\text{(T41A)}}{\text{ABC CAS\# DLY}} + \underset{\text{(INCLUDE DERATE)}}{\text{CAS\# BUFFER DLY}} + \underset{\text{('F657)}}{\text{DATA BUFFER DLY}} = 44.5$$

$$\text{K2} = \underset{\text{(T32E)}}{\text{ABC DSTB DLY}} + \underset{\text{('AS02)}}{\text{NOR GATE DLY}} + \underset{\text{(T32G)}}{\text{ABC RAS DLY}} + \underset{\text{(INCLUDE DERATE)}}{\text{RAS BUFFER DLY}} + \underset{\text{('F657)}}{\text{DATA BUFFER DLY}} = 79$$

$$\text{K3} = \underset{\text{(T32E)}}{\text{ABC DSTB DLY}} + \underset{\text{('AS02)}}{\text{2X NOR GATE DLY}} + \underset{\text{(T34)}}{\text{ABC CAS\# DLY}} + \underset{\text{(INCLUDE DERATE)}}{\text{CAS\# BUFFER DLY}} + \underset{\text{('F657)}}{\text{DATA BUFFER DLY}} = 81.5$$

(See Figure 6 for a diagram of the timing model used.)

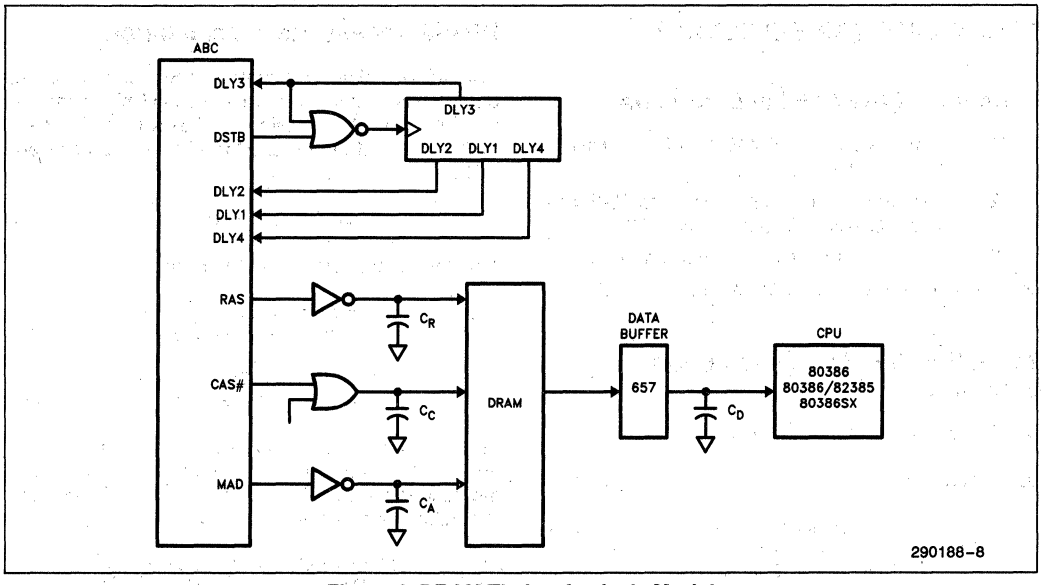


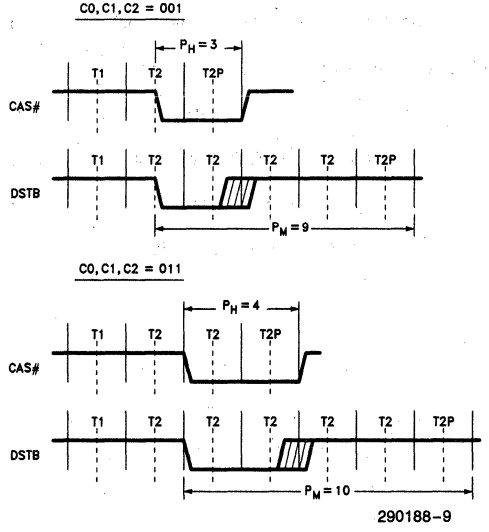
Figure 6. DRAM Timing Analysis Model

Tables 2 and 3 define the number of DRAM wait states that the motherboard CPU will see for all combinations of the configuration bits C0, C1 and C2.

Table 3. Configuration and DRAM Calculation Clock Phase Counts

Config Inputs			SCLK Phases	
C0	C1	C2	PH	PM
0	0	0	3	7
0	0	1	3	9
0	1	0	3	11
0	1	1	4	10
1	0	0	4	12
1	0	1	4	14
1	1	0	4	16
1	1	1	6	16

PH, PM Definition Examples



NOTES:
1. The phase counts are from the clock edge that either fires CAS# (Hit) or fires DSTB (Miss) to the end of cycle, as shown above.
2. Cache systems typically require additional read data setup. The BC WS# (Wait State) strap inserts an additional wait state into system board memory reads, and can be used to accommodate this increased setup if required. If WS# is tied low, then the phase counts above all increase by two.

Validation of DRAM Selection

After Th and Tm have been calculated the performance expectations of the DRAM can be checked.

First the number of clock phases both hit and miss DRAM cycles are allowed are calculated. For Configurations 0, 1 & 2 this is 2 × the number of non-pipelined waitstates + 1. For other Configurations this is just 2 × the number of non-pipelined waitstates. The phases for hits are called Ph, Pm for misses.

The following equations must then be satisfied:

$$Ph/(2*Clk\ Freq.) - Th - CPU\ Data\ setup \geq 0 \quad (7)$$

$$Pm/(2*Clk\ Freq.) - Tm - CPU\ Data\ setup \geq 0 \quad (8)$$

Two examples of Delay Line Tap Selection and DRAM Performance Verification are given below, one for an 80386 system and one for an 80386SX system.

Sample Calculation—80386 20 MHz 100 ns DRAMs 1/5 Performance

Target Dram

Key Specs (ns)

Trac	100
Trp	80
Trah	15
Trcd	25
Tasc	0
Tcac	35

Delay Line Calculations

DLY3 = Trp = 80 ns

DLY4 = Trah + 10 = 15 + 10 = 25 ns

DLY2 = Trcd + 10 = 25 + 10 = 35 ns
or
= Tasc + Trah + 30 = 0 + 15 + 30 = 45 ns

DLY1 = Trac − 10 = 100 − 10 = 90 ns
or
= Trcd + Tcac = 25 + 35 = 60 ns
or
= Tasc + Trah + Tcac + 20
= 0 + 15 + 35 + 20 = 70 ns

Delay Line Summary

DLY1 90
DLY2 45
DLY3 80
DLY4 25

Page Hit Access Time & Performance

Th = Tcac + 44.5
= 35 + 44.5 = 79.5 ns

80386 Data Setup Time = 10 ns

1 Waitstate Margin (Pipelined)

Ph/(2*CLK Freq.) − Th − 386 Data Setup = 100 − 79.5 − 10
= 10.5 ns

Page Miss Access Time & Performance

Tm is the maximum of EQN 6a and 6b.

Tm = DLY3 + Trac + 79
= 80 + 100 + 79 = 259

or

Tm = DLY3 + DLY2 + Tcac + 81.5
= 80 + 45 + 35 + 81.5 = 241.5

5 Waitstate (Pipelined) Margin

Pm/(2* CLK Freq.) − Tm − 80386 Data Setup = 300 − 259 − 10
= 31 ns

Sample Calculation—80386SX 16 MHz 100 ns DRAMs

0/3 Performance

Only DLY1 changes

DLY1 = Trac − 25 = 100 − 25 = 75 ns

Delay Line Summary

DLY1 75
DLY2 45
DLY3 80
DLY4 25

Page Hit Access Time & Performance

Th = Tcac + 44.5
= 35 + 44.5 = 79.5

80386SX Data Setup = 5 ns

0 Waitstate Margin (Pipelined)

Ph/(2* CLK Freq.) − Th − 80386SX Data Setup > = 0
93.75 − 79.5 − 5 = 9.25 ns

Page Miss Access Time & Performance

Tm = 259

(Same as for 20 MHz 386 Case)

3 Waitstate Margin (Pipelined)

Pm/(2* CLK Freq.) − Tm − 80386SX Data Setup > = 0
281.25 − 259 − 5 = 17.5 ns

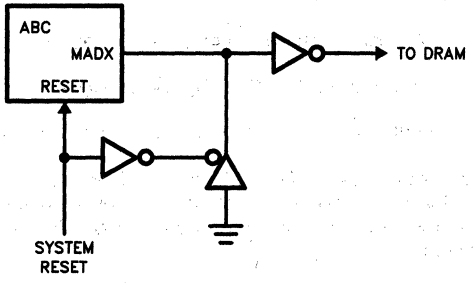
MAD BUS RESET CONFIGURATION

The ABC samples the MAD bus at the falling edge of RESET to determine system configuration as shown:

Table 4

MAD Bus Bits											Options
10	9	8	7	6	5	4	3	2	1	0	
0	0										256K DRAMs
0	1										1M DRAMs
1	1										4M DRAMs
										0	32 Bit Memory
										1	16 Bit Memory
									0		SS1 = 0
									1		SS1 = 1
							0	0			Invalid
							0	1			Single Bank
							1	0			Two Banks
							1	1			Four Banks
						0					Reserved
						1					Normal Mode
					0						C2 = 0
					1						C2 = 1
				0							C1 = 0
				1							C1 = 1
			0								C0 = 0
			1								C0 = 1
		0									SS2 = 0
		1									SS2 = 1

NOTES:
1. When either MAD09 or MAD10 is sensed as a zero, it's output driver is tri-stated, thus allowing these two pins to be tied directly to ground. For example, if 1M DRAMs are used, MAD10 should be tied to ground, since 1M DRAMs only require use of bits 0–9. MD09 should be lightly pulled up (~ 10K).
2. For MAD bits 0–8, any bit that is to be sensed as a one should be lightly pulled up. Any bit that is to be sensed as a zero must be driven low by a tri-state driver that is active while the ABC RESET input is active, and then tri-stated from the falling edge of RESET, as depicted in the figure:



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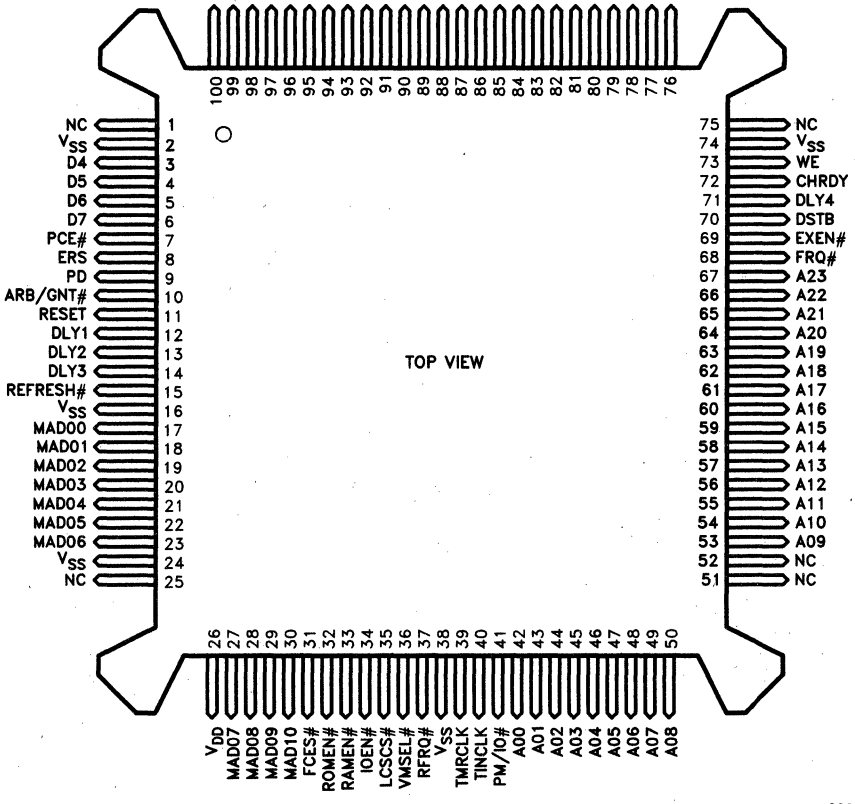
3. MAD4 sensed as a 0 is a reserved state. This bit should be lightly pulled up.
4. MAD0 is typically configured low for an 80386 system, and high for an 80386SX system.
5. MAD1 and MAD8 are respectively the system select bits SS1 and SS2. These bits determine the definition of ABC ports E0, E1 and 103, as described in the section on ABC ports and registers.
6. MAD5, MAD6 and MAD7 are respectively the DRAM performance select bits C2, C1 and C0. The effect of these bits is described in the DRAM control section.

82309 Address Bus Controller Pin Definitions

Signal Name	Pin Number	I/O	Description
A<00:23>	42–50, 53–67	I	Micro Channel Address 0 to 23
HIMEM#	84	I	Micro Channel Address 24 to 31 = FF (Active Low). Used in decoding the top-of-memory mapping of the BIOS EPROMs.
MADE24	85	I	Micro Channel Address 24 to 31 = 00 (Active High)
ROMEN#	32	O	EPROM Decode. In systems that support shadow RAM, if ROM is enabled (bit 1 in port E1), accesses to ROM space actually generate both ROMEN# and RAMEN#. In this mode, reads are from ROM, and writes are to RAM.
RAMEN#	33	O	DRAM Decode
IOEN#	34	O	Motherboard I/O devices decode (Active Low). Decode also includes memory decode of video RAM.
LCSCS#	35	O	Chip Select for the LCS (82306) Chip (Active Low). Decodes address range 0–3FFH when CPU master, or 100–3FFFH when CPU is not master.
VMSEL#	36	O	VGA Memory Space Selected (Active Low) (000A0000–000BFFFF)
S0#	89	I	Micro Channel S0# Signal
S1#	90	I	Micro Channel S1# Signal
PM/IO#	41	I	Microprocessor M/IO# Signal
PW/R#	91	I	Microprocessor W/R# Signal
PD/C#	92	I	Microprocessor D/C# Signal
PADS#	93	I	Microprocessor ADS# Signal
SCLK	94	I	Microprocessor CLK2
HLDA	95	I	HLDA Signal from the Processor
PRDYI#	96	I	READY# Signal from the Processor
M/IO#	86	I	Micro Channel M/IO# Signal
CMD#	87	I	Micro Channel CMD Signal

82309 Address Bus Controller Pin Definitions (Continued)

Signal Name	Pin Number	I/O	Description
WE	73	O	DRAM Write Enable Signal (Active High)
RAS<0:3>	76–79	O	DRAM RAS Strobes (Active High)
CAS# <0:3>	80–83	O	DRAM CAS Strobe Enables (Active Low)
MAD<00:10>	17–23, 27–30	B	DRAM Muxed Address bus. These signals are sampled at reset to determine ABC configuration.
DSTB	70	O	Output to Delay Line. A pulse put into the delay line controls page miss timing.
DLY<1:4>	12–14, 71	I	Inputs from the Delay Line. DLY1 controls CHRDY timing in non-CPU cycles. DLY2 controls RAS active to CAS active timing. DLY3 controls RAS precharge, and DLY4 controls row-to-column address multiplex.
CHRDY	72	O	DRAM Ready Signal (Active High)
REFRESH#	15	I	Refresh Operation in Progress (Active Low)
FCES#	31	O	Request to BC to terminate CPU accesses to system board memory.
TINCLK	40	I	14.3 MHz Clock for Refresh Timer
RFRQ#	37	O	Refresh Request (Active Low)
TMRCLK	39	O	14.3 MHz Clock divided by 12 to get 1.19 MHz.
FRQ#	68	O	Asynchronous Cache Flush Request. Activated in I/O writes to ports E0, E1, or 100–107 (POS Address Space).
EXEN#	69	O	Read/Write Strobe for Ports 00E0–00E7 (Active Low)
ERS	8	I	Sampling Strobe for Ports 00E2–00E7
PD	9	I	Select Signal for POS Register 10X
ARB/GNT#	10	I	Micro Channel ARB/GNT# Signal
D<0:7>	97–100, 3–6	I/O	Data Bus
PCE#	7	O	Enable Parity Checking (MER<0>)
RESET	11	I	Synchronous reset input. RESET falling edge used to synchronize ABC internal clock to CPU phase.
NC	1, 25, 51, 52, 75		No Connect
V_{DD}	26, 28		Power
V_{SS}	2, 16, 24, 38, 74		Ground



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NOTE:
NC = No Connect

82309 PARAMETRICS

ABSOLUTE MAXIMUM RATINGS*

Case Temperature under Bias .... −40°C to +85°C
Storage Temperature ..... −65°C to +150°C
Voltage to Any Pin with
Respect to Ground ..... −0.3V to (V_{CC}+0.3)V
DC Supply Voltage (V_{CC}) ..... −0.3V to +7.0V
DC Input Current ..... ±10 mA

**Notice: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

NOTICE: Specifications contained within the following tables are subject to change.

D.C. CHARACTERISTICS

T_C = 0°C to +70°C, V_{CC} = 5V ±10%

Symbol	Parameter	Min	Max	Units	Conditions
V_{IL}	Input Low Voltage		0.8	V	
V_{IH}	Input High Voltage	2.0		V	
V_{IL}	Input Low Voltage		0.8	V	SCLK
V_{IH}	Input High Voltage	V_{CC} − 0.8		V	SCLK
V_{OL}	Output Low Voltage		0.4	V	I_{OL} = 4 mA
V_{OH}	Output High Voltage	2.4		V	I_{OH} = 4 mA
I_{CC}	Power Supply Current		180	mA	No DC Loads
I_{LI}	Input Leakage Current		±10	μA	$V_{SS} < V_{IN} < V_{CC}$
I_{OZ}	Tri-State Output Leakage Current		±10	μA	$V_{SS} < V_{OUT} < V_{CC}$

82309 ADDRESS BUS CONTROLLER A.C. SPECS

T_C = 0°C to +70°C, V_{CC} = 5V ± 10%

Symbol	Parameter	Kit 16 MHz		Kit 20 MHz		Kit 25 MHz		CL(PF)	Notes
		Min	Max	Min	Max	Min	Max		
T1	SCLK PERIOD	31.25		25		20			
T2A	SCLK HIGH/LOW TIME (50%)	12		10		8			
T2B	SCLK HIGH/LOW TIME (90%)	8		6.5		6			
T3	RESET SETUP	10		10		10			
T4	RESET HOLD	4		4		4			
T5A	STATUS SETUP TO SCLK	11		11		8			1
T5B	CMD# SETUP TO SCLK	11		11		8			1
T6	PADS#,PW/R#,PD/C#,PM/IO# SETUP	25		22		13			
T7	PADS#,PW/R#,PD/C#,PM/IO# HOLD	4		4		4			
T8	ADDRESS,M/IO#,MADE24,REFRESH# SETUP	10		10		10			
T9	ADDRESS,M/IO#,MADE24,REFRESH# HOLD	10		10		10			
T10	ADDRESS, M/IO# SETUP	40		50		36			3
T11	ADDRESS, M/10# HOLD	30		30		30			3, 12
T12	MADE24 SETUP	32		40		28			3
T13	MADE24 HOLD	30		30		30			3, 12
T14	M/IO#,ARB/GNT# SETUP TO ERS	20		20		20			
T15	M/IO#,ARB/GNT# HOLD FROM ERS	10		10		10			
T16	PRDYI# SETUP	18		18		15			
T17	PRDYI# HOLD	3		3		3			
T18A	ROMEN#,RAMEN#,IOEN#,VMSEL# DLY FRM MADE24 HIMEM#	2	30	2	30	2	30	75	
T18B	ROMEN#,RAMEN#,IOEN#,VMSEL# DLY FRM ADDR	2	38	2	38	2	38	75	15
T18C	ROMEN#,RAMEN#,IOEN#,VMSEL# DLY FRM A20	2	35	2	35	2	35	75	15
T19	LCSCS# DELAY	2	45	2	45	2	45	75	
T20A	FCES# DELAY FROM SCLK	3	45	3	35	3	30	25	5
T20B	FCES# DLY FRM ADDR, M/IO#, MADE24		50					25	2, 5
T21	PD SETUP TO CMD# ↑	100		100		100			
T22	WRITE DATA SETUP	30		30		30			
T23	WRITE DATA HOLD	5		5		5			
T24	READ DATA VALID DELAY		200		200		200	75	
T24A	CMD# ↓ TO READ DATA LOW-Z	25		25		25		75	
T25	READ DATA FLOAT DELAY	2	35	2	35	2	35	75	
T26	EXEN# DELAY (INACTIVE)	2	50	2	50	2	50	50	
T26A	EXEN# DELAY (ACTIVE)	25	150	25	150	25	150	50	
T27A	CHRDY DELAY (FROM ADDR)	2	50	2	50	2	50	50	4, 5, 7
T27B	CHRDY DLY FROM STATUS OR CMD#	0	33	0	33	0	33	50	4, 5, 7
T29	TMRCLK HIGH/LOW TIME	300		300		300		50	
T30	RFRQ# PULSE WIDTH	300		300		300		50	
T31	TINCLK HIGH/LOW TIME	21		21		21			
T32B	CMD# ↑-RAS ↓ (REFRESH CYCLE ONLY)	0	55	0	55	0	55	75	10
T32C	CMD# ↑-CAS# ↑	0	38	0	38	0	38	75	
T32E	SCLK-DSTB ↓	4	27	4	27	4	27	50	8
T32F	DLY3 ↑-DSTB ↑	0	50	0	50	0	50	50	
T32G	DLY3 ↑-RAS ↑	4	26	4	26	4	26	75	
T32I	SCLK-RAS ↓	8	40	8	40	8	40	75	8
T33	DLY1 ↓ TO CHRDY ↑	5	30	5	30	5	30	50	
T34	DLY2 ↓ TO CAS# ↓	3	27	3	27	3	27	75	

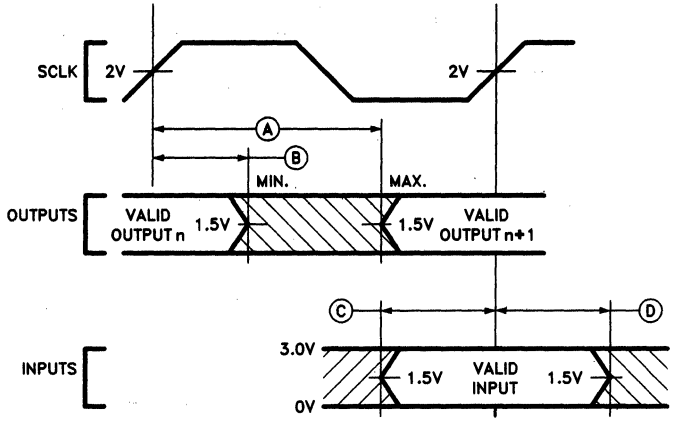
82309 ADDRESS BUS CONTROLLER A.C. SPECS (Continued)

Symbol	Parameter	Kit 16 MHz		Kit 20 MHz		Kit 25 MHz		CL(PF)	Notes
		Min	Max	Min	Max	Min	Max		
T35	CMD# ↓ TO CAS# ↓ (WRITE CYCLES ONLY)	25	115	25	115	25	115	75	6
T39A	WE DLY FROM STATUS	2	30	2	30	2	30	75	14
T39B	WE DLY FROM CMD# ↑	2	30	2	30	2	30	75	14
T41A	CAS# ↓ DELAY FROM SCLK (READS)	2	30	2	30	2	30	75	
T41B	CAS# ↑ DELAY FROM SCLK	5	34	5	34	5	34	75	9
T41C	CAS# ↓ DELAY FROM SCLK (WRITES)	2	38	2	38	2	38	75	
T43A	ADDR TO MAD DELAY (COLUMN ADDR)		45		45		40	75	13
T43B	SCLK TO MAD DELAY (COLUMN ADDR)		36		36		31	75	13
T43C	CMD# TO MAD DELAY (COLUMN ADDR)		38		38		38	75	13
T43D	SCLK TO MAD DELAY (ROW ADDR)		50		50		50	75	13
T44	WE DELAY FROM SCLK	2	42	2	42	2	42	75	
T45	DLY4 ↓ TO MAD	6	32	6	32	6	32	75	
T46	MAX PAGE MODE RAS ACTIVE	15 μs		15 μs		15 μs			10, 11

NOTES:

1. Status and CMD# are asychronous inputs. T5 simply guarantees that they are recognized at a particular clock edge.
2. FCES# is speced from address only in 0WS pipelined/1WS non-pipelined memory cycles, which are only supported at 16 MHz.
3. Address, M/IO# and MADE24 setup and hold times are speced relative to the Phase 2 SCLK edge only in 0WS pipelined/1WS non-pipelined memory cycles, which are only supported at 16 MHz. (This Phase 2 edge is in the middle of the first T2 state, or the middle of the T1P state.)
4. The 82309 de-activates CHRDY for motherboard I/O and VGA Memory cycles (as decoded by IOEN#), and then re-activates it when CMD# is activated. The 82309 also de-activates CHRDY for non-CPU (DMA or channel master) accesses to motherboard DRAM that are decoded as page misses. CHRDY is then re-activated according to the appropriate external DRAM control delay line tap (DLY1), or else when CMD# is activated, whichever comes later.
5. FCES# is used to terminate CPU accesses to motherboard DRAM, as these cycles are not broadcast on the Micro Channel. CHRDY is used to terminate DMA and channel master accesses to motherboard DRAM, which are broadcast.
6. The large value for T35 (Min) guarantees that data being written into motherboard DRAM by a channel master or DMA controller has adequate time to propogate through the data buffers between the channel or DMA and memory. T35 (Min) is guaranteed on any non-CPU write, both page hit and page miss. (The Micro Channel specs 0NS of data setup to CMD# active.) T35 (Max) applies only when CMD# ↓-to-CAS# ↓ is indeed the limiting spec; specifically, when neither T34 (Max) nor T41A (Max) limits CAS# activation.
7. The 82309 guarantees that any time it de-asserts CHRDY, it will not re-assert it until after CMD# is activated.
8. These specs are referenced with respect to the causal SCLK edge, which differs in different frequency systems. At 16 MHz, the appropriate edge is one clock phase after the edge that recognizes status in non-CPU cycles, or one phase after the edge that samples PADS# active in CPU cycles. At 20 MHz, the appropriate edge is two clock phases after these events. The 82309 distinguishes 16 MHz from 20 MHz via the memory performance configuration inputs C0, C1 and C2. 16 MHz is assumed anytime these inputs indicate a zero wait state pipelined read page hit. (C0, C1, C2 = 000,001,010).
9. This spec insures a minimum CAS# high time of 25 ns at 16 MHz. (16 MHz is the worst case since the CAS# inactive and CAS# active SCLK edges are only one phase apart. At 20 MHz, these edges are always at least two phases apart.)
10. Refresh cycles are RAS only, and are forced to be page misses. Thus, the refresh interval (typically 15 μs) defines the required page mode RAS active time. RAS is de-activated at the end of a refresh cycle since typical page mode DRAMs spec a maximum RAS active time less than 15 μs for refresh cycles. (Note that the first access to any bank following a refresh cycle is also a forced page miss.)
11. Functional spec only . . . Not tested. Max page mode RAS active is governed by refresh interval.
12. T11 and T13 are speced relative to the clock edge that samples the page hit/miss outcome. This edge also is used by the 82309 to internally latch the channel address. At 20 MHz, T11 & T13 are speced relative to the end of the first T2 state or the end of T1P. Note, however, the large T11 & T13 values in the spec, which seem like they would be difficult to meet going directly into a T2P, where the CPU puts out a new address. This is not a problem, however, since the minimum memory cycles at 20 MHz run T1•T2•T2P•T2P•T1P•T2P•T2P, and the 82308 does not open the transparent channel address latch until the beginning of the last T2P, i.e., the 82309 effectively only sees the last T2P in terms of pipelined addressing regardless of how many T2P states the CPU actually executes.
13. T43A, T43B, and T43C all refer to column address, as the 82309 assumes a page hit as the default case until proven otherwise. In case of a page miss, the row address is muxed onto the MAD lines from the same clock edge that de-activates RAS and fires a pulse (DSTB) into the delay line. The column address is then muxed onto the MAD lines by delay tap DLY4.
14. In Non-CPU cycles, WE (active high from the 82309) is simply an inverted version of channel S0#, which indicates a write cycle when low. This signal is internally latched (transparent latch) by the leading edge of CMD#, and then released by the trailing edge of CMD#, hence the need for T39B.
15. A20 typically has more logic in its path than the other address bits, hence the tighter spec. T18B applies to all bits except A20.

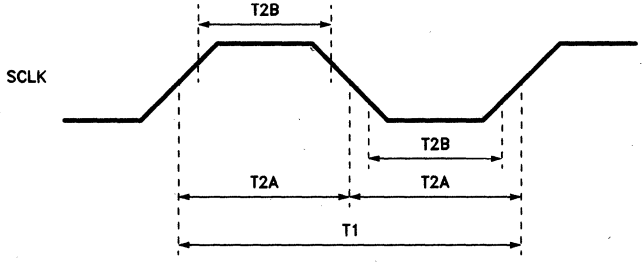
DRIVE LEVELS AND MEASUREMENT POINTS FOR A.C. SPECIFICATIONS



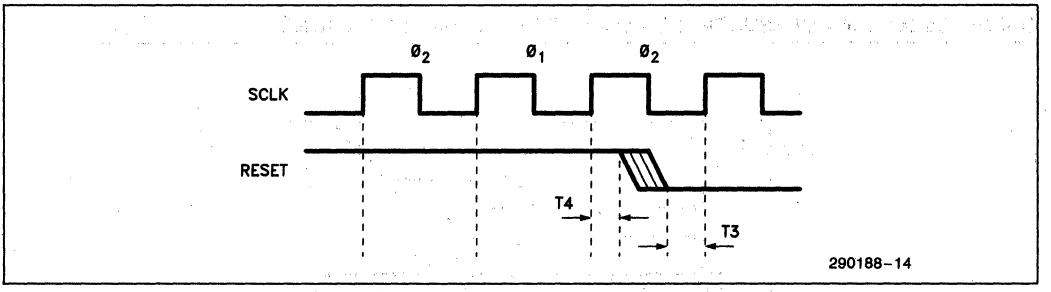
290188-12

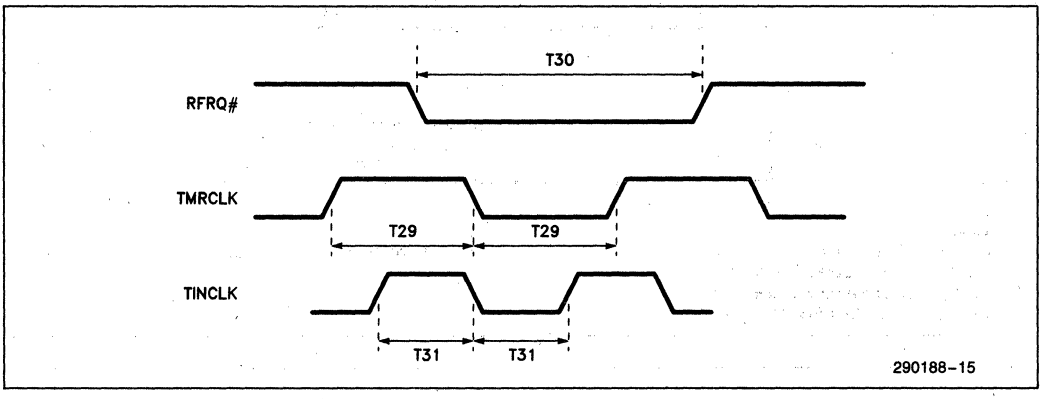
LEGEND:
A. Maximum Output Delay Specification.
B. Minimum Output Delay Specification.
C. Minimum Input Setup Specification.
D. Minimum Input Hold Specification.

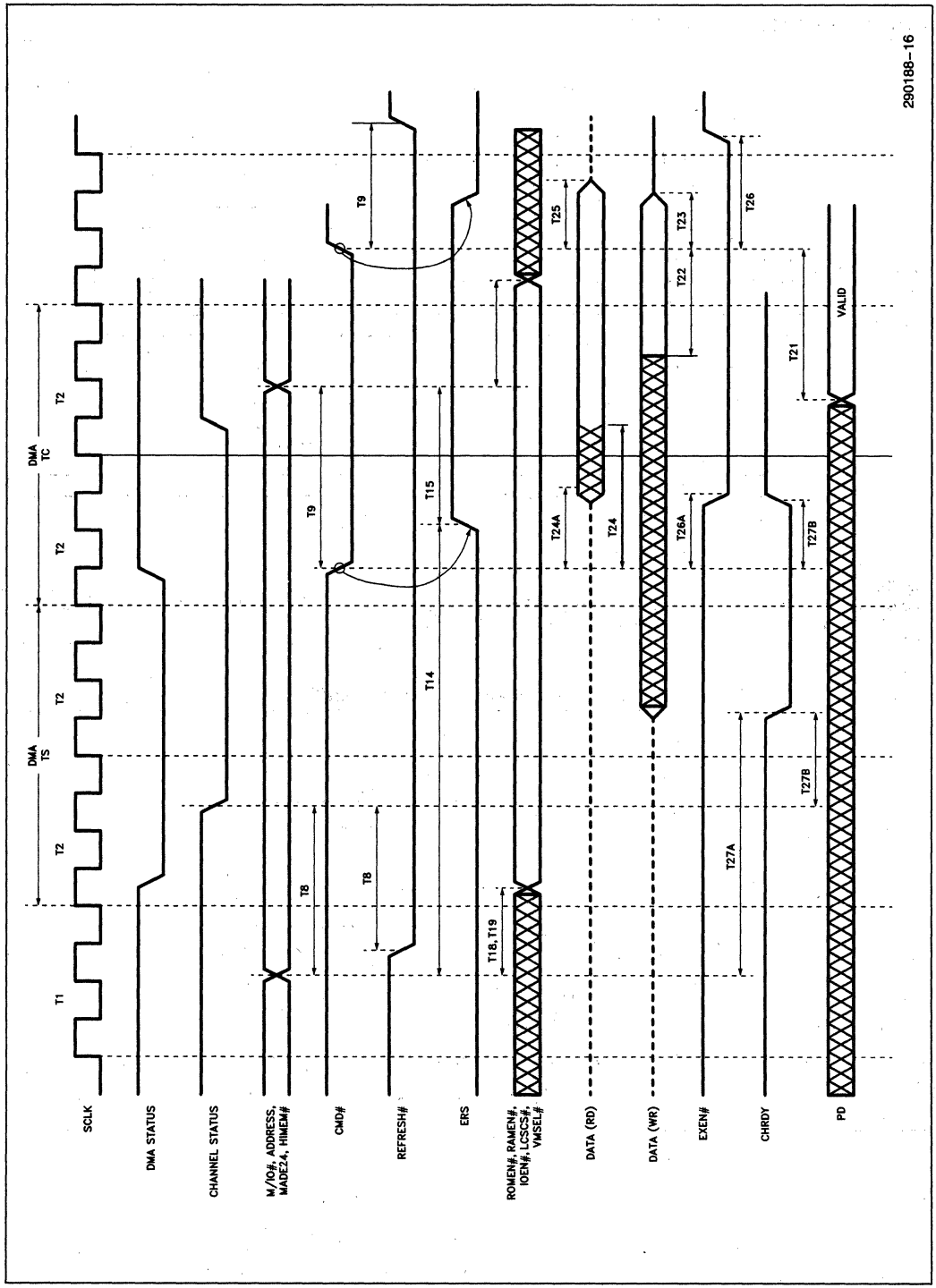
Input waveforms have tr ≤ 2.0 ns from 0.8V to 2.0V.



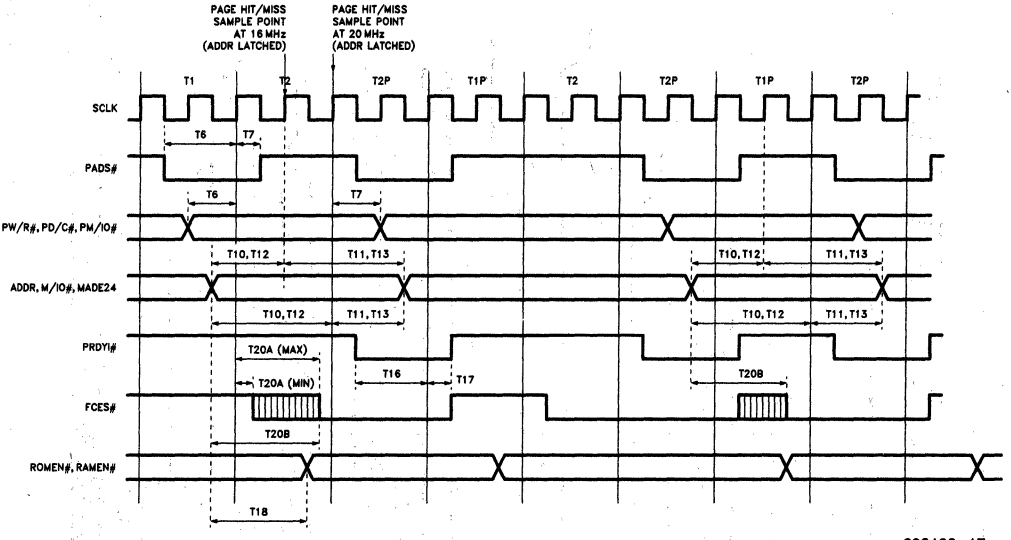
290188-13


Ø2
Ø1
Ø2
SCLK
RESET
T4
T3
290188-14


T30
RFRQ#
TMRCLK
T29
T29
TINCLK
T31
T31
290188-15

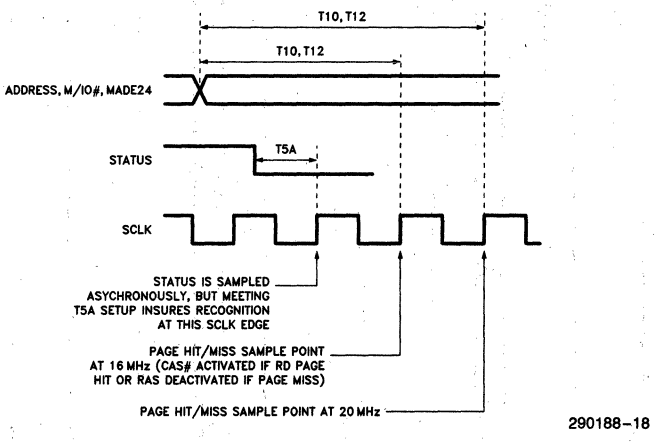

290188-16
SCLK
DMA STATUS
CHANNEL STATUS
M/IO#, ADDRESS, MADE24, HIMEM#
CMD#
REFRESH#
ERS
ROMEN#, RAMEN#, IOEN#, LCSCS#, VMSEL#
DATA (RD)
DATA (WR)
EXEN#
CHRDY
PD
VALID
T1
T2
DMA TS
DMA TC
T8
T9
T14
T15
T18, T19
T21
T22
T23
T24
T24A
T25
T26
T26A
T27A
T27B

82309/80386 INTERFACE TIMINGS

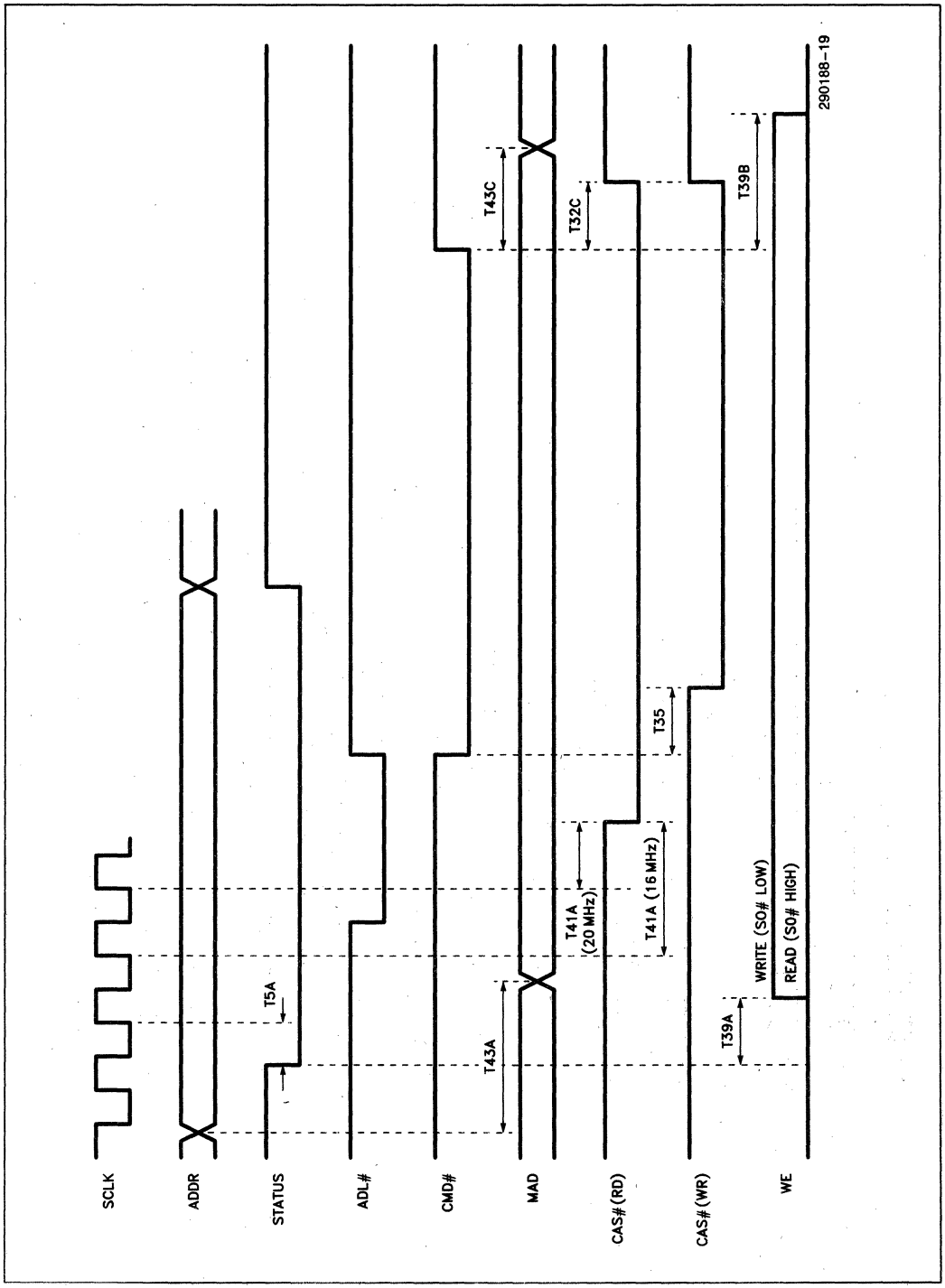


NOTE:
Once the ABC fires FCES#, it remains active until the ABC detects and end of cycle via its PRDYI# input. This allows the BC or other external devices to extend DRAM cycles if desired.

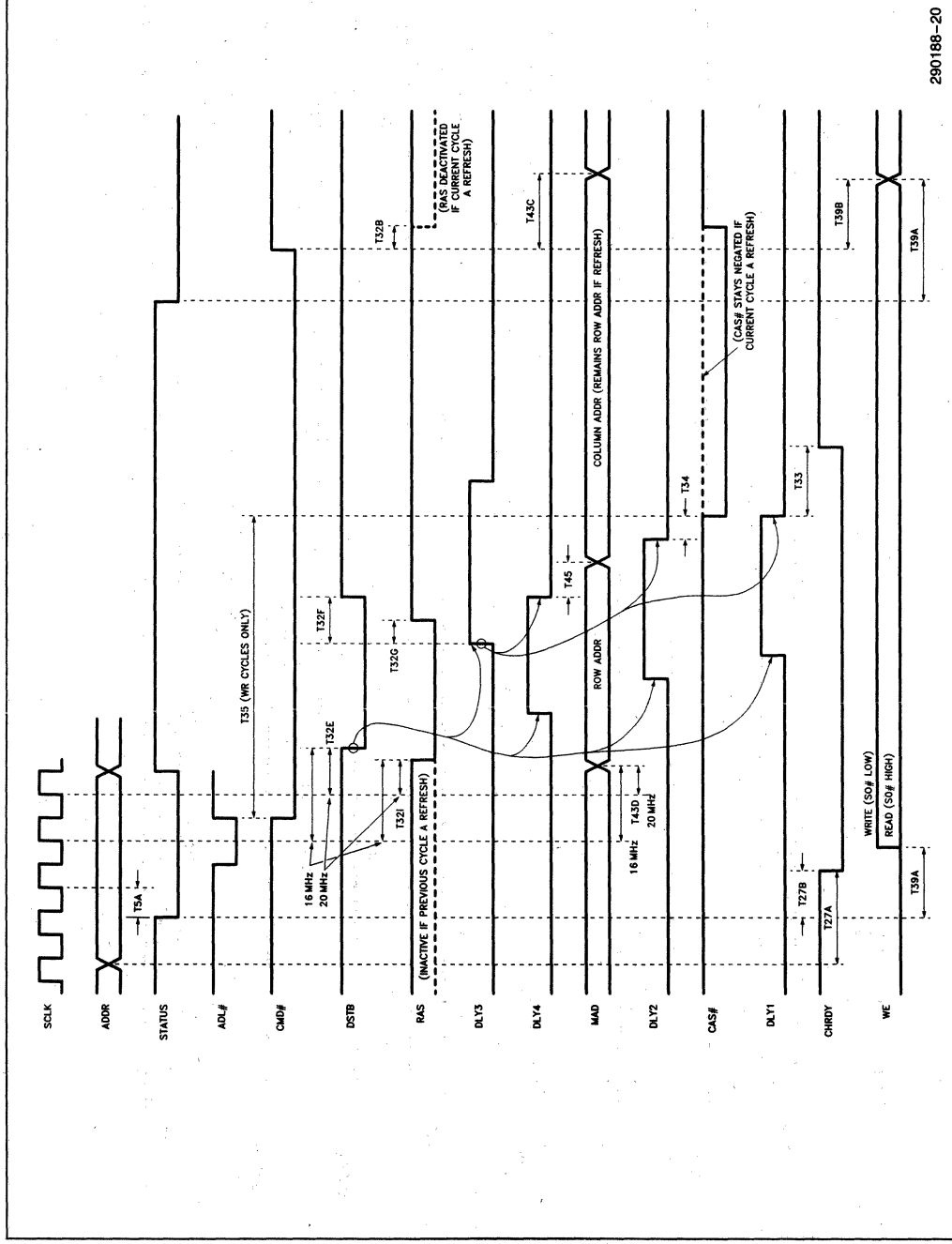
ADDRESS, M/IO#, MADE 24 SETUP FOR DMA/Micro Channel MASTER



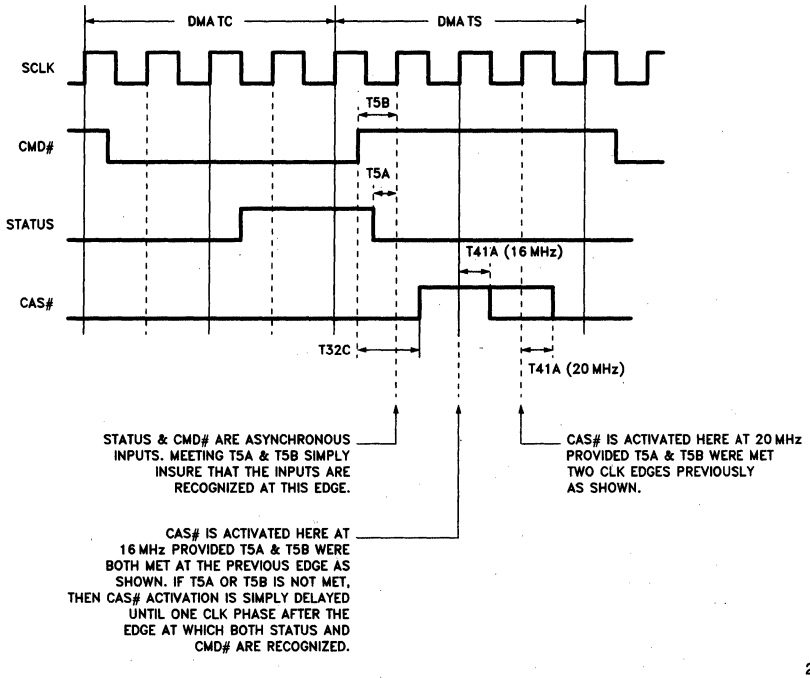
DMA/CHANNEL MASTER ACCESSES (PAGE HIT)



DMA/CHANNEL MASTER ACCESSES TO DRAM (PAGE MISS)



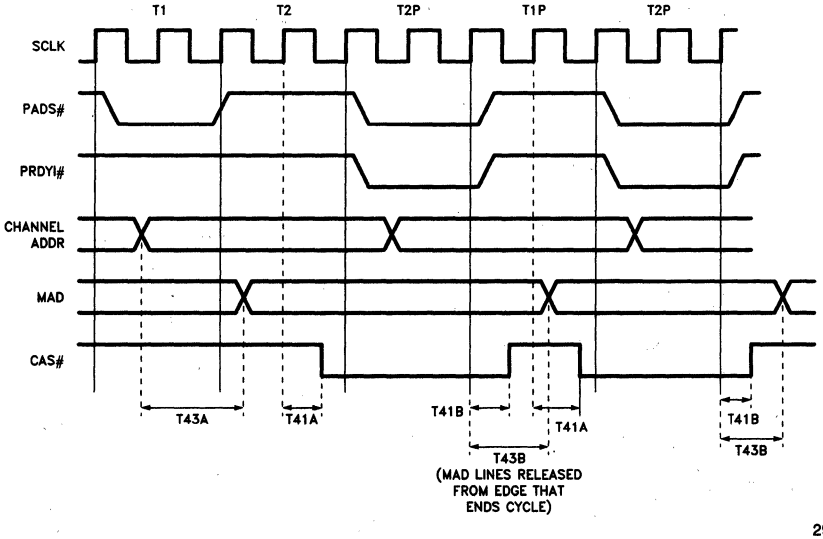
DMA MASTER ... BACK-TO-BACK RD PAGE HITS



290188-21

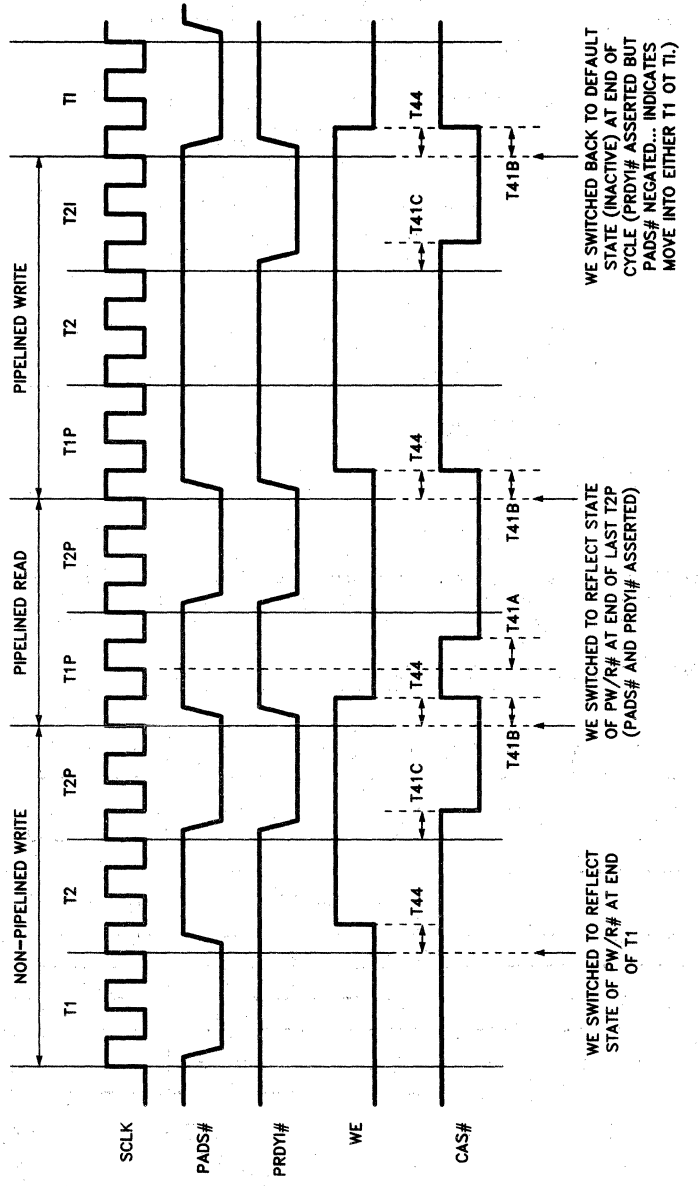
The requirement that T5B be met before CAS# is allowed (one or two phases later) insures adequate CAS# high time in back-to-back cycles. (One SCLK phase at 16 MHz; Two SCLK phases at 20 MHz.)

0 WAIT STATE (PIPELINED) READ PAGE HITS



290188-22

WE TIMING IN CPU CYCLES

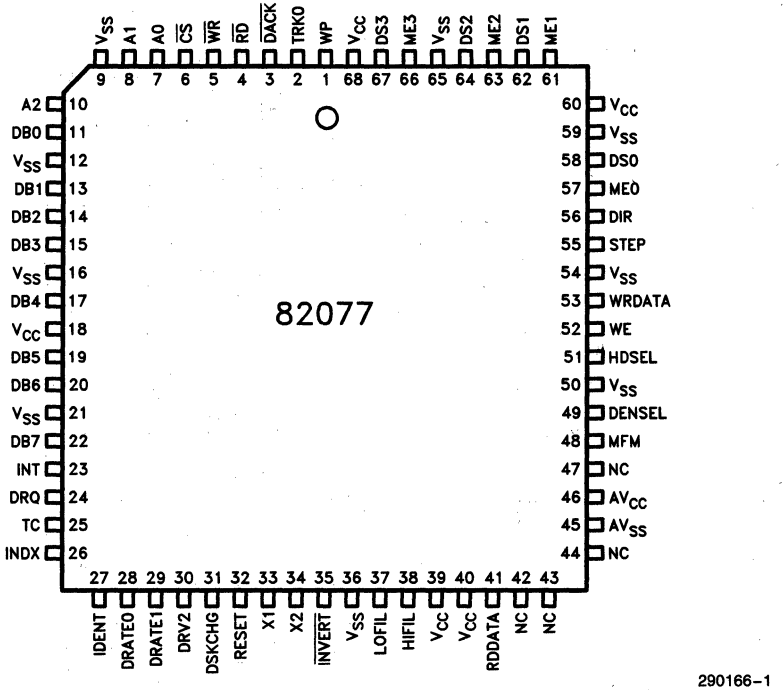


82077
CHMOS SINGLE-CHIP FLOPPY DISK CONTROLLER

- **Single-Chip Floppy Disk Solution**
  - **— 100% PC-AT Hardware Compatible**
  - **— 100% PS/2™ Hardware Compatible**
  - **— Integrated Drive and Data Bus Buffers**
- **Integrated Analog Data Separator**
  - **— 250 Kbits/sec**
  - **— 300 Kbits/sec**
  - **— 500 Kbits/sec**
  - **— 1 Mbits/sec (82077-1 only)**
- **High Speed Processor Interface**
- **Vertical Recording Support**
- **12 mA Data Bus Drivers, 40 mA Disk Drivers**
- **Four Fully Decoded Drive Select and Motor Signals**
- **Programmable Write Precompensation Delays**
- **Addresses 256 Tracks Directly, Supports Unlimited Tracks**
- **16 Byte FIFO**
- **68-Pin PLCC**

The 82077 floppy disk controller has completely integrated all of the logic required for floppy disk control. The 82077, a 24 MHz crystal, a resistor package and a device chip select implements a PC-AT or PS/2™ solution. All programmable options default to compatible values. The dual PLL data separator has better performance than most board level/discrete PLL implementations. The FIFO allows better system performance in multi-master systems (e.g. PS/2™).

The 82077 is fabricated with Intel's CHMOS III technology and is available in a 68-lead PLCC (plastic) package.



290166-1

Figure 1. 82077 Pinout

"For a complete data sheet, please refer to the Floppy Disk Controller section of the Intel Microprocessor and Peripherials Handbook (Volume II. Peripherials)".

PS/2™ is a trademark of IBM.

October 1988
Order Number: 290166-001

82706
INTEL VIDEO GRAPHICS ARRAY

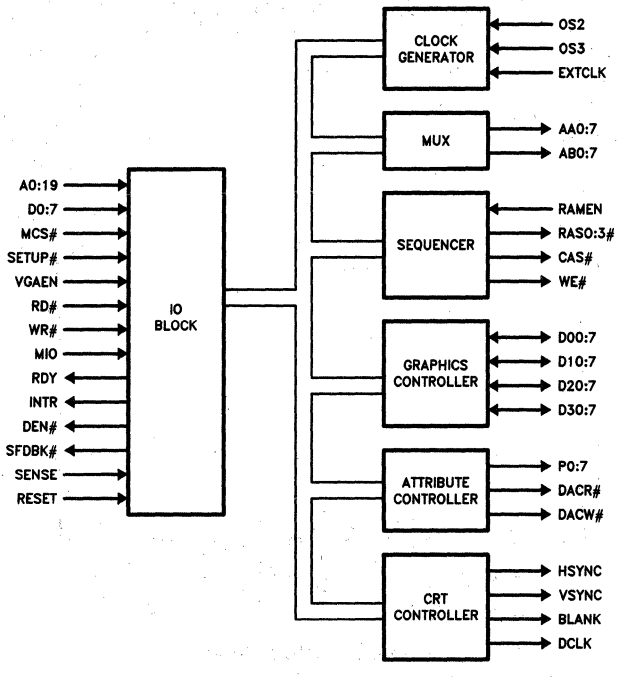
- **Single Chip Video Graphics Array for IBM PC/XT/AT*, Personal System/2* and Compatible Systems**
- **100% Gate, Register, and BIOS Level Compatibility with IBM VGA**
- **EGA/CGA/MDA BIOS Compatibility**
- **Inmos IMSG 171 Palette/DAC Interface**
- **4 mA Drive Capability on Output Pins**
- **Implemented in High Speed CHMOS III Technology**
- **Available in 132-Pin Plastic Quad Flat Pack Package**
  (See Packaging Spec. Order #231369)

The 82706 is the Intel VGA compatible display controller. It is 100% register compatible with all IBM VGA modes and provides software compatibility at the BIOS level with EGA, CGA, and MDA. All video monitors designed for IBM PS/2* systems are supported by the Intel VGA controller. The 82706 provides an 8-bit video data path to any Inmos IMSG 171 compatible palette/DAC. It also acts as a CRT controller and video memory controller. The 82706 supports 256 Kbytes of video memory.

The 82706 is designed for compatibility with the Intel 80286 and 80386 microprocessors and other microprocessors.

Implemented in low power CHMOS technology, the 82706 VGA Controller is packaged in a fine pitch (25 mil) surface mount gull wing package. It can be enabled or disabled under software control via the 82306 Peripheral Bus Controller.

*IBM PC, XT, AT, Personal System/2, PS/2, and MicroChannel are trademarks of International Business Machines.

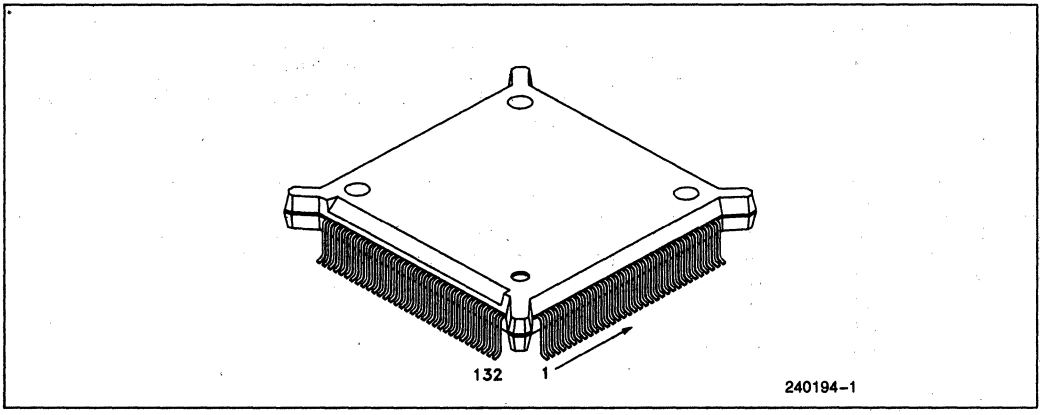


240194-2

Figure 1. Block Diagram

November 1988
Order Number: 240194-002

PLASTIC QUAD FLAT PACK (PQFP)



Pinout (Top View)

82706 PIN DESCRIPTION

Left side of package (top view):

Number	Name	Active	I/O	Description
1	AB4	HI	O	DRAM address bus, planes 2 and 3 (continued from top side of package).
2	AB5	HI	O	
3	AB6	HI	O	
4	AB7	HI	O	
5	V_{DD}			
6	A0	HI	I	System address bus, from current MicroChannel* master. Used to select display buffer words, VGA registers, or video DAC registers.
7	A1	HI	I	
8	A2	HI	I	
9	A3	HI	I	
10	A4	HI	I	
11	A5	HI	I	
12	A6	HI	I	
13	A7	HI	I	
14	A8	HI	I	
15	A9	HI	I	
16	A10	HI	I	
17	A11	HI	I	
18	A12	HI	I	
19	A13	HI	I	
20	A14	HI	I	
21	A15	HI	I	
22	A16	HI	I	
23	A17	HI	I	
24	A18	HI	I	
25	A19	HI	I	
26	$\overline{MCS}$	LO	I	Display buffer (memory) select, generated from A24:20. These inputs do not qualify I/O cycles.
27	RESET	HI	I	Device reset. Tri-States all VGA pins when active.
28	RAMEN	HI	I	RAM Enable. When inactive, tri-states all VGA DRAM interface pins to allow board test of DRAMs or to allow another device to share control of the DRAM.
29	SENSE	HI	I	Switch sense input. The state of this pin can be read from Input Status 0 register, bit 4, and indicates if a monochrome or color monitor is attached to the Display Connector. BIOS requires this information to set the video mode correctly.
30	$\overline{SETUP}$	LO	I	VGA Setup. Used during Programmable Option Select (POS) operation. Analogous to MicroChannel-CD SETUP signals for the other adapter slots. After RESET, the 82706 requires the setup pin to be pulled low. An I/O write to port address XX2h must write a "1" to data bit 0 while setup is low. Then setup must be pulled high. Once this is complete, the 82706 can respond to CPU accesses.
31	VGAEN	HI	I	VGA Enable. Allows VGA to respond to memory or I/O cycles when active.
32	FCO		O	
33	FCI		O	

82706 PIN DESCRIPTION (Continued)

Bottom side of package (top view):

Number	Name	Active	I/O	Description
34	V_{SS}			
35	$\overline{RAS0}$	LO	O	Row Address Strobe for plane 0.
36	$\overline{RAS1}$	LO	O	Row Address Strobe for plane 1.
37	$\overline{RAS2}$	LO	O	Row Address Strobe for plane 2.
38	$\overline{RAS3}$	LO	O	Row Address Strobe for plane 3.
39	$\overline{WE}$	LO	O	RAM Write Enable for all planes.
40	V_{DD}			
41	$\overline{CAS}$	LO	O	Column Address Strobe for all planes.
42	HSYNC		O	Horizontal and Vertical Sync to Display Connector.
43	VSYNC		O	These are programmable to be active high or low.
44	BLANK	LO	O	Video Blank to Video DAC and Display Connector.
45	V_{SS}			
46	$\overline{RD}$	LO	I	Read Strobe, active for memory or I/O cycles.
47	$\overline{WR}$	LO	I	Write Strobe, active for memory or I/O cycles.
48	MIO	HI	I	Memory/$\overline{IO}$; high for memory cycles, low for I/O.
49	O1			Pull up to VDD using 10K resistor.
50	OS2		I	Video clocks. OS2 (28.3 MHz) is used for modes with 720
51	OS3		I	pixel horizontal resolution. OS3 (25.17 MHz) is used for
52	EXTCLK		I	modes with 320 or 640 pixel horizontal resolution. EXTCLK is a MicroChannel video extension signal, which allows using a user-defined clock.
53	V_{SS}			
54	DCLK		O	Pixel clock to Video DAC.
55	$\overline{DACR}$	LO	O	Video DAC read and write strobes.
56	$\overline{DACW}$	LO	O	
57	V_{DD}			
58	P7	HI	O	Pixel output bus to Video DAC.
59	P6	HI	O	
60	P5	HI	O	
61	P4	HI	O	
62	P3	HI	O	
63	P2	HI	O	
64	P1	HI	O	
65	P0	HI	O	
66	V_{SS}			

82706 PIN DESCRIPTION (Continued)

Right side of package (top view):

Number	Name	Active	I/O	Description
67	V_{DD}			
68	D7	HI	I/O	System data bus. The VGA may be accessed by any MicroChannel bus master.
69	D6	HI	I/O	
70	D5	HI	I/O	
71	D4	HI	I/O	
72	D3	HI	I/O	
73	D2	HI	I/O	
74	D1	HI	I/O	
75	D0	HI	I/O	
76	V_{SS}			
77	RDY	HI	O	Bus ready signal.
78	INTR	LO	O	Interrupt request. When enabled, INTR is activated during vertical retrace.
79	$\overline{DEN}$	LO	O	Data Enable to the VGA's data bus transceiver. The direction of the transceiver is controlled by the bus controller array.
80	$\overline{SFDBK}$	LO	O	VGA Selected Feedback. Active when VGA is address selected for a memory or I/O cycle, as an acknowledgement of its presence at the address specified. Used during diagnostics.
81	V_{DD}			
82	D00	HI	I/O	DRAM data bus, plane 0.
83	D01	HI	I/O	
84	D02	HI	I/O	
85	D03	HI	I/O	
86	D04	HI	I/O	
87	D05	HI	I/O	
88	D06	HI	I/O	
89	D07	HI	I/O	
90	V_{SS}			
91	D10	HI	I/O	DRAM data bus, plane 1.
92	D11	HI	I/O	
93	D12	HI	I/O	
94	D13	HI	I/O	
95	D14	HI	I/O	
96	D15	HI	I/O	
97	D16	HI	I/O	
98	D17	HI	I/O	
99	V_{DD}			

82706 PIN DESCRIPTION (Continued)

Top side of package (top view):

Number	Name	Active	I/O	Description
100	V_{SS}			
101	D20	HI	I/O	DRAM data bus, plane 2.
102	D21	HI	I/O	
103	D22	HI	I/O	
104	D23	HI	I/O	
105	D24	HI	I/O	
106	D25	HI	I/O	
107	D26	HI	I/O	
108	D27	HI	I/O	
109	V_{DD}			
110	D30	HI	I/O	DRAM data bus, plane 3.
111	D31	HI	I/O	
112	D32	HI	I/O	
113	D33	HI	I/O	
114	D34	HI	I/O	
115	D35	HI	I/O	
116	D36	HI	I/O	
117	D37	HI	I/O	
118	V_{SS}			
119	V_{DD}			
120	AA0	HI	O	DRAM address bus, planes 0 and 1.
121	AA1	HI	O	
122	AA2	HI	O	
123	AA3	HI	O	
124	AA4	HI	O	
125	AA5	HI	O	
126	AA6	HI	O	
127	AA7	HI	O	
128	V_{SS}			
129	AB0	HI	O	DRAM address bus, planes 2 and 3.
130	AB1	HI	O	
131	AB2	HI	O	
132	AB3	HI	O	

FUNCTIONAL DESCRIPTION

The 82706 interfaces the host processor and video memory, and provides palette DAC support and display of video data. All accesses between the host and video memory go through the 82706. These accesses are arbitrated with display refresh requirements to allow the CPU to read or write video memory at any time without having to wait for display retrace.

Video memory contains 256 Kbytes organized as four 64K x 8 maps. The starting address of the video memory in the host address space is programmable, providing three different start addresses. Display data from video memory is formatted into an 8-bit value clocked out on pins P0–P7, which may drive a DAC or go directly to a TTL monitor interface.

CRT Controller

In addition to generating horizontal and vertical sync timings, the CRT controller (CRTC) generates addressing for DRAM refresh and timings to support the cursor and underline capabilities.

Graphics Controller

The graphics controller provides the interface between video memory and both the host processor and the attribute controller. In alphanumeric (A/N) modes, display data is latched from video memory and sent in parallel to the attribute controller. In All Points Addressable (APA) modes, latched display data is serialized before being sent to the attribute controller.

Two read modes and four write modes are supported. Processor reads to video memory cause one byte from each of the four memory maps to be latched. Read mode 0 causes the host processor to read this latched data from a selected map, allowing access to each bit plane separately. Read mode 1 causes the pixel values in each selected map to be compared to a reference value stored in the Color Compare register. Each bit of the byte read contains a 1 when the latched pixel value matches the reference value.

Memory maps may be masked for write operations, allowing the host processor to update any or all memory maps with a single 8-bit access. In write mode 0, logical operations may be performed between pixel data latched by the previous read operation and either write data, which may be rotated, or data stored in the Set/Reset register. Logical operations supported are AND, OR, XOR, or write data unmodified. Write mode 1 simply copies latched data to the memory maps. Write Modes 2 and 3 are similar to write mode 0. In write mode 2, each enabled memory map is updated with 8 bits of the value in the corresponding bit position of the write data. Write mode 3 writes each enabled map with 8 bits of the value in the Set/Reset register. The bit mask value is derived by ANDing write data with the value in the bit mask register.

Attribute Controller

Display data in APA modes, and character generator and attribute data in A/N modes is sent to the attribute controller from the graphics controller. The attribute controller handles cursor insertion, panning, underlining, and blinking. The 8-bit per pixel output value is available on pins P0–P7.

Sequencer

The sequencer generates DRAM memory timings and arbitrates all accesses to video memory. It inserts CPU memory cycles at appropriate times between display memory fetches. The sequencer contains map mask registers which can prevent maps from being updated by memory accesses.

Preliminary product information describes products for which full characterization data is not yet available. Intel believes this information is accurate and reliable. However, it is subject to change without notice.

Table 1. Modes of Operation

GRAPHICS MODES		
Mode	**Resolution**	**Colors**
4, 5	320 x 200	4 out of 256K
6	640 x 200	2 out of 256K
D	320 x 200	16 out of 256K
E	640 x 200	16 out of 256K
F	640 x 350	Monochrome
10	640 x 350	16 out of 256K
11	640 x 480	2 out of 256K
12	640 x 480	16 out of 256K
13	320 x 200	256 out of 256K

ALPHA (TEXT) MODES					
Mode	**Rows**	**Columns**	**Char. Box**	**Resolution**	**Colors**
0, 1	25	40	9 x 16	320 x 200 (CGA)	16 out of 256K
				320 x 350 (EGA)	16 out of 256K
				360 x 400 (VGA)	16 out of 256K
2, 3	25	80	9 x 16	640 x 200 (CGA)	16 out of 256K
				640 x 350 (EGA)	16 out of 256K
				720 x 400 (VGA)	16 out of 256K
7	25	80	9 x 16	720 x 350 (EGA)	Monochrome
				720 x 400 (VGA)	Monochrome

REGISTER SET

Register Name	R/W	Index	Read Port	Write Port
GENERAL REGISTERS				
Miscellaneous Output	W			03C2
	R		03CC	
Input Status 0	R		03C2	
Input Status 1	R		03?A	
Feature Control	W			03?A
	R		03CA	
GRAPHICS CONTROLLER				
Graphics Address	R/W		03CE	03CE
Set/Reset	R/W	00	03CF	03CF
Enable Set/Reset	R/W	01	03CF	03CF
Color Compare	R/W	02	03CF	03CF
Data Rotate	R/W	03	03CF	03CF
Read Map Select	R/W	04	03CF	03CF
Graphics Mode	R/W	05	03CF	03CF
Miscellaneous	R/W	06	03CF	03CF
Color Don't Care	R/W	07	03CF	03CF
Bit Mask	R/W	08	03CF	03CF
SEQUENCER				
Sequencer Address	R/W		03C4	03C4
Reset	R/W	00	03C5	03C5
Clocking Mode	R/W	01	03C5	03C5
Map Mask	R/W	02	03C5	03C5
Character Map Select	R/W	03	03C5	03C5
Memory Mode	R/W	04	03C5	03C5
ATTRIBUTE CONTROLLER				
Address	R/W		03C0	03C0
Palette Registers	R/W	00–0F	03C1	03C0
Attribute Mode Control	R/W	10	03C1	03C0
Overscan Color	R/W	11	03C1	03C0
Color Plane Enble	R/W	12	03C1	03C0
Horizontal PEL Panning	R/W	13	03C1	03C0
Color Select	R/W	14	03C1	03C0

REGISTER SET (Continued)

Register Name	R/W	Index	Read Port	Write Port
CRT CONTROLLER				
CRT Controller Address	R/W		03?4	03?4
Horizontal Total	R/W	00	03?5	03?5
Horizontal Display Enable	R/W	01	03?5	03?5
Start Horizontal Blanking	R/W	02	03?5	03?5
End Horizontal Blanking	R/W	03	03?5	03?5
Start Horizontal Retrace Pulse	R/W	04	03?5	03?5
End Horizontal Retrace	R/W	05	03?5	03?5
Vertical Total	R/W	06	03?5	03?5
Overflow	R/W	07	03?5	03?5
Preset Row Scan	R/W	08	03?5	03?5
Maximum Scan Line	R/W	09	03?5	03?5
Cursor Start	R/W	0A	03?5	03?5
Cursor End	R/W	0B	03?5	03?5
Start Address High	R/W	0C	03?5	03?5
Start Address Low	R/W	0D	03?5	03?5
Cursor Location High	R/W	0E	03?5	03?5
Cursor Location Low	R/W	0F	03?5	03?5
Vertical Retrace Start	R/W	10	03?5	03?5
Vertical Retrace End	R/W	11	03?5	03?5
Vertical Display Enable End	R/W	12	03?5	03?5
Offset	R/W	13	03?5	03?5
Underline Location	R/W	14	03?5	03?5
Start Vertical Blank	R/W	15	03?5	03?5
End Vertical Blank	R/W	16	03?5	03?5
CRTC Mode Control	R/W	17	03?5	03?5
Line Compare	R/W	18	03?5	03?5

NOTES:
? = B in Monochrome Emulation Modes
? = D in Color Emulation Modes
All addresses are given in Hex

Register Name	R/W	Index	Read Port	Write Port
VIDEO DIGITAL TO ANALOG CONVERTER				
PEL Address (Write Mode)	R/W		03C8	03C8
PEL Address (Read Mode)	W			03C7
DAC State	R		03C7	
PEL Data	R/W		03C9	03C9
PEL Mask	R/W		03C6	03C6

NOTE:
1. DAC state register is located on the 82706. PEL Address, PEL Data, and PEL mask are located on the Palette DAC. The 82706 decodes accesses to these registers to generate DACR and DACW.

82706 PARAMETRICS

ABSOLUTE MAXIMUM RATINGS*

Case Temperature Under Bias .... −40°C to +85°C
Storage Temperature ..... −65°C to +150°C
Voltage to Any Pin with Respect to Ground .... −0.3V to +(V_{CC} +0.3)V
DC Supply Voltage (V_{CC}) ..... −0.3 to +7.0V
DC Input Current ..... ±10 mA

**Notice: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

NOTICE: Specifications contained within the following tables are subject to change.

D.C. CHARACTERISTICS T_C = 0°C to +70°C, V_{CC} = 5V ±10%

Symbol	Parameter	Min	Max	Units	Notes
V_{IL}	Input Low Voltage		0.8	V	
V_{IH}	Input High Voltage	2.0		V	
V_{OL}	Output Low Voltage		0.4	V	I_{OL} = 4 mA (Note 1)
V_{OH}	Output High Voltage	2.4		V	I_{OH} = 4 mA (Note 1)
V_{OL1}	Output Low Voltage		0.4	V	I_{OL} = 2 mA (Note 2)
V_{OH1}	Output High Voltage	2.4		V	I_{OH} = 2 mA (Note 2)
I_{CC}	Power Supply Current		100	mA	
I_{LI}	Input Leakage Current		10	μA	$V_{SS} < V_{IN} < V_{CC}$
I_{OZ}	Tri-State Output Leakage Current	−10	10	μA	$V_{SS} < V_{OUT} < V_{CC}$

NOTES:
1. Applies to all outputs except those listed in Note 2.
2. Applies only to pins INTR, DEN, FC0, FC1, and WE.

A.C. CHARACTERISTICS T_C = 0°C to +70°C, V_{CC} = 5V ±10%

Timing Requirements
AC Timings are referenced to 1.5V

Symbol	Parameter	Min	Max	Units	Notes
T1	Clock Cycle Time	35	10000	ns	
T2	Clock High Time	10	10000	ns	
T3	Clock Low Time	14	10000	ns	
T4	A19:0, MI0 Valid to RD or WR Low	35		ns	
T4A	A19:0, MCS Hold from CAS Low	0		ns	(Note 6)
T4B	A19:0, MCS Hold from RD High	0		ns	(Note 7)
T4C	RDY High to RD, WR High	0		ns	(Note 5)
T5	WR Pulse Width	70		ns	(Note 2)
T6	D7:0 Set-Up to WR High	60		ns	(Note 2)
T7	WR High to D7:0 Hold	16		ns	(Notes 2, 8)
T7A	DEN High to D7:0 Hold	0		ns	(Notes 1, 8)
T7B	RDY High to D7:0 Hold	0		ns	(Note 6)
T7C	WR Low to D7:0 Valid		30	ns	(Note 6)
T8	D37:00 Valid to CLK High	0		ns	
T9	CLK High to D37:00 Hold	40		ns	
T9A	CAS High to D37:00 Hold	0		ns	

Timing Responses
AC Timings are referenced to 1.5V

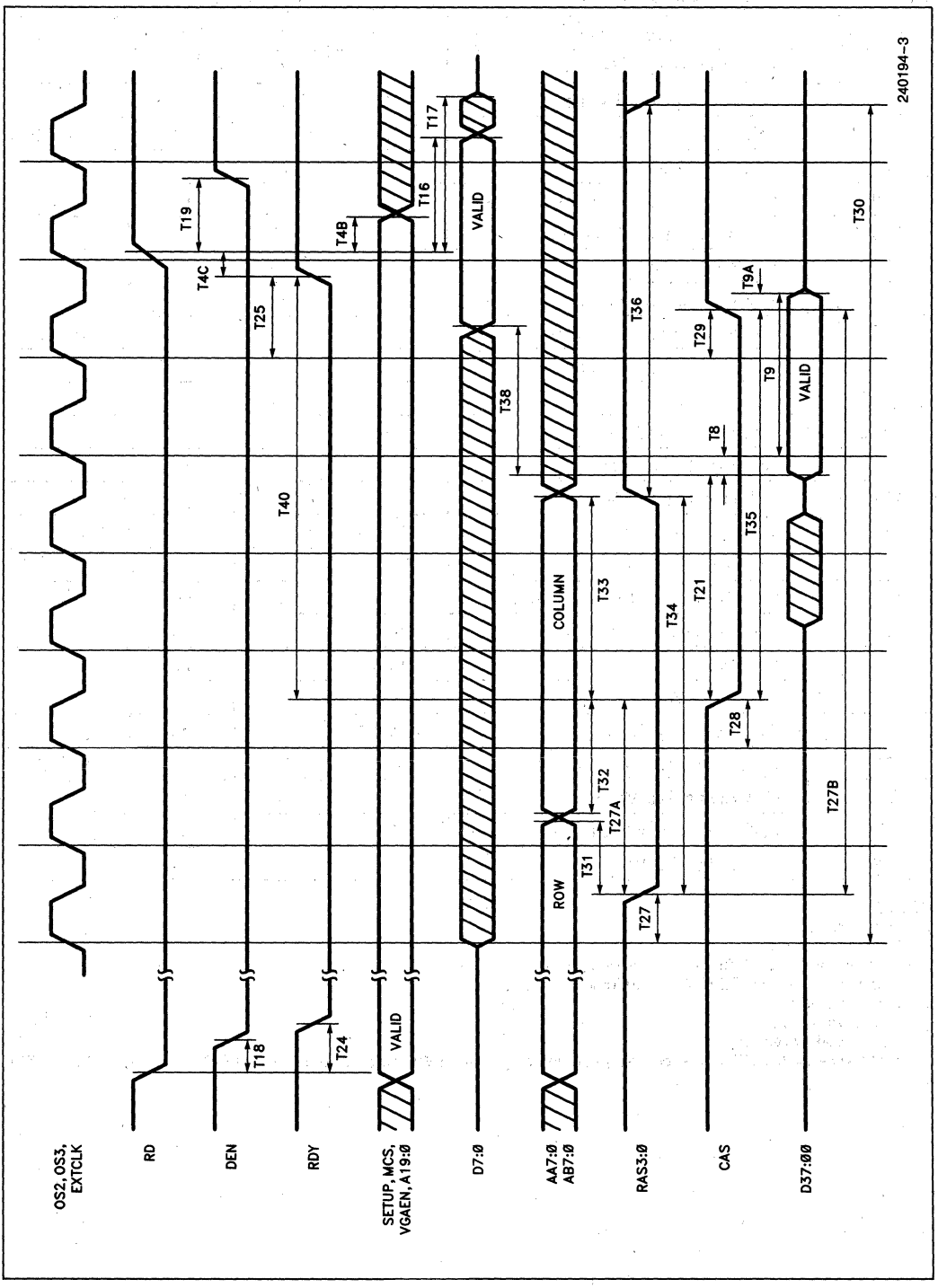
Symbol	Parameter	Min	Max	Units	Notes
T10	DCLK High Time	7		ns	(Note 3)
T11	DCLK Low Time	9		ns	(Note 4)
T12	P7:0 Valid to DCLK High	12		ns	
T13	DCLK High to P7:0 Invalid	15		ns	
T13A	DCLK High to BLANK Valid		40	ns	
T13B	DCLK High to HSYNC, VSYNC Valid		65	ns	
T14	A19:0 MI0 Valid to SFDBK Valid		60	ns	
T15	RD Low to D7:0 Valid		60	ns	
T16	RD High to D7:0 Invalid	0		ns	
T17	RD High to D7:0 Float		20	ns	

A.C. CHARACTERISTICS T_C = 0°C to +70°C, V_{CC} = 5V ±10% (Continued)

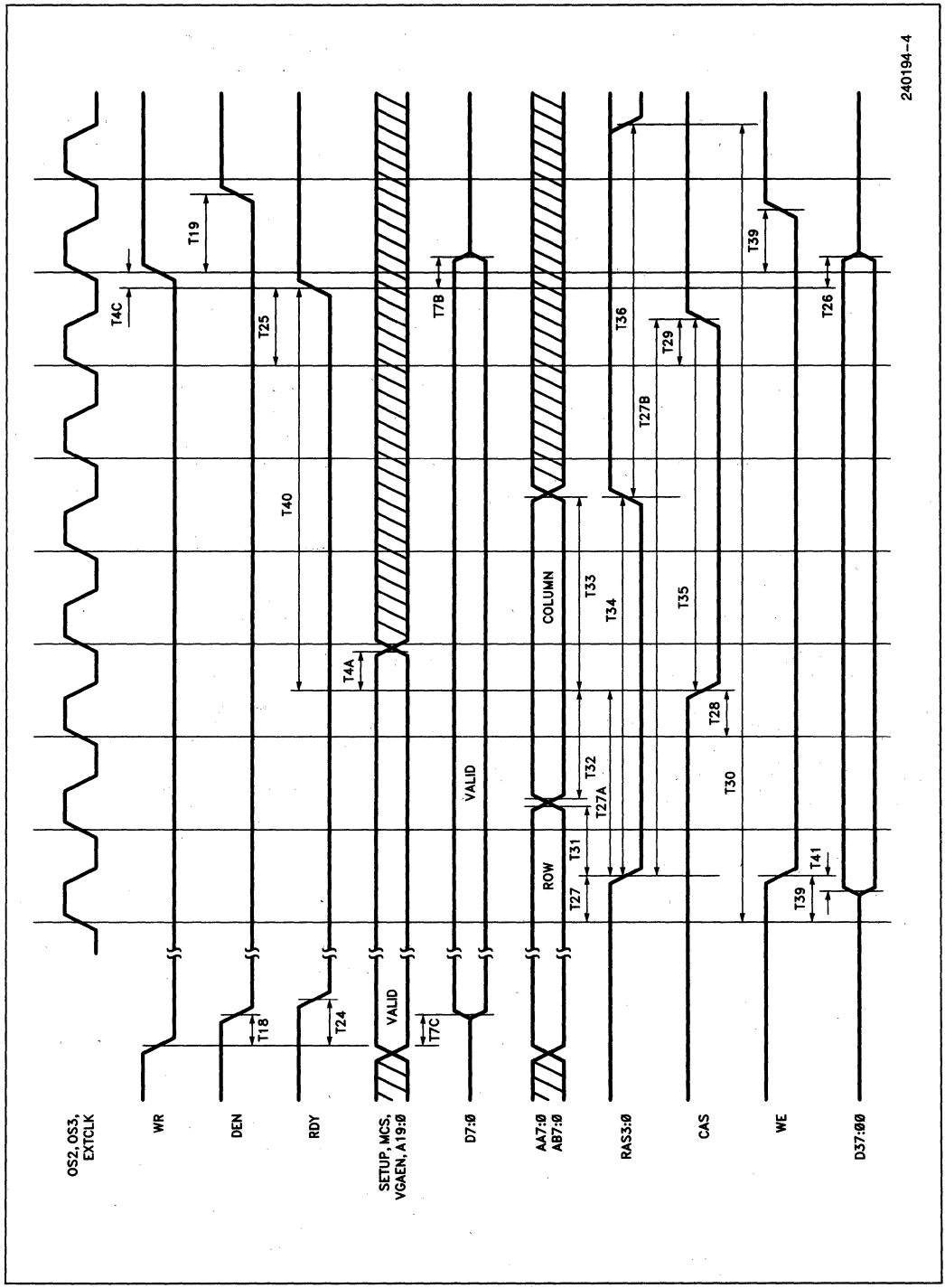
Symbol	Parameter	Min	Max	Units	Notes
T18	RD, WR Low to DEN Low		65	ns	
T19	RD, WR High to DEN High	5	30	ns	
T20	WR High to DEN High	6		ns	(Note 2)
T21	CAS Low to D37:00 Valid		70	ns	
T22	RD, WR Low to DACR, DACW Low		55	ns	
T23	RD, WR High to DACR, DACW High	4	25	ns	
T24	RD, WR Low to RDY Low		40	ns	
T25	CLK High to RDY High	0	60	ns	
T26	DATA Hold from RDY High	0		ns	(Note 6)
T27	CLK High to RAS 3:0 Low		50	ns	
T27A	RAS Low to CAS Low	50	70	ns	
T27B	RAS Low to CAS High	60		ns	
T28	CLK High to CAS Low		45	ns	
T29	CLK High to CAS High		45	ns	
T30	DRAM Cycle Time	8T1-10		ns	
T31	Row Address Hold Time	T1-10		ns	
T32	Column Address Set-up Time	10		ns	
T33	Column Address Hold Time	2T1-10		ns	
T34	RAS Pulse Width	4T1-10		ns	
T35	CAS Pulse Width	4T1-10		ns	
T36	RAS Precharge Time	4T1-15		ns	
T38	D37:00 Valid to D7:0 Valid		76	ns	(Note 7)
T39	CLK High to WE Valid		50	ns	
T40	CAS Low to RDY High	58		ns	
T41	D37:00 Valid to WE	0		ns	

NOTES:
1. I/O cycles.
2. I/O write cycles only.
3. T10 is typically at least T3 (Clock Low Time) − 4.
4. T11 is typically at least T2 (Clock High Time) − 1.
5. Memory cycles only.
6. Memory write cycles.
7. Memory read cycles only.
8. For I/O write cycles, D7:0 must be held past the rising edge of WR for at least T7 or until DEN goes high (T20 + T7A), whichever is least.

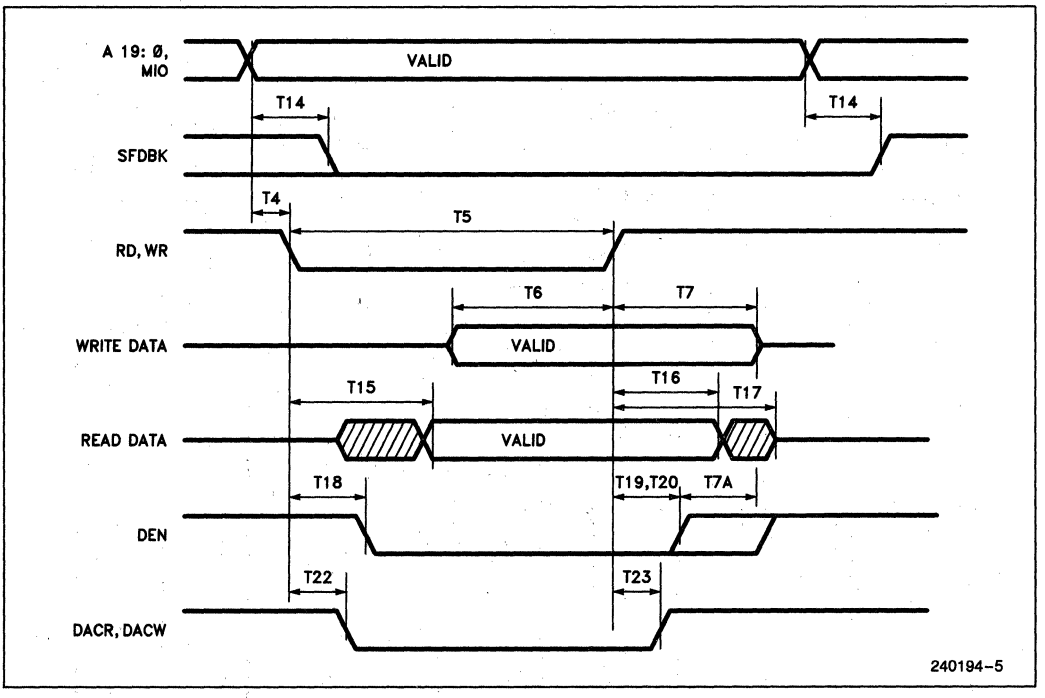
MEMORY READ


240194-3
OS2, OS3, EXTCLK
RD
DEN
RDY
SETUP, MCS, VGAEN, A19:0
D7:0
AA7:0 AB7:0
RAS3:0
CAS
D37:00
T19
T4C
T25
T40
T4B
T17
T16
VALID
T38
T36
T29
T9A
T9
T8
T35
T34
T21
T33
COLUMN
T32
T27A
T31
ROW
T27
T28
T30
T27B
T18
T24
VALID

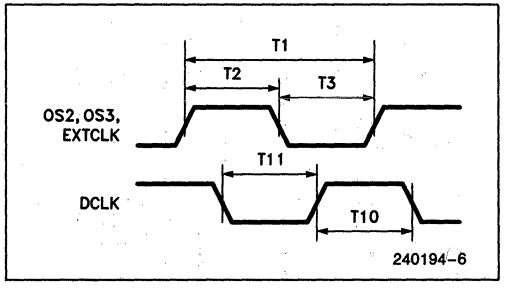
MEMORY WRITE



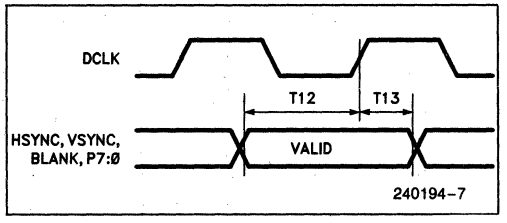
I/O CYCLE



CLOCK TIMINGS



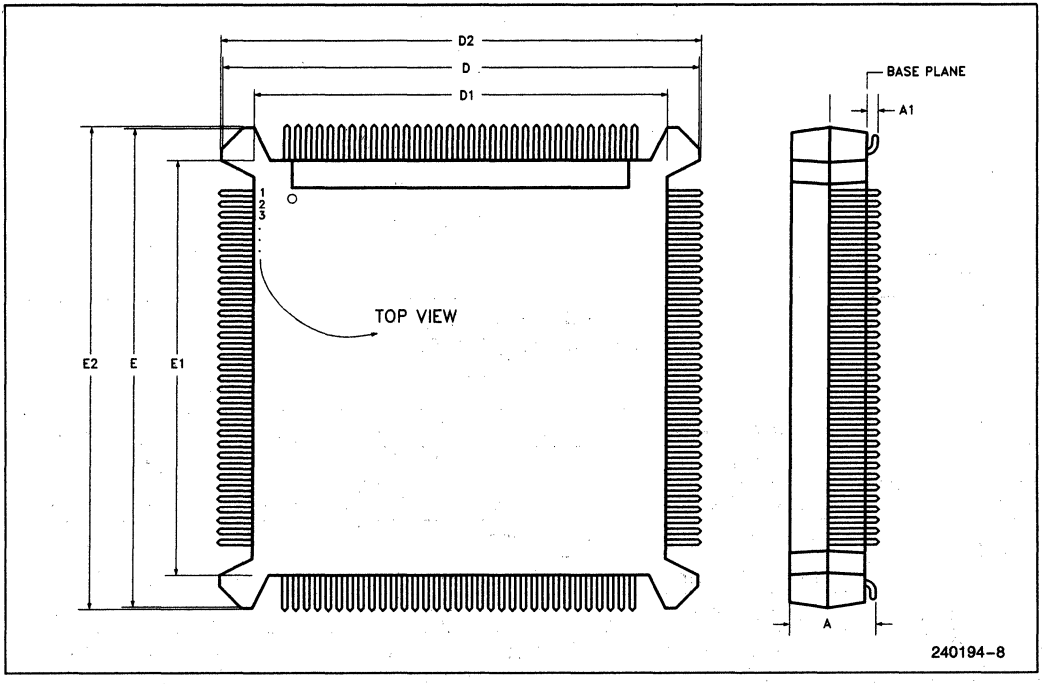
VIDEO TIMINGS



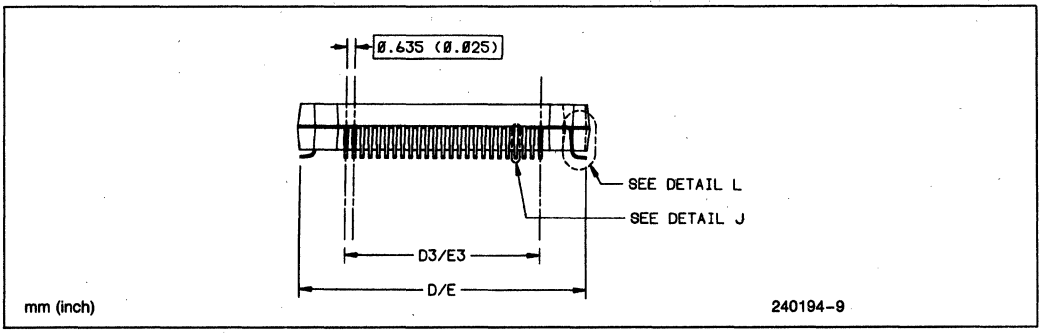
PLASTIC PACKAGING INFORMATION

The 82706 comes in a JEDEC Standard Gull Wing package (25 mil pitch), with "bumpers" on the corners for ease of handling.

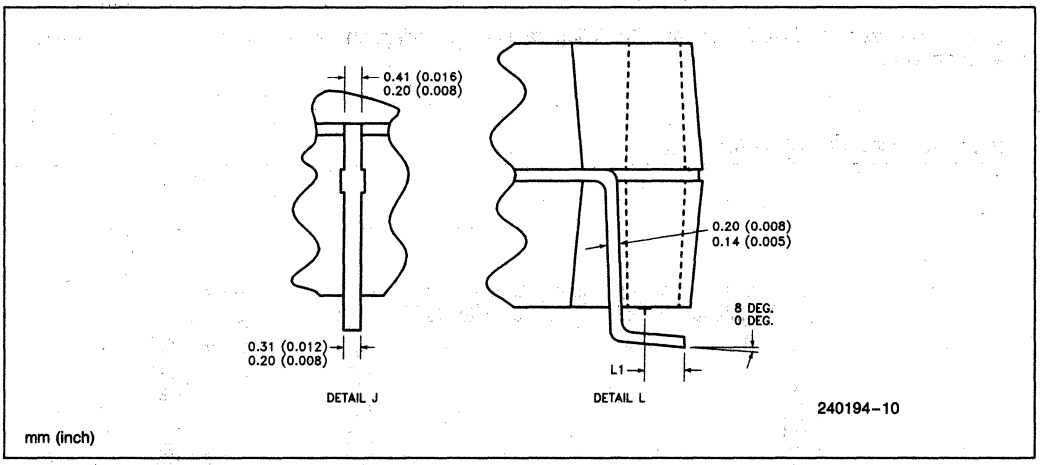
PRINCIPAL DIMENSIONS & DATUMS



TERMINAL DETAILS



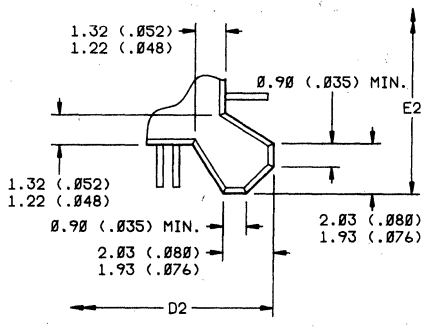
TYPICAL LEAD



Case Outline Drawings
Plastic Fine Pitch Chip Carrier
0.84 mm Pitch

Symbol	Description	Min	Max	Min	Max
N	Lead Count	132		132	
A	Package Height	0.160	0.170	4.06	4.32
A1	Standoff	0.020	0.030	0.51	0.76
D, E	Terminal Dimension	1.075	1.085	27.31	27.56
D1, E1	Package Body	0.947	0.953	24.05	24.21
D2, E2	Bumper Distance	1.097	1.103	27.86	28.02
D3, E3	Lead Dimension	0.800 Ref		20.32 Ref	
L1	Foot Length	0.020	0.030	0.51	0.76
		Inch		mm	

BUMPER DETAIL



mm (inch)

DATA SHEET REVISION REVIEW

This 82706 data sheet, version -002, contains updates and improvements to the previous version. A revision summary is listed here for your convenience.

The sections significantly revised since version -001 are:

Packaging Information — Drawing of ceramic package replaced with drawing of plastic package.
— Plastic package information section added containing mechanical information.

Pin Description — A note was added to the description of the SETUP pin.

Register Set — Video DAC register information added.

Timing Specs — Values for timings T7, T8, and T9 changed.
— Spec T21 added.

Timing Diagrams — Memory Read timing diagram altered as follows:
— SETUP and VGAEN added.
— T8 and T9 are now referenced from clock cycle earlier.
— T21 is added.
— T38 reference is changed.