HARDWARE DESIGN WITH THE IMS G191 SERIALIZER PALETTE-DAC

23.1 Introduction

To obtain the best possible picture quality from the SGS-THOMSON IMS G191 XGA display device, it is essential that it operates in a quiet electrical environment and that its input and output signals comply strictly with the requirements specified in the datasheet. This note is intended to help the graphics system designer meet those requirements and hence realise the full potential for picture quality inherent in the IMS G191 product family.

23.2 Power supply recommendations

It is essential that the device is provided with an adequately decoupled power supply. The greatest care with the other signals will be to no avail if the power supply is noisy.

First and foremost, a PCB with Ground and VDD planes should be used. This minimises the inductance and resistance in series with the power source, resulting in less noise than that which would result if the power rails were routed on the signal layers. An added bonus is that that the power planes act as a shield between signal layers, reducing crosstalk. The benefits of this will be dealt with later.

Separate analog ground and power planes should be defined around the area of the analog interface to the IMS G191, connected directly to the **AGND** and **AVDD** pins of the device. These should cover the **Vref**, **Rref**, **GateRef**, **RamVref**, **CompRef** and DAC pins. The AGND plane should be connected to the main board GND plane at one point only. The AVDD plane should be connected to the regular board VDD by a 1uH inductor. (Note this inductor should be capable of passing 50mA of DC current.)

Both pairs of power supplies (AVDD/AGND and VDD/GND) should be decoupled with a low frequency (33μF) decoupling capacitor and with high frequency decoupling (0.1μF) capacitors across each pair of power pins.

All the components associated with the DACs and the reference circuitry should be placed over the analog power planes, as close as physically possible to the IMS G191. As far as possible, digital signals should be kept away from this region of the board

A diagram of a suitable power supply arrangement is shown in Figure 23.1.

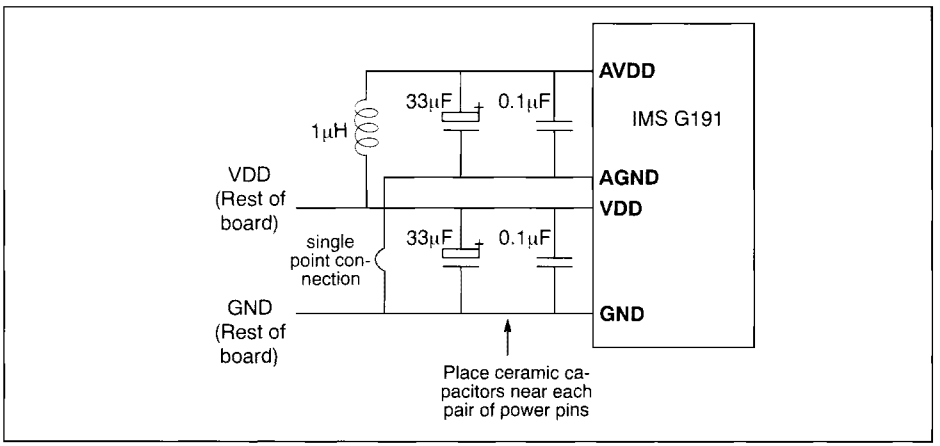

Figure 23.1 Suggested power supply arrangement

Another point to consider is that the power supplied to the actual die can be corrupted by the parasitic inductance inherent in the device package and leads. If the chip has to draw a sudden pulse of current, a back-e.m.f. is generated across this inductance which results in "ringing" on the internal supply rails. This effect cannot be eliminated, but it is helpful not to compound it. In order to obtain the best picture quality therefore, the device should be soldered directly onto the PCB and should not be socketed.

23.3 Phase locked loop requirements

Why use a phase locked loop?

The IMS G191 device employs two on-chip phase-locked loops (PLLs). One multiplies a relatively low-frequency (4MHz) input clock up to the pixel rate and the second supplies a clock signal for the XGA display controller. The use of phase-locked loops avoids routing high-frequency clocks around the board, reducing system design complexity.

PLL external circuitry

1μF capacitors must be fitted between **PLLCap3Pin1** and **PLLCap3Pin2** and between **PLLCap4Pin1** and **PLLCap4Pin2**. They must have sufficiently low e.s.l. (equivalent series inductance) and e.s.r. (equivalent series resistance) such that the total impedance connected between each pair of **PLLCap** pins across the frequency range 100kHz to 10MHz is less than 3Ω. The use of ceramic capacitors is recommended because many tantalum capacitors have an e.s.r. greater than 3Ω.

The total PCB track length must be less than 50mm to minimise the resistance and inductive reactance in series with the capacitor. If this rule is obeyed then the capacitor e.s.r. will form nearly all of the impedance in the 100kHz - 10MHz range. It is then only necessary to ensure that the e.s.r. is less than 3Ω.

PLLCap1-2 and **PLLCapRet1-2** should be connected as shown in the *Analogue interfaces* section of the IMS G191 Datasheet. Capacitors C1, C2, C5 and C6 should be 10% ceramic components with the values given in the datasheet.

23.4 External voltage reference circuitry

The IMS G191 employs an external 2.5 volt reference, in combination with an external precision resistor to set the full scale DAC output current of each of three video DACs (Red,Green and Blue).

This reference voltage, connected to the **Vref** pin, is used in combination with internal reference circuitry to set a reference current through the external resistor connected to the **Rref** pin. The internal reference circuitry will then source a current through this resistor in order to maintain 2.5V across the resistor.

In order to achieve minimum noise levels on the DAC output signals it is important to take care when defining the layout around the reference circuitry since any noise coupled onto the **Vref** input or the **Rref** input will cause noise to appear on the DAC outputs.

The 10nF noise decoupling capacitors between **Vref**, **Rref** and **AGND** should be surface-mount ceramic capacitors placed close to the **VRef** and **Rref** pins.

GateRef should be decoupled to **AVDD** by a 10nF capacitor as shown in the *Analogue interfaces* section of the IMS G191 Datasheet.

An example IMS G191 DAC external reference circuit using an LM336Z-2.5 voltage reference device is shown in Figure 23.2.

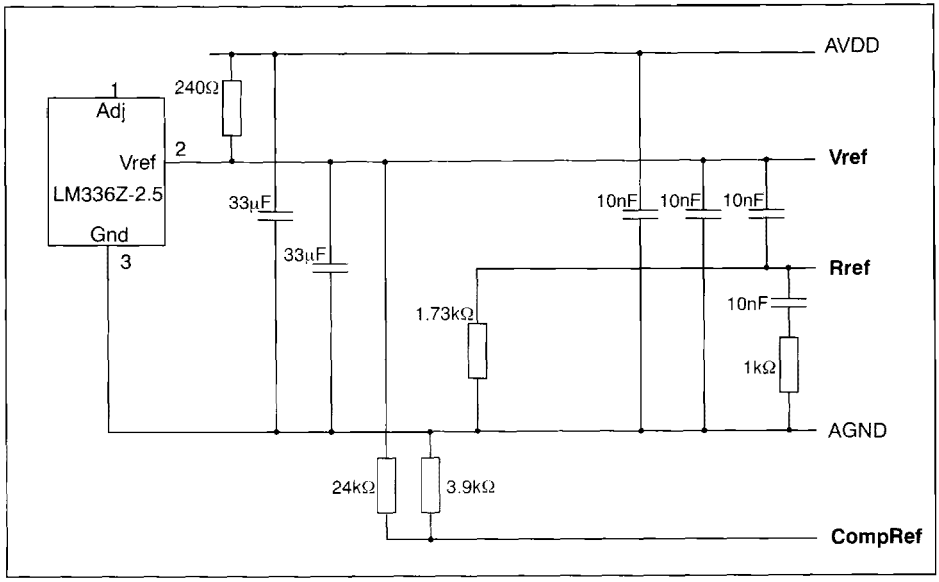

Figure 23.2 IMS G191 DAC external reference circuit

23.5 The DAC output circuitry

Double Termination

DAC outputs are driven at the pixel rate and hence should be treated with extreme care. Sluggish edges and/or noise on these outputs will degrade the picture quality.

The IMS G191 is designed to drive a 75Ω transmission line terminated at the driving end with a 150Ω resistor and terminated at the monitor with 75Ω. This gives an effective DC impedance of 150Ω||75Ω (= 50Ω).

The PCB track from the DAC output pin to the termination resistor should be shorter than 25mm, in which case it can be treated as a lumped capacitance. This capacitance should be minimised to keep the RC time constant at the DAC output small. The best way to do this is to place surface-mounted resistors adjacent to the **Red**, **Green** and **Blue** pins just outside the device package outline.

The PCB tracks from the termination resistors to the 75Ω video connectors should be sized to form 75Ω transmission lines to minimise reflections, thus improving the DAC output waveform. Because the characteristic impedance of PCB tracks can only be guaranteed to within ±10%, these tracks should be made less than 50mm long so that their transmission line delay is short. Reflections due to mismatch will then occur mainly during the DAC output rise and fall times, so that settling time is not unduly affected. An added bonus of keeping the distance between the device and the video connectors short is that RFI is kept to a minimum.

The recommended arrangement is shown in Figure 23.3.

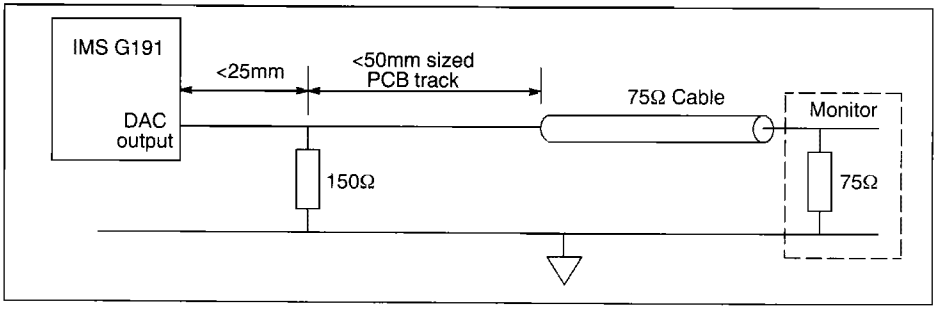

Figure 23.3 Double termination of DAC output

Note that a PCB with power planes MUST be used if transmission lines are to be formed from PCB tracks. The power planes will also shield the DAC outputs from logic signals on the opposite side of the board. Shielding from signals on the same side can be achieved by running ground tracks either side of each DAC output.

Output protection

CMOS devices are susceptible to damage from high electrostatic voltages. Normal antistatic precautions should be observed when handling them during system manufacture.

Once assembled into a system, devices are much less exposed to static damage. However if the analogue outputs are made available at connectors to other equipment there is still a risk of over or under voltage behaviour. Protection diodes to the power rails are recommended at the analogue outputs for this reason. This is shown in Figure 23.6.

23.6 Digital signals - avoiding overshoot, undershoot and output drive limitations

It is important that all the inputs and outputs of the device obey the DC operating conditions specified in the product datasheet. Failure to comply with this will degrade the power supply to the device and the quality of the analogue output. Care should also be taken to ensure that other digital signals on the board do not induce noise into sensitive analogue areas.

Inputs

All inputs are protected from electrostatic discharge (esd) by circuits which appear very much like diodes. These are NOT intended to absorb transients caused by poor design and/or layout of the driving circuitry. The equivalent circuit of Figure 23.4 illustrates the problem.

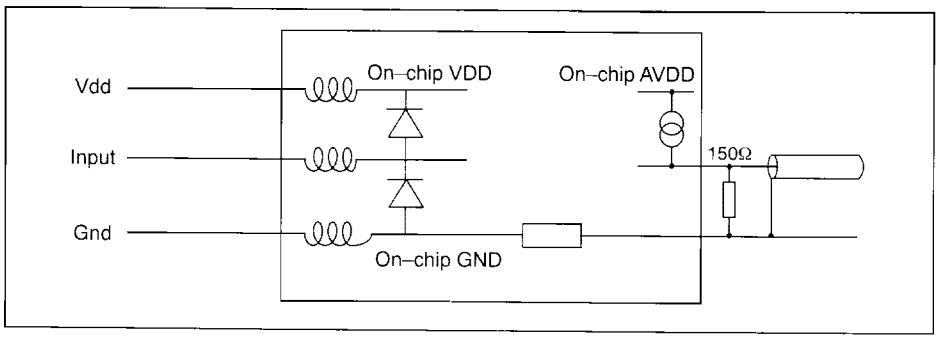

Figure 23.4 Equivalent circuit of a typical input pin

If the input reaches GND–0.5V, the diode to GND will turn on. Further negative excursions of the input will start to drag the on-chip GND supply in a negative direction. This will have a detrimental effect on the DAC circuitry in that noise will occur on the DAC outputs. Inputs which rise above Vout+0.5V will not cause this effect because the DACs have their VDD supply separated from that of the digital inputs. However, the reliability of the chip will be degraded. Therefore undershoot and overshoot greater than 0.5V outside the supply rails should be eliminated. Persistant problems may be solved by clamping with external Schottky diodes.

The most common occurrence of undershoot and overshoot is on the pixel inputs (**PixData0-31**), caused by driver outputs not being matched to the PCB track leading to the device. The symptom is usually that of vertical lines appearing on the screen separated by a number of pixels equal to the multiplex ratio.

Minimising the length of the PCB tracks from the VRAMs to the IMS G191 will reduce this problem. If this is not possible, the easiest solution is to insert a series termination resistor at the driver output to match its impedance to that of the PCB track. See Figure 23.5.

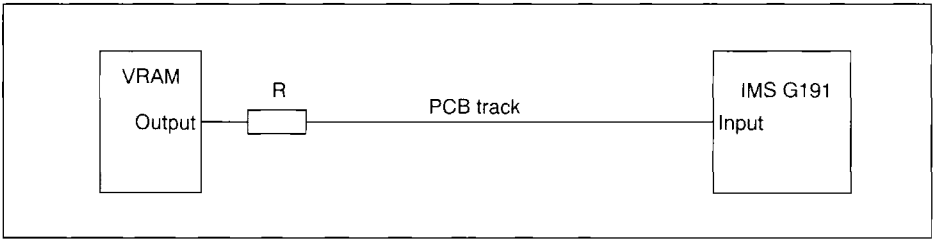

Figure 23.5 Series termination of video RAM outputs

A suitable value for R should fall within the range 10Ω to 100Ω, depending on the PCB and output driver characteristics. It should be determined by experiment, i.e. R should be varied until the undershoot and overshoot occurring at the device inputs is within 0.5V of the power supplies.

The problem of overshoot and undershoot can also be minimised by using slower logic families to drive signals into the IMS G191. This has the advantage of reducing the edge rate of the signals without adding termination resistors. Faster logic families, such as 'F' series TTL, should only be used in preference to slower devices where there is no other way of satisfying timing specifications.

Other advantages of using slower edge rates include less RFI and less risk of noise coupling into sensitive analogue circuitry.

23.7 Radiated power from graphics systems

In order to comply with FCC and European regulations, computing systems, including their graphics components, must not emit Radio Frequency Interference beyond set limits. The following guidelines are intended to help designers minimize the RFI emitted from the video components of a graphics system.

All conductors carrying time varying currents radiate electromagnetic radiation. This radiation may in turn induce currents in other nearby conductors. Radiated power from a conductor increases when it is physically large and is separated from a ground plane by a large distance. That is to say, good radiating aerials are large open systems. In a typical graphics board, the major radiating aerials are the tracks and wires surrounding the video components which carry the high frequency video signals.

To minimise the radiated power from a board a number of basic rules can be applied:

1 Keep tracks leading to and from the IMS G191 short, particularly the clocks and DAC outputs.

2 Always use at least a four-layer board with VDD and GND planes.

3 Avoid flying leads carrying high frequency signals which are not screened.

4 Place load resistors as close as possible to the analogue outputs.

5 Since some of the highest current transients occur in the VDD and GND supplies, it is important to ensure that the power supply is efficiently decoupled to GND close to the device for low and high frequencies. This can be particularly important if an inductor has been used to isolate a local VDD plane for the device from the main VDD power plane.

Radiated power increases with the frequency of the radiating signal (to the fourth power). It is therefore desirable to have as few signals as possible with very fast edge rates since these will have high frequency components. As mentioned earlier, the use of slower logic families and series termination of powerfully driven signals will reduce the risk of excessively fast edges.

In summary, to minimise RFI emissions, keep all tracks carrying video and near-video rate signals as short as possible, keep edge rates as slow as possible and ensure good power supply coupling around all the video circuitry.

23.8 Summary

Figure 23.6 shows a suggested circuit summarising some of the techniques described earlier in this note. These include power supply decoupling, series termination of a digital output, decoupling of the voltage reference and double termination of an analogue output.

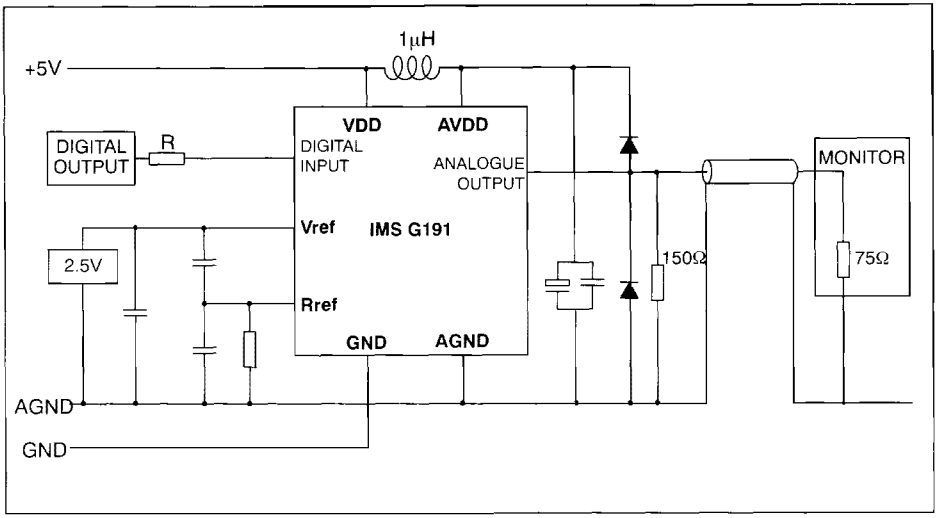

Figure 23.6 Suggested circuit

Summary – DOs and DON'Ts

DOs

- Do use a board with power planes
- Do use 33μF tantalum and 0.1μF capacitors for supply decoupling
- Do solder the device directly into the PCB
- Do use double termination from the analogue outputs to the monitor
- Do keep termination resistors within 25mm of DAC outputs - surface mounted resistors inside the device package outline are recommended
- Do size PCB track from termination resistor to video connector such that it forms a 75Ω transmission line less than 50mm long
- Do keep DAC outputs away from logic signals - preferably shield with ground tracks

DON'Ts

- Don't use separate supplies for **VDD** and **AVDD**
- Don't put the IMS G191 in an IC socket
- Don't allow digital inputs to transgress the supply rails by more than 0.5V
- Don't make edge rates of logic signals any faster than necessary