Integrated Circuit Systems, Inc.

ICS1890

Data Sheet Brief

10Base-T/100Base-TX Integrated PHYceiver™

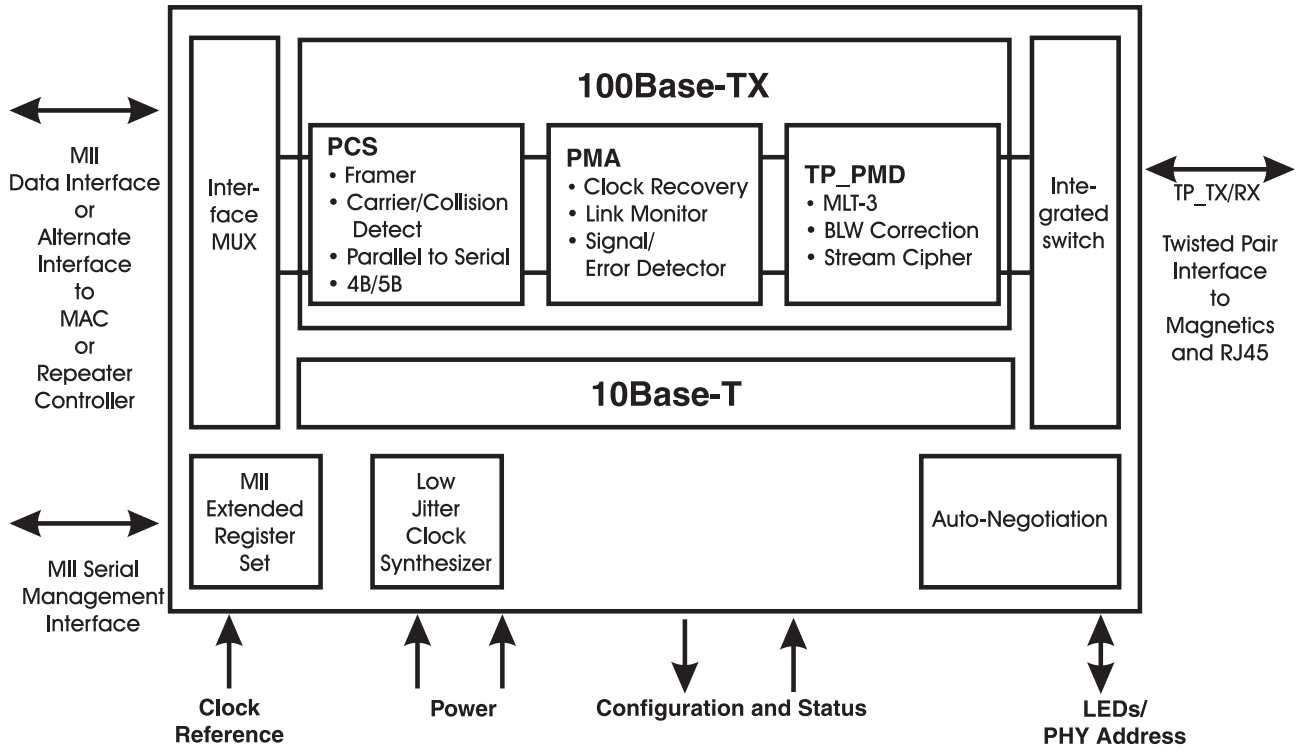
General Description

The **ICS1890** is a fully integrated physical layer device supporting 10 and 100Mb/s CSMA/CD Ethernet applications. DTE (adapter cards or motherboards), switching hub, repeater and router applications are fully supported. The **ICS1890** is compliant with the ISO/IEC 8802-3 Ethernet standard for 10 and 100Mb/s operation. A Media Independent Interface allowing direct chip-to-chip connection, motherboard-to-daughterboard connection or connection via an AUI-like cable is provided. A station management interface is provided to enable command information and status information exchange. The **ICS1890** interfaces directly to transmit and receive isolation transformers and can support shielded twisted pair (STP) and unshielded twisted pair (UTP) category 5 cables up to 105 meters. Operation in half duplex or full duplex modes at either 10 or 100 Mbps speeds is possible with control by Auto-Negotiation or manual selection. By employing Auto-Negotiation the technology capabilities of the remote link partner may be determined and operation automatically adjusted to the highest performance common operating mode.

Features

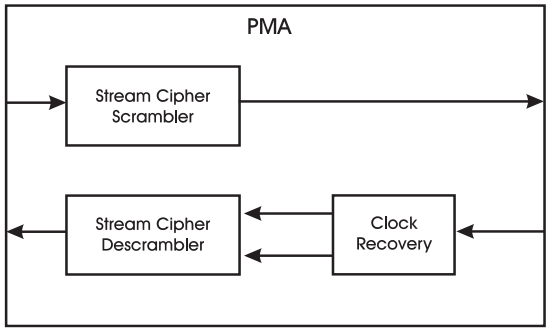
- One chip integrated physical layer
- All CMOS, Low power design (<200mA max)
- Small footprint 64-pin 14mm ^{2} QFP package
- ISO/IEC 8802-3 CSMA/CD compliant
- Media Independent Interface (MII)
- Alternate 100M stream and 10M 7-wire serial interfaces provided
- 10Base-TX Half & Full Duplex
- 100Base-TX Half & Full Duplex
- Fully integrated TP-PMD including Stream Cipher Scrambler, MLT-3 encoder, Adaptive Equalization, and Baseline Wander Correction Circuitry

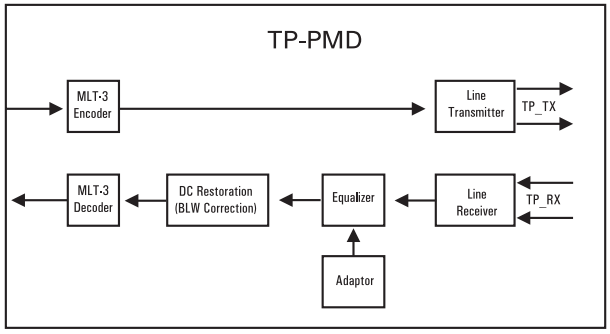
Block Diagram



PHYceiver and QuickPoll are trademarks of Integrated Circuit Systems, Inc. Patents pending.

Detailed PMA and TP=PMD Block Diagrams





Electrical Characteristics

Absolute Maximum Ratings

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS
Supply Voltage (VSS)	VDD			7	V
Digital Inputs/Outputs		VSS- 0.5		VDD + 0.5	V
Ambient Operating Temperature	TA	-55		125	°C
Storage Temperature				150	°C
Junction Temperature				175	°C
Soldering Temperature				260	°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above indicated in the operational sections is not implied. Exposure to absolute maximum rated conditions for extended periods of time may affect product reliability.

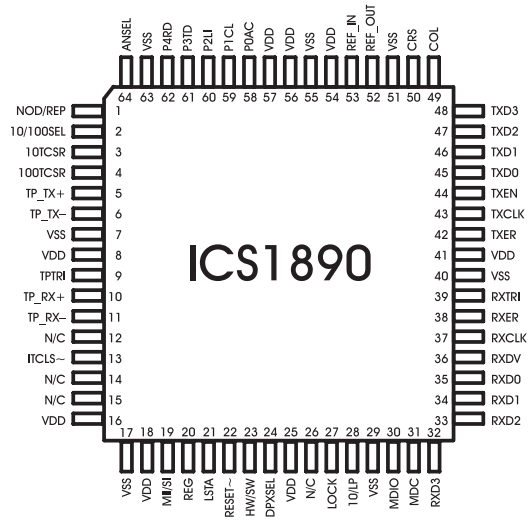
PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS
Supply Voltage (VSS)	VDD	4.75		5.25	V
Ambient Operating Temperature	TA	0		70	°C
Input Low Voltage	VIL			0.8	V
Input High Voltage	VOH	2			V
Output Low Voltage	VOL			0.4	V
Output High Voltage	VOH	2.4			V
Supply Current	IDD		175	195	mA

Pin Descriptions

PIN NUMBER	PIN NAME	I/O	Description	PIN NUMBER	PIN NAME	I/O	DESCRIPTION
1	NOD/REP	I	Node/Repeater Mode	33	RXD2*	O	Receive Data 2
2	10/100SEL	I/O	10/100 Select	34	RXD1*	O	Receive Data 1
3	10TCSR		10M Transmit Current Set Resistor	35	RXD0*	O	Receive Data 0
4	100TCSR		100M Transmit Current Set Resistor	36	RXDV*	O	Receive Data Valid
5	TP_TX	O	Twisted Pair Transmit Data+	37	RXCLK*	O	Receive Clock
6	TP_TX-	O	Twisted Pair Transmit Data-	38	RXER	O	Receive Error
7	VSS			39	RXTRI	I	Receive MAC-PHY Interface Tristate
8	VDD		Ditigal Domain Power (Transmitter)	40	VSS		
9	TPTRI	I	Twisted Pair Tristate	41	VDD		Digital Domain Power
10	TP_RX+	I	Twisted Pair Receive Data+	42	TXER*	I	Transmit Error
11	TP_RX-	I	Twisted Pair Receive Data-	43	TXCLK*	O	Transmit Error
12	N/C			44	TXEN*	I	Transmit Enable
13	ITCLS~	I	Invert Transmit Clock Latching Setting	45	TXD0*	I	Transmit Data 0
14	N/C			46	TXD1*	I	Transmit Data 1
15	N/C			47	TXD2*	I	Transmit Data 2
16	VDD		Receive Domain Power (Receiver)	48	TXD3*	I	Transmit Data 3
17	VSS			49	COL*	O	Collision Detect
18	VDD		Receive Domain Power (Receiver)	50	CRS*	O	Carrier Sense
19	MII/SI	I	MII Data/Stream Interface	51	VSS		
20	REG		Ground for high order register access	52	REF_OUT	O	Frequency Reference Output
21	LSTA*	O	Link Status	53	REF_IN	I	Frequency Reference Input
22	RESET~	I	System Reset	54	VDD		Digital Domain Power
23	HW/SW	I	Hardware/Software Priority	55	VSS		
24	DPXSEL	I/O	Duplex Select	56	VDD		Transmit Domain Power (TPLL)
25	VDD		Receive Domain Power (RPLL)	57	VDD		Digital Domain Power
26	N/C			58	P0AC	I/O	Special PHY ID 0/Activity LED
27	LOCK	O	Cipher Lock	59	P1CL	I/O	Special PHY ID 1/Collision det LED
28	10/LP	I	10M Serial/Link Pulse Interface	60	P2LI	I/O	Special PHY ID 2/Link Integrity LED
29	VSS			61	P3TD	I/O	Special PHY ID 3/Transmit data LED
30	MDIO	I/O	Management Data Input/Output	62	P4RD	I/O	Special PHY ID 4/Receive data LED
31	MDC	I	Management Data Clock	63	VSS		
32	RXD3*	O	Receive Data 3	64	ANSEL	I/O	Auto-Negotiation Selec

* Redefined for other MAC-PHY interface.

Pin Configuration



ICS1890

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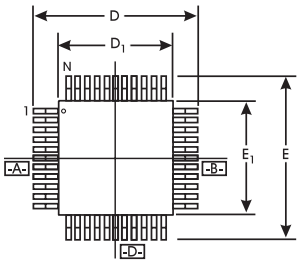
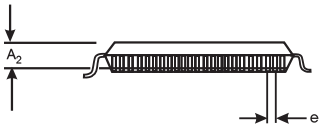
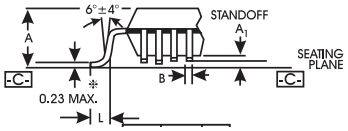


TQFP/MQFP Package





DIMENSION NAME	LEAD COUNT (N) 64L			TQFP	MQFP
	BODY THICKNESS			1.4	2.7
	FOOTPRINT (BODY+) Nominal			2.0	3.20
	DIMENSIONS	TOLERANCE TQFP	TOLERANCE MQFP		
Full Package Height	A	MAX.	MAX.	1.60	3.00
Package Standoff	A_1	MAX.	MAX.	0.15	0.25
Package Thickness	A_2	±0.05	+0.10/-0.05	1.4	2.7
Tip-to-Tip Width	D	BASIC	±0.25	16.0	17.20
Body Width	D_1	BASIC	±0.10	14.0	14.00
Tip-to-Tip Width	E	BASIC	±0.25	16.0	17.20
Body Width	E1	BASIC	±0.10	14.0	14.00
Footlength	L	±0.15	+0.10/-0.10	0.60	0.88
Lead Pitch	e	BASIC	BASIC	0.80	0. 80
Lead Width w/Plate	B	+0.08/-0.05	+0.10/-0.05	0.37	0.35
Lead Height w/Plate	*	+0.04/-0.07	MAX.	0.16	0.23

Dimensions in millimeters.

Ordering Information

ICS1890Y

ICS1890Y-14

Example:

ICS XXXX Y

Package Type
Y=MQFP Y-14=TQFP

Device Type (3 or 4 digit numbers)

Prefix
ICS, AV=Standard Device

Applications Diagram

Cable-Side Schematic