DESCRIPTION

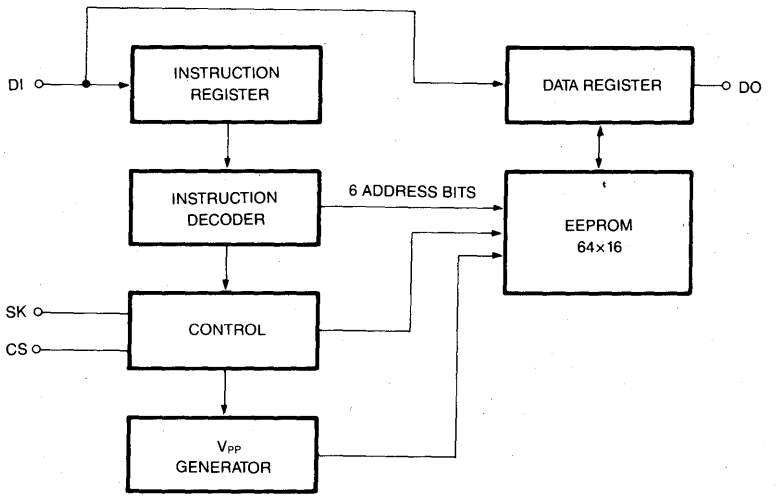
HYUNDAI's HY93C46 serial EEPROM provides a practical solution to a number of typical problems encountered in some microprocessor applications. These problems include ; the loss of data during a power shut-down, the absence of external address and data buses, the need for additional batteries and the meeting of special power on/off requirements.

Typical byte wide EEPROMs require a separate address bus and data bus to interface with a MPU. Most single-chip microcomputers have no external data or address bus, and often require non-volatile storage of data in the event of a power shut-down, whether planned or unplanned. One solution is to employ a single chip microcomputer with a power down standby mode for its on-chip RAM. However, this solution requries an additional battery and is inherently low inreliability and longevity, and has special power on/off requirements.

The HY93C46 is a 1,024-bit electrically erasable PROM with 64-registers of 16-bits. Because data is written in or read out from the device serially, no address bus or data bus is required—resulting in a low pin count package (8 pin DIP), and easy interface with any microprocessor-based system via I/O ports of a MPU.

The HY93C46 is fabricated in floating-gate CMOS EEPROM technology for very low power consumption between 33%−50% of typical NMOS devices. Deselecting the device will further reduce power consumption more than 80%, about 10% of NMOS standby current. The HY93C46 operates on 5V±10% power supply. High voltage required for programming is generated on-chip and controlled by internal logic.

Figure 1. Functional Block Diagram



7

PIN DESCRIPTIONS

SK-Serial clock : Clock generated externally by user for shifting data into or out of the HY93C46

CS-Chip select : When high enables the internal logic of the device. Note that CS must be brought low between instructions.

DI-Data in : Serial data a input; instructions and data bits shift in from this pin under the control of SK and CS.

DO-Data out : Serial data output; data is shifted out from this pin under control of SK and CS. DO is also used to monitor the ready/busy status of the device. DO is active only during data output or during the status checking period of WRITE/ERASE cycles. It is in high impedance state during all other periods.

FUNCTIONAL DESCRIPTION

The HY93C46 has seven instructions, which are 9-bits in length(see instruction set table for the HY93C46).

Each 9-bit instruction begins with a "1" as the start bit. The HY93C46 has 2 opcode bits and 6 address bits for READ, WRITE, and ERASE;or it has 4 opcode bits(2 imbedded in the address field) for the remaining instructions (ERASE/WRITE enable and disable. ERASE /WRITE all Register.) The address bits become dont't cares for these four instructions. On power-up, the HY93C46 is set to the programming disable state. This protects the device from accidental ERASE or WRITE during system power-up. To execute a WRITE or ERASE instruction, an EWEN(erase/write enable) instruction must be executed first. After data is written into the device, an EWDS instruction may be executed to disable the erase/write logic and prevent accidental programming.

READ

To read data out of the HY93C46, first shift in the 9-bit instruction. The address of the desired memory location is encoded in the address field of the read instruction. Note that the chip select pin(CS) must be brought low for a minimum of 1μs between consecutive instruction cycles to synchronize the internal logic of the device. To reduce the possibility of accidental programming, execute an EWDS instruction after each write operation and deselect the device(CS low) after each operation. Note further that data placed on the DI pin must be stable and satisfy the data setup time for the device (400ns), before the low-to-high transition of the serial clock (SK) input.

After the last address bit is shifted into the HY93C46, data from the memory location will be transferred to the data shift register and will be ready to be shifted out under the control of the shift clock(SK). A dummy "0" bit always preceeds the 16-bit output data. This dummy bit will be placed on the DO pin after the low-to-high transition of SK input for the last bit of the instruction and should be ignored. Start reading the first data bit that is shifted out after the next low-to-high transition of SK(see Figure 2).

ERASE

When the HY93C46 is erased, memory bits are set to logic "1"(i.e., reading an earsed memory location will get 16 ones). To erase a memory location, shift in the ERASE instruction with the address field set to the desired memory location address. After the last address bit is shifted in, drop CS to start the self-timed erasing cycle. In order to verify completion of the ERASE operation, raise CS again after tcs(1μs min.). The DO pin will output the device status. A low level indicates the device is busy. After approximately 10ms, the DO pin will change from a low level to a high level, indication the device has completed the ERASE cycle. CS should then be set to a low level, ready for loading of the next instruction. The sequence for erasing a memory is as follows, assuming

the erase/write enable instruction (EWEN) has been executed :

1. Set CS high(assuming CS is low when not accessing the HY93C46.)
2. Shift in ERASE instruction with the correct address.
3. Set CS low.
4. Set CS high, after minimum of 1μs.
5. Monitor DO pin;a change from low to high indicates the ERASE cycle is completed.

The "erase all" (ERAL) instruction is executed in the same manners as "erase register"(ERASE), except that the address bits of the instruction are don't care. Note that 9 bits are still needed to shift into the HY93C46 for those instrucations which have a don't care address field.

INSTRUCTION SET FOR HY93C46

INSTRUCTION	START BIT	OPCODE	ADDRESS	DATA	COMMENTS
READ	1	10	A_5, A_4, A_3, A_2, A_1, A_0		READ Register A_5, A_4, A_3, A_2, A_1, A_0
WRITE	1	01	A_5, A_4, A_3, A_2, A_1, A_0	D_{15}-D_0	WRITE Register A_5, A_4, A_3, A_2, A_1, A_0
ERASE	1	11	A_5, A_4, A_3, A_2, A_1, A_0		ERASE Register A_5, A_4, A_3, A_2, A_1, A_0
EWEN	1	00	11_{XXXX}		ERASE/WRITE Enable
EWDS	1	00	00_{XXXX}		ERASE/WRITE Disable
ERAL	1	00	10_{XXXX}		Erase All Registers
WRAL	1	00	01_{XXXX}	D_{15}-D_0	Write All Registers

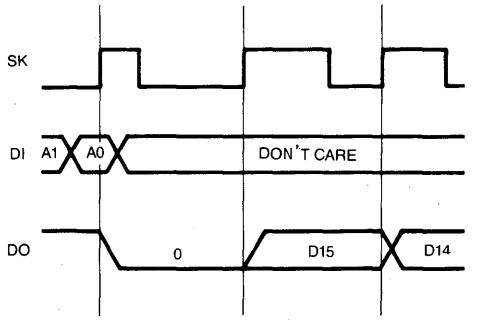
WRITE

After the 9-bit write instruction is shifted in, an additional 16 bits of data to be stored must be shifted in. After the last bit of data is loaded, chip select(CS) should be set low to initiate the WRITE cycle. The internal programming voltage generator will be turned on, and the programming will be finished in about 10ms. The ready/busy status of the HY93C46 can be read similar to the erase operation—through the DO pin, by returning the CS pin to high after the WRITE cycle is started.

The sequence for writing 16 bits of data into the HY93C46 can be summarized as follows, assuming that erase/write(EWEN) is already enabled :

1. Set CS high to enable the device.
2. Shift in the WRITE instruction with the address of the memory location to be modified.
3. Shift in the 16-bit data to be stored in that location.

Figure 2. Read Operation Timing



1. SK does not have to be symmetrical or regular, as long as it satisfies the data sheet limits.
2. After the last bit of instruction is shifted in, logic level at the DI pin will not affect internal operation.
3. Data(not the instructions) can be shifted into the HY93C46 MSB first or into LSB first;data shifted out from DO will be in the same order.

4. Set CS low to initiate the WRITE cycle.
5. Set CS high again after 1μs or more, to monitor the ready/busy status.

7

6. Monitor DO pin;a change from low to high indicates the write cycle is completed.

The "write all" instruction(WRAL) is similar to the WRITE instruction, except that the address field of the instruction is ignored, and the 16-bit data that follows the instruction will be written to all memory locations. Note that a location should be erased before new data can be written in. Erasing is recommended before writing to a previously written memory location, but it is possible to change data. Writing is a uni-directional operation;bits that are 1 may be changed to 0 only. For example, if an address contains FFF0(hex), then bits 15 to 4 may to changed. Data FFF0 could be writen as FF70, FF30, FF10, and FF900 sequentially, without intervening erasures. Note that all 16 bits must be specified at each write, even if the data remains the same.

POWER REQUIREMENTS

The on-chip programming voltage generator is only turned on during WRITE or ERASE instructions. During these periods, the operation current will increase to a few milliamperes.

The HY93C46 will consume much less power when executing an instruction that does not require programming voltage—and even lower power consumption when the device is deselected. We recommend that a decoupling capacitor of 0.1μF or higher be placed between V_{CC} and GND near the device.

INTERFACING EXAMPLE

The HY93C46 can interface with most micro processor systems with only four connections in addition to power and ground. The following illustrated the connections to the 6500/1, 8051, and 6805 microcontrollers, and the 6522, 8255 peripheral I/O ports.

Figure 3. Interfacing with 6500/1

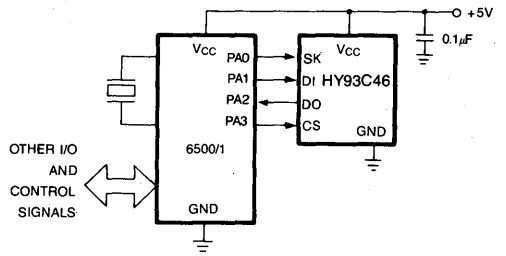


Figure 4. Interfacing with 8051

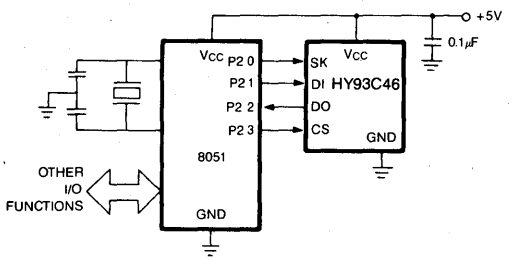


Figure 5. Interfacing with 6805

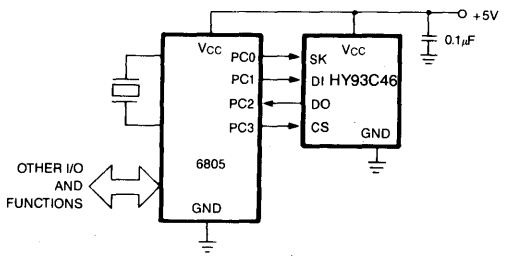


Figure 6. Interfacing with 6522

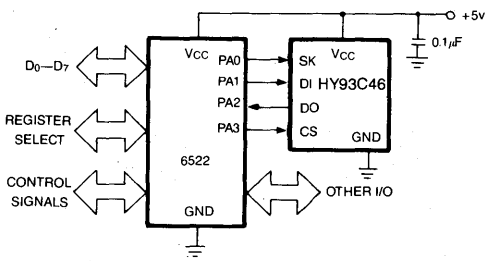
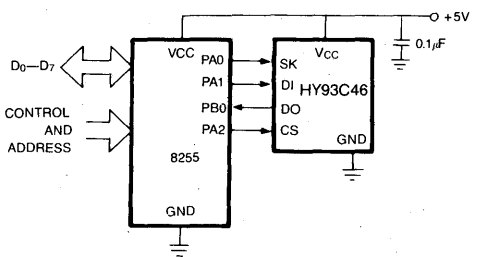
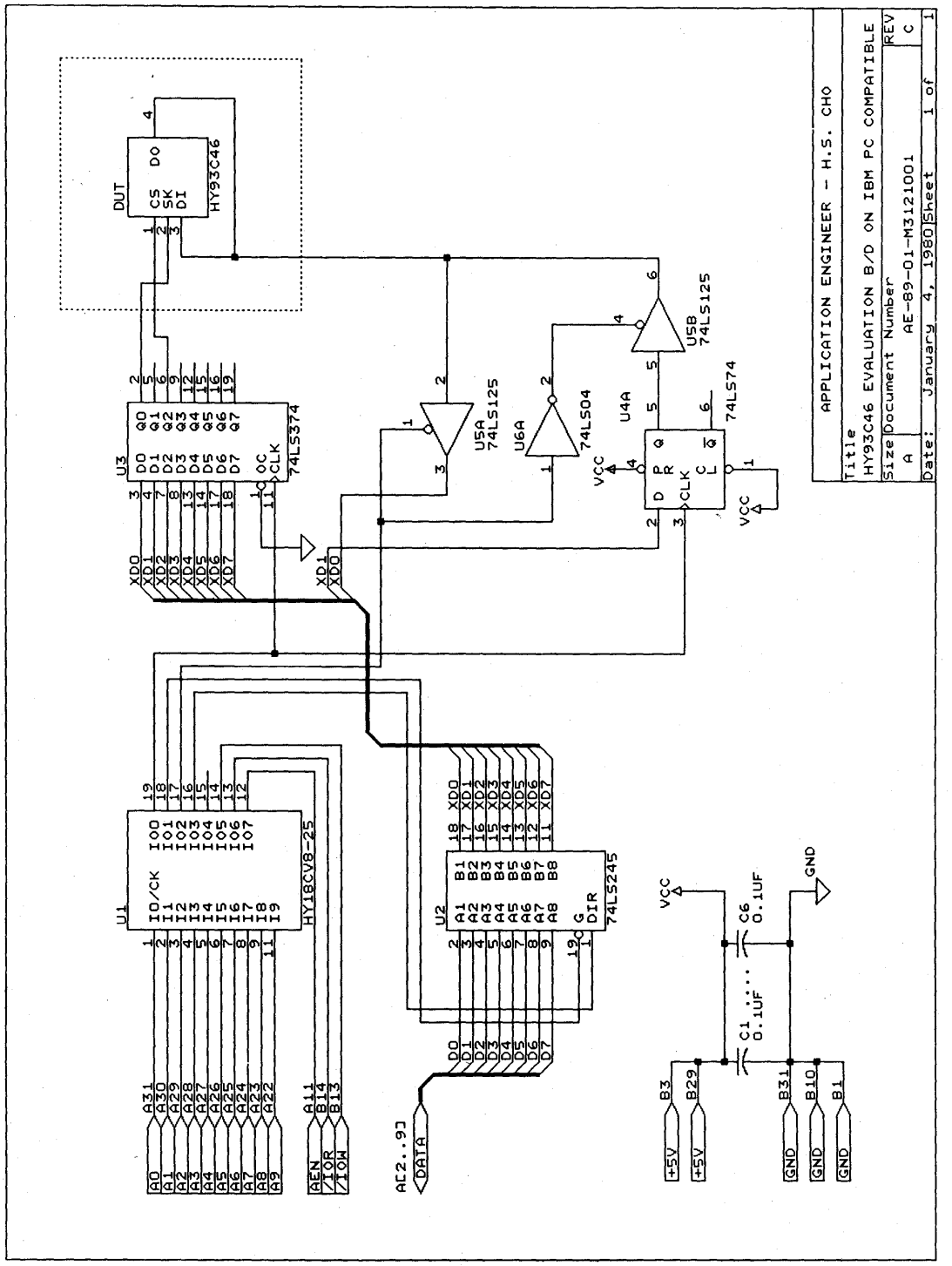


Figure 7. Interfacing with 8255 (mode 0, control word 2)



HY93C46 EVALUATION CIRCUITRY

SCHEMATIC



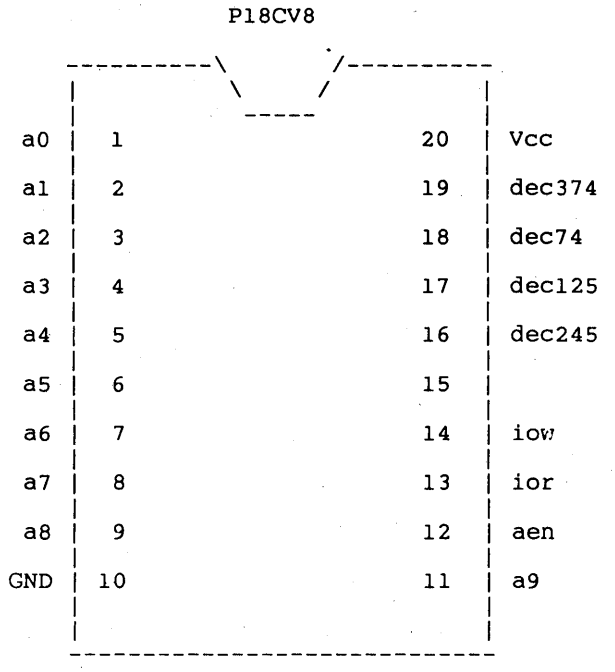
ADDRESS DECODER EQUATION SOURCE FILE FOR ABEL™ 3.0

```
module _decode1
title 'Address Decoder for HY93C46 Evaluation Board
Design by H.S.Cho - HEI Application Engineer
Dec. 13,1989
This address decoder logic implemented to HY18CV8 of the HEI EEPLD.

ul              device  'p18cv8';

a0,a1,a2,a3,a4  pin     1,2,3,4,5;
a5,a6,a7,a8,a9  pin     6,7,8,9,11;
aen             pin     12;
ior             pin     13;
iow             pin     14;

dec374          pin     19;
dec74           pin     18;
dec125          pin     17;
dec245          pin     16;


h,l,z = 1,0,.z.;
ioadd = [a9,a8,a7,a6,a5,a4,a3,a2,a1,a0];


equations

!dec374 = (ioadd == ^h300) & !aen ;
!dec74  = (ioadd == ^h300) & !aen;
!dec125 = (ioadd == ^h301) & !aen;
!dec245 = (ioadd == ^h300) # (ioadd == ^h301) & !aen & !ior;


test_vectors  'Test address decoder '

([aen,ioadd,ior,iow] -> [dec374,dec74,dec125,dec245])
 [ 1 ,^h300, h , h ] -> [  l   , l   ,  h   ,   l  ];
 [ 1 ,^h301, h , h ] -> [  h   , h   ,  l   ,   h  ];
 [ 1 ,^h301, l , h ] -> [  h   , h   ,  l   ,   l  ];

end _decode1
```

ADDRESS DECODER DOCUMENT FILE

```
ABEL(tm) 3.00a  -  Document Generator
Address Decoder for HY93C46 Evaluation Board
Design by H.S.Cho - HEI Application Engineer
Dec. 13,1989
This address decoder logic implemented to HY18CV8 of the HEI EEPLD.
Equations for Module _decode1

Device u1


- Reduced Equations:

    dec374 = !(!a0 & !a1 & !a2 & !a3 & !a4 & !a5 & !a6 & !a7 & a8 & a9 &
            !aen);

    dec74 = !(!a0 & !a1 & !a2 & !a3 & !a4 & !a5 & !a6 & !a7 & a8 & a9 &
           !aen);

    dec125 = !(a0 & !a1 & !a2 & !a3 & !a4 & !a5 & !a6 & !a7 & a8 & a9 &
            !aen);

    dec245 = !(a0 & !a1 & !a2 & !a3 & !a4 & !a5 & !a6 & !a7 & a8 & a9 &
            !aen & !ior
              # !a0 & !a1 & !a2 & !a3 & !a4 & !a5 & !a6 & !a7 & a8 & a9);
```

```
ABEL(tm) 3.00a  -  Document Generator
Address Decoder for HY93C46 Evaluation Board
Design by H.S.Cho - HEI Application Engineer
Dec. 13,1989
This address decoder logic implemented to HY18CV8 of the HEI EEPLD.
Chip diagram for Module _decode1

Device u1
```




```
end of module _decode1
```

ADDRESS DECODER JEDEC FILE

```
ABEL(tm) 3.00a FutureNet Div, Data I/O Corp.  JEDEC file for: P18CV8
Created on:
Address Decoder for HY93C46 Evaluation Board
Design by H.S.Cho - HEI Application Engineer
Dec. 13,1989
This address decoder logic implemented to HY18CV8 of the HEI EEPLD.*
QP20* QF2696* QV4*
L0000
100110111011101110111011101110110110
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100110111011101110111011101110110110
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00000000000000000000000000000000000000
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00000000000000000000000000000000000000
00000000000000000000000000000000000000*
L2664
1011
1011
1011
1011
0000
0000
0011
0011*
N Test address decoder *
V0001 000000001N1011XLHLLN*
V0002 100000001N1011XHLHHN*
V0003 100000001N1001XLLHHN*
C25E2*
7A84
```

FREE EVALUATION SOFTWARE

A HY93C46 evaluation software (IBM PC compatible) is available now. The program can be used for reading data from, modifying the data basis on bit, writing data into the HY93C46. Also, it is useful for you to verify data endurance test from 1 to 65,535 cycles. All the instructions in this sheet can be applicable to the HY93C46. When you need this program, contact to your nearest HYUNDAI representatives or distributors, or Semiconductor Application Engineering in Semiconductor Marketing & Sales Division.

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- IBM is registered trademark of IBM Corporation