HYUNDAI SEMICONDUCTOR

HY534256A

256K×4-Bit CMOS DRAM

M1C1200A-JAN92

DESCRIPTION

The HY534256A is a high speed, low power 262,144×4 bit CMOS dynamic random access memory. Fabricated with the HYUNDAI CMOS process, the HY534256A offers a fast page mode for high bandwide operation, fast usable speed, CMOS standby current, and inherently high CMOS reliability.

All inputs and outputs are TTL compatible. Fast page mode operation allows random or sequential access of up to 512×4 bits within a row with cycle times as fast as 40ns.

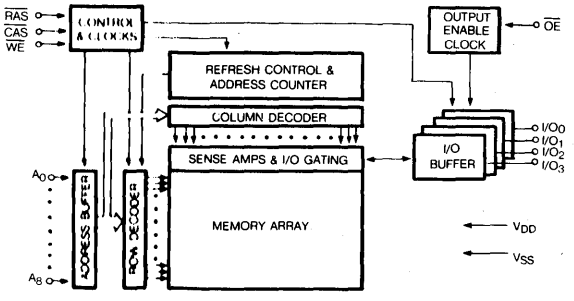
The HY534256A design is optimized for cache based mainframe, minicomputers, graphics, digital signal processing and high performance microprocessor systems.

FEATURES

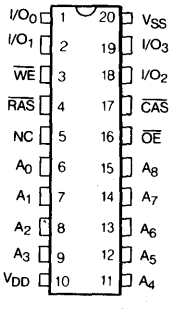
- **Low power dissipation**
  - **Operating current, 60ns : 90mA(max.)**
  - **TTL Standby current : 2mA(max.)**
  - **CMOS Standby Current : 1mA(max.)**
- **Read-Modify-Write capability**
- **$\overline{RAS}$-only, Hidden, $\overline{CAS}$-Before-$\overline{RAS}$ refresh capability**
- **Fast Page mode operation for a sustained data rate up to 25 MHz**
- **512 refresh cycles/8ms**
- **High reliability 300 mil 20 pin P-DIP, 20/26 pin SOJ and 400 mil ZIP.**
- **Fast access time and cycle time (ns)**

	HY534256A-60	HY534256A-70	HY534256A-80
Max $\overline{RAS}$ Access Time, t_{RAC}	60	70	80
Max $\overline{CAS}$ Access Time, t_{CAC}	20	20	20
Min Fast Page Mode Cycle Time, t_{PC}	40	40	45
Min Cycle Time, t_{RC}	110	130	150

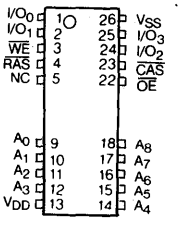
BLOCK DIAGRAM



PIN CONNECTIONS



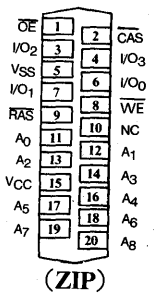
(P-DIP)



(SOJ)

PIN NAMES

$\overline{RAS}$	ROW ADDRESS STROBE
$\overline{CAS}$	COLUMN ADDRESS STROBE
$\overline{WE}$	WRITE ENABLE
$\overline{OE}$	OUTPUT ENABLE
A_0-A_8	ADDRESS INPUT
I/O_0-I/O_3	DATA INPUT/OUTPUT
V_{DD}	POWER(+5V)
V_{SS}	GROUND



(ZIP)

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
T_{BIAS}	Ambient Temperature	0 to 70	℃
T_{STG}	Storage Temperature	−55 to +150	℃
V_{TERM}	Voltage on Any Pin Relative to V_{SS}	−1.0 to 7.0	V
V_{DD}	Voltage on V_{DD} Relative to V_{SS}	−1.0 to 7.0	V
I_{OUT}	Short Circuit Output Current	50	mA
P_T	Power Dissipation	0.6	W

NOTE : Operation at or above Absolute Maximum Ratings can adversely affect device reliability.

DC CHARACTERISTICS

(T_A=0°C to 70°C, V_{DD}=5V± 10%, V_{SS}=0V, unless otherwise noted.)

SYMBOL	PARAMETER	TEST CONDITIONS	SPEED	HY534256A		UNIT	NOTE
				MIN.	MAX.		
$\|I_{LI}\|$	Input Leakage Current(any input pin)	$V_{SS} \le V_{IN} \le V_{DD}$			10	μA	
$\|I_{LO}\|$	Output Leakage Current for High Impedance State	$V_{SS} \le D_{OUT} \le V_{DD}$ $\overline{RAS}$, $\overline{CAS}$ at V_{IH}			10	μA	
I_{DD1}	V_{DD} Supply Current, Operating	$t_{RC}=t_{RC}$(min.)	−60		90	mA	1, 2
			−70		80		
			−80		70		
I_{DD2}	V_{DD} Supply Current, TTL Standby	$\overline{RAS}$, $\overline{CAS}$ at V_{IH} other inputs$\ge V_{SS}$			2	mA	
I_{DD3}	V_{DD} Supply Current, $\overline{RAS}$-only Refresh	$t_{RC}=t_{RC}$(min.)	−60		90	mA	2
			−70		80		
			−80		70		
I_{DD4}	V_{DD} Supply Current, Fast page mode	Minimum Cycle	−60		70	mA	1, 2
			−70		60		
			−80		50		
I_{DD5}	V_{DD} Supply Current, $\overline{CAS}$-Before-$\overline{RAS}$ Refresh	$\overline{RAS} \ge V_{DD}-0.2V$, $\overline{CAS}=V_{IH}$ Other inputs$\ge V_{SS}$			1	mA	
I_{DD6}	V_{DD} Supply Current $\overline{CAS}$-Before-$\overline{RAS}$ Refresh	$t_{RC}=t_{RC}$(min.)	−60		90	mA	2
			−70		80		
			−80		70		
V_{IL}	Input Low Voltage(all inputs)			−1	0.8	V	
V_{IH}	Input High Voltage(all inputs)			2.4	V_{DD}+1	V	
V_{OL}	Output Low Voltage	I_{OL}=4.2mA			0.4	V	
V_{OH}	Output High Voltage	I_{OH}=−5mA		2.4		V	

NOTES :

1. I_{DD} is dependent on output loading when the device output is selected. Specified I_{DD}(max.) is measured with output open.
2. I_{DD} is dependent upon the number of address transitions, Specified I_{DD}(max.) is measured with a maximum of of two transitions per address cycle in Fast page mode.

AC CHARACTERISTICS

(T_A=0°C to 70°C, V_{DD}=5V± 10%, V_{SS}=0V, unless otherwise noted.)

#	SYMBOL	PARAMETER	HY534256A						UNIT	NOTE
			60		70		80			
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
1	t_{RAS}	$\overline{RAS}$ Pulse Width	60	10K	70	10K	80	10K	ns	
2	t_{RC}	Random Read or Write Cycle Time	110		120		150		ns	
3	t_{RP}	$\overline{RAS}$ Precharge Time	40		50		60		ns	
4	t_{CSH}	$\overline{CAS}$ Hold Time	60		70		80		ns	
5	t_{CAS}	$\overline{CAS}$ Pulse Width	20	10K	20	10K	20	10K	ns	
6	t_{RCD}	$\overline{RAS}$ to $\overline{CAS}$ Delay	15	40	20	50	20	60	ns	
7	t_{RCS}	Read Command Set-up Time	0		0		0		ns	
8	t_{ASR}	Row Address Set-up Time	0		0		0		ns	
9	t_{RAH}	Row Address Hold Time	10		10		10		ns	
10	t_{ASC}	Column Address Set-up Time	0		0		0		ns	
11	t_{CAH}	Column Address Hold Time	15		15		15		ns	
12	t_{RSH}	$\overline{RAS}$ Hold Time	20		20		20		ns	8
13	t_{CRP}	$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	5		5		5		ns	8
14	t_{RCH}	Read Command Hold Time Referenced to $\overline{CAS}$	0		0		0		ns	
15	t_{RRH}	Read Command Hold Time Referenced to $\overline{RAS}$	0		0		0		ns	
16	t_{ROH}	$\overline{RAS}$ Hold Time Referenced to $\overline{OE}$	10		10		15		ns	
17	t_{OAC}	Access Time from $\overline{OE}$		20		25		20	ns	3,4,5
18	t_{CAC}	Access Time from $\overline{CAS}$		20		20		20	ns	5, 7
19	t_{RAC}	Access Time from $\overline{RAS}$		60		70		80	ns	3
20	t_{AA}	Access Time from Column Address		30		35		40	ns	11
21	t_{LZ}	$\overline{OE}$ or $\overline{CAS}$ to Output Low Impedance	0		0		0		ns	
22	t_{HZ}	$\overline{OE}$ or $\overline{CAS}$ to Output High Impedance	0	20	0	20	0	20	ns	
23	t_{AR}	Column Address Hold Time from $\overline{RAS}$	50		55		60		ns	
24	t_{RAD}	$\overline{RAS}$ to Column Address Delay Time	15	30	15	35	15	40	ns	1
25	t_{CWL}	Write Command to $\overline{CAS}$ Lead Time	20		20		20		ns	
26	t_{WCS}	Write Command Set-up Time	0		0		0		ns	9
27	t_{WCH}	Write Command Hold Time	10		15		15		ns	
28	t_{WP}	Write Command Pulse Width	10		15		15		ns	11
29	t_{WCR}	Write Command Hold Time from $\overline{RAS}$	50		55		60		ns	
30	t_{RWL}	Write Command to $\overline{RAS}$ Lead Time	20		20		20		ns	
31	t_{DS}	Data-In Set-up Time	0		0		0		ns	10
32	t_{DH}	Data-In Hold Time	10		15		15		ns	10
33	t_{WOH}	Write to $\overline{OE}$ Hold Time	20		20		20		ns	
34	t_{OED}	$\overline{OE}$ to Data Delay	20		20		20		ns	
35	t_{RWC}	Read-Modify-Write(RMW)Cycle-Time	165		185		205		ns	

#	SYMBOL	PARAMETER	HY534256A						UNIT	NOTE
			60		70		80			
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
36	t_{CWD}	$\overline{CAS}$ to $\overline{WE}$ Delay	50		50		50		ns	9
37	t_{RWD}	$\overline{RAS}$ to $\overline{WE}$ Delay	90		100		110		ns	9
38	t_{AWD}	Column Address to $\overline{WE}$ Delay	60		65		70		ns	9
39	t_{PC}	Fast Page Mode Read or Write Cycle Time	40		40		45		ns	
40	t_{PCM}	Fast Page Mode Read-Modify-Write Cycle Time	95		95		100		ns	
41	t_{CP}	$\overline{CAS}$ precharge Time	10		10		10		ns	
42	t_{RAL}	Column Address to $\overline{RAS}$ Lead Time	30		35		40		ns	
43	t_{CPA}	Access Time from Column Precharge		35		35		40	ns	12
44	t_{DHR}	Data Hold Time Referenced to $\overline{RAS}$	50		55		60		ns	
45	t_{CSR}	$\overline{CAS}$ Set-up Time($\overline{CAS}$ Before $\overline{RAS}$ Cycle)	5		5		5		ns	
46	t_{RPC}	$\overline{RAS}$ to $\overline{CAS}$ Precharge Time	0		0		0		ns	
47	t_{CHR}	$\overline{CAS}$ Hold Time($\overline{CAS}$ Before $\overline{RAS}$ Cycle)	15		15		15		ns	
48	t_T	Transition Time(Rise and Fall)	3	50	3	50	3	50	ns	13
49	t_{REF}	Refresh Interval(512 Cycle)		8		8		8	ms	
50	t_{RASP}	$\overline{RAS}$ Pulse width(Fast Page Mode)	60	100K	70	100K	80	100K	ns	
51	t_{CPT}	$\overline{CAS}$ Precharge Time(CBR Counter Test Cycle)	40		40		40		ns	

NOTES :

1. Operation within the t_{RAD}(max.) limit insures that t_{RAC}(max.) can be met. t_{RAD}(max.) is specified as a referenced point only. If t_{RAD} is greater than the specified t_{RAD}(max.) limit, then the access time is controlled by t_{AA} and t_{CAC}.
2. t_{RCD}(max.) is specified for reference only. Operation within t_{RCD}(max.) and t_{RAD}(max.) limit insure that t_{RAC}(max.) and t_{AA} (max.) can be met. If t_{RCD} is greater than the specified t_{RCD}(max.) then the access time is controlled by t_{AA} and t_{CAC}.
3. Assume $t_{RAD} \leq t_{RAD}$(max.) If t_{RAD} is greater than t_{RAD}(max.) then t_{RAC} will increase by the amount that t_{RAD} exceeds t_{RAD}(max.)
4. Assume $t_{RCD} \leq t_{RCD}$(max.). If t_{RCD} is greater than t_{RCD}(max.) then t_{RAC} will increase by the amount that t_{RCD} exceeds t_{RCD}(max.)
5. Measured with a load equivalent to two TTL loads and 100pF.
6. Assume that $t_{RCD} \geq t_{RCD}$(max.), $t_{RAD} \leq t_{RAD}$(max.)
7. Assume that $t_{RCD} \leq t_{RCD}$(max.) and $t_{RAD} \geq$(max.)
8. Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.
9. t_{WCS}, t_{RWD}, t_{CWD} and t_{AWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only : If $t_{WCS} > t_{WCS}$(min), the cycle is an early write cycle and the data out pin will remain open circuit(high impedance) throughout the entire cycle : if $t_{RWD} > t_{RWD}$(min), $t_{CWD} > t_{CWD}$ (min) and $t_{AWD} \geq t_{AWD}$(min), the cycle is a read/write and the data output will contain data from the selected cell : if neither of the above sets of conditions is satisfied, the condition of the data out(at access time) is indeterminate.
10. t_{DS} and t_{DH} are referenced to the latter occurence of $\overline{CAS}$ or $\overline{WE}$
11. t_{HZ} define the time at which the data output achieves the open circuit condition and is not referenced to the output voltage levels.
12. Access time is determined by the longer of t_{AA}, t_{CAC} or t_{CAP}.
13. V_{IL}(max.) and AC measurements assumen t_T=5ns
14. An initial
15. An initial pause of 200μs is required after power-up and followed by a minimum of 8 initialization cycles(any combination of cycles containing a $\overline{RAS}$ clock such as $\overline{RAS}$-only refresh). 8 initialization cycles are required after extended period of bias without clocks.

3

CAPACITANCE

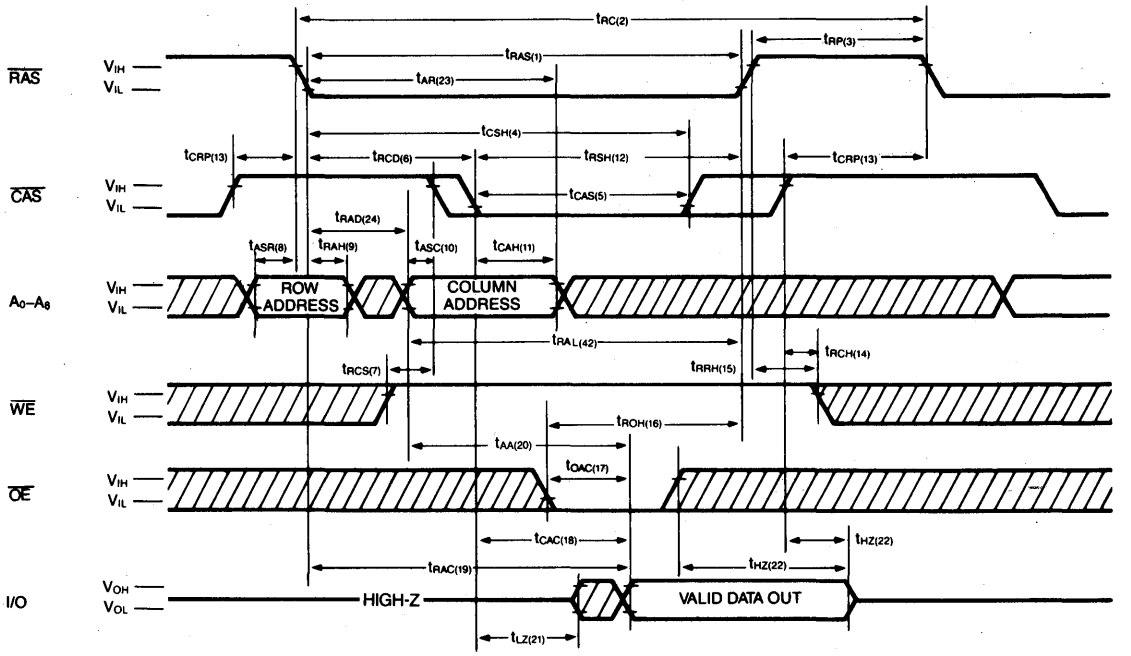
(T_A=25, C, V_{DD}=5V± 10%, V_{SS}=0V, unless otherwise noted)

SYMBOL	PARAMETER	TYP.	MAX.	UNIT
C_{IN1}	Address, Data input	–	5	pF
C_{IN2}	$\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, $\overline{OE}$	–	7	pF
C_{OUT}	Data Out	–	7	pF

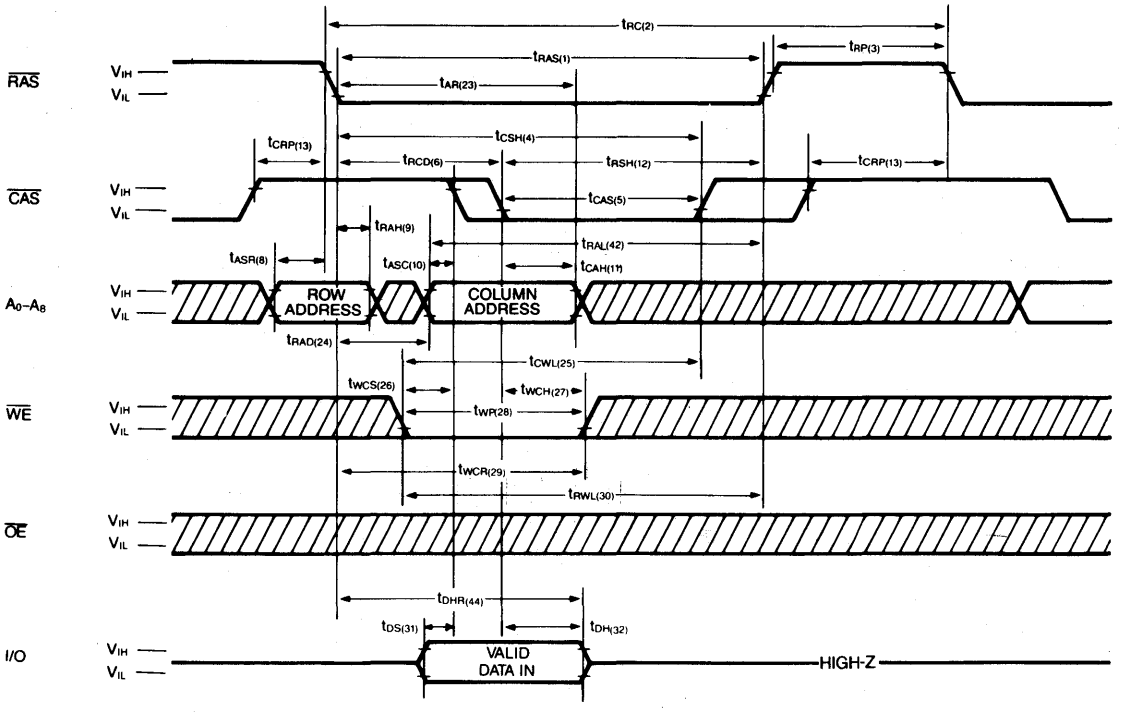
NOTE : Capacitance is measured at worst case of voltage levels with a programmable capacitance meter.

TIMING DIAGRAM

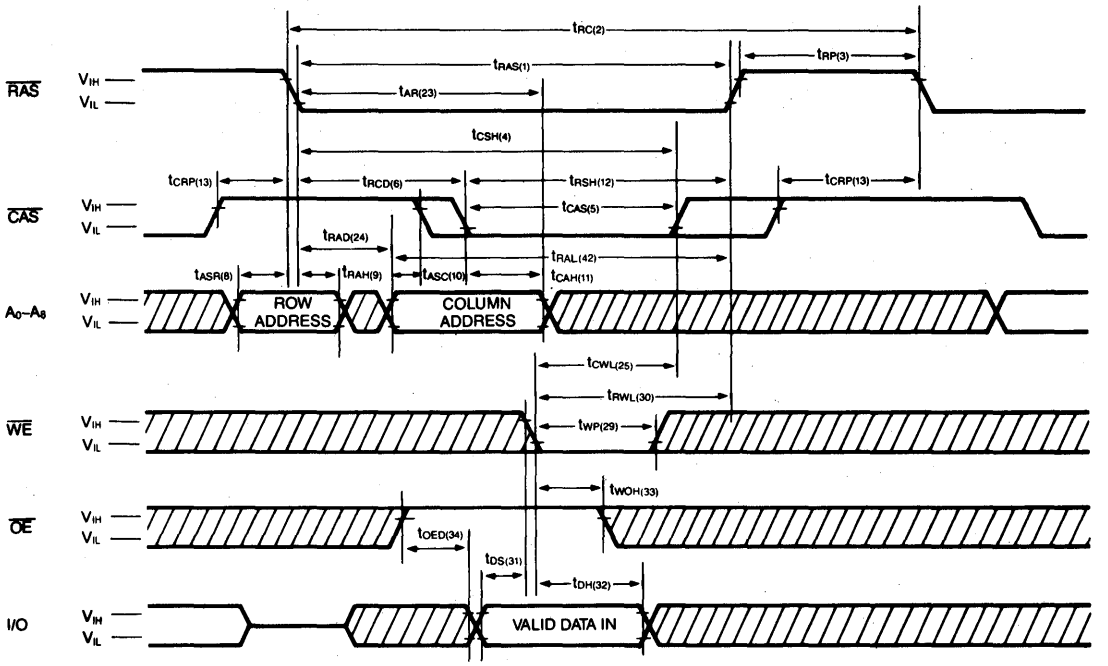
READ CYCLE



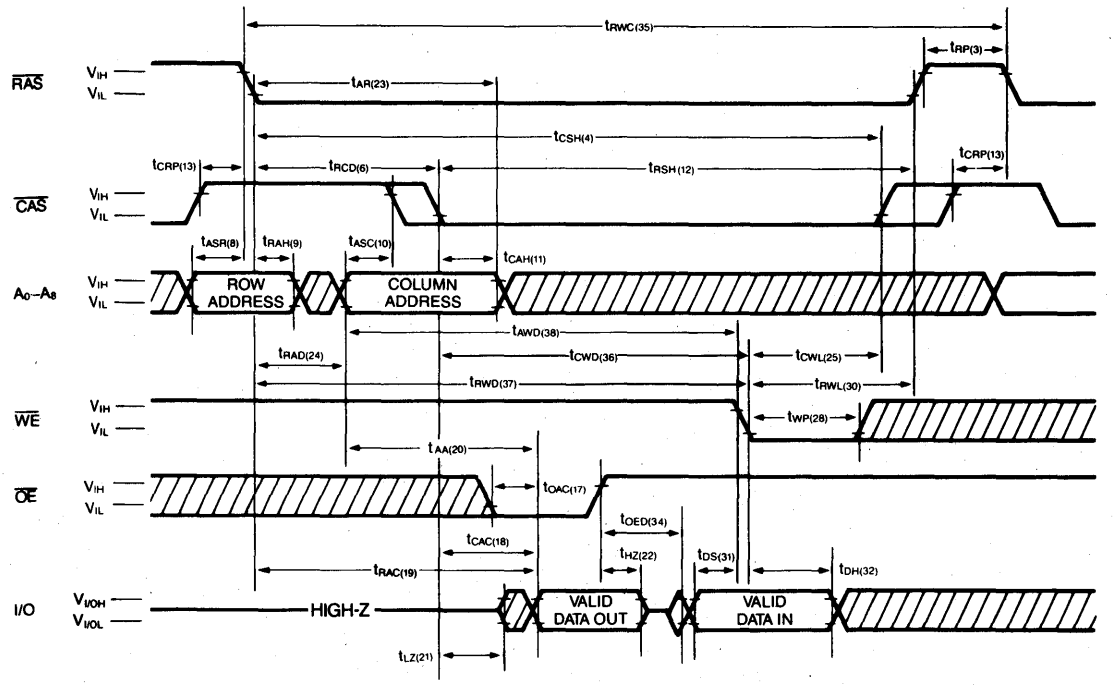
EARLY WRITE CYCLE



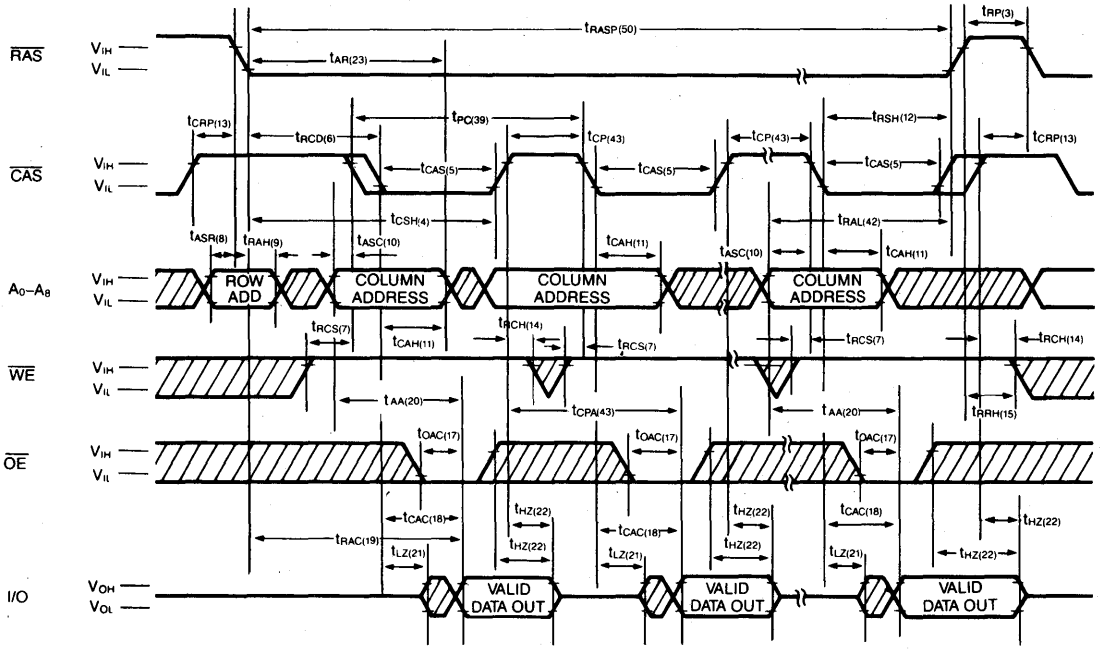
WRITE CYCLE ($\overline{OE}$ CONTROLLED)



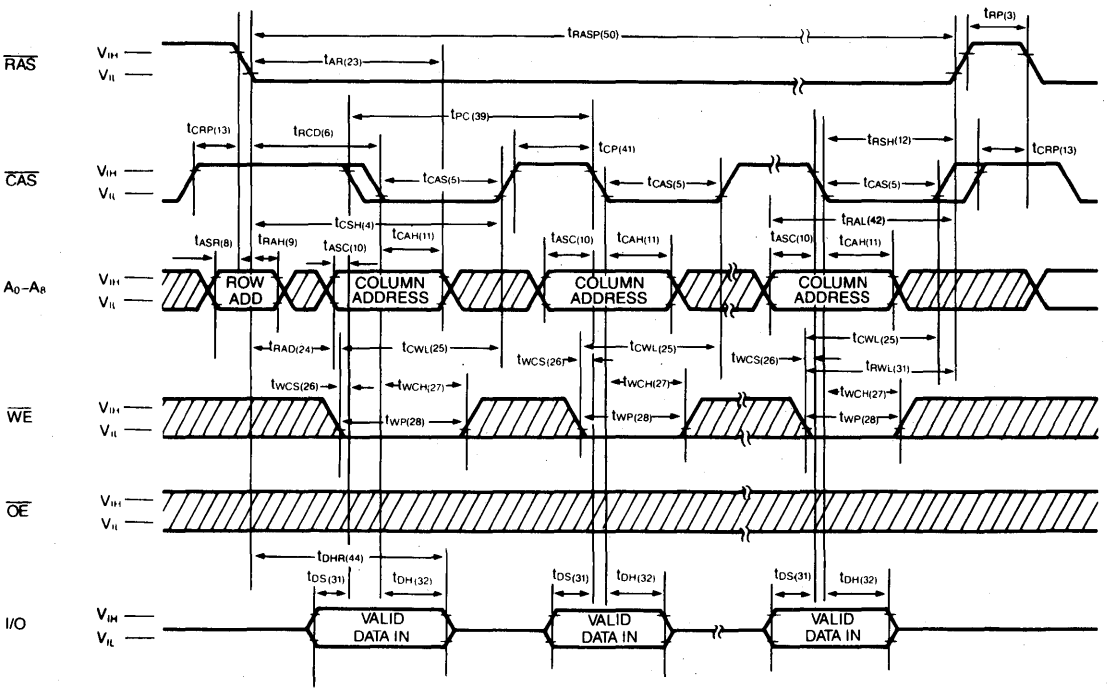
READ-MODIFY-WRITE CYCLE



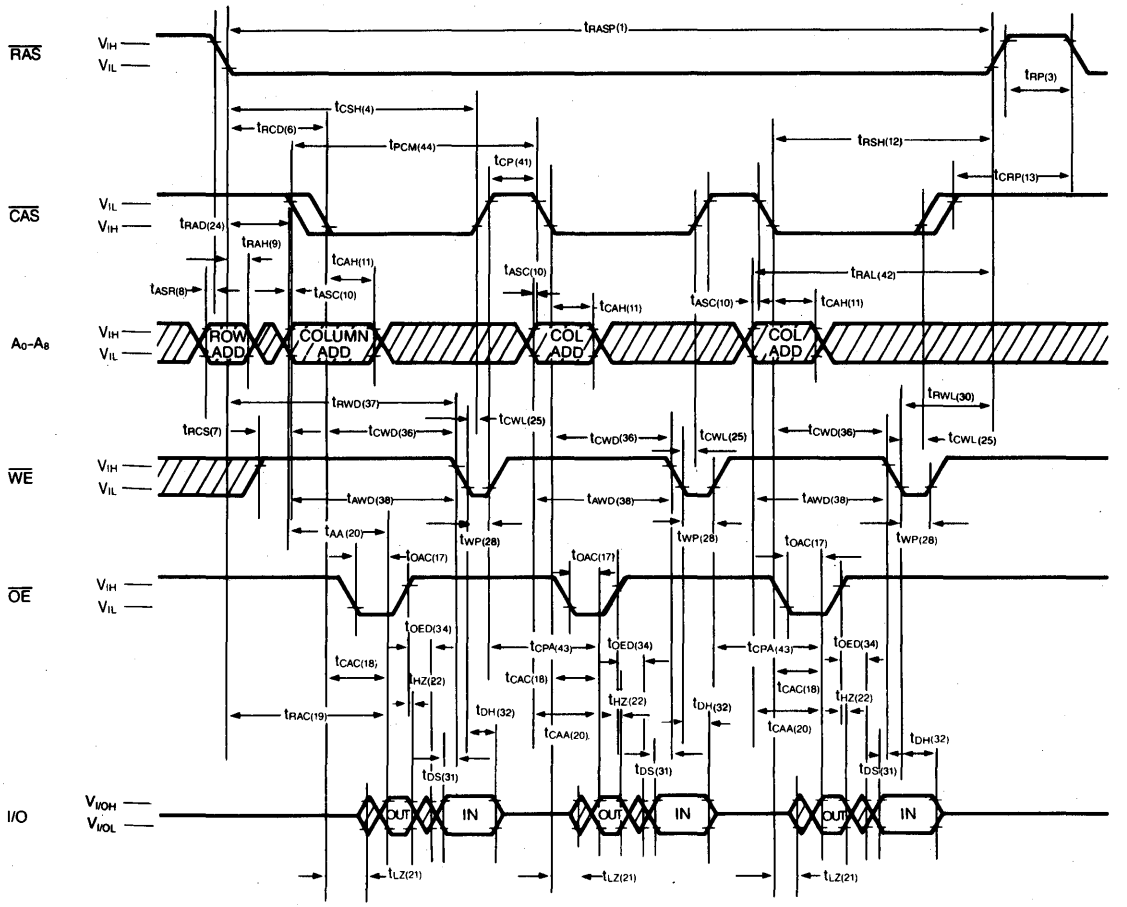
FAST PAGE MODE READ CYCLE



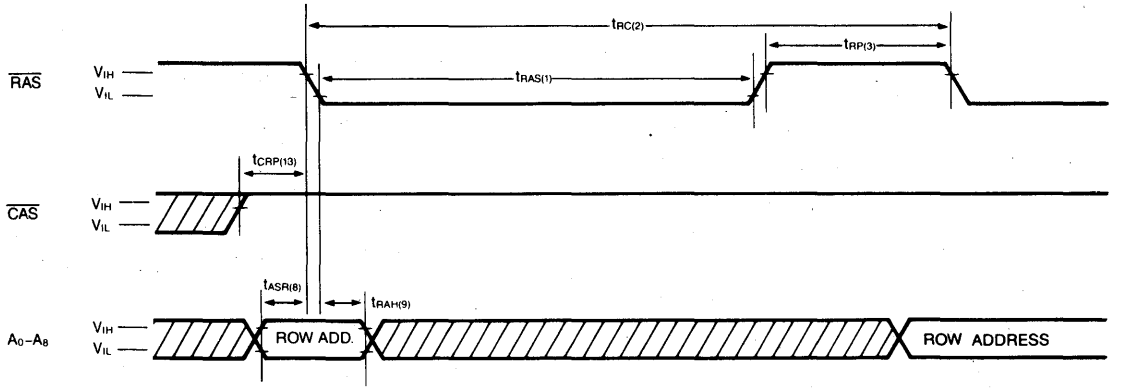
FAST PAGE MODE EARLY WRITE CYCLE



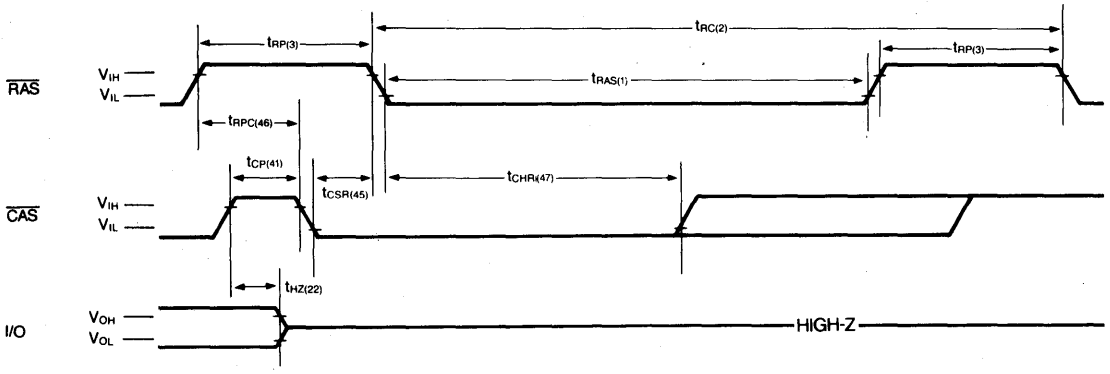
FAST PAGE MODE READ-MODIFY-WRITE CYCLE



RAS-ONLY REFRESH CYCLE

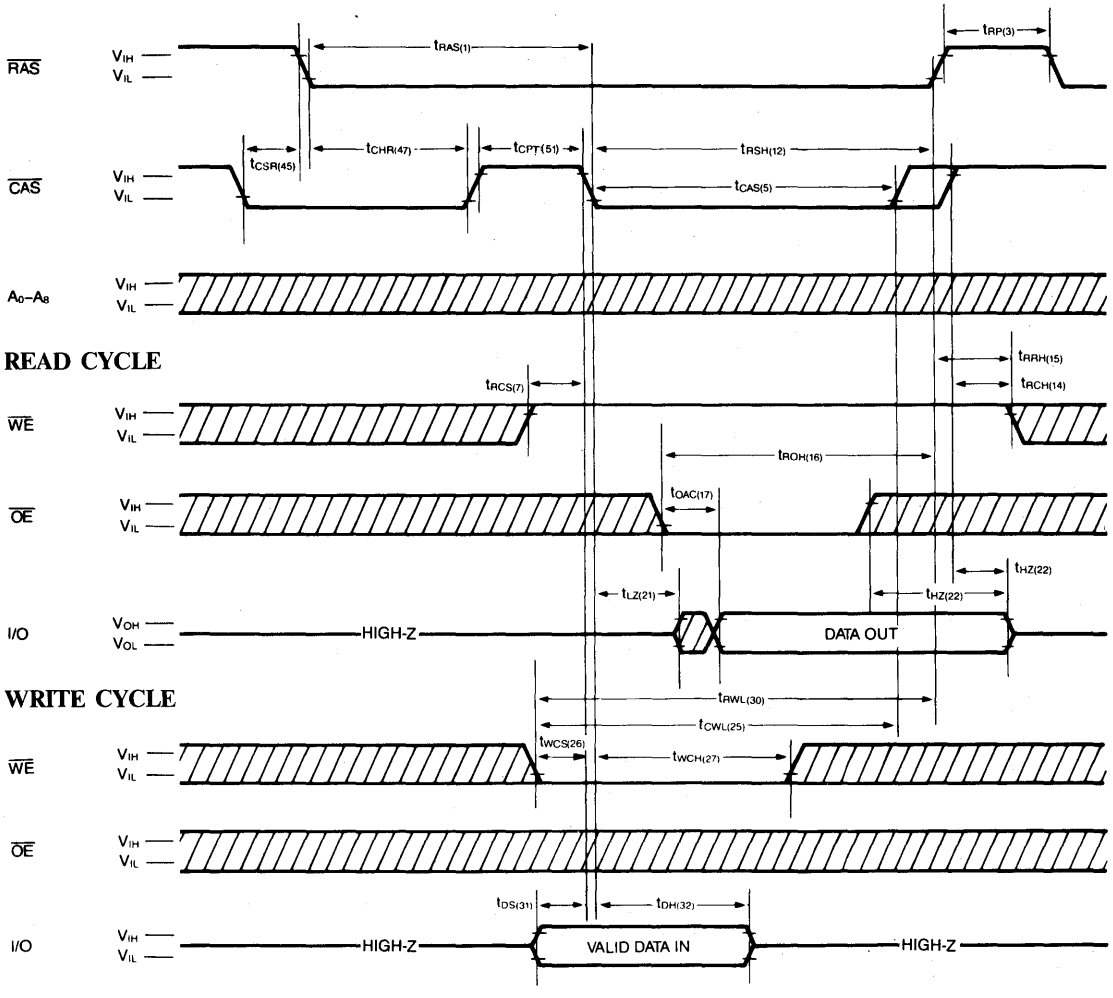


CAS-BEFORE-RAS REFRESH CYCLE



Note: $\overline{WE}$, $\overline{OE}$, A_0–A_8 = Don't care

CAS-BEFORE-RAS REFRESH COUNTER TEST CYCLE



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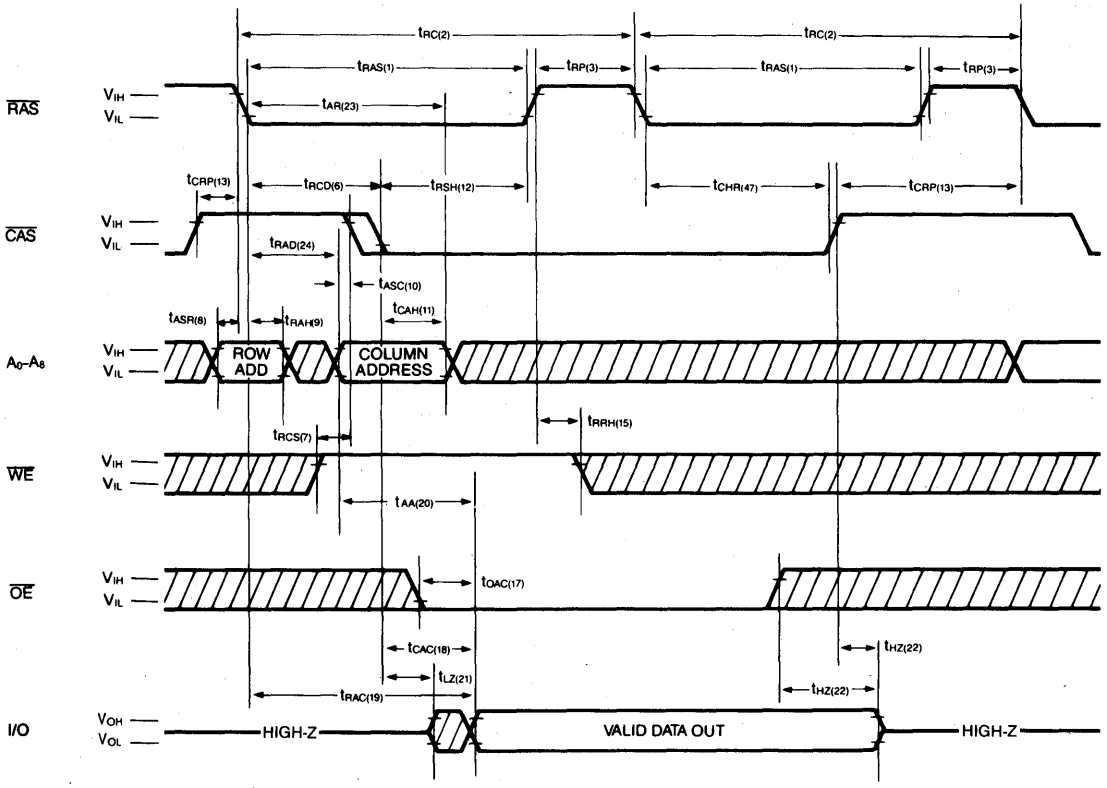
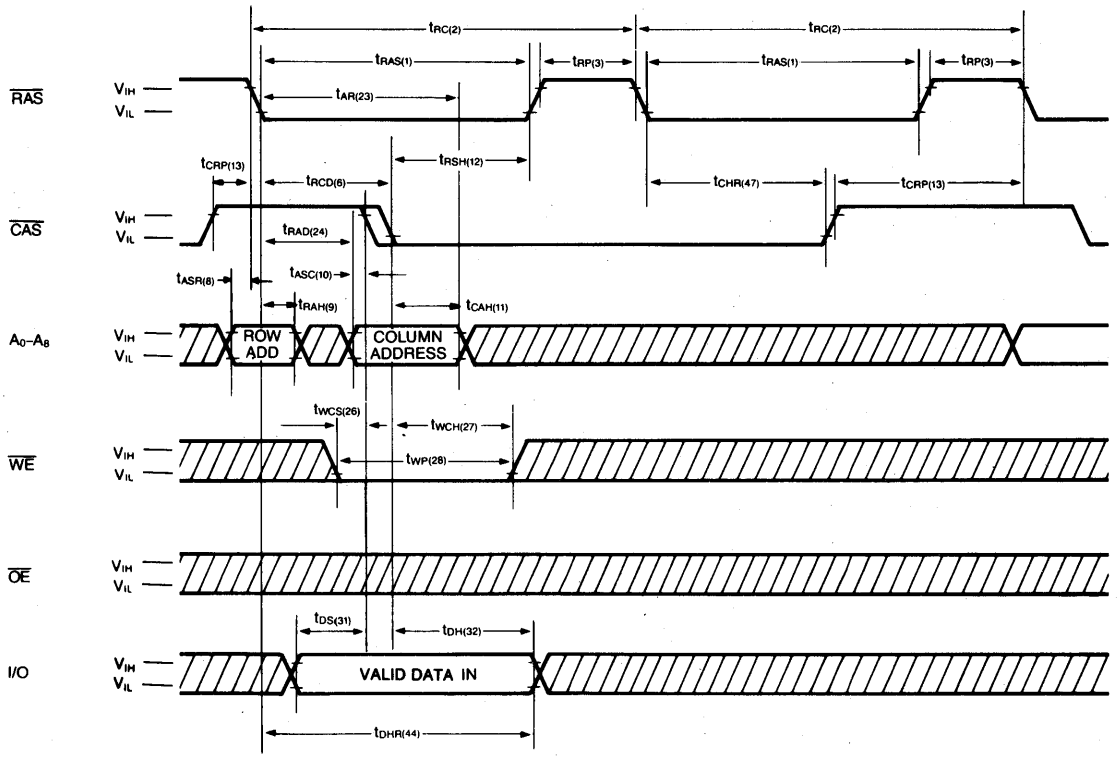
HIDDEN REFRESH CYCLE (READ)



HIDDEN REFRESH CYCLE (WRITE)



FUNCTIONAL DESCRIPTION

The HY534256A is a CMOS dynamic RAM optimized for high data bandwidth and low power applications. The functionality is similar to a traditional dynamic RAM. The HY534256A reads and writes 4 bits of data at a time by multiplexing a 18 bit address into a 9 bit row and a 9 bit column address. The row address is latched by the Row Address Strobe($\overline{RAS}$). The column address, however, flows through the internal address buffer and is latched by the Column Address Strobe ($\overline{CAS}$). Because access time is primarily dependent on a valid column address, the delay time between $\overline{RAS}$ and $\overline{CAS}$ can be long without affecting the access time.

MEMORY CYCLE

The memory cycle is initiated by bringing $\overline{RAS}$ low. Any memory cycle once initiated must not be ended or aborted prior to fulfilling the minimum t_{RAS} timing specification. This ensures proper device operation and data integrity. Additionally, a new cycle cannot be initiated until the minimum precharge time, t_{RP}, and t_{CP} has elapsed.

READ CYCLE

A read cycle is performed by maintaining the Write Enable ($\overline{WE}$) signal high during the $\overline{RAS}$ operation. The column address must be held for a minimum time specified by t_{AR}. Data out is controlled by the Out Enable($\overline{OE}$) and $\overline{CAS}$(See the write cycle description).

Data out becomes valid only when t_{RAC}, t_{AA}, t_{OAC} and t_{CAC} are all satisfied. Consequently, the access time is dependent upon the timing relationship among t_{RAC}, t_{OAC} and t_{CAC} are all satisfied.

WRITE CYCLE

A write cycle is performed by taking $\overline{WE}$ low during a $\overline{RAS}$ operation.

The column address is latched by $\overline{CAS}$, The input data must be valid at or before the falling edge of $\overline{WE}$ or $\overline{CAS}$, whichever occurs last. Consequently, the write cycle can be $\overline{WE}$ controlled or $\overline{CAS}$ controlled depending upon the latter of $\overline{WE}$ or $\overline{CAS}$ low transition. In a $\overline{CAS}$ controlled write cycle(the leading edge or $\overline{WE}$ occurs prior to or coincident with the $\overline{CAS}$ low transition)the input/output (I/O) pin will be in the high impedance state at the beginning of the write function. Terminating the write action with $\overline{CAS}$ going high will maintain the I/O in the high impedance state, terminating with $\overline{WE}$ going high allows the output to go active, and $\overline{OE}$ must be brought high to allow for inputs on the I/O.

The HY534256A incorporates a self-timed write feature which simplifies the system interface and optimizes data bandwidth. After the write funcition has been initiated, the HY534256A internally completes the write action and unlatches the address and data latches. Thus, the latches are ready for the next input/output cycle. This eliminates the need for long address and data hold times during the write operation and allows a subsequent column address to be applied earlier. This minimizes a write pulse width, write precharge time, and hold time which provides maximum flexibility in system design.

REFRESH CYCLE

To retain data, 512 $\overline{RAS}$ refresh cycle are required in an 8 ms period. The refresh operation can be performed two ways :

1. Clocking each of 512 row address(A_0 through A_8) with $\overline{RAS}$ at least every 8 ms period. Any combination of $\overline{RAS}$ cycle such as read, write, read-modify-write, or $\overline{RAS}$-only refresh cycle will perform a refresh.
2. $\overline{CAS}$-before-$\overline{RAS}$ refresh cycle : If $\overline{CAS}$ go low prior to $\overline{RAS}$ go low, the chip enters $\overline{CAS}$-before-$\overline{RAS}$ refresh cycle. The HY534256A will use an internal nine bits counter output as the source of the row address and will ignore the external address inputs.

This $\overline{CAS}$-before-$\overline{RAS}$ refresh mode is a refresh only mode and no data access is

allowed. Also, the $\overline{CAS}$-before-$\overline{RAS}$ refresh cycle does not cause device selection and the state of the data output pin will remain in a high impedance state.

In order to guarantee the reliable operation of $\overline{CAS}$-before-$\overline{RAS}$ refresh mode, an internal counter test mode is provided. The user can use the counter test mode to write in a data pattern consecutively (512 write cycles) and, then verify the data which has been written by 512 consecutive read cycles.

DATA RETENTION MODE

The HY534256A offers a CMOS standby mode that is entered by causing the $\overline{RAS}$ clock to swing between a valid V_{IL} and an "extra high" V_{IH} within 0.2V of V_{DD}. While the $\overline{RAS}$ clock is at the "extra high" level, the HY534256A power consumption is reduced to the low I_{DD5} level. Overall I_{DD} consumption when operating in this mode can be calculated as follows :

$$I=\frac{(t_{RC})\times(I\ active)+(t_{RX}-t_{RC})\times(I_{DD5})}{t_{RX}}$$

Where t_{RC} = Refersh Cycle Time
t_{RX} = Refresh Interval/512

FAST PAGE MODE OPERATION

Fast page mode operation permits all 512 columns within a selected row of the device to be randomly accessed at a high data rate. Maintaining $\overline{RAS}$ low while sucessive $\overline{CAS}$ cycles are performed retains the row address internally, eliminating the need to reapply it. The column address buffer acts as transparent or flow through latch while $\overline{CAS}$ is high. Access begins from the valid column address rather than from $\overline{CAS}$, eliminating t_{ASC} and t_T from the critical timing path. $\overline{CAS}$ latches the address into column address buffer and acts as an output enable.

During this operation, read, write, and read-modify-write, or read-write-read cycles are possible at random or sequential address within a low. Following the entry cycle into fast page mode, access time is t_{AA} or t_{CAP} dependent. It the column address is valid prior to or coincident by t_{CAP} as shown in figure 1. If the column address is valid after the rising edge of $\overline{CAS}$, then the access time is determined by the valid column address specified by t_{AA}, For both cases, the falling edge of $\overline{CAS}$ latches the address and enable the output.

Fast page mode provides a sustanined data rate over 25 MHz for applications that require high data rate such as bit mapped graphics or high speed signal processing. The following equation can be used to calculate the data rate :

$$\text{Data Rate}=\frac{512}{t_{RC}+511\times t_{PC}}$$

DATA OUT OPERATION

The HY534256A input/output(I/O) is controlled by $\overline{OE}$, $\overline{CAS}$, $\overline{WE}$ and $\overline{RAS}$. A $\overline{RAS}$ low transition enables data to transfer into and from a selected row address. A $\overline{RAS}$ high transition disables data transfer and will latch the output data if the output is enabled. After a memory cycle is initiated by a $\overline{RAS}$ low transition, a $\overline{CAS}$ low transition or a $\overline{CAS}$ low level enables the internal I/O data. A $\overline{CAS}$ high transition or a $\overline{CAS}$ high level disables the I/O data path and disables the output driver if the driver was enabled. A $\overline{CAS}$ low transition while $\overline{RAS}$ is high has no effect on the I/O data path, nor on the output driver.

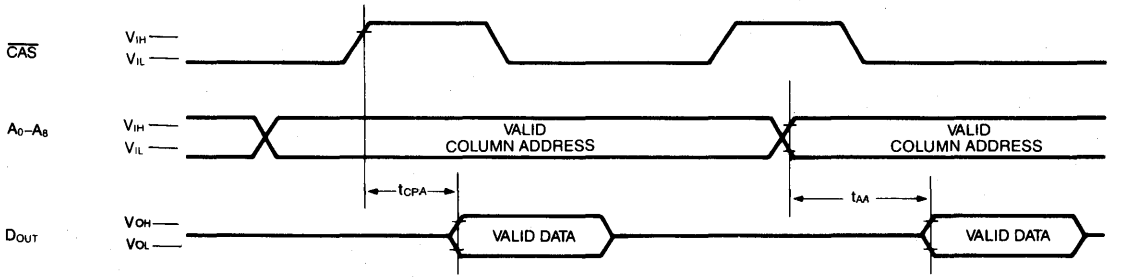
An $\overline{OE}$ low transiton or an $\overline{OE}$ low level enables the output driver when the I/O data path is enabled. An $\overline{OE}$ high transition or an OE high level disables the output driver, but does not disable the data when it has been enabled. A $\overline{WE}$ low level disables the output driver when a $\overline{CAS}$ low level occurs. If the $\overline{WE}$ low transition occurs after the $\overline{CAS}$ low transition such that the output driver is enable prior to the $\overline{WE}$ low transition, it is neccessary to use $\overline{OE}$ to disable the output driver prior to the $\overline{WE}$ low transition to allow data in set-up time(t_{DS}). A $\overline{WE}$ high transition passes control of the output drive to $\overline{OE}$.

POWER ON

An initial pause of 200 μs is required after the application of V_{DD} power supply, followed by a minimum of eight initialization cycles(any combination of cycles containing a $\overline{RAS}$ clock such as $\overline{RAS}$-only refresh cycle). Eight initialization cycles are required after extended periods of bias without clocks(greater than the refresh interval).

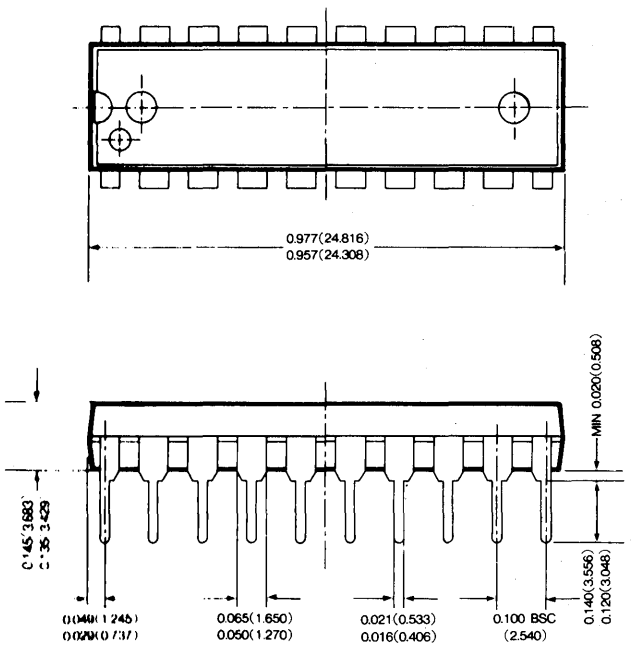
The V_{DD} current (I_{DD}) requirement of the HY534256A during power on is dependent upon the input levels of $\overline{RAS}$ and $\overline{CAS}$. If $\overline{RAS}=V_{SS}$ during power on, the device would go into an active cycle and I_{DD} would exhibit large current transients. It is recommended that $\overline{RAS}$ and $\overline{CAS}$ track with V_{DD} or be held at a valid V_{IH} during power on.

FIGURE 1. FAST PAGE MODE ACCESS TIME DETERMINATION

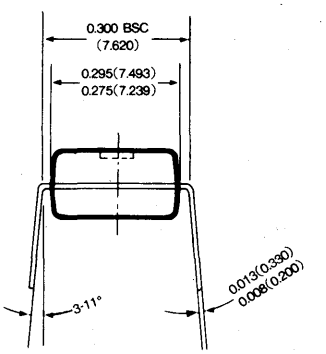


PACKAGE INFORMATION

• 20 PIN PLASTIC DUAL IN LINE PACKAGE – 300 MIL

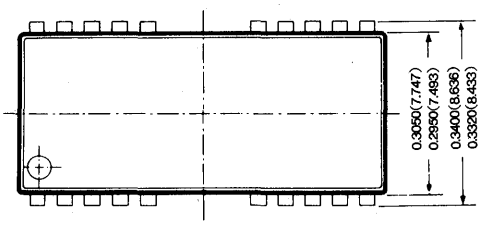


UNIT : INCH(mm) MAX/MIN

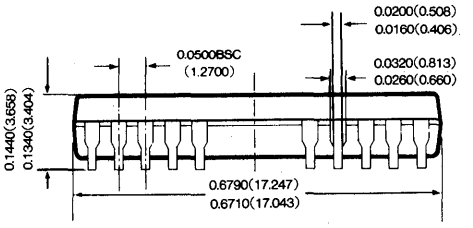


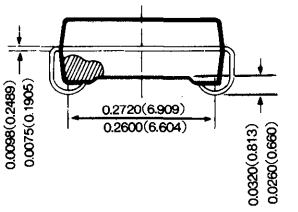
3

• 20/26 PIN SMALL OUTLINE J-FORM PACKAGE – 300 MIL



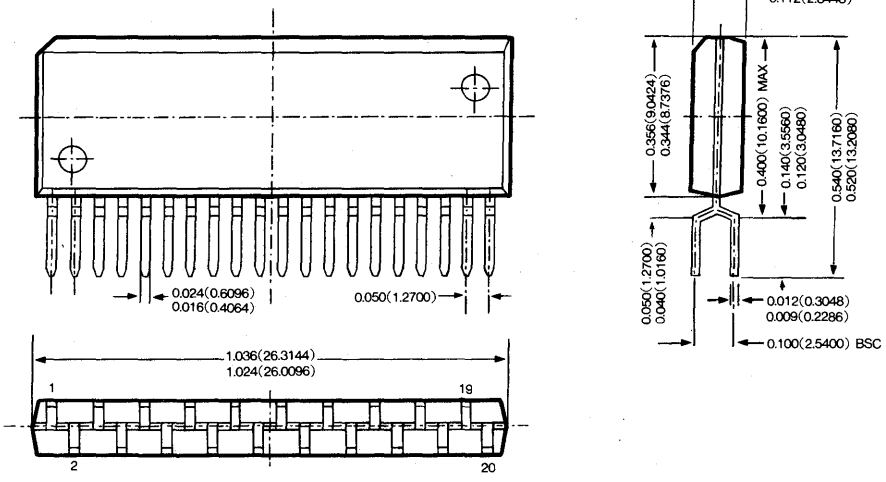
UNIT : INCH(mm) MAX / MIN





• 20 PIN ZIGZAG-IN-LINE PACKAGE−400MIL

UNIT : INCH(mm) MAX/MIN



3