HM538253 Series

Preliminary

262,144-Word x 8-Bit Multiport CMOS Video RAM

HITACHI

Rev. 2
Apr. 2, 1992

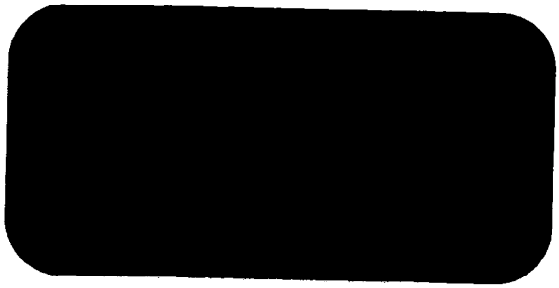
The HM538253 is a 2-Mbit multiport video RAM equipped with a 256-kword x 8-bit dynamic RAM and a 512-word x 8-bit SAM (full-sized SAM). Its RAM and SAM operate independently and asynchronously. The HM538253 has basically upward-compatibility with the HM534253A / HM538123A except that pseudo-write-transfer cycle is replaced with masked-write-transfer cycle, which has been approved by JEDEC. Furthermore, several new features are added to the HM538253 without conflict with the conventional features. Stopping column feature realizes much flexibility to the length of split SAM register. Persistent mask is also installed according to the TMS34020 features.

Features

- Multiport organization
  - Asynchronous and simultaneous operation of RAM and SAM capability
    - RAM: 256 kword x 8 bit
    - SAM: 512 word x 8 bit
- Access time
  - RAM: 70 ns/80 ns/100 ns max
  - SAM: 22 ns/25 ns/25 ns max
- Cycle time
  - RAM: 130 ns/150 ns/180 ns min
  - SAM: 25 ns/30 ns/30 ns min
- Low power
  - Active: RAM: 715 mW max; SAM: 468 mW max
  - Standby: 38.5 mW max
- Masked-write-transfer cycle capability
- Stopping column feature capability
- Persistent mask capability
- High-speed page mode capability
- Mask write mode capability
- Bidirectional data transfer cycle between RAM and SAM capability
- Split transfer cycle capability
- Block write mode capability
- Flash write mode capability
- 3 veriations of refresh (8 ms/512 cycles)
  - $\overline{RAS}$-only refresh
  - $\overline{CAS}$-before-$\overline{RAS}$ refresh
  - Hidden refresh
- TTL compatible

Ordering Information

Type No.	Access time	Package
HM538253J-7	70 ns	400 mil 40-pin plastic SOJ (CP-40D)
HM538253J-8	80 ns	
HM538253J-10	100 ns	
HM538253TT-7	70 ns	44-pin thin small outline package (TTP-40DA)
HM538253TT-8	80 ns	
HM538253TT-10	100 ns	
HM538253RR-7	70 ns	44-pin thin small outline package (TTP-40DAR)
HM538253RR-8	80 ns	
HM538253RR-10	100 ns	

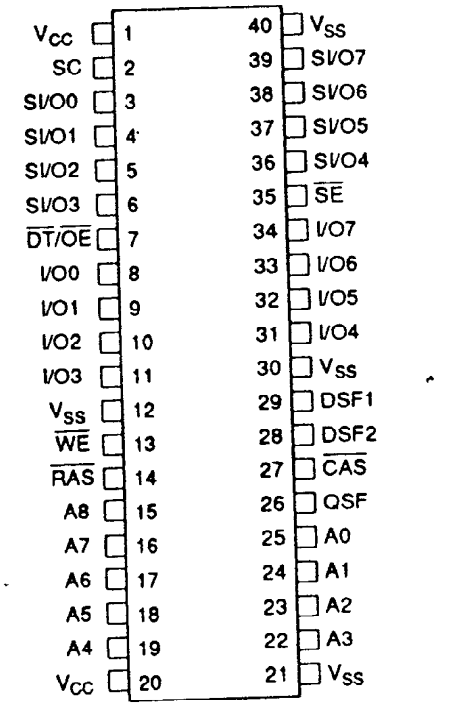


Hitachi semiconductor

Preliminary: This document contains information on a new product. Specifications and information contained herein are subject to change without notice.

Pin Arrangement

HM538253J Series

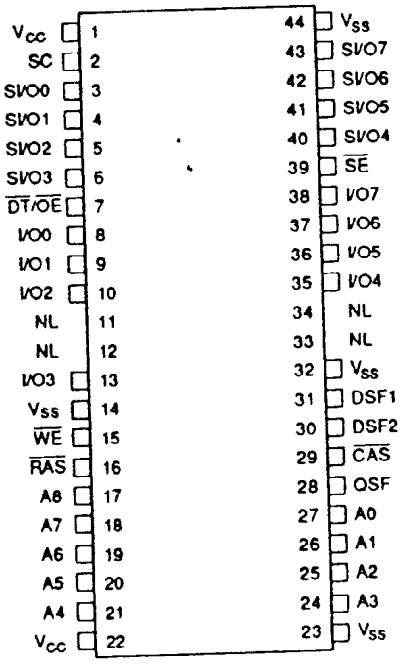


(Top View)

Pin Description

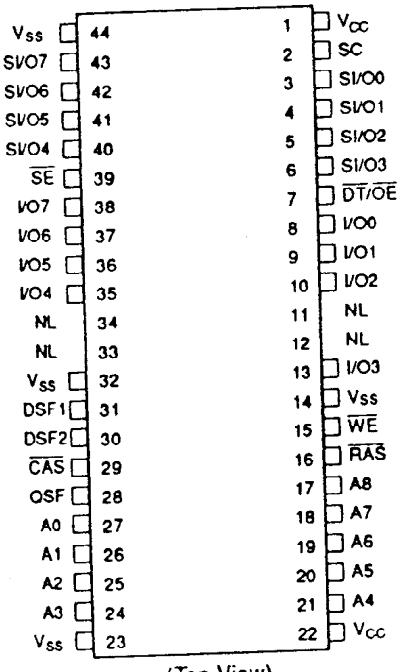
Pin name	Function
A0 – A8	Address inputs
I/O0 – I/O7	RAM port data inputs/outputs
SI/O0 – SI/O7	SAM port data inputs/outputs
$\overline{RAS}$	Row address strobe
$\overline{CAS}$	Column address strobe
$\overline{WE}$	Write enable
$\overline{DT/OE}$	Data transfer/output enable
SC	Serial clock
$\overline{SE}$	SAM port enable
DSF1, DSF2	Special function input flag
QSF	Special function output flag
V_{CC}	Power supply
V_{SS}	Ground
NL	No lead

HM538253TT Series



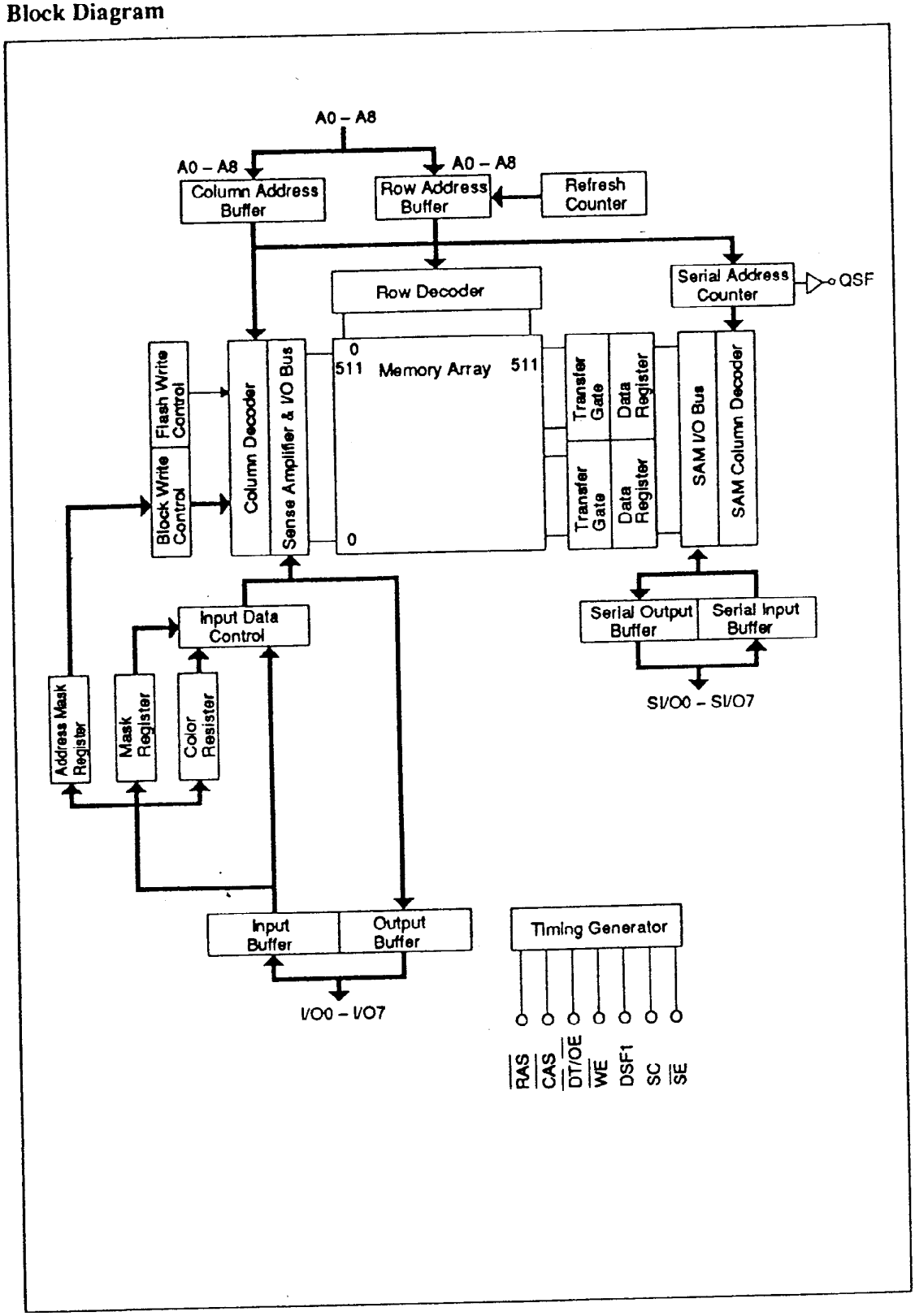
(Top View)

HM538253RR Series



(Top View)

Block Diagram



Pin Functions

$\overline{RAS}$ (input pin): $\overline{RAS}$ is a basic RAM signal. It is active in low level and standby in high level. Row address and signals as shown in table 1 are input at the falling edge of $\overline{RAS}$. The input level of these signals determine the operation cycle of the HM538253.

Table 1. Operation Cycles of the HM538253

Mnemonic Code	$\overline{RAS}$					$\overline{CAS}$		Address		I/On Input	
	$\overline{CAS}$	DT/$\overline{OE}$	$\overline{WE}$	DSF1	DSF2	DSF1	DSF2	$\overline{RAS}$	$\overline{CAS}$	$\overline{RAS}$	$\overline{CAS}$/$\overline{WE}$
CBRS	0	–	0	1	0	–	0	Stop	–	–	–
CBRR	0	–	1	0	0	–	0	–	–	–	–
CBRN	0	–	1	1	0	–	0	–	–	–	–
MWT	1	0	0	0	0	–	0	Row	TAP	WM	–
MSWT	1	0	0	1	0	–	0	Row	TAP	WM	–
RT	1	0	1	0	0	–	0	Row	TAP	–	–
SRT	1	0	1	1	0	–	0	Row	TAP	–	–
RWM	1	1	0	0	0	0	0	Row	Column	WM	Input data

Mnemonic Code	Write Mask	Pers W.M.	Register		No.of Bndry	Function
			WM	Color		
CBRS	–	–	–	–	Set	CBR refresh with stop resister set
CBRR	–	Reset	Reset	–	Reset	CBR refresh with register reset
CBRN	–	–	–	–	–	CBR refresh (no reset)
MWT	Yes	No Yes	Load/use Use	–	–	Masked write transfer (new/old mask)
MSWT	Yes	No Yes	Load/use Use	–	Use	Masked split write transfer (new/old mask)
RT	–	–	–	–	–	Read transfer
SRT	–	–	–	–	Use	Split read transfer
RWM	Yes	No Yes	Load/use Use	–	–	Read/write (new/old mask)

Table 1. Operation Cycles of the HM538253 (cont)

Mnemonic	RAS					CAS		Address		I/On Input	
Code	CAS	DT/OE	WE	DSF1	DSF2	DSF1	DSF2	RAS	CAS	RAS	CAS/WE
BWM	1	1	0	0	0	1	0	Row	Column	WM	Column Mask
RW (No)	1	1	1	0	0	0	0	Row	Column	–	Input Data
BW (No)	1	1	1	0	0	1	0	Row	Column	–	Column Mask
FWM	1	1	0	1	0	–	0	Row	–	WM	–
LMR and Old Mask Set	1	1	1	1	0	0	0	(Row)	–	–	Mask Data
LCR	1	1	1	1	0	1	0	(Row)	–	–	Color
Option	0	0	0	0	0	–	0	Mode	–	Data	–

Mnemonic Code	Write Mask	Pers W.M.	Register WM	Register Color	No.of Bndry	Function
BWM	Yes	No Yes	Load/use Use	Use	–	Block write (new/old mask)
RW (No)	No	No	–	–	–	Read/write (no mask)
BW (No)	No	No	–	Use	–	Block write (no mask)
FWM	Yes	No Yes	Load/use Use	Use	–	Masked flash write (new/old mask)
LMR and Old Mask Set	–	Set	Load	–	–	Load mask register and old mask set
LCR	–	–	–	Load	–	Load color resister set
Option	–	–	–	–	–	–

Notes: 1. With CBRS, all SAM operations use stop register.
2. After LMR, RWM, BWM, FWM, MWT, and MSWT, use old mask which can be reset by CBRR.
3. DSF2 is fixed low in all operation. (for the addition of operation mode in future)

$\overline{CAS}$ (input pin): Column address and DSF1 signals are fetched into chip at the falling edge of $\overline{CAS}$, which determines the operation mode of the HM538253. $\overline{CAS}$ controls output impedance of I/O in RAM.

A0 – A8 (input pins): Row address (AX0 – AX8) is determined by A0 – A8 level at the falling edge of $\overline{RAS}$. Column address (AY0 – AY8) is determined by A0 – A8 level at the falling edge of $\overline{CAS}$. In transfer cycles, row address is the address on the word line which transfers data with SAM data register, and column address is the SAM start address after transfer.

$\overline{WE}$ (input pin): $\overline{WE}$ pin has two functions at the falling edge of $\overline{RAS}$ and after. When $\overline{WE}$ is low at the falling edge of $\overline{RAS}$, the HM538253 turns to mask write mode. According to the I/O level at the time, write on each I/O can be masked. ($\overline{WE}$ level at the falling edge of $\overline{RAS}$ is don't care in read cycle.) When $\overline{WE}$ is high at the falling edge of $\overline{RAS}$, a no mask write cycle is executed. After that, $\overline{WE}$ switch read/write cycles. In a transfer cycle, the direction of transfer is determined by $\overline{WE}$ level at the falling edge of $\overline{RAS}$. When $\overline{WE}$ is low, data is transferred from SAM to RAM (data is written into RAM), and when $\overline{WE}$ is high, data is transferred from RAM to SAM (data is read from RAM).

I/O0 – I/O7 (input/output pins): I/O pins function as mask data at the falling edge of $\overline{RAS}$ (in mask write mode). Data is written only to high I/O pins. Data on low I/O pins are masked and internal data are retained. After that, they function as inut/output pins as those of a standard DRAM. In block write cycle, they function as address mask data at the falling edges of $\overline{CAS}$ and $\overline{WE}$.

$\overline{DT}/\overline{OE}$ (input pin): $\overline{DT}/\overline{OE}$ pin functions as $\overline{DT}$ (data transfer) pin at the falling edge of $\overline{RAS}$ and as $\overline{OE}$ (output enable) pin after that. When $\overline{DT}$ is low at the falling edge of $\overline{RAS}$, this cycle becomes a transfer cycle. When $\overline{DT}$ is high at the falling edge of $\overline{RAS}$, RAM and SAM operate independently.

SC (input pin): SC is a basic SAM clock. In a serial read cycle, data outputs from an SI/O pin synchronously with the rising edge of SC. In a serial write cycle, data on an SI/O pin at the rising edge of SC is fetched into the SAM data register.

$\overline{SE}$ (input pin): $\overline{SE}$ pin activates SAM. When $\overline{SE}$ is high, SI/O is in the high impedance state in serial read cycle and data on SI/O is not fetched into the SAM data register in serial write cycle. $\overline{SE}$ can be used as a mask for serial write because internal pointer is incremented at the rising edge of SC.

SI/O0 – SI/O7 (input/output pins): SI/Os are input/output pins in SAM. Direction of input/output is determined by the previous transfer cycle. When it was a read transfer cycle, SI/O outputs data. When it was a masked write transfer cycle or write transfer cycle, SI/O inputs data.

DSF1 (input pin): DSF1 is a special function data input flag pin. It is set to high at the falling edge of $\overline{RAS}$ when new functions such as color register and mask register read/write, split transfer, and flash write, are used.

DSF2 (input pin): DSF2 is also a special function data input flag pin. This pin is fixed to low level in all operations of the HM538253.

QSF (output pin): QSF outputs data of address A8 in SAM. QSF is switched from low to high by accessing address 255 in SAM and from high to low by accessing 511 address in SAM.

Operation of HM538253

RAM Port Operation

RAM Read Cycle ($\overline{DT}/\overline{OE}$ high, $\overline{CAS}$ high and DSF1 low at the falling edge of $\overline{RAS}$, DSF1 low at the falling edge of $\overline{CAS}$)

Row address is entered at the $\overline{RAS}$ falling edge and column address at the $\overline{CAS}$ falling edge to the device as in standard DRAM. Then, when $\overline{WE}$ is high and $\overline{DT}/\overline{OE}$ is low while $\overline{CAS}$ is low, the selected address data outputs through I/O pin. At the falling edge of $\overline{RAS}$, $\overline{DT}/\overline{OE}$ and $\overline{CAS}$ become high to distinguish RAM read cycle from transfer cycle and CBR refresh cycle. Address access time (t_{AA}) and $\overline{RAS}$ to column address delay time (t_{RAD}) specifications are added to enable high-speed page mode.

RAM Write Cycle (Eraly Write, Delayed Write, Read-Modify-Write)
($\overline{DT}/\overline{OE}$ high, $\overline{CAS}$ high and DSF1 low at the falling edge of $\overline{RAS}$, DSF1 low at the falling edge of $\overline{CAS}$)

- No Mask Write Cycle ($\overline{WE}$ high at the falling edge of $\overline{RAS}$)

When $\overline{CAS}$ is set low and $\overline{WE}$ is set low after $\overline{RAS}$ low, a write cycle is executed.
If $\overline{WE}$ is set low before the $\overline{CAS}$ falling edge, this cycle becomes an early write cycle and all I/O become in high impedance.
If $\overline{WE}$ is set low after the $\overline{CAS}$ falling edge, this cycle becomes a delayed write cycle. I/O does not become high impedance in this cycle, so data should be entered with $\overline{OE}$ in high.

- Mask Write Mode ($\overline{WE}$ low at the falling edge of $\overline{RAS}$)

If $\overline{WE}$ is set low at the falling edge of $\overline{RAS}$, two modes of mask write cycle are capable.
1. In new mask mode, mask data is loaded and used. Whether or not an I/O is written depends on I/O level at the falling edge of $\overline{RAS}$. The data is written in high level I/Os, and the data is masked and retained in low level I/Os. This mask data is effective during the $\overline{RAS}$ cycle. So, in page mode cycles the mask data is retained during the page access.
2. If a load mask register cycle (LMR) has been performed, the mask data is not loaded from I/O pins and the mask data stored in mask registers persistently are used. This operation is known as persistent write mask, set by LMR cycle and reset by CBRR cycle.

High-Speed Page Mode Cycle ($\overline{DT}/\overline{OE}$ high, $\overline{CAS}$ high and DSF1 low at the falling edge of $\overline{RAS}$)

High-speed page mode cycle reads/writes the data of the same row address at high speed by toggling $\overline{CAS}$ while $\overline{RAS}$ is low. Its cycle time is one third of the random read/write cycle. In this cycle, read, write, and block write cycles can be mixed. Note that address access time (t_{AA}), $\overline{RAS}$ to column address delay time (t_{RAD}), and access time from $\overline{CAS}$ precharge (t_{ACP}) are added. In one $\overline{RAS}$ cycle, 512-word memory cells of the same row address can be accessed. It is necessary to specify access frequency within t_{RASP} max (100 µs).

Color Register Set/Read Cycle ($\overline{CAS}$ high, $\overline{DT/OE}$ high, $\overline{WE}$ high and DSF1 high at the falling edge of $\overline{RAS}$)

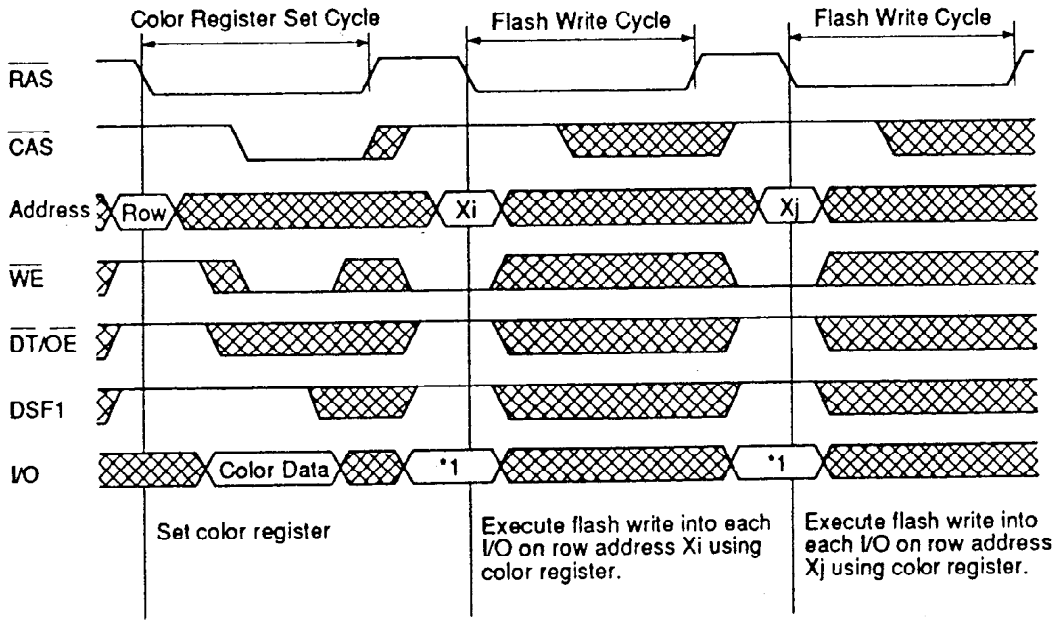
In color register set cycle, color data is set to the internal color register used in flash write cycle or block write cycle. 8 bits of internal color register are provided at each I/O. This register is composed of static circuits, so once it is set, it retains the data until reset. Since color register set cycle is just as same as the usual read and write cycle, read, early write and delayed write cycle can be executed. In this cycle, the HM538253 refreshes the row address fetched at the falling edge of $\overline{RAS}$.

Mask Register Set/Read Cycle ($\overline{CAS}$ high, $\overline{DT/OE}$ high, $\overline{WE}$ high, and DSF1 high at the falling edge of $\overline{RAS}$)

In mask register set cycle, mask data is set to the internal mask register used in mask write cycle, block write cycle, flash write cycle, masked write transfer, and masked split write transfer. 8 bits of internal mask register are provided at each I/O. This mask register is composed of static circuits, so once it is set, it retains the data until reset. Since mask register set cycle is just as same as the usual read and write cycle, read, early write and delayed write cycle can be executed.

Flash Write Cycle ($\overline{CAS}$ high, $\overline{DT/OE}$ high, $\overline{WE}$ low, and DSF1 high at the falling edge of $\overline{RAS}$)

In a flash write cycle, a row of data (512 word x 8 bit) is cleared to 0 or 1 at each I/O according to the data of color register mentioned before. It is also necessary to mask I/O in this cycle. When $\overline{CAS}$ and $\overline{DT/OE}$ is set high, $\overline{WE}$ is low, and DSF1 is high at the falling edge of $\overline{RAS}$, this cycle starts. Then, the row address to clear is given to row address. Mask data is as same as that of a RAM write cycle. Cycle time is the same as those of RAM read/write cycles, so all bits can be cleared in 1/512 of the usual cycle time. (See figure 1.)



*1 I/O Mask Data (In new mask mode)
Low: Mask
High: Non Mask
In persistent mask mode, I/O don't care

Figure 1 Use of Flash Write

Block Write cycle ($\overline{CAS}$ high, $\overline{DT/OE}$ high and DSF1 low at the falling edge of $\overline{RAS}$, DSF1 high and $\overline{WE}$ low at the falling edge of $\overline{CAS}$)

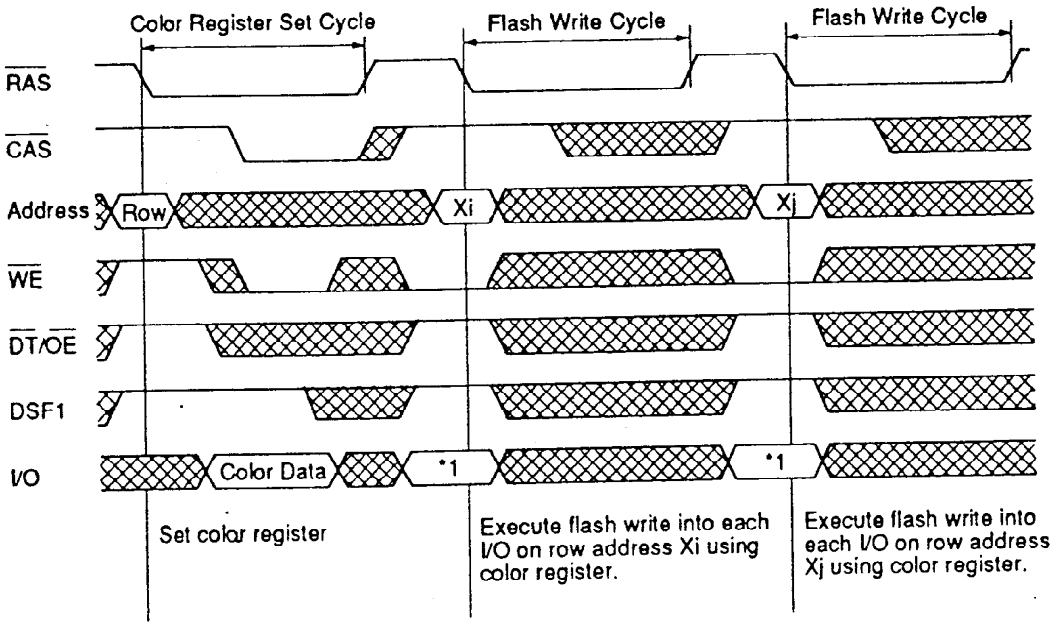
In a block write cycle, 4 columns of data (4 word x 8 bit) is cleared to 0 or 1 at each I/O according to the data of color register. Column addresses A0 and A1 are disregarded. The data on I/Os and addresses can be masked. I/O level at the falling edge of $\overline{CAS}$ determines the address to be cleared. (See Figure 2.) Block write cycle is as the same as the usual write cycle, so early and delayed write, read-modify-write, and page mode write cycle can be executed.

- No mask Mode Block Write Cycle ($\overline{WE}$ high at the falling edge of $\overline{RAS}$)

The data on 8 I/Os are all cleared when $\overline{WE}$ is high at the falling edge of $\overline{RAS}$.

- Mask Block Write Cycle ($\overline{WE}$ low at the falling edge of $\overline{RAS}$)

When $\overline{WE}$ is low at the falling edge of $\overline{RAS}$, the HM538253 starts mask block write mode to clear the data on an optional I/O. The mask data is the same as that of a RAM write cycle.



*1 I/O Mask Data (In new mask mode)
Low: Mask
High: Non Mask
In persistent mask mode, I/O don't care

Figure 2 Use of Block Write

Transfer Operation

The HM538253 provides the read transfer cycle, split read transfer cycle, masked write transfer cycle and masked split write transfer cycle as data transfer cycles. Theses transfer cycles are set by driving $\overline{CAS}$ high and $\overline{DT}/\overline{OE}$ low at the falling edge of $\overline{RAS}$. They have following functions:
(1) Transfer data between row address and SAM data register
Read transfer cycle and split read transfer cycle: RAM to SAM
Masked write transfer cycle and masked split write transfer cycle: SAM to RAM
(2) Determine SI/O state
Read transfer cycle: SI/O output
Masked write transfer cycle: SI/O input
(3) Determine first SAM address to access after transferring at column address (SAM start address).
SAM start address must be determined by read transfer cycle or masked write transfer cycle (split transfer cycle isn't available)before SAM access, after power on, and determined for each transfer cycle.
(4) Use the stopping columns (boundaries) in the serail shift register. If the stopping columns have been set, split transfer cycles use the stopping columns, but any boundaries cannot be set as the start address.
(5) Load/use mask data in masked write transfer cycle and masked split write transfer cycle.

Read Transfer Cycle ($\overline{CAS}$ high, $\overline{DT}/\overline{OE}$ low, $\overline{WE}$ high and DSF1 low at the falling edge of $\overline{RAS}$)

This cycle becomes read transfer cycle by driving $\overline{DT}/\overline{OE}$ low, $\overline{WE}$ high and DSF1 low at the falling edge of $\overline{RAS}$. The row address data (512 x 8 bits) determined by this cycle is transferred to SAM data register synchronously at the rising edge of $\overline{DT}/\overline{OE}$. After the rising edge of $\overline{DT}/\overline{OE}$, the new address data outputs from SAM start address determined by column address. In read transfer cycle, $\overline{DT}/\overline{OE}$ must be risen to transfer data from RAM to SAM.
This cycle can access SAM even during transfer (real time read transfer). In this case, the timing t_{SDD} (min) specified between the last SAM access before transfer and $\overline{DT}/\overline{OE}$ rising edge and t_{SDH} (min) specified between the first SAM access and $\overline{DT}/\overline{OE}$ rising edge must be satisfied. (See figure 3.)
When read transfer cycle is executed, SI/O becomes output state by first SAM access. Input must be set high impedance before t_{SZS} (min) of the first SAM access to avoid data contention.

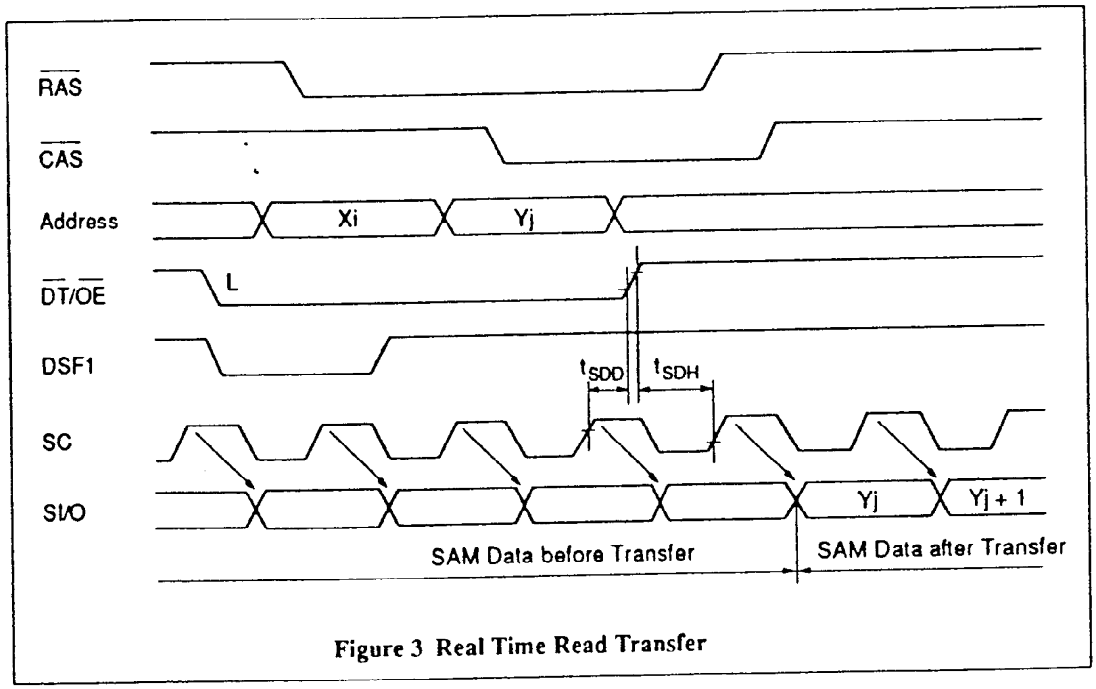


Figure 3 Real Time Read Transfer

Masked Write Transfer cycle ($\overline{CAS}$ high, $\overline{DT}/\overline{OE}$ low, $\overline{WE}$ low, and DSF1 low at the falling edge of $\overline{RAS}$)

Masked write transfer cycle can transfer only selected I/O data in a row of data input by serial write cycle to RAM. Whether one I/O data is transferred or not depends on the corresponding I/O level (mask data) at the falling edge of $\overline{RAS}$. This mask transfer operation is the same as a mask write operation in RAM cycles, so the persistent mode can be supported. The row address of data transferred into RAM is determined by the address at the falling edge of $\overline{RAS}$. The column address is specified as the first address for serial write after terminating this cycle. Also in this cycle, SAM access becomes enabled after t_{SRD} (min) after $\overline{RAS}$ becomes high. SAM access is inhibited during $\overline{RAS}$ low. In this period, SC must bot be risen. Data transferred to SAM by read transfer cycle or split read transfer cycle can be written to other addreses of RAM by write transfer cycle. However, the adddress to write data must be the same as that of the read transfer cycle or the split read transfer cycle (row address AX8)

Split Read Transfer Cycle ($\overline{CAS}$ high, $\overline{DT}/\overline{OE}$ low, $\overline{WE}$ high and DSF1 high at the falling edge of $\overline{RAS}$)

To execute a continuous serial read by real time read transfer, the HM538253 must satisfy SC and $\overline{DT}/\overline{OE}$ timings and requires an external circuit to detect SAM last address. Split read transfer cycle makes it possible to execute a continuous serial read without the above timing limitation.
The HM538253 supports two types of split register operation. One is the normal split register operation to split the data register into two halves. The other is the boundary split register operation using stopping columns described later.
Figure-4 shows the block diagram for the normal split register operation. SAM data register (DR) consists of 2 split buffers, whose organizations are 256-word x 8-bit each. Let us suppose that data is read from upper data reagister DR1 (The row address AX8 is 0 and SAM address A8 is 1.). When split read transfer is executed setting row address AX8 0 and SAM start addresses A0 to A7, 256-word x 8-bit data are transferred from RAM to the lower data register DR0 (SAM address A8 is 0) automatically. After data are read from data register DR1, data start to be read from SAM start addresses of data register DR0. If the next split read transfer isn't executed while data are read from data register DR0, data start to be read from SAM start address 0 of DR1 after data are read from data register DR0. If split read transfer is executed setting row address AX8 1 and SAM start addresses A0 to A7 while data are read from data register DR1, 256-word x 8-bit data are transferred to data register DR2. After data are read from data register DR1, data start to be read from SAM start addresses of data register DR2. If the next split read transfer isn't executed while data is read from data register DR2, data start to be read from SAM start address 0 of data register DR1 after data are read from data register DR2. In split read data transfer, the SAM start address A8 is automatically set in the data register which isn't used.
The data on SAM address A8, which will be accessed next, outputs to QSF, QSF is switched from low to high by accessing SAM last address 255 and from high to low by accessing address 511.
Split read transfer cycle is set when $\overline{CAS}$ is high, $\overline{DT}/\overline{OE}$ is low, $\overline{WE}$ is high and DSF1 is high at the falling edge of $\overline{RAS}$. The cycle can be executed asyncronously with SC. However, HM538253 must be satisfied tSTS (min) timing specified between SC rising (Boundary address) and $\overline{RAS}$ falling. In split transfer cycle, the HM538253 must satisfy t_{RST} (min), t_{CST} (min) and t_{AST} (min) timings specified between $\overline{RAS}$ or $\overline{CAS}$ falling and column address. (See figure 5.)
In split read transfer, SI/O isn't switched to output state. Therefore, read transfer must be executed to switch SI/O to output state when the previous transfer cycle is masked write transfer cycle or masked split write transfer cycle.

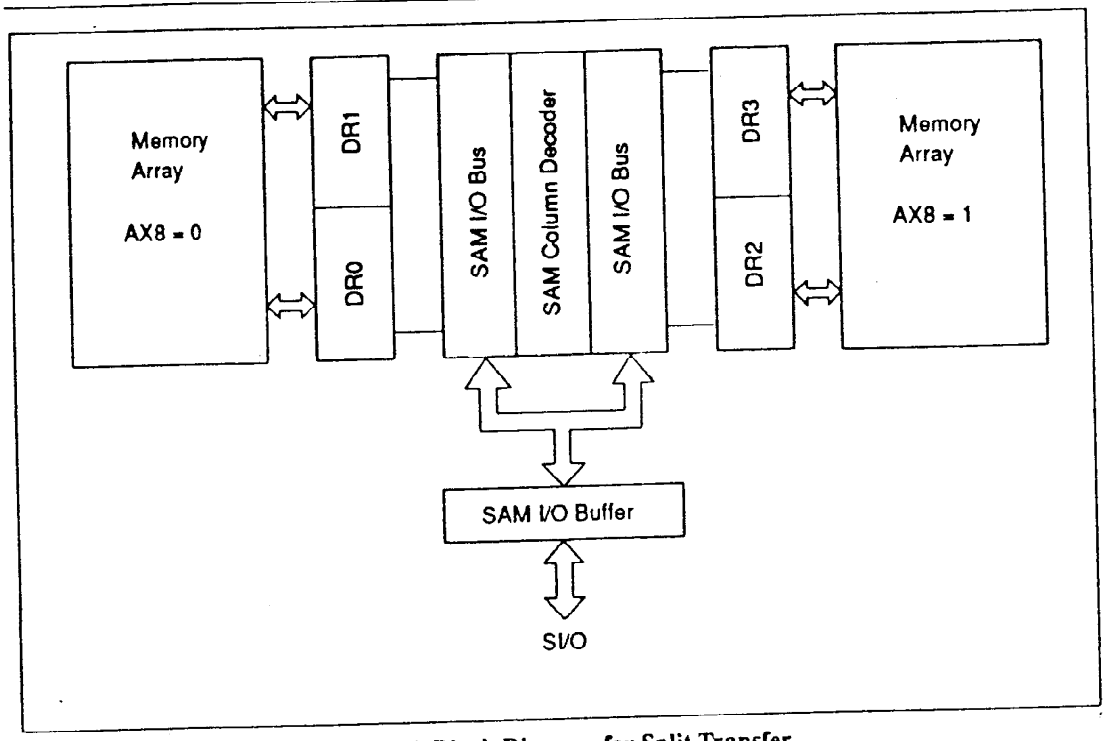


Figure 4 Block Diagram for Split Transfer

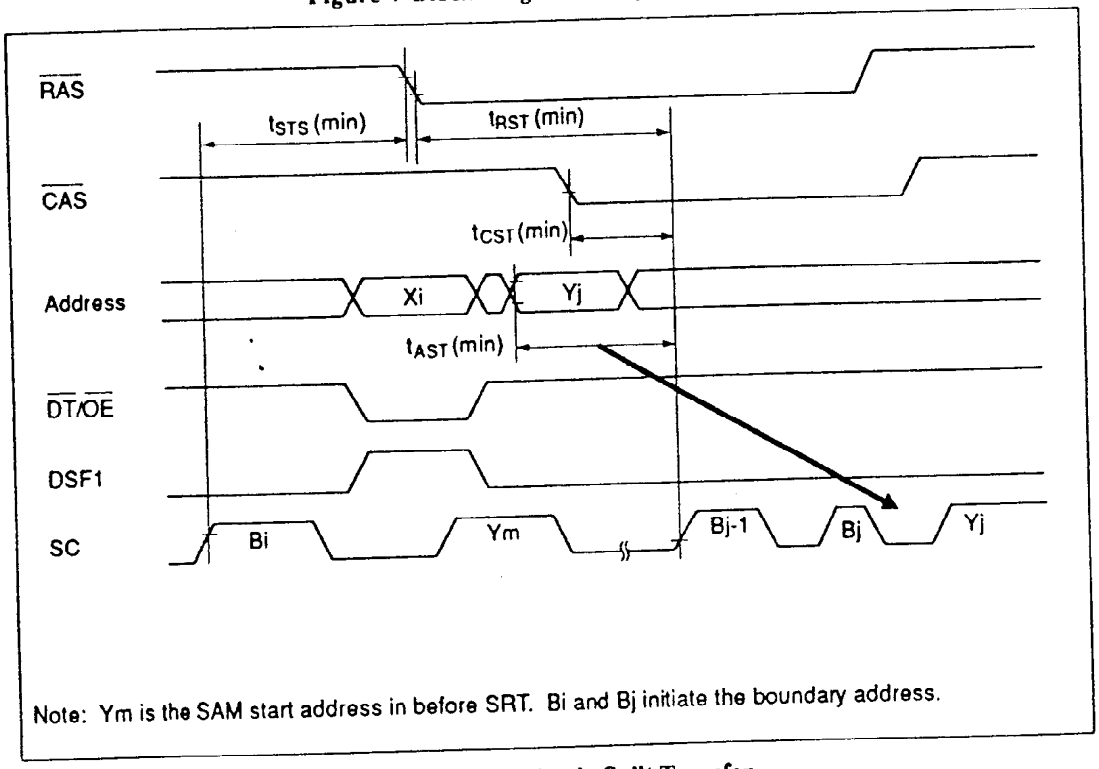


Figure 5 Limitation in Split Transfer

Masked Split Write Transfer Cycle ($\overline{CAS}$ high, $\overline{DT}/\overline{OE}$ low, $\overline{WE}$ low and DSF1 high at the falling edge of $\overline{RAS}$)

A continuous serial write cannot be executed because accessing SAM is inhibited during $\overline{RAS}$ low in write transfer. Masked split write transfer cycle makes it possible. In this cycle, t_{STS} (min), t_{RST} (min), t_{CST} (min) and t_{AST} (min) timings must be satisfied like split read transfer cycle. And it is impossible to switch SI/O to input state in this cycle. If SI/O is in output state, masked write transfer cycle should be executed to switch SI/O into input state. Data transferred to SAM by read transfer cycle or split read transfer cycle can be written to other addresses of RAM by split write transfer cycle. However, in this split write transfer cycle, the MSB of row address (AX8) to write data must be the same as that of the read transfer cycle or the split read transfer cycle. In this cycle, the boundary split register operation using stopping columns is capable like split read transfer cycle.

Stopping Column in Split Transfer Cycle

The HM538253 has the boundary split register operation using stopping columns. If a CBRS cycle has been performed, split transfer cycle performs the boundary operation. Figure 6 shows an example of boundary split register. (Boundary code is B7.)
First of all a read data transfer cycle is executed, and SAM start addresses A0 to A8 are set. The RAM data are transferred to the lower SAM, and SAM serial read starts from the start address (Y1) on the lower SAM. After that, a split read transfer cycle is executed, and the next start address (Y2) is set. The RAM data are transferred to the upper SAM. When the serial read arrive at the first boundary after the split read transfer cycle, the next read jumps to the start address (Y2) on the upper SAM (jump 1) and continues. Then the second split read transfer cycle is executed, and another start address (Y3) is set. The RAM data are transferred to the lower SAM. When the serial read arrive at the other boundary again, the next read jumps to the start address (Y3) on the lower SAM. In stopping column, split transfer is needed for jump operation between lower SAM and upper SAM.

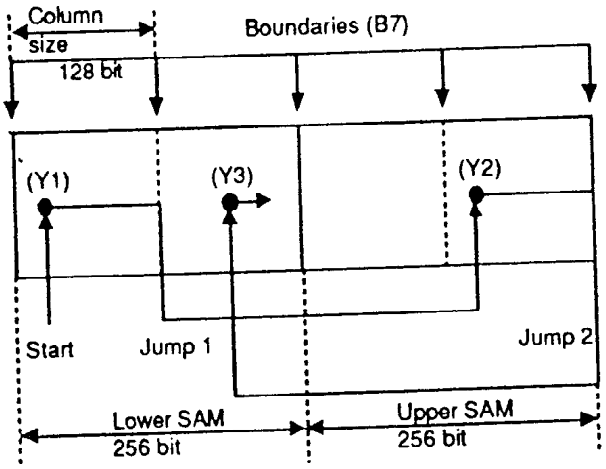


Figure 6 Example of Boundary Split Register

Stopping Column Set Cycle (CBRS)

This cycle becomes stopping column set cycle by driving $\overline{CAS}$ low, $\overline{WE}$ low, DSF1 high at the falling edge of $\overline{RAS}$. Stopping column data (boundaries) are latched from address inputs on the falling edge of $\overline{RAS}$. To determine the boundary, A2 to A7 can be used and don't care A0, A1, and A8. In the HM538253, 7 types of boundary (B2 to B8) can be set including the default case. (See stopping column boundary table.) If A2 to A6 are set to high and A7 is set to low, the boundaries (B7) are selected. Figure 6 shows the example. Once a CBRS is executed, the stopping column operation mode continues until CBRR.

Stopping Column Boundary Table

		Stop Address					
Boundary code	Column size	A2	A3	A4	A5	A6	A7
B2	4	0	*	*	*	*	*
B3	8	1	0	*	*	*	*
B4	16	1	1	0	*	*	*
B5	32	1	1	1	0	*	*
B6	64	1	1	1	1	0	*
B7	128	1	1	1	1	1	0
B8	256	1	1	1	1	1	1

Notes: 1.A0, A1, and A8: don't care
2.*: don't care

Register Reset Cycle (CBRR)

This cycle becomes register reset cycle (CBRR) by driving $\overline{CAS}$ low, $\overline{WE}$ high, and DSF1 low at the falling edge of $\overline{RAS}$. A CBRR can reset the persistent mask operation and stopping column operation, so the HM538253 becomes the new mask operation and boundary code B8. When a CBRR is executed for stopping column operation reset, it needs to safisfy t_{STS} (min) and t_{RST} (min) between $\overline{RAS}$ falling and SC rising.

SAM Port Operation

Serial Read Cycle

SAM port is in read mode when the previous data transfer cycle is read transfer cycle. Access is synchronized with SC rising, and SAM data is output from SI/O. When $\overline{SE}$ is set high, SI/O becomes high impedance, and the internal pointer is incremented by the SC rising. After indicating the last address (address 511), the internal pointer indicates address 0 at the next access.

Serial Write Cycle

If previous data transfer cycle is masked write transfer cycle or write transfer cycle, SAM port goes into write mode. In this cycle, SI/O data is fetched into data register at the SC rising edge like in the serial read cycle. If $\overline{SE}$ is high, SI/O data isn't fetched into data register. Internal pointer is incremented by the SC rising, so $\overline{SE}$ high can be used as mask data for SAM. After indicating the last address (address 511), the internal pointer indicates address 0 at the next access.

Refresh

RAM Refresh

RAM, which is composed of dynamic circuits, requires refresh to retain data. Refresh is executed by accessing all 512 row addresses within 8 ms. There are three refresh cycles: (1) $\overline{RAS}$-only refresh cycle, (2) $\overline{CAS}$-before-$\overline{RAS}$ (CBRN, CBRS, and CBRR) refresh cycle, and (3) Hidden refresh cycle. Besides them, the cycles which activate $\overline{RAS}$ such as read/write cycles or transfer cycles can refresh the row address. Therefore, no refresh cycle is required when all row addresses are accessed within 8 ms.

(1) $\overline{RAS}$-Only Refresh Cycle: $\overline{RAS}$-only refresh cycle is executed by activating only $\overline{RAS}$ cycle with $\overline{CAS}$ fixed to high after inputting the row address (= refresh address) from external circuits. To distinguish this cycle from data transfer cycle, $\overline{DT}/\overline{OE}$ must be high at the falling edge of $\overline{RAS}$.

(2) CBR Refresh Cycle: CBR refresh cycle (CBRN, CBRS and CBRR) are set by activating $\overline{CAS}$ before $\overline{RAS}$. In this cycle, refresh address need not to be input through external circuits because it is input through an internal refresh counter. In this cycle, output is in high impedance and power dissipation is lowered because $\overline{CAS}$ circuits don't operate.

(3) Hidden Refresh Cycle: Hidden refresh cycle executes CBR refresh with the data output by reactivating $\overline{RAS}$ when $\overline{DT}/\overline{OE}$ and $\overline{CAS}$ keep low in normal RAM read cycles.

SAM Refresh

SAM parts (data register, shift resister and selector), organized as fully static circuitry, require no refresh.

Absolute Maximum Ratings

Parameter	Symbol	Value	Unit
Voltage on any pin relative to V_{SS}	V_T	−1.0 to +7.0	V
Supply voltage relative to V_{SS}	V_{CC}	−0.5 to +7.0	V
Short circuit output current	Iout	50	mA
Power dissipation	P_T	1.0	W
Operating temperature	Topr	0 to +70	°C
Storage temperature	Tstg	−55 to +125	°C

Recommended DC Operating Conditions (Ta = 0 to +70°C)

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Supply voltage	V_{CC}	4.5	5.0	5.5	V	1
Input high voltage	V_{IH}	2.4	—	6.5	V	1
Input low voltage	V_{IL}	−0.5*2	—	0.8	V	1

Notes: 1. All voltage referenced to V_{SS}
2 −3.0 V for pulse width ≤ 10 ns.

DC Characteristics (Ta = 0 to +70°C, V_{CC} = 5 V ± 10%, V_{SS} = 0 V)

		HM538253								
		-7		-8		-10				
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Unit	Test conditions	
Operating current	I_{CC1}	—	120	—	105	—	90	mA	$\overline{RAS}$, $\overline{CAS}$ cycling	SC = V_{IL}, $\overline{SE}$ = V_{IH}
	I_{CC7}	—	190	—	160	—	140	mA	t_{RC} = min	$\overline{SE}$ = V_{IL}, SC cycling, t_{SCC} = min
Standby current	I_{CC2}	—	7	—	7	—	7	mA	$\overline{RAS}$, $\overline{CAS}$ = V_{IH}	SC = V_{IL}, $\overline{SE}$ = V_{IH}
	I_{CC8}	—	85	—	70	—	70	mA		$\overline{SE}$ = V_{IL}, SC cycling, t_{SCC} = min
$\overline{RAS}$-only refresh current	I_{CC3}	—	120	—	105	—	90	mA	$\overline{RAS}$ cycling, $\overline{CAS}$ = V_{IH}	SC = V_{IL}, $\overline{SE}$ = V_{IH}
	I_{CC9}	—	190	—	160	—	140	mA	t_{RC} = min	$\overline{SE}$ = V_{IL}, SC cycling, t_{SCC} = min
Page mode current	I_{CC4}	—	130	—	115	—	100	mA	$\overline{CAS}$ cycling, $\overline{RAS}$ = V_{IL}	SC = V_{IL}, $\overline{SE}$ = V_{IH}
	I_{CC10}	—	200	—	170	—	150	mA	t_{PC} = min	$\overline{SE}$ = V_{IL}, SC cycling, t_{SCC} = min
$\overline{CAS}$-before-$\overline{RAS}$ refresh current	I_{CC5}	—	95	—	85	—	70	mA	$\overline{RAS}$ cycling, t_{RC} = min	SC = V_{IL}, $\overline{SE}$ = V_{IH}
	I_{CC11}	—	165	—	140	—	120	mA		$\overline{SE}$ = V_{IL}, SC cycling, t_{SCC} = min
Data transfer current	I_{CC6}	—	130	—	115	—	100	mA	$\overline{RAS}$, $\overline{CAS}$ cycling	SC = V_{IL}, $\overline{SE}$ = V_{IH}
	I_{CC12}	—	200	—	170	—	150	mA	t_{RC} = min	$\overline{SE}$ = V_{IL}, SC cycling, t_{SCC} = min
Input leakage current	I_{LI}	−10	10	−10	10	−10	10	µA		
Output leakage current	I_{LO}	−10	10	−10	10	−10	10	µA		
Output high voltage	V_{OH}	2.4	—	2.4	—	2.4	—	V	I_{OH} = −1 mA	
Output low voltage	V_{OL}	—	0.4	—	0.4	—	0.4	V	I_{OL} = 2.1 mA	

Notes: 1. I_{CC} depends on output load condition when the device is selected. I_{CC} max is specified at the output open condition.
2. Address can be changed once while $\overline{RAS}$ is low and $\overline{CAS}$ is high.

Capacitance (Ta = 25°C, V_{CC} = 5 V ± 10%, f = 1 MHz, Bias: Clock, I/O = V_{CC}, address = V_{SS})

Parameter	Symbol	Typ	Max	Unit	Note
Input capacitance (Address)	C_{I1}	—	5	pF	1
Input capacitance (Clocks)	C_{I2}	—	5	pF	1
Output capacitance (I/O, SI/O, QSF)	$C_{I/O}$	—	7	pF	1

Notes: 1. This parameter is sampled and not 100% tested.

AC Characteristics (Ta = 0 to +70°C, V_{CC} = 5 V ± 10%, V_{SS} = 0 V) *1, *16

Test Conditions

- Input rise and fall times: 5 ns
- Input pulse levels: V_{SS} to 3.0 V
- Input timing reference levels: 0.8 V, 2.4 V
- Output timing reference levels: 0.8 V, 2.0 V
- Output load: RAM 1TTL + CL (50 pF)
  SAM, QSF 1TTL + CL (30 pF)
  (Including scope and jig)

Common Parameter

		HM538253							
		-7		-8		-10			
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Unit	Notes
Random read or write cycle time	t_{RC}	130	—	150	—	180	—	ns	
$\overline{RAS}$ precharge time	t_{RP}	50	—	60	—	70	—	ns	
$\overline{RAS}$ pulse width	t_{RAS}	70	10000	80	10000	100	10000	ns	
$\overline{CAS}$ pulse width	t_{CAS}	20	—	20	—	25	—	ns	
Row address setup time	t_{ASR}	0	—	0	—	0	—	ns	
Row address hold time	t_{RAH}	10	—	10	—	10	—	ns	
Column address setup time	t_{ASC}	0	—	0	—	0	—	ns	
Column address hold time	t_{CAH}	12	—	15	—	15	—	ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	20	50	20	60	20	75	ns	2
$\overline{RAS}$ hold time referenced to $\overline{CAS}$	t_{RSH}	20	—	20	—	25	—	ns	

Common Parameter (cont)

		HM538253							
		-7		-8		-10			
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**	**Notes**
$\overline{CAS}$ hold time referenced to $\overline{RAS}$	t_{CSH}	70	—	80	—	100	—	ns	
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	10	—	10	—	10	—	ns	
Transition time (rise to fall)	t_T	3	50	3	50	3	50	ns	3
Refresh period	t_{REF}	—	8	—	8	—	8	ms	
$\overline{DT}$ to $\overline{RAS}$ setup time	t_{DTS}	0	—	0	—	0	—	ns	
$\overline{DT}$ to $\overline{RAS}$ hold time	t_{DTH}	10	—	10	—	10	—	ns	
DSF1 to $\overline{RAS}$ setup time	t_{FSR}	0	—	0	—	0	—	ns	
DSF1 to $\overline{RAS}$ hold time	t_{RFH}	10	—	10	—	10	—	ns	
DSF1 to $\overline{CAS}$ setup time	t_{FSC}	0	—	0	—	0	—	ns	
DSF1 to $\overline{CAS}$ hold time	t_{CFH}	12	—	15	—	15	—	ns	
Data-in to $\overline{CAS}$ delay time	t_{DZC}	0	—	0	—	0	—	ns	4
Data-in to $\overline{OE}$ delay time	t_{DZO}	0	—	0	—	0	—	ns	4
Output buffer turn-off delay referenced to $\overline{CAS}$	t_{OFF1}	—	20	—	20	—	20	ns	5
Output buffer turn-off delay referenced to $\overline{OE}$	t_{OFF2}	—	15	—	20	—	20	ns	5

Read Cycle (RAM), Page Mode Read Cycle

		HM538253							
		-7		-8		-10			
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Unit	Notes
Access time from $\overline{RAS}$	t_{RAC}	—	70	—	80	—	100	ns	6, 7
Access time from $\overline{CAS}$	t_{CAC}	—	20	—	20	—	25	ns	7, 8
Access time from $\overline{OE}$	t_{OAC}	—	20	—	20	—	25	ns	7
Address access time	t_{AA}	—	35	—	40	—	45	ns	7, 9
Read command setup time	t_{RCS}	0	—	0	—	0	—	ns	
Read command hold time	t_{RCH}	0	—	0	—	0	—	ns	10
Read command hold time referenced to $\overline{RAS}$	t_{RRH}	10	—	10	—	10	—	ns	10
$\overline{RAS}$ to column address delay time	t_{RAD}	15	35	15	40	15	55	ns	2
Column address to $\overline{RAS}$ lead time	t_{RAL}	35	—	40	—	45	—	ns	
Column address to $\overline{CAS}$ lead time	t_{CAL}	35	—	40	—	45	—	ns	
Page mode cycle time	t_{PC}	45	—	50	—	55	—	ns	
$\overline{CAS}$ precharge time	t_{CP}	7	—	10	—	10	—	ns	
Access time from $\overline{CAS}$ precharge	t_{ACP}	—	40	—	45	—	50	ns	
Page mode $\overline{RAS}$ pulse width	t_{RASP}	70	100000	80	100000	100	100000	ns	

Write Cycle (RAM), Page Mode Write Cycle, Color Register Set Cycle

		HM538253							
		-7		-8		-10			
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Unit	Notes
Write command setup time	t_{WCS}	0	—	0	—	0	—	ns	11
Write command hold time	t_{WCH}	12	—	15	—	15	—	ns	
Write command pulse width	t_{WP}	15	—	15	—	15	—	ns	
Write command to $\overline{RAS}$ lead time	t_{RWL}	20	—	20	—	20	—	ns	
Write command to $\overline{CAS}$ lead time	t_{CWL}	20	—	20	—	20	—	ns	
Data-in setup time	t_{DS}	0	—	0	—	0	—	ns	12
Data-in hold time	t_{DH}	12	—	15	—	15	—	ns	12
$\overline{WE}$ to $\overline{RAS}$ setup time	t_{WS}	0	—	0	—	0	—	ns	
$\overline{WE}$ to $\overline{RAS}$ hold time	t_{WH}	10	—	10	—	10	—	ns	
Mask data to $\overline{RAS}$ setup time	t_{MS}	0	—	0	—	0	—	ns	
Mask data to $\overline{RAS}$ hold time	t_{MH}	10	—	10	—	10	—	ns	
$\overline{OE}$ hold time referenced to $\overline{WE}$	t_{OEH}	15	—	20	—	20	—	ns	
Page mode cycle time	t_{PC}	45	—	50	—	55	—	ns	
$\overline{CAS}$ precharge time	t_{CP}	7	—	10	—	10	—	ns	
$\overline{CAS}$ to data-in delay time	t_{CDD}	20	—	20	—	20	—	ns	13
Page mode $\overline{RAS}$ pulse width	t_{RASP}	70	100000	80	100000	100	100000	ns	

Read-Modify-Write Cycle

		HM538253							
		-7		-8		-10			
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Unit	Notes
Read-modify-write cycle time	t_{RWC}	180	—	200	—	230	—	ns	
$\overline{RAS}$ pulse width (read-modify-write cycle)	t_{RWS}	120	10000	130	10000	150	10000	ns	
$\overline{CAS}$ to $\overline{WE}$ delay time	t_{CWD}	45	—	45	—	50	—	ns	14
Column address to $\overline{WE}$ delay time	t_{AWD}	60	—	65	—	70	—	ns	14
$\overline{OE}$ to data-in delay time	t_{ODD}	20	—	20	—	20	—	ns	12
Access time from $\overline{RAS}$	t_{RAC}	—	70	—	80	—	100	ns	6, 7
Access time from $\overline{CAS}$	t_{CAC}	—	20	—	20	—	25	ns	7, 8
Access time from $\overline{OE}$	t_{OAC}	—	20	—	20	—	25	ns	7
Address access time	t_{AA}	—	35	—	40	—	45	ns	7, 9
$\overline{RAS}$ to column address delay time	t_{RAD}	15	35	15	40	15	55	ns	
Read command setup time	t_{RCS}	0	—	0	—	0	—	ns	
Write command to $\overline{RAS}$ lead time	t_{RWL}	20	—	20	—	20	—	ns	
Write command to $\overline{CAS}$ lead time	t_{CWL}	20	—	20	—	20	—	ns	
Write command pulse width	t_{WP}	15	—	15	—	15	—	ns	
Data-in setup time	t_{DS}	0	—	0	—	0	—	ns	12
Data-in hold time	t_{DH}	12	—	15	—	15	—	ns	12
$\overline{OE}$ hold time referenced to $\overline{WE}$	t_{OEH}	15	—	20	—	20	—	ns	

Refresh Cycle

		HM538253							
		-7		-8		-10			
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Unit	Notes
$\overline{CAS}$ setup time ($\overline{CAS}$-before-$\overline{RAS}$ refresh)	t_{CSR}	10	—	10	—	10	—	ns	
$\overline{CAS}$ hold time ($\overline{CAS}$-before-$\overline{RAS}$ refresh)	t_{CHR}	10	—	10	—	10	—	ns	
$\overline{RAS}$ precharge to $\overline{CAS}$ hold time	t_{RPC}	10	—	10	—	10	—	ns	

Flash Write Cycle, Block Write Cycle, and Register Read Cycle

		HM538253							
		-7		-8		-10			
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Unit	Notes
$\overline{CAS}$ to data-in delay time	t_{CDD}	20	—	20	—	20	—	ns	13
$\overline{OE}$ to data-in delay time	t_{ODD}	15	—	20	—	20	—	ns	13

CBR Refresh with Register Reset

		HM538253							
		-7		-8		-10			
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Uni	Notes
Split transfer setup time	t_{STS}	20	—	20	—	25	—	ns	
Split transfer hold time referenced to $\overline{RAS}$	t_{RST}	70	—	80	—	100	—	ns	

Read Transfer Cycle

Parameter	Symbol	HM538253 -7 Min	-7 Max	-8 Min	-8 Max	-10 Min	-10 Max	Unit	Notes
$\overline{DT}$ hold time referenced to $\overline{RAS}$	t_{RDH}	60	10000	65	10000	80	10000	ns	
$\overline{DT}$ hold time referenced to $\overline{CAS}$	t_{CDH}	20	—	20	—	25	—	ns	
$\overline{DT}$ hold time referenced to column address	t_{ADH}	25	—	30	—	30	—	ns	
$\overline{DT}$ precharge time	t_{DTP}	20	—	20	—	30	—	ns	
$\overline{DT}$ to $\overline{RAS}$ delay time	t_{DRD}	60	—	70	—	80	—	ns	
SC to $\overline{RAS}$ setup time	t_{SRS}	25	—	30	—	30	—	ns	
1st SC to $\overline{RAS}$ hold time	t_{SRH}	70	—	80	—	100	—	ns	
1st SC to $\overline{CAS}$ hold time	t_{SCH}	25	—	25	—	25	—	ns	
1st SC to column address hold time	t_{SAH}	40	—	45	—	50	—	ns	
Last SC to $\overline{DT}$ delay time	t_{SDD}	5	—	5	—	5	—	ns	
1st SC to $\overline{DT}$ hold time	t_{SDH}	10	—	15	—	15	—	ns	
$\overline{DT}$ to QSF delay time	t_{DQD}	—	30	—	35	—	35	ns	15
QSF hold time referenced to $\overline{DT}$	t_{DQH}	5	—	5	—	5	—	ns	
Serial data-in to 1st SC delay time	t_{SZS}	0	—	0	—	0	—	ns	
Serial clock cycle time	t_{SCC}	25	—	30	—	30	—	ns	
SC pulse width	t_{SC}	5	—	10	—	10	—	ns	
SC precharge time	t_{SCP}	10	—	10	—	10	—	ns	
SC access time	t_{SCA}	—	22	—	25	—	25	ns	15
Serial data-out hold time	t_{SOH}	5	—	5	—	5	—	ns	
Serial data-in setup time	t_{SIS}	0	—	0	—	0	—	ns	
Serial data-in hold time	t_{SIH}	15	—	15	—	15	—	ns	
$\overline{RAS}$ to column address delay time	t_{RAD}	15	35	15	40	15	55	ns	
Column address to $\overline{RAS}$ lead time	t_{RAL}	35	—	40	—	45	—	ns	

Read Transfer Cycle (cont)

		HM538253							
		-7		-8		-10			
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Unit	Notes
$\overline{RAS}$ to QSF delay time	t_{RQD}	—	70	—	75	—	85	ns	15
$\overline{CAS}$ to QSF delay time	t_{CQD}	—	35	—	35	—	35	ns	15
QSF hold time referenced to $\overline{RAS}$	t_{RQH}	20	—	20	—	25	—	ns	
QSF hold time referenced to $\overline{CAS}$	t_{CQH}	5	—	5	—	5	—	ns	

Masked Write Transfer Cycle

		HM538253							
		-7		-8		-10			
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Unit	Notes
SC setup time referenced to $\overline{RAS}$	t_{SRS}	25	—	30	—	30	—	ns	
$\overline{RAS}$ to SC delay time	t_{SRD}	20	—	25	—	25	—	ns	
Serial output buffer turn-off time referenced to $\overline{RAS}$	t_{SRZ}	10	40	10	45	10	50	ns	
$\overline{RAS}$ to serial data-in delay time	t_{SID}	40	—	45	—	50	—	ns	
$\overline{RAS}$ to QSF delay time	t_{RQD}	—	70	—	75	—	85	ns	15
$\overline{CAS}$ to QSF delay time	t_{CQD}	—	35	—	35	—	35	ns	15
QSF hold time referenced to $\overline{RAS}$	t_{RQH}	20	—	20	—	25	—	ns	
QSF hold time referenced to $\overline{CAS}$	t_{CQH}	5	—	5	—	5	—	ns	
Serial clock cycle time	t_{SCC}	25	—	30	—	30	—	ns	
SC pulse width	t_{SC}	5	—	10	—	10	—	ns	
SC precharge time	t_{SCP}	10	—	10	—	10	—	ns	
SC access time	t_{SCA}	—	22	—	25	—	25	ns	15
Serial data-out hold time	t_{SOH}	5	—	5	—	5	—	ns	
Serial data-in setup time	t_{SIS}	0	—	0	—	0	—	ns	
Serial data-in hold time	t_{SIH}	15	—	15	—	15	—	ns	

Split Read Transfer Cycle, Masked Split Write Transfer Cycle

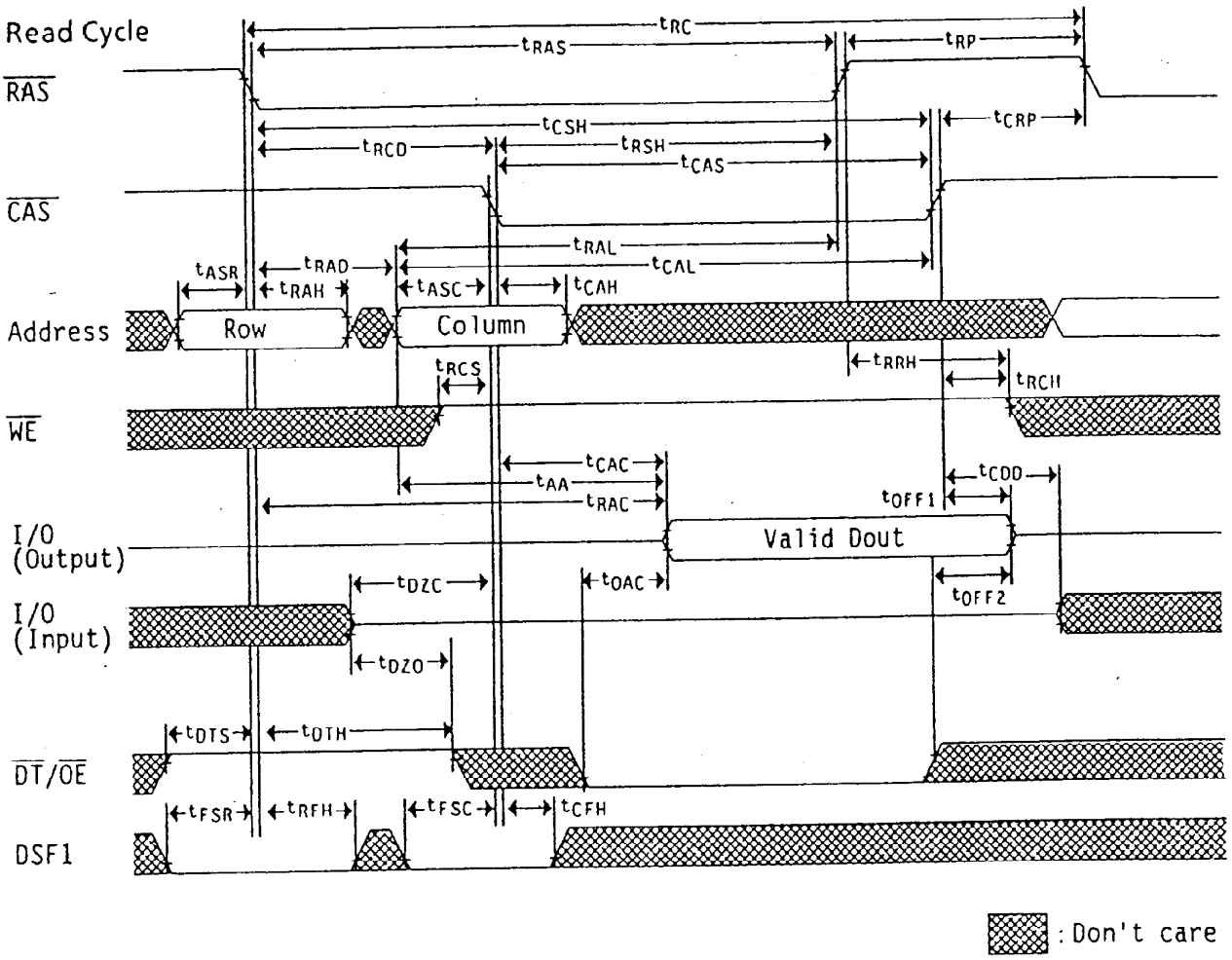
		HM538253							
		-7		-8		-10			
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Unit	Notes
Split transfer setup time	t_{STS}	20	—	20	—	25	—	ns	
Split transfer hold time referenced to $\overline{RAS}$	t_{RST}	70	—	80	—	100	—	ns	
Split transfer hold time referenced to $\overline{CAS}$	t_{CST}	20	—	20	—	25	—	ns	
Split transfer hold time referenced to column address	t_{AST}	35	—	40	—	45	—	ns	
SC to QSF delay time	t_{SQD}	—	30	—	30	—	30	ns	15
QSF hold time referenced to SC	t_{SQH}	5	—	5	—	5	—	ns	
Serial clock cycle time	t_{SCC}	25	—	30	—	30	—	ns	
SC pulse width	t_{SC}	5	—	10	—	10	—	ns	
SC precharge time	t_{SCP}	10	—	10	—	10	—	ns	
SC access time	t_{SCA}	—	22	—	25	—	25	ns	15
Serial data-out hold time	t_{SOH}	5	—	5	—	5	—	ns	
Serial data-in setup time	t_{SIS}	0	—	0	—	0	—	ns	
Serial data-in hold time	t_{SIH}	15	—	15	—	15	—	ns	
$\overline{RAS}$ to column address delay time	t_{RAD}	15	35	15	40	15	55	ns	
Column address to $\overline{RAS}$ lead time	t_{RAL}	35	—	40	—	45	—	ns	

Serial Read Cycle, Serial Write Cycle

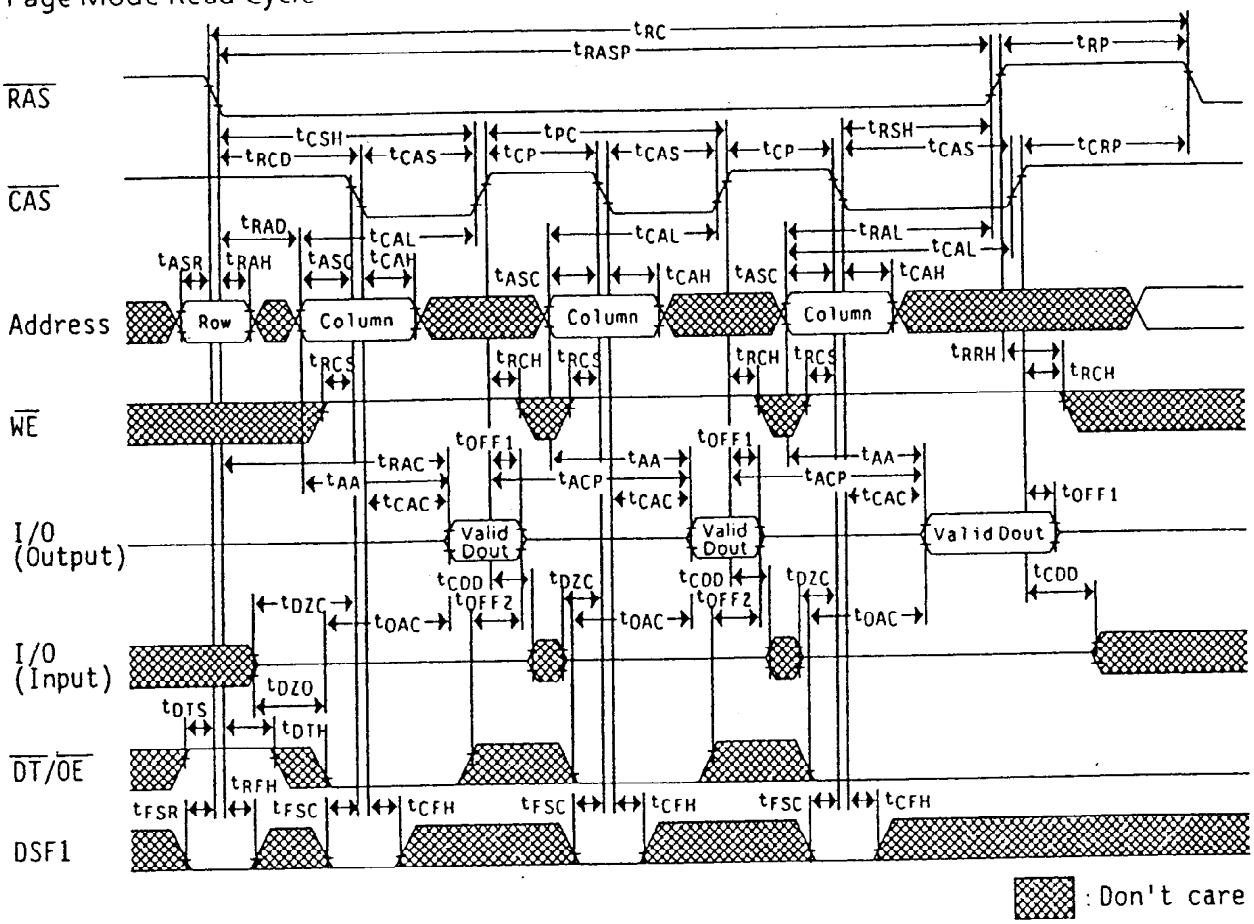
		HM538253							
		-7		-8		-10			
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Unit	Notes
Serial clock cycle time	t_{SCC}	25	—	30	—	30	—	ns	
SC pulse width	t_{SC}	5	—	10	—	10	—	ns	
SC precharge width	t_{SCP}	10	—	10	—	10	—	ns	
Access time from SC	t_{SCA}	—	22	—	25	—	25	ns	15
Access time from $\overline{SE}$	t_{SEA}	—	20	—	25	—	25	ns	15
Serial data-out hold time	t_{SOH}	5	—	5	—	5	—	ns	
Serial output buffer turn-off time referenced to $\overline{SE}$	t_{SHZ}	—	15	—	20	—	20	ns	5,17
$\overline{SE}$ to serial output in low-Z	t_{SLZ}	0	—	0	—	0	—	ns	5,17
Serial data-in setup time	t_{SIS}	0	—	0	—	0	—	ns	
Serial data-in hold time	t_{SIH}	15	—	15	—	15	—	ns	
Serial write enable setup time	t_{SWS}	0	—	0	—	0	—	ns	
Serial wrtie enbable hold time	t_{SWH}	15	—	15	—	15	—	ns	
Serial write disable setup time	t_{SWIS}	0	—	0	—	0	—	ns	
Serial write disable hold time	t_{SWIH}	15	—	15	—	15	—	ns	

Notes:
1. AC measurements assume t_T = 5 ns.
2. When $t_{RCD} > t_{RCD}$ (max) and $t_{RAD} > t_{RAD}$ (max), access time is specified by t_{CAC} or t_{AA}.
3. V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Transition time t_T is measured between V_{IH} and V_{IL}.
4. Data input must be floating before output buffer is turned on. In read cycle, read-modify-write cycle and delayed write cycle, either t_{DZC} (min) or t_{DZO} (min) must be satisfied.
5. t_{OFF1} (max), t_{OFF2} (max), t_{SHZ} (max) and t_{SLZ} (min) are defined as the time at which the output acheives the open circuit condition (V_{OH} – 100 mV, V_{OL} + 100 mV). This parameter is sampled and not 100% tested.
6. Assume that $t_{RCD} \leq t_{RCD}$ (max) and $t_{RAD} \leq t_{RAD}$ (max). If t_{RCD} or t_{RAD} is greater than the maximum recommended value shown in this table, t_{RAC} exceeds the value shown.
7. Measured with a load circuit equivalent to 1 TTL loads and 50 pF.
8. When $t_{RCD} \geq t_{RCD}$ (max) and $t_{RAD} \leq t_{RAD}$ (max), access time is specified by t_{CAC}.
9. When $t_{RCD} \leq t_{RCD}$ (max) and $t_{RAD} \geq t_{RAD}$ (max), access time is specified by t_{AA}.
10. If either t_{RCH} or t_{RRH} is satisfied, operation is guaranteed.
11. When $t_{WCS} \geq t_{WCS}$ (min), the cycle is an early write cycle, and I/O pins remain in an open circuit (high impedance) condition.
12. These parameters are specified by the later falling edge of $\overline{CAS}$ or $\overline{WE}$.
13. Either t_{CDD} (min) or t_{ODD} (min) must be satisfied because output buffer must be turned off by $\overline{CAS}$ or $\overline{OE}$ prior to applying data to the device when output buffer is on.
14. When $t_{AWD} \geq t_{AWD}$ (min) and $t_{CWD} \geq t_{CWD}$ (min) in read-modify-write cycle, the data of the selected address outputs to an I/O pin and input data is written into the selected address. t_{ODD} (min) must be satisfied because output buffer must be turned off by $\overline{OE}$ prior to applying data to the device.
15. Measured with a load circuit equivalent to 1 TTL loads and 30 pF.
16. After power-up, pause for 100 µs or more and execute at least 8 initialization cycle (normal memory cycle or refresh cycle), then start operation. Hitachi recommends that 8 initialization cycle is CBRR for internal register reset.
17. When t_{SHZ} and t_{SLZ} are measured in the same VCC and Ta condition and tr and tf of $\overline{SE}$ are less than 5 ns, $t_{SHZ} \leq t_{SLZ}$ + 5 ns.
18. After power-up, QSF output is High-Z, so 1SC cycle is needed to be Low-Z it.
19. DSF2 pin is open pin, but Hitachi recommends it is fixed low in all operation for the addition mode in future.

■ Timing Waveforms



Page Mode Read Cycle



Write Cycle

The write cycle state table as shown below is applied to early write, delayed write, page mode write, and read-modify write.

Write Cycle State Table

Menu	Cycle	$\overline{RAS}$	$\overline{CAS}$	$\overline{RAS}$	$\overline{RAS}$	$\overline{CAS}$
		DSF1	DSF1	$\overline{WE}$	I/O	I/O
		W1	W2	W3	W4	W5
RWM	Write mask (new/old) Write DQs to I/Os	0	0	0	Write mask*1	Valid data
BWM	Write mask (new/old) Block write	0	1	0	Write mask*2	Column mask*2
RW	Normal write (no mask)	0	0	1	Don't care*1	Valid data
BW	Block write (no mask)	0	1	1	Don't care*2	Column mask*2
LMR	Load write mask resister	1	0	1	Don't care	Write mask data*3
LCR	Load color resister	1	1	1	Don't care	Color data

Note 1

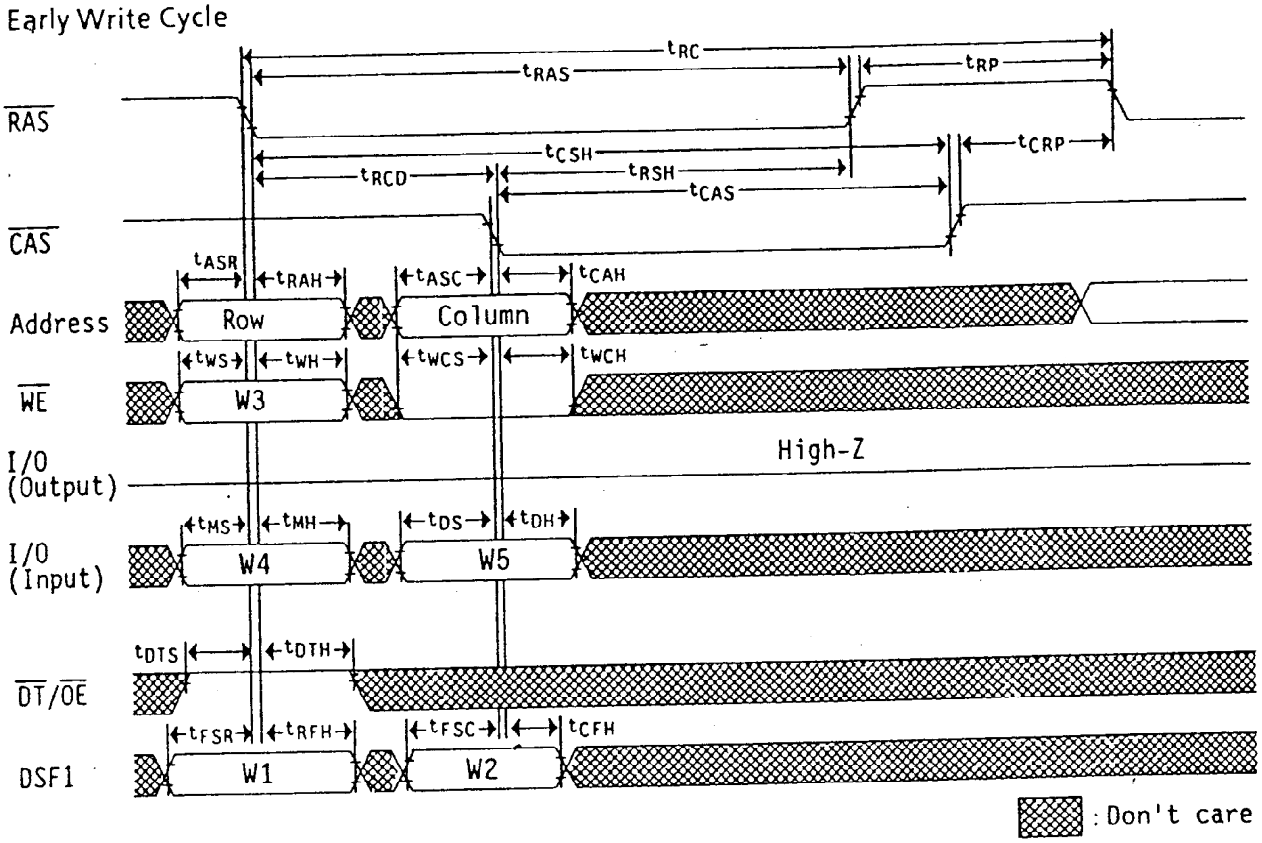
$\overline{WE}$	Mode	I/O data/$\overline{RAS}$
Low	New Mask Mode	Mask
	Persistent Mask Mode	Don't care (mask register used)
High	No mask	Don't care

I/O Mask Data (In new mask mode)
Low: Mask
High: Non Mask
In persistent mask mode, I/O don't care

Note 2: reference Figure 2 use of Block Write

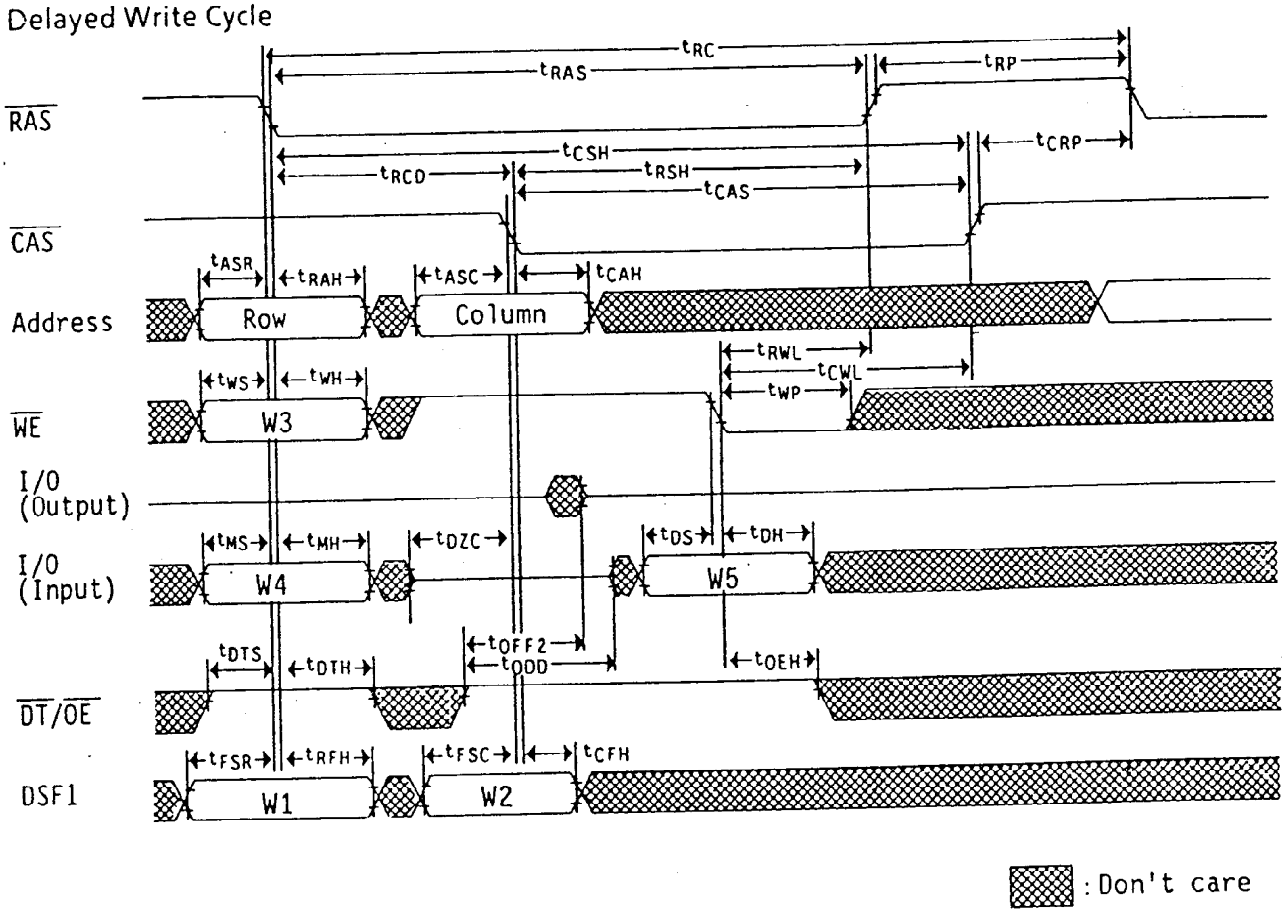
Note 3: I/O Write Mask Data
Low: Mask
High: Non mask

Early Write Cycle



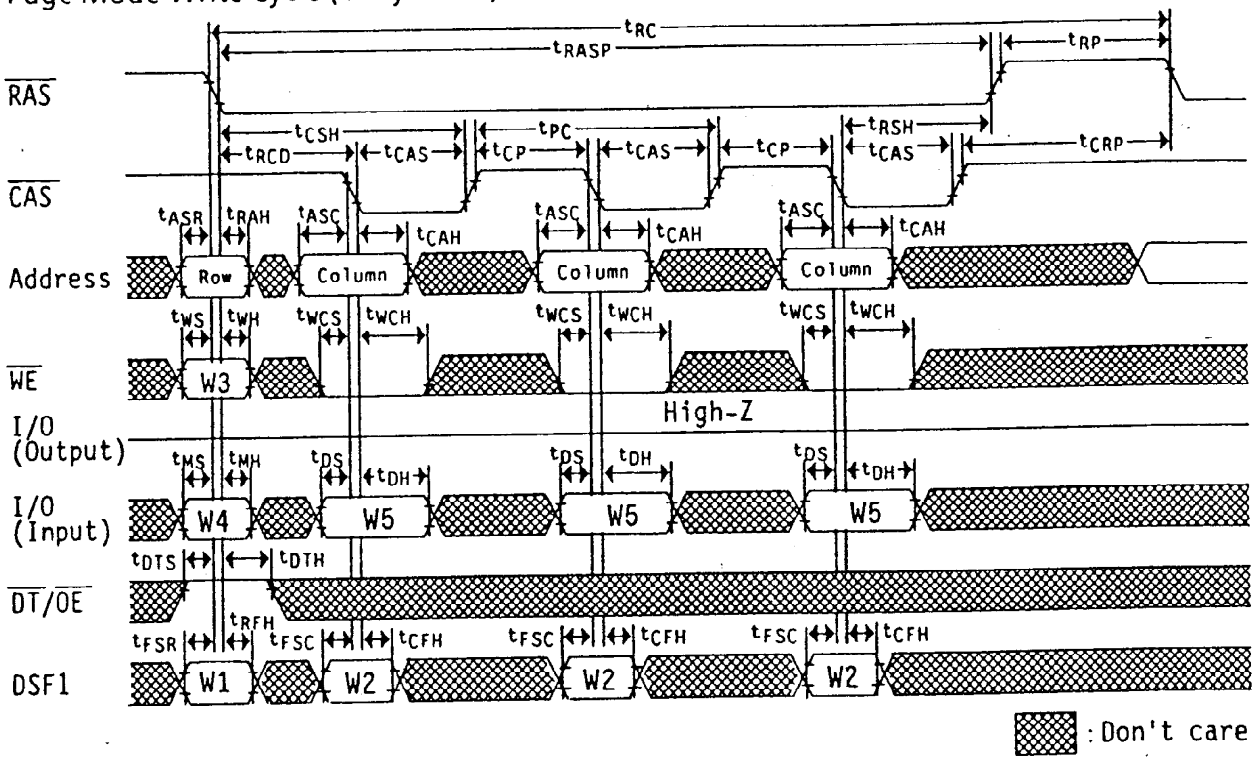
W1 to W5: See Write Cycle State Table for the logic states.

Delayed Write Cycle



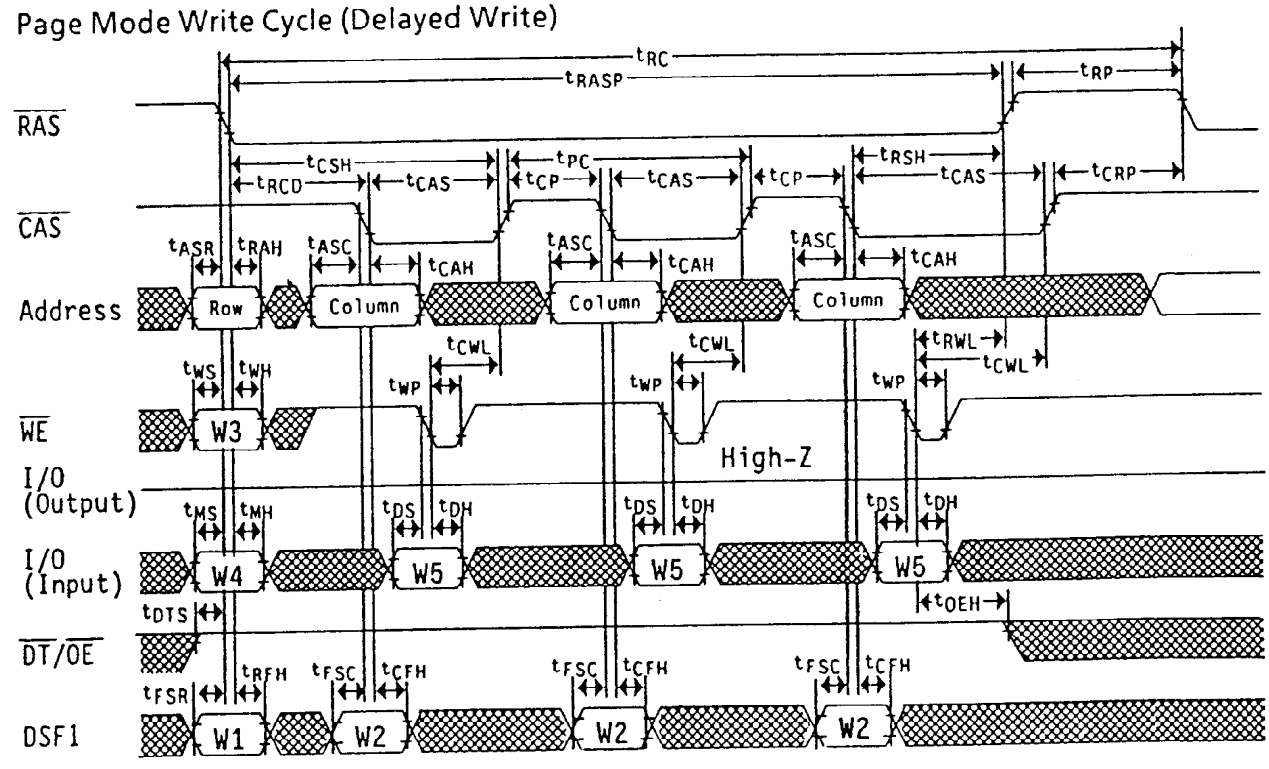
W1 to W5: See Write Cycle State Table for the logic states.

Page Mode Write Cycle (Early Write)



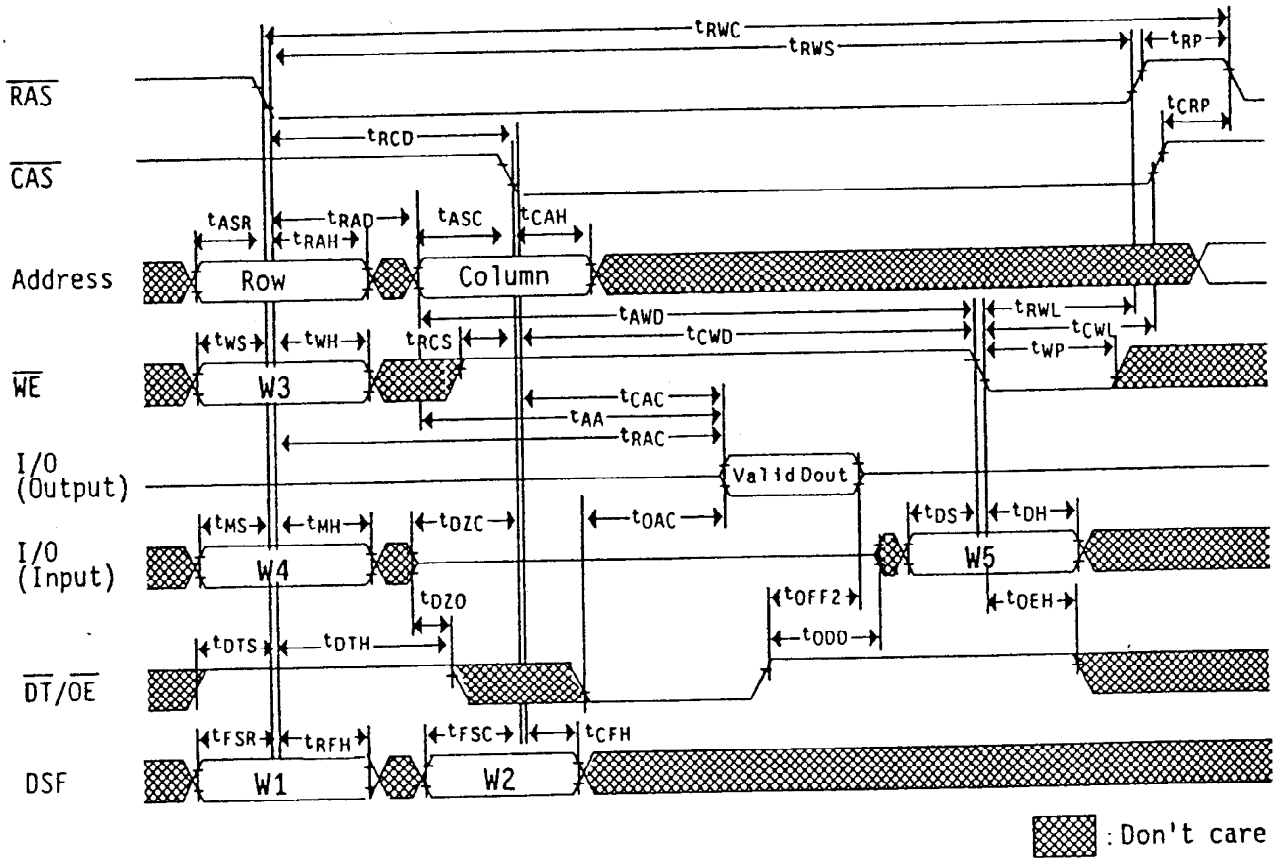
W1 to W5: See Write Cycle State Table for the logic states.

Page Mode Write Cycle (Delayed Write)



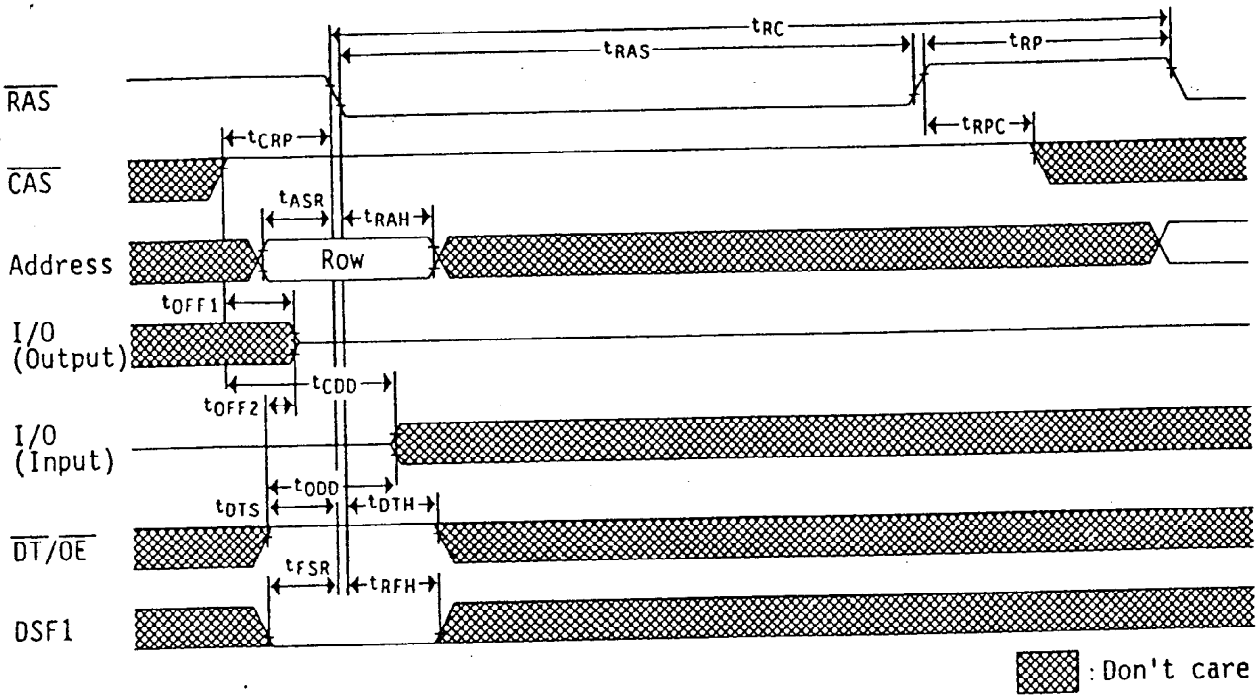
W1 to W5: See Write Cycle State Table for the locgic states.

Read- Modify-Write Cycle

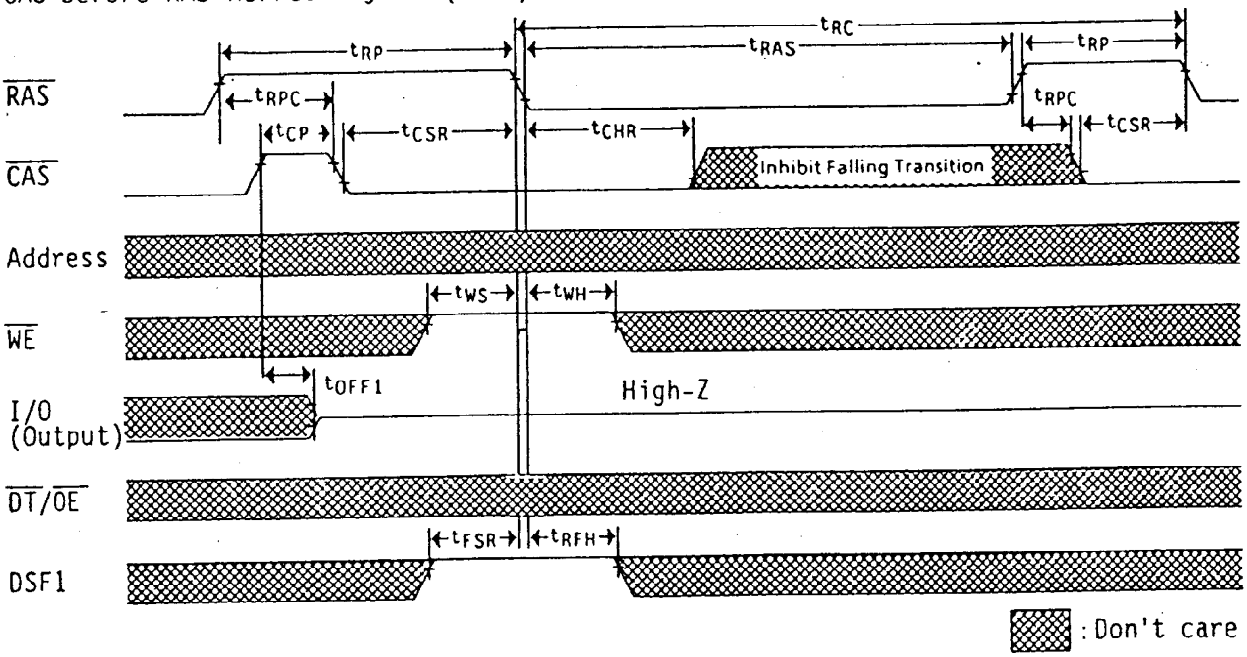


W1 to W5: See Write Cycle State Table for the logic states.

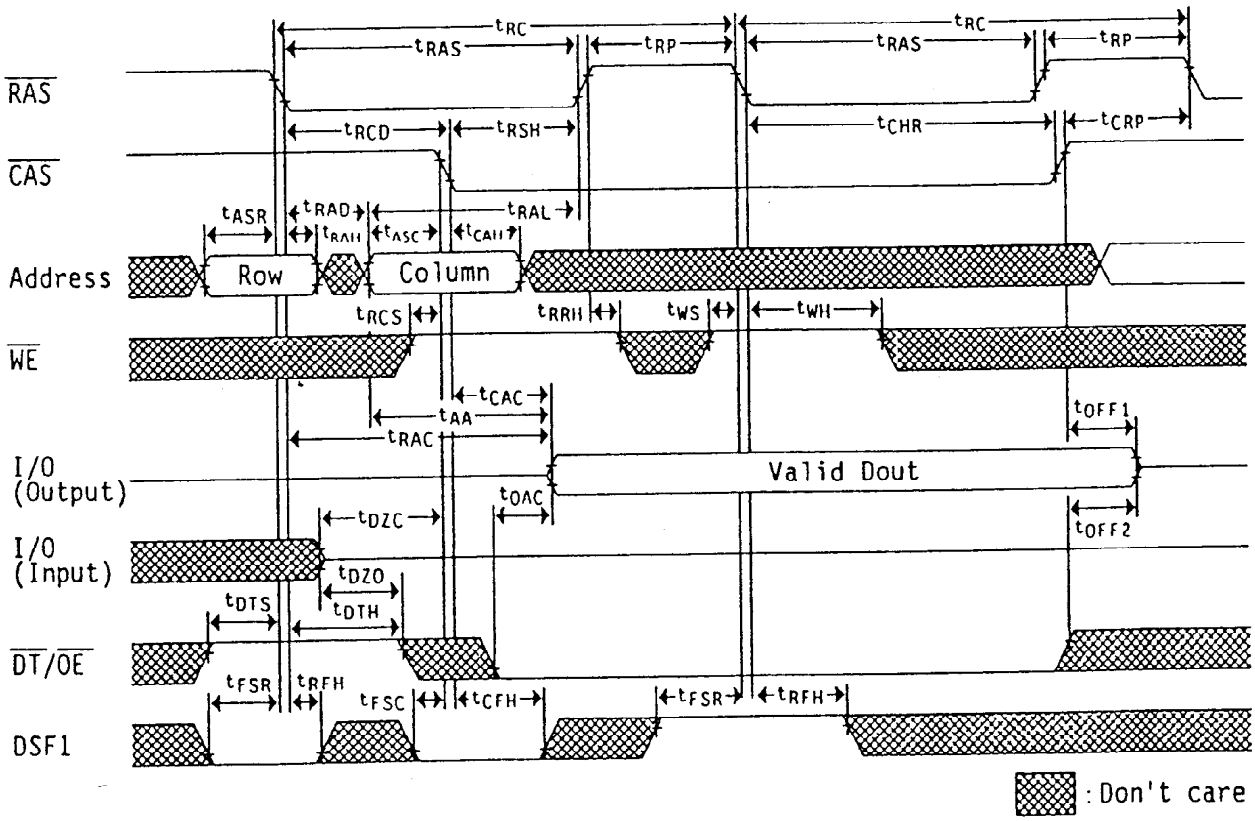
- $\overline{\text{RAS}}$-Only Refresh Cycle



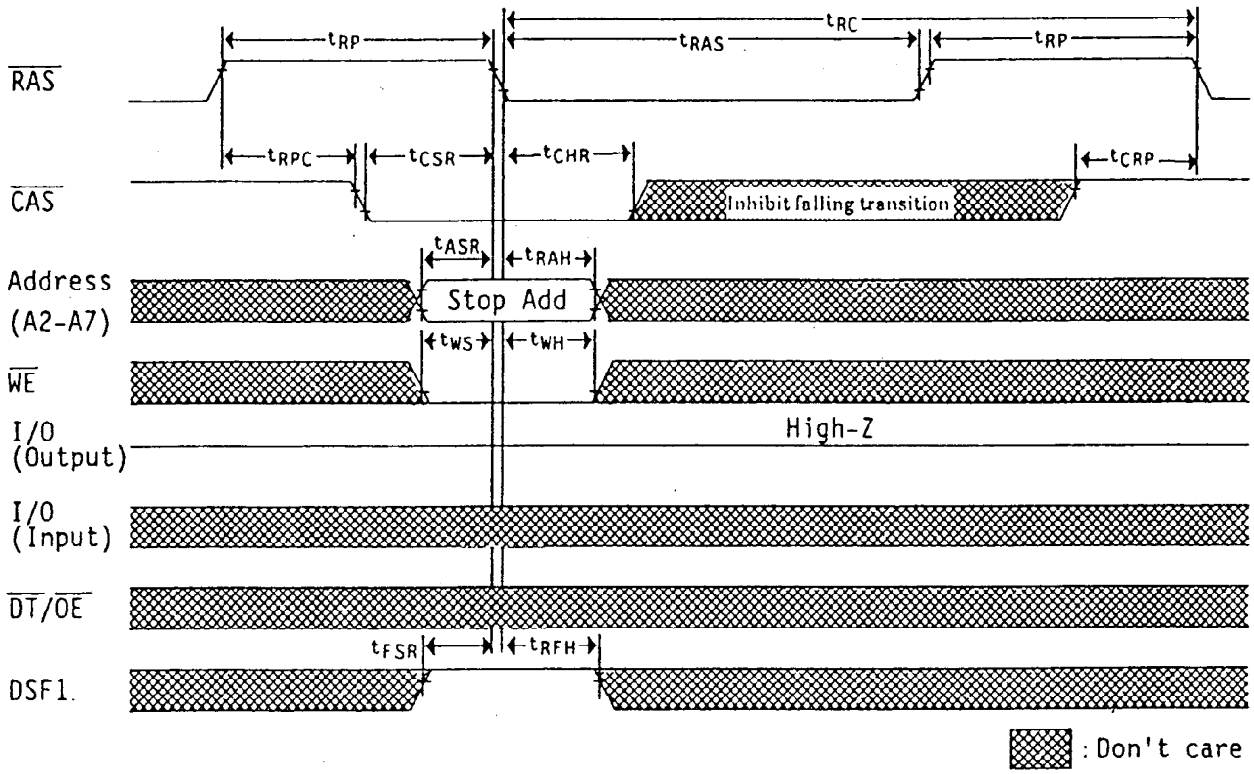
$\overline{CAS}$-Before-$\overline{RAS}$ Refresh Cycle (CBRN)



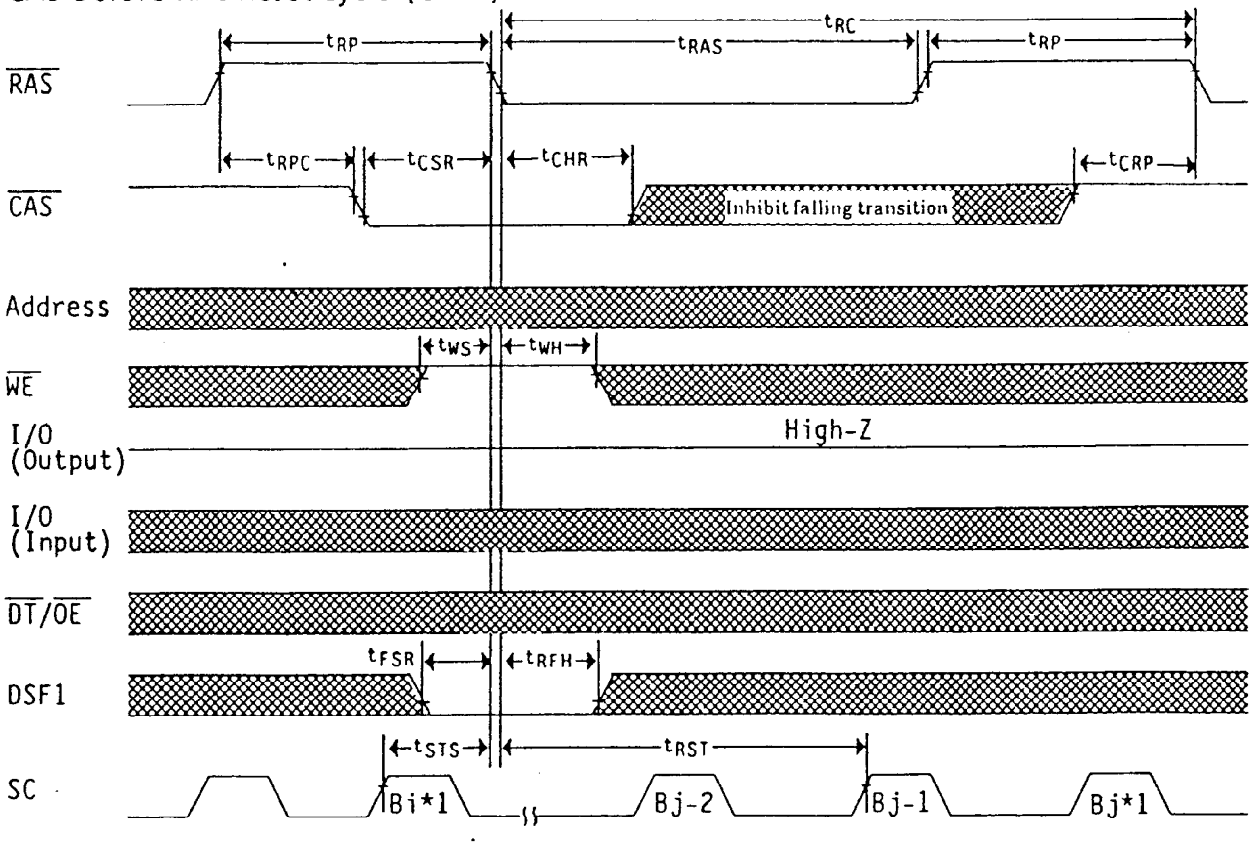
Hidden Refresh Cycle



$\overline{CAS}$-Before-$\overline{RAS}$ Set Cycle (CBRS)

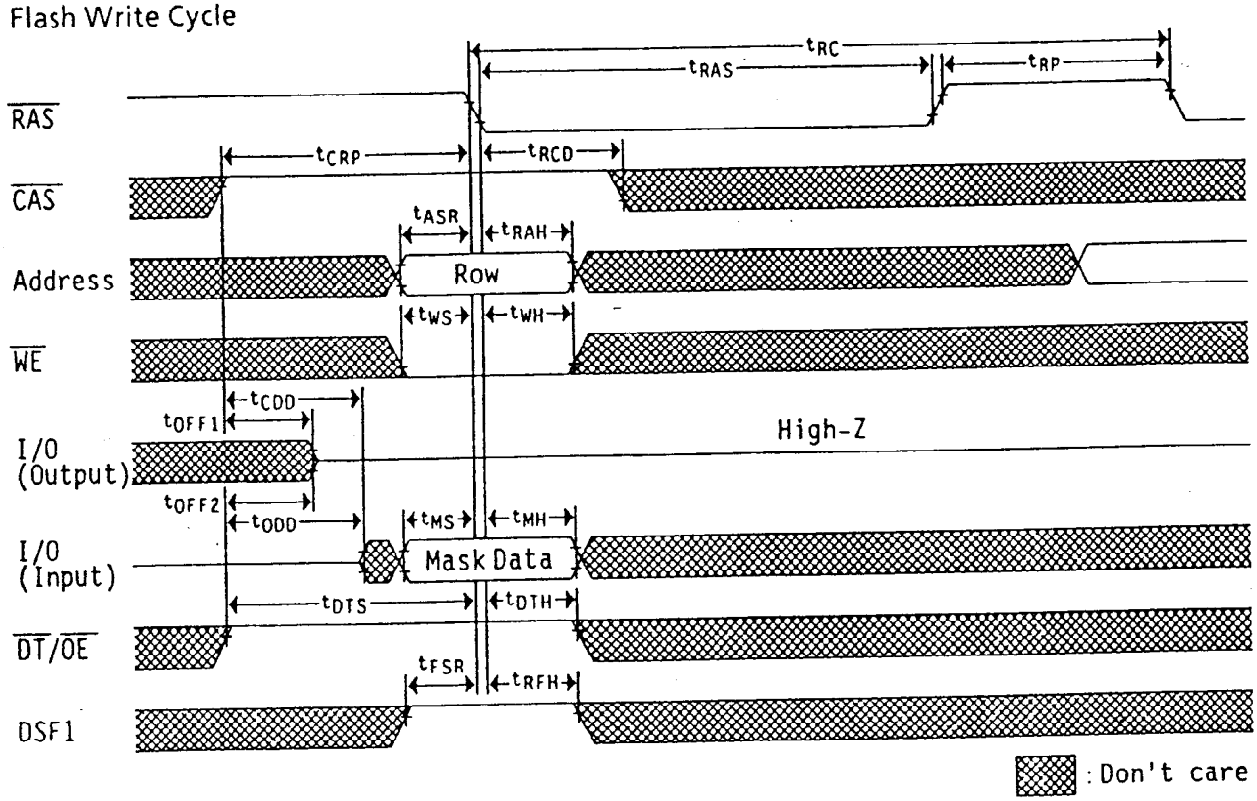


$\overline{CAS}$-Before-$\overline{RAS}$ Reset Cycle (CBRR)

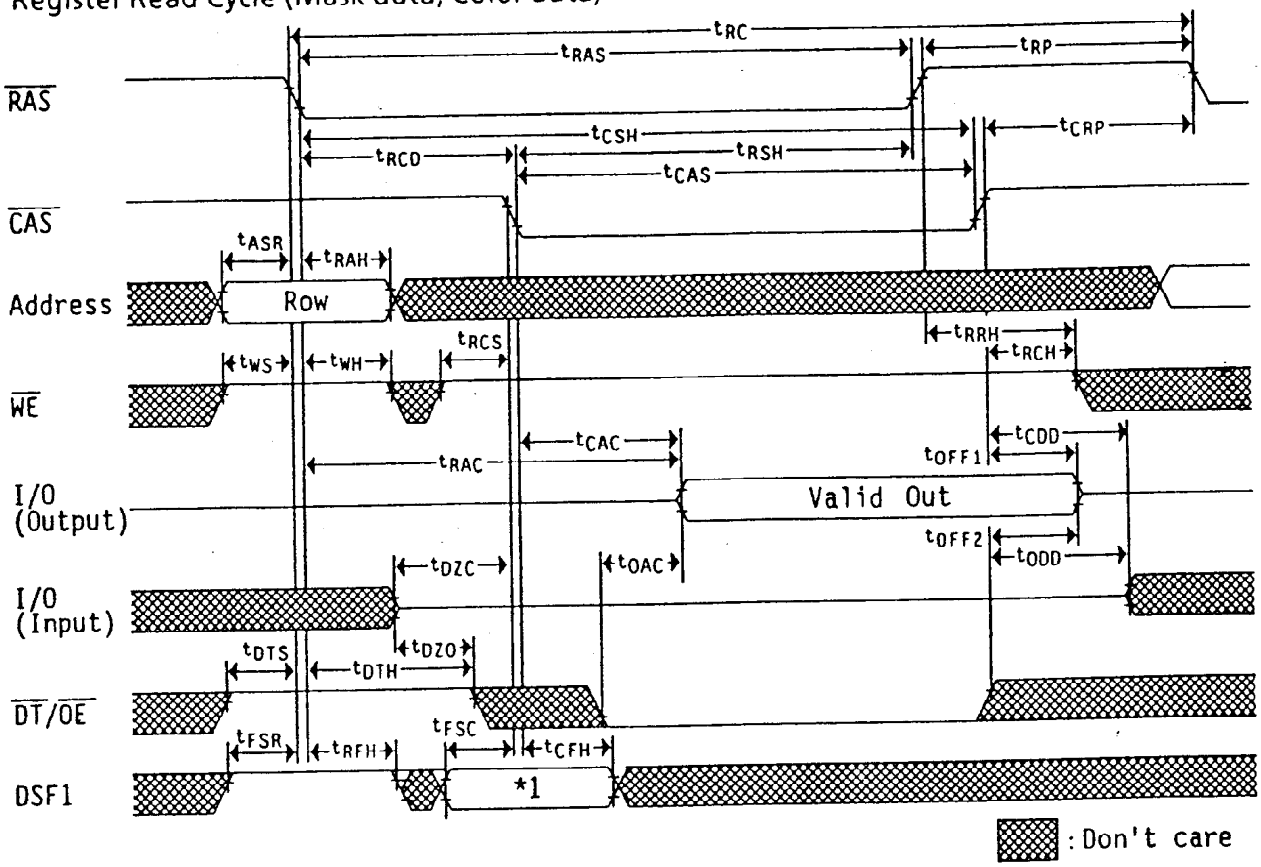


Note: 1. Bi, Bj initiate the boundary addresses.

Flash Write Cycle



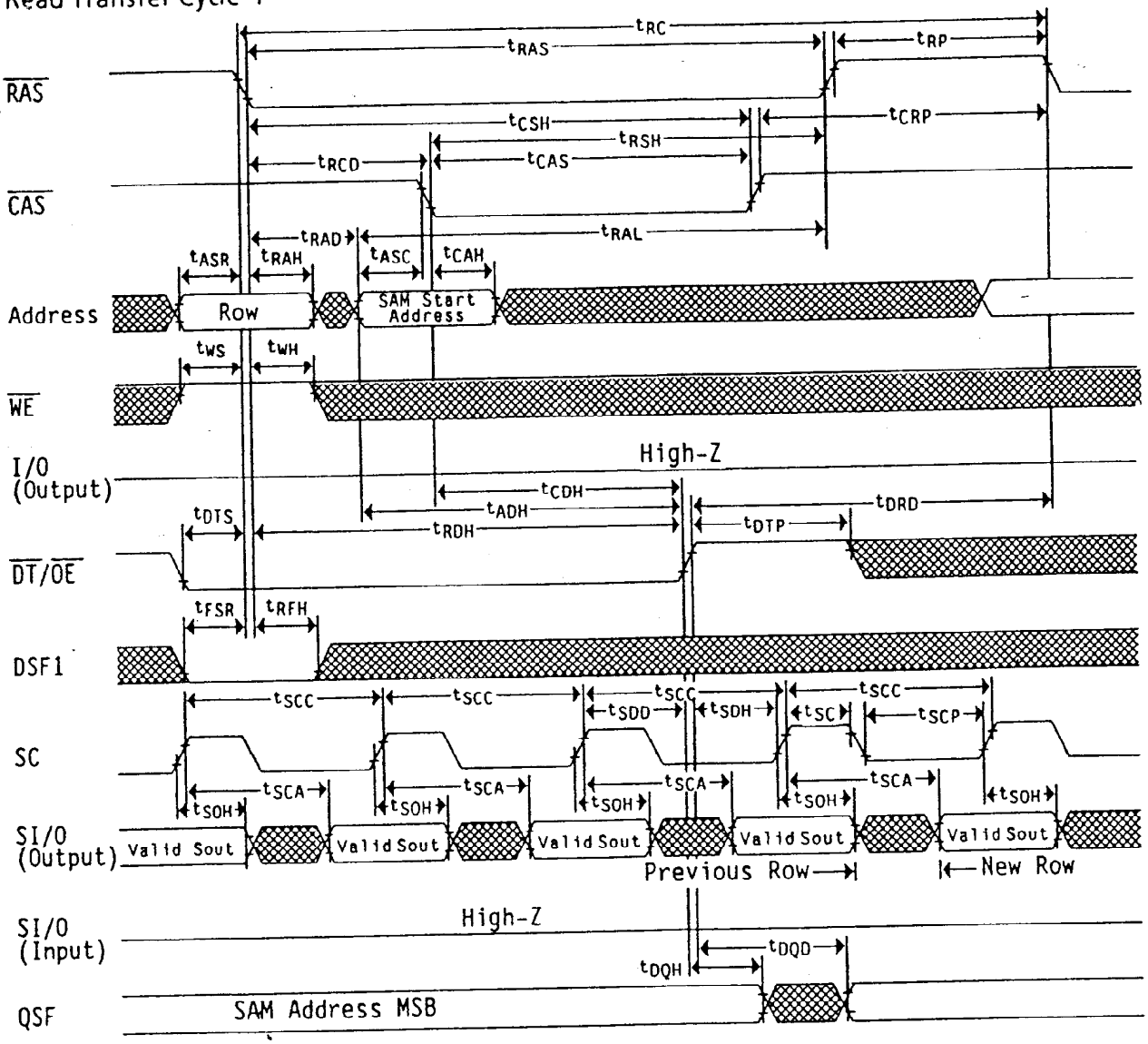
Register Read Cycle (Mask data, Color data)



Note: 1. State of DSF1 at falling edge of $\overline{CAS}$

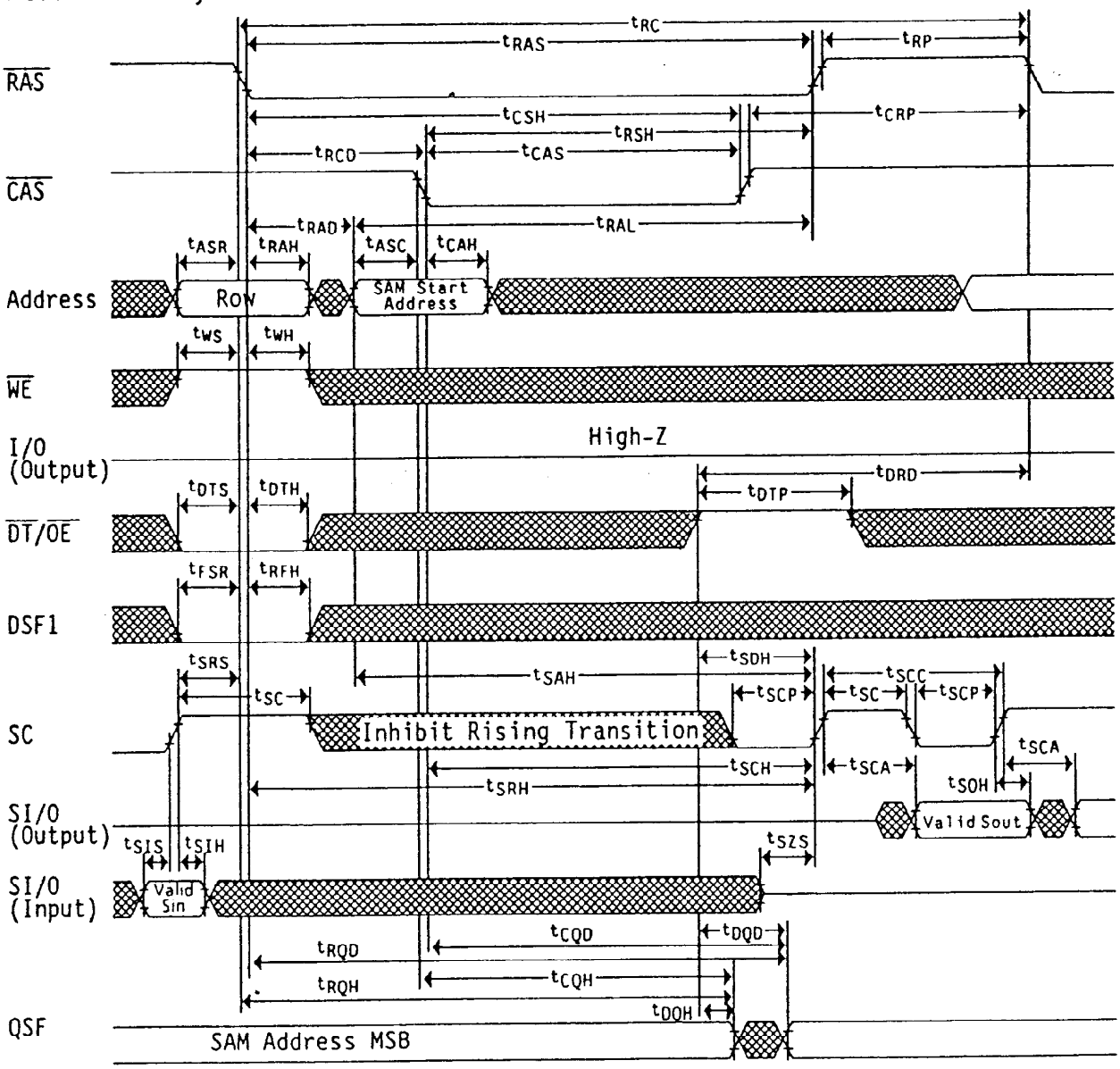
State	0	1
Accessed Data	Mask Data (LMR)	Color Data (LCR)

Read Transfer Cycle-1

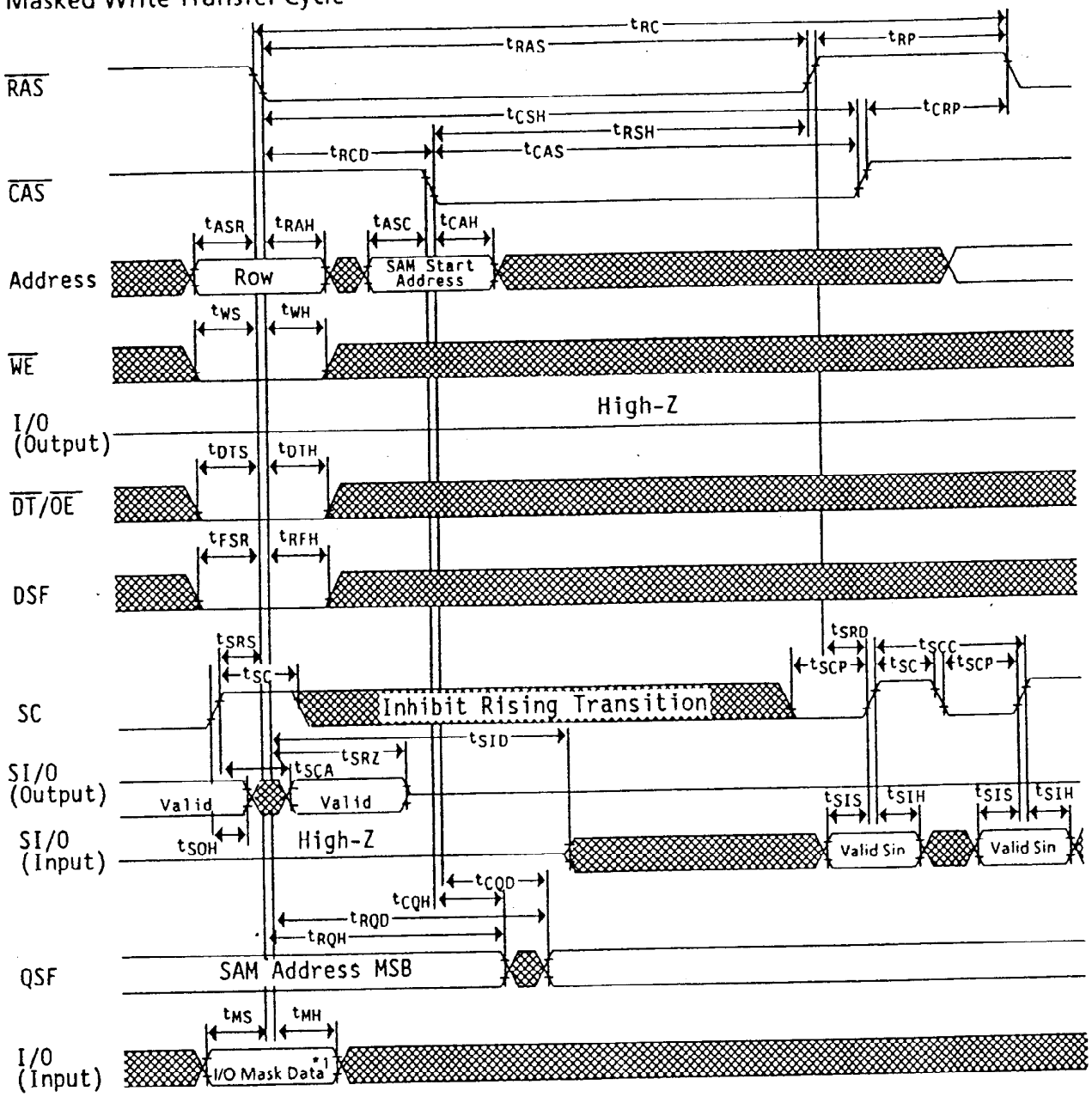


: Don't care

Read Transfer Cycle – 2



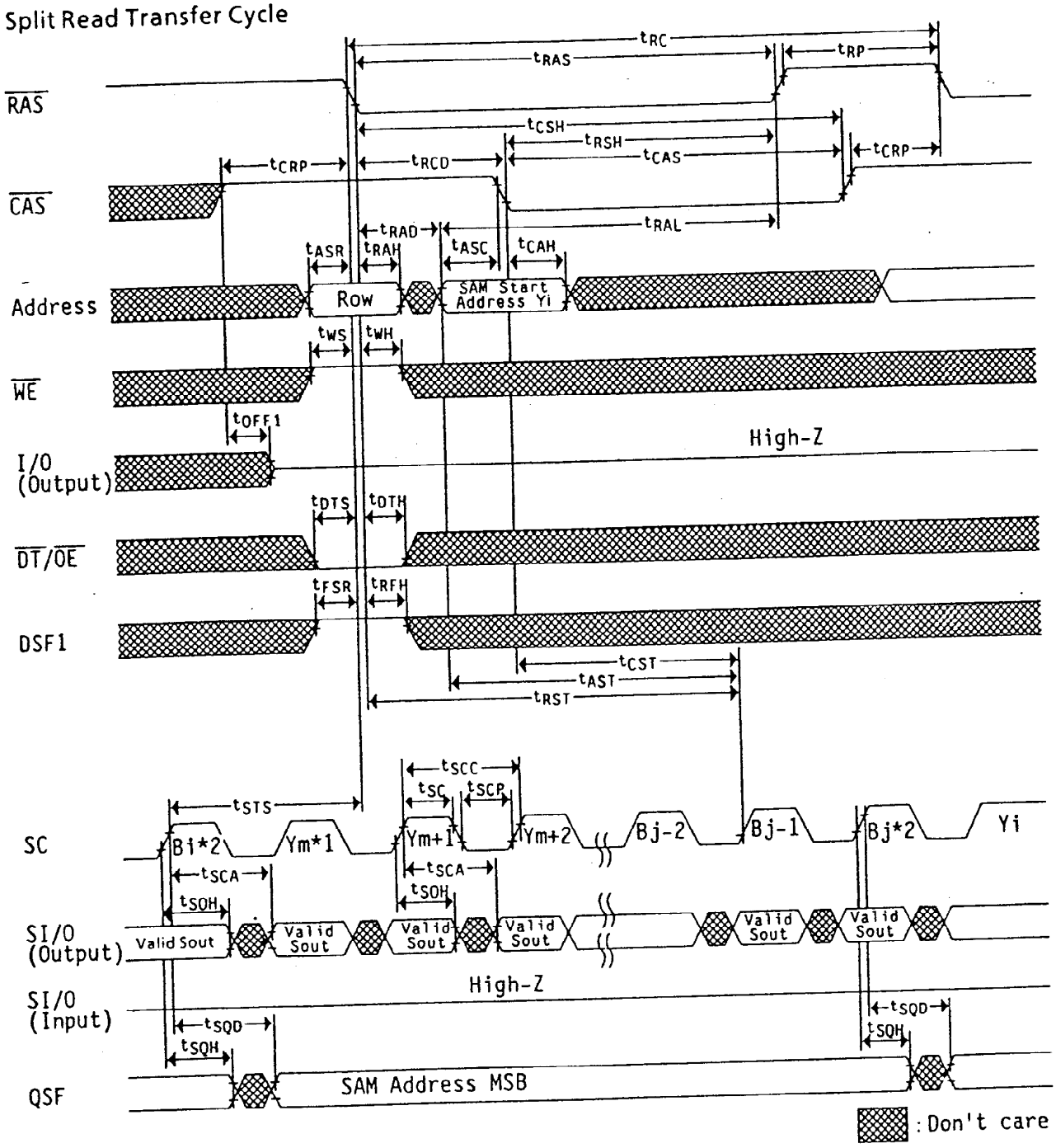
Masked Write Transfer Cycle



Note: 1. I/O Mask Data (In new mask mode)
Low : Mask
High : Non Mask
I/O : Don't care in persistent mask mode.

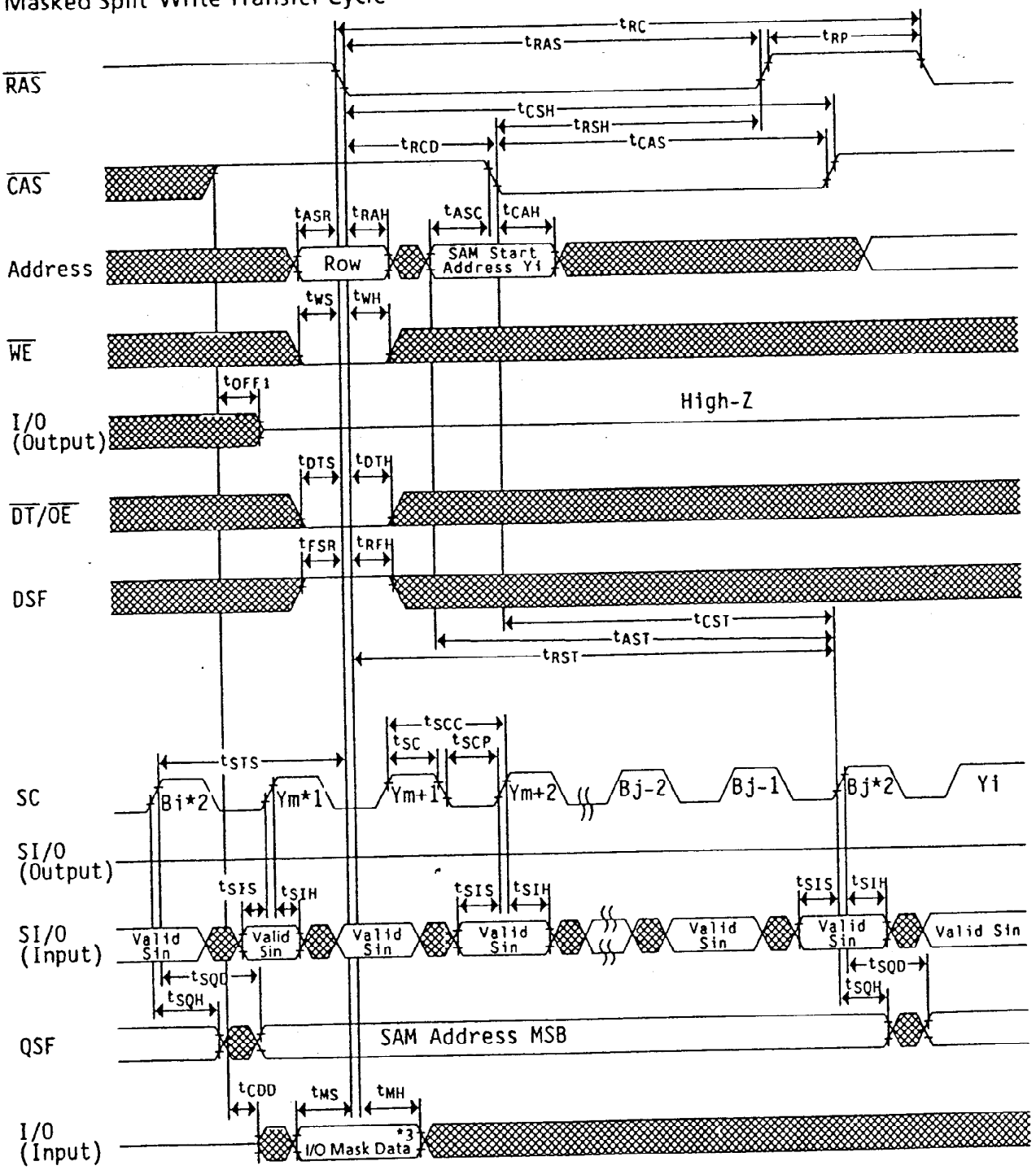
: Don't care

Split Read Transfer Cycle



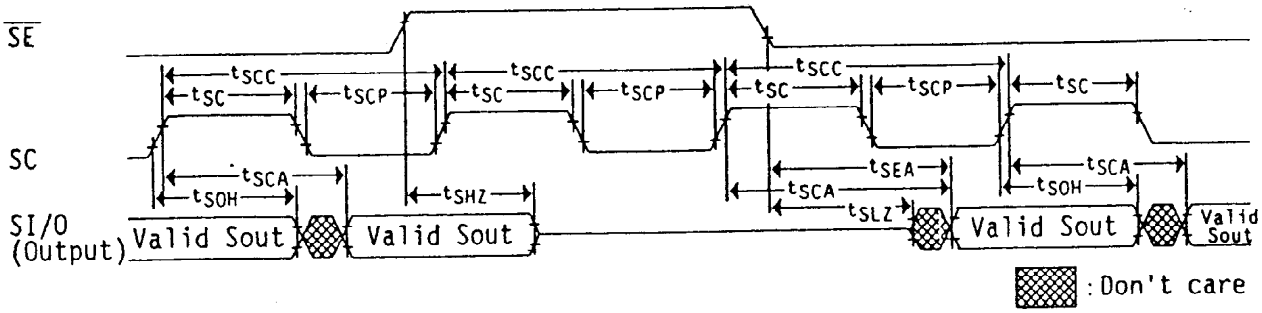
Notes: 1. Ym is the SAM start address in before SRT.
2. Bi, Bj initiate the boundary address.

Masked Split Write Transfer Cycle

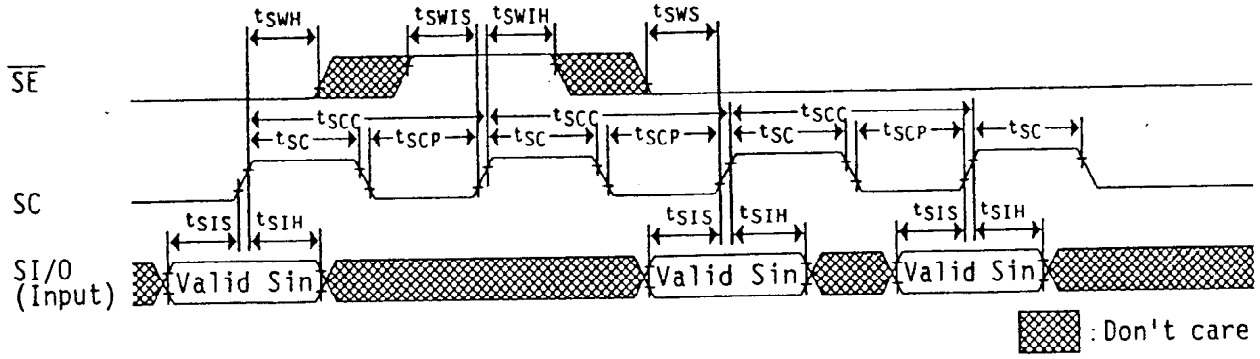


Notes: 1. Ym is the SAM start address in before SRWT.
2. Bi, Bj initiate the boundary address.
3. I/O Mask Data (In new mask mode)
Low : Mask
High : Non Mask
I/O : Don't care in persistent mask mode.

Serial Read Cycle



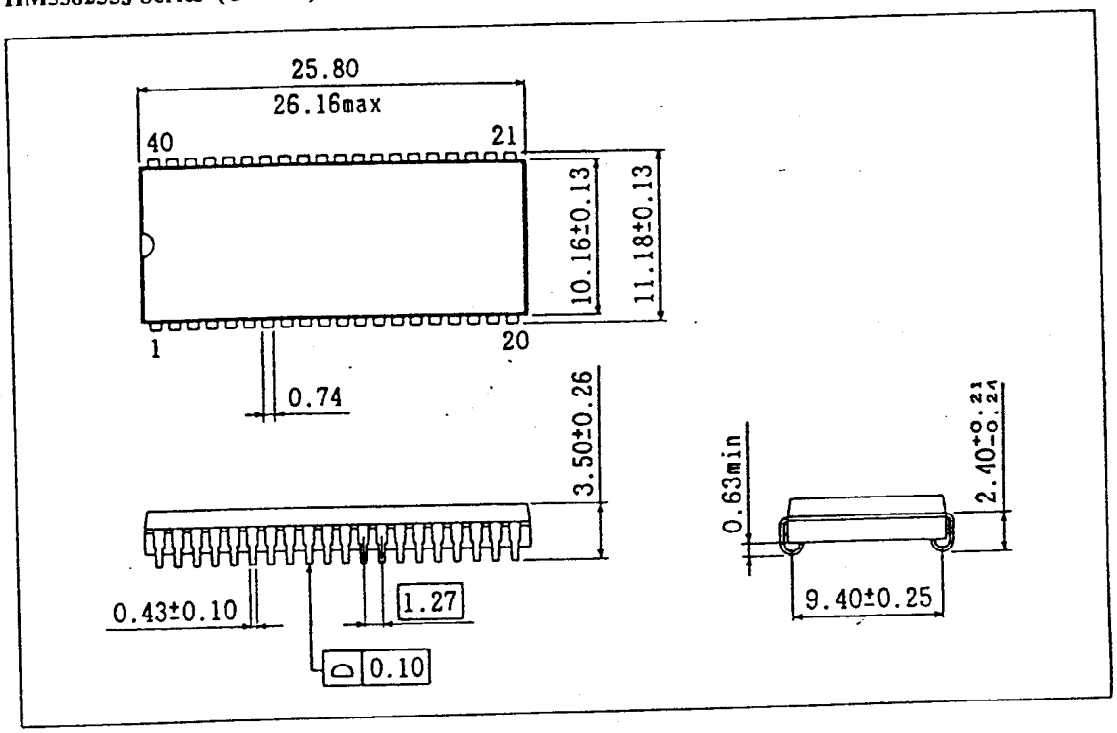
Sereal Write Cycle



Package Outline

Unit: mm

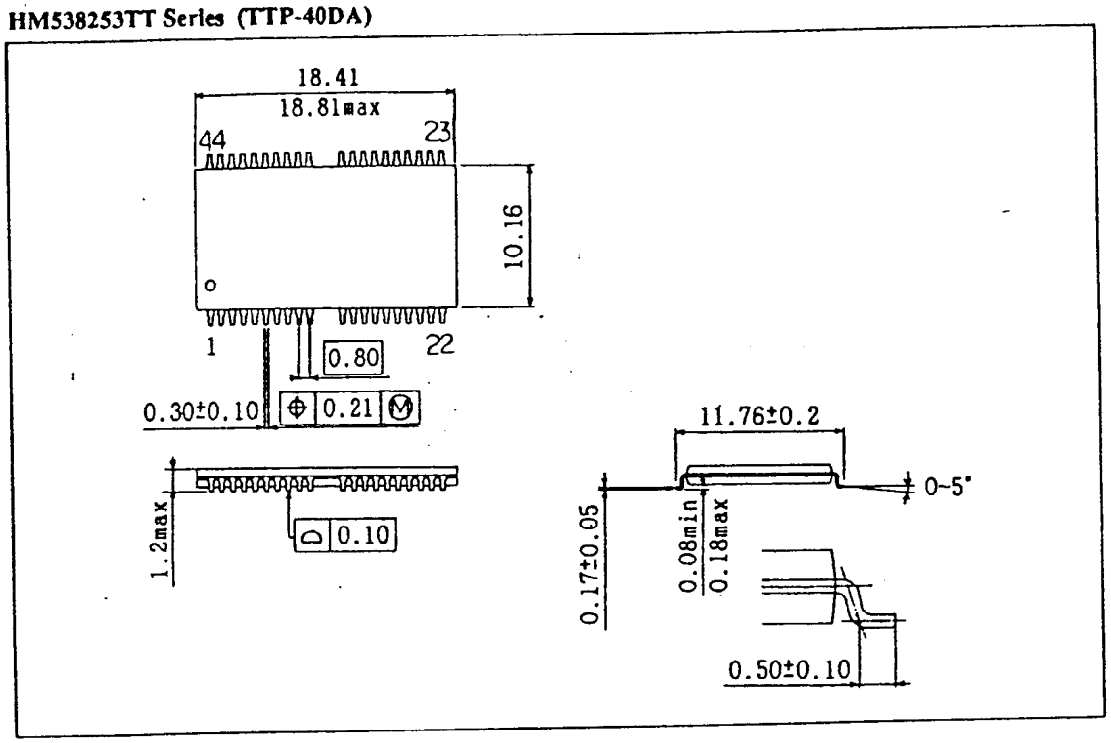
HM538253J Series (CP-40D)



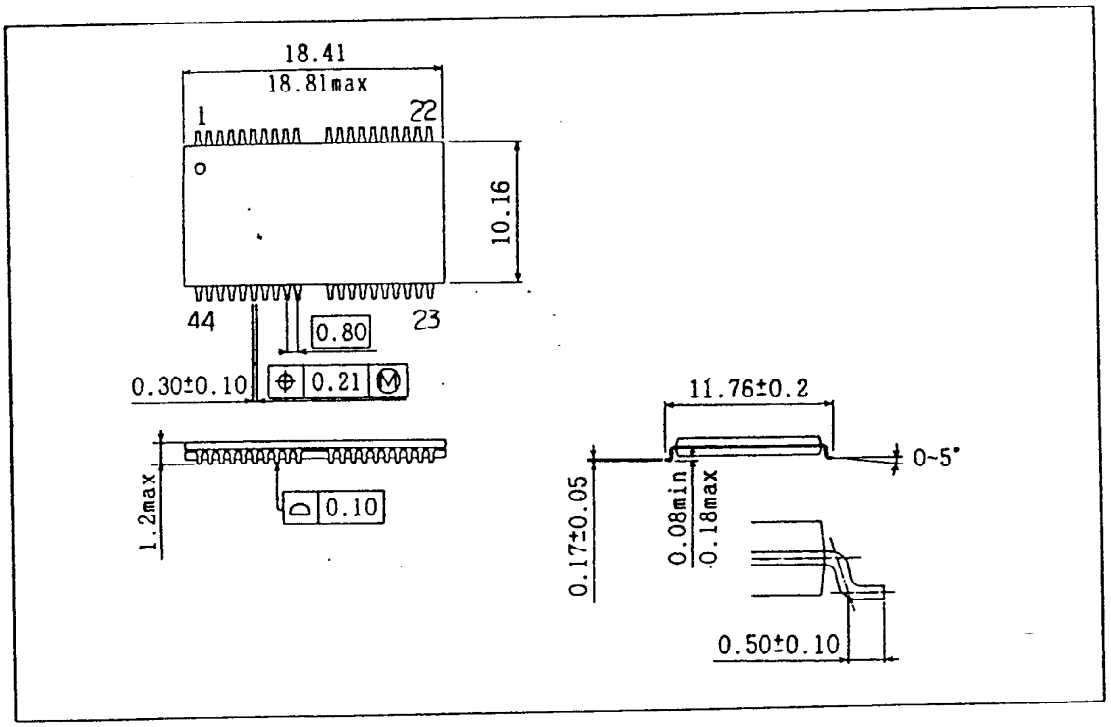
Package Outline (cont)

Unit: mm

HM538253TT Series (TTP-40DA)



HM538253RR Series (TTP-40DAR)



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Revision Record

Rev.	Date	Contents of Modification	Drawn by	Approved by
0	Apr. 26, 1991	Initial issue	S.Ishikawa	K.Oishi
1	Sep. 27, 1991	Addition of HM538253TT/RR series. Addition of HM538253-7 Change of Low Power (Active) RAM: 633 mW (max) → 715 mW (max) SAM: 385 mW (max) → 468 mW (max) Pin Descriptioon Addition of No lead Change of stopping column boundary table. Addition of note17 for AC characteristics. Addition of note for Masked Write Transfer Cycle and Masked Split Transfer Cycle. Pin Arrangement Addition of TSOP Operation of HM538253 Change of Mask Resister Set/Read Cycle and DSF1 low → and DSF1 high Figure 1/Figure 2: Change of DSF1 Figure 2: Address Mask → Column Mask Addition of note for DC Characteristics Capacitance Change of V_{CC} range:5 V → 5 V ± 10% AC Characteristics Addition of Output load t_{RAH}: 15 ns (min) → 10 ns (min) t_{RCD}: 25 ns (min) → 20 ns (min) t_{DTH}: 15 ns (min) → 10 ns (min) t_{RFH}: 15 ns (min) → 10 ns (min) t_{RAD}: 20 ns (min) → 15 ns (min) t_{RWL}: 25 ns (min) → 20 ns (min) t_{CWL}: 25 ns (min) → 20 ns (min) t_{WH}: 15 ns (min) → 10 ns (min) t_{MH}: 15 ns (min) → 10 ns (min) t_{RWC}: 235 ns (min) → 230 ns (min) t_{RWS}: 155 ns (min) → 150 ns (min) t_{CWD}: 55 ns (min) → 50 ns (min) t_{AWD}: 75 ns (min) → 70 ns (min) t_{RAD}: 20 ns (min) → 15 ns (min) t_{RWL}: 25 ns (min) → 20 ns (min) t_{CWL}: 25 ns (min) → 20 ns (min) t_{CHR}: 15/20 ns (min) → 10/10 ns (min)	S.Ishikawa	M. Yamamura

Revision Record (cont)

Rev.	Date	Contents of Modification	Drawn by	Approved by
1	Sep. 27, 1991	AC Characteristics (cont) t_{RDH}: 70 ns (min) → 65 ns (min) t_{ADH}: 35 ns (min) → 30 ns (min) t_{DTP}: 30 ns (min) → 20 ns (min) t_{DRD}: 90 ns (min) → 80 ns (min) t_{SRH}: 90 ns (min) → 80 ns (min) t_{SCH}: 30 ns (min) → 25 ns (min) t_{RAD}: 20 ns (min) → 15 ns (min) (P25/P27) Change of note 5 V_{OH}: -200 mV → -100 mV V_{OL}: +200 mV → +100 mV Change of note 17 t_{SLZ} are in the same → t_{SLZ} are measured in the same Addition of note for Write Cycle State Table Change of BWM/BW: Address mask → Column mask Change of package dimensions: HM538253TT Series (TTP 40DA), HM538253RR Series (TTP 40DAR) Change of Timing waveforms	S.Ishikawa	M. Yamamura
2	Apr. 2, 1992	Change of Cycle time RAM: 135 ns (min) → 130 ns (min) Change of Block Write cycle DSF1 high at the falling edge of $\overline{CAS}$ and $\overline{WE}$ → DSF1 high and $\overline{WE}$ low at the falling edge of $\overline{CAS}$ Addition of note for Stopping Column in Split Transfer Cycle Addition of note for Register Reset Cycle AC Characteristics Change of Out put load: SAM 1TTL + CL(30 pF) → SAM, QSF 1TTL + CL(30 pF) t_{RC}: 135 ns (min) → 130 ns (min) t_{RP}: 55 ns (min) → 50 ns (min) t_{OFF2}: 20 ns (max) → 15 ns (max) t_{WCH}/ t_{CAH}/ t_{CFH}: 15 ns (min) → 12 ns (min) t_{DH}: 15 ns (min) → 12 ns (min) (P22/ P23) t_{OEH}: 20 ns (min) → 15 ns (min) (P22/ P23) t_{ODD}: 20 ns (min) → 15 ns (min) t_{DRD}: 65 ns (min) → 60 ns (min) t_{RWC}: 185 ns (min) → 180 ns (min) t_{DQD}: 35 ns (max) → 30 ns (max) Addition of notes 15 for t_{RQD}/ t_{CQD} Change of notes for t_{DQD}/t_{RQD}/ t_{CQD}/ t_{SQD}: notes 7 → notes 15		

Revision Record (cont)

Rev.	Date	Contents of Modification	Drawn by	Approved by
2	Apr. 2, 1992	AC Characteristics (cont) t_{SEA}: 22 ns (max) → 20 ns (max) t_{SHZ}: 20 ns (max) → 15 ns (max) Addition of note 16, 18, 19 for AC Characteristics Change of Timing Waveforms	S.ISHIKAWA	M.YAMAMURA