SRM20257L10/12

CMOS 256K-BIT STATIC RAM

- **Low Supply Current**
- **Access Time 100ns/120ns**
- **32,768 Words x 8-Bit Asynchronous**
- **Two Chip Select Terminals**

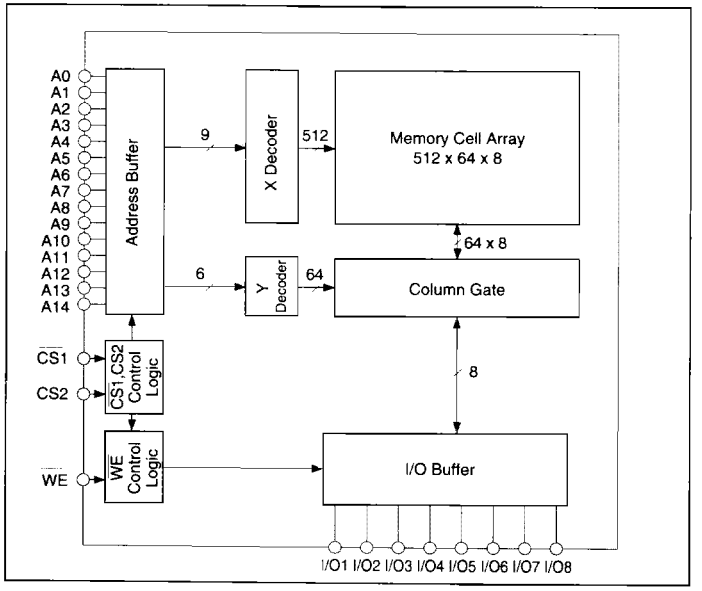
■ DESCRIPTION

The SRM20257L10/12 is a 32,768 word x 8-bit asynchronous, static, random access memory fabricated using advanced CMOS technology. Its very low standby power requirement makes it ideal for applications requiring non-volatile storage with back-up batteries. The asynchronous and static nature of the memory requires no external clock or refresh circuit. Input and output ports are TTL compatible and the 3-state output allows easy expansion of memory capacity. The inclusion of two chip select terminals simplifies the design of peripheral circuits for the memories.

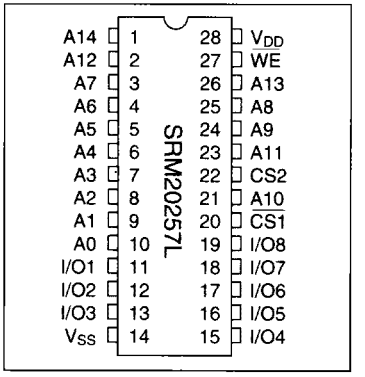
■ FEATURES

- Fast access time ..... SRM20257L10 100ns (Max)
  SRM20257L12 120ns (Max)
  SRM20100L10 100ns (Max)
- Low supply current ..... Standby : 2μA (Typ)
  Operation: 13mA/1MHz (Typ)
- Completely static ..... No clock required
- Single power supply ..... 5V ± 10%
- TTL compatible inputs and outputs
- 3-state output
- Battery back-up operation
- Package ..... SRM20257LC10/12 Plastic DIP-28pin
  SRM20257LM10/12 Plastic SOP2-28pin

■ BLOCK DIAGRAM



■ PIN CONFIGURATION



■ PIN DESCRIPTION

A0 to A14	Address Input
WE	Write Enable
CS1	Chip Select 1
CS2	Chip Select 2
I/O1 to 8	Data Input/Output
VDD	Power Supply (+5V)
VSS	Power Supply (0V)

■ ABSOLUTE MAXIMUM RATINGS

(V_{SS}=0V)

Parameter	Symbol	Ratings	Unit
Supply voltage	V_{DD}	-0.5 to 7.0	V
Input voltage	V_I	-0.5* to 7.0	V
Input/Output voltage	$V_{I/O}$	-0.5* to V_{DD}+0.3	V
Power dissipation	P_D	1.0	W
Operating temperature	T_{opr}	0 to 70	°C
Storage temperature	T_{stg}	-65 to 150	°C
Soldering temperature and time	T_{sol}	260°C, 10s (Lead only)	—

* V_I, $V_{I/O}$ (Min) = -3.0V when pulse width is less than or equal to 50ns.

■ DC RECOMMENDED OPERATING CONDITIONS

(V_{SS} = 0V, Ta = 0 to 70°C)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Supply voltage	V_{DD}	—	4.5	5.0	5.5	V
	V_{SS}	—	0	0	0	V
Input voltage	V_{IH}	—	2.2	—	V_{DD} + 0.3	V
	V_{IL}	—	-0.3*	—	0.8	V

* V_{IL} (Min) = -1.0V when pulse width is less than or equal to 50ns.

■ ELECTRICAL CHARACTERISTICS

● DC Electrical Characteristics

(V_{DD} = 5V ± 10%, V_{SS} = 0V, Ta = 0 to 70°C)

Parameter	Symbol	Conditions	SRM20257L10			SRM20257L12			Unit
			Min	Typ*	Max	Min	Typ*	Max	
Input leakage	I_{LI}	V_I = 0 to V_{DD}	-1	—	1	-1	—	1	µA
Standby supply current	I_{DDS}	$\overline{CS1}$ = V_{IH} or CS2=V_{IL}	—	0.5	3.0	—	0.5	3.0	mA
	I_{DDS1}	$\overline{CS1}$=CS2≥V_{DD}-0.2V or CS2≤0.2V	—	2	100	—	2	100	µA
Average operating current	I_{DDA}	V_I=V_{IL}, V_{IH}, $I_{I/O}$ = 0mA, tcyc=Min	—	40	70	—	37	70	mA
	I_{DDA1}	V_I=V_{IL}, V_{IH}, $I_{I/O}$ = 0mA, tcyc=1µs	—	13	—	—	13	—	mA
Operating supply current (DC)	I_{DDO}	V_I=V_{IL}, V_{IH}, $I_{I/O}$ = 0mA	—	25	45	—	25	45	mA
Output leakage	I_{LO}	$\overline{CS1}$ = V_{IH} or CS2 = V_{IL}, or OE = V_{IH}, $V_{I/O}$ = 0 to V_{DD}	-1	—	1	-1	—	1	µA
High level output voltage	V_{OH}	I_{OH}= -1.0mA	2.4	V_{DD}-0.1	—	2.4	V_{DD}-0.1	—	V
Low level output voltage	V_{OL}	I_{OL}= 2.1mA	—	0.2	0.4	—	0.2	0.4	V

* Typical values are measured at T_a=25°C and V_{DD}=5.0V.

● Terminal Capacitance

(f = 1MHz, Ta = 25°C)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Address Capacitance	C_{ADD}	V_{ADD} = 0V	—	—	8	pF
Input Capacitance	C_I	V_I = 0V	—	—	8	pF
I/O Capacitance	$C_{I/O}$	$V_{I/O}$ = 0V	—	—	8	pF

● AC ELECTRICAL CHARACTERISTIC

O Read Cycle

(V_{DD} = 5V ± 10%, V_{SS} = 0V, Ta = 0 to 70°C)

Parameter	Symbol	Conditions	SRM20257L10		SRM20257L12		Unit
			Min	Max	Min	Max	
Read cycle time	t_{RC}	*1	100	—	120	—	ns
Address access time	t_{ACC}		—	100	—	120	ns
$\overline{CS1}$ access time	t_{ACS1}		—	100	—	120	ns
CS2 access time	t_{ACS2}		—	100	—	120	ns
$\overline{CS1}$ output set time	t_{CLZ1}		10	—	10	—	ns
$\overline{CS1}$ output floating	t_{CHZ1}	*2	—	35	—	40	ns
CS2 output set time	t_{CLZ2}		10	—	10	—	ns
CS2 output floating	t_{CHZ2}		—	35	—	40	ns
Output hold time	t_{OH}	*1	10	—	10	—	ns

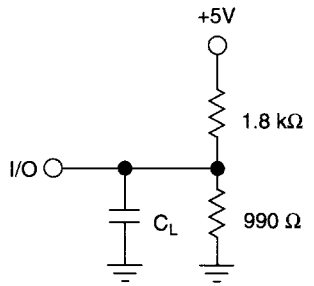
O Write Cycle

(V_{DD} = 5V ± 10%, V_{SS} = 0V, Ta = 0 to 70°C)

Parameter	Symbol	Conditions	SRM20257L10		SRM20257L12		Unit
			Min	Max	Min	Max	
Write cycle time	t_{WC}	*1	100	—	120	—	ns
Chip select time ($\overline{CS1}$)	t_{CW1}		80	—	85	—	ns
Chip select time (CS2)	t_{CW2}		80	—	85	—	ns
Address valid to end of write	t_{AW}		80	—	85	—	ns
Address setup time	t_{AS}		0	—	0	—	ns
Write pulse width	t_{WP}		70	—	80	—	ns
Address hold time	t_{WR}		0	—	0	—	ns
Input data setup time	t_{DW}		45	—	50	—	ns
Input data hold time	t_{DH}		0	—	0	—	ns
Write to output floating	t_{WHZ}	*2	—	35	—	40	ns
Output active from end of write	t_{OW}		10	—	10	—	ns

*1 Test Conditions.

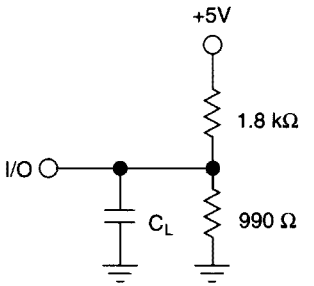
1. Input pulse level : 0.6V to 2.4V
2. tr = tf = 5ns
3. Input and output timing reference levels : 1.5V
4. Output load



C_L = 100pF (Includes Jig Capacitance)

*2 Test Conditions

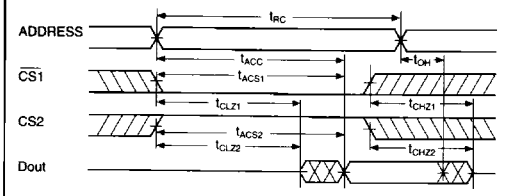
1. Input pulse level : 0.6V to 2.4V
2. tr = tf = 5ns
3. Input timing reference levels : 1.5V
4. Output timing reference levels
   t_{CLZ1}, t_{CLZ2}, tow: ±200mV (the level displaced from stable output voltage level)
5. Output load



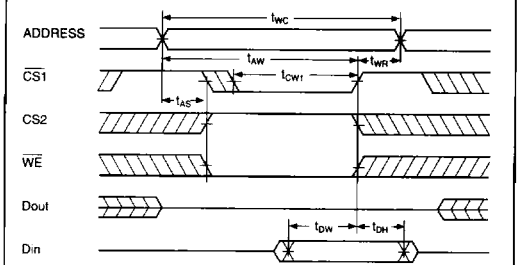
C_L = 5pF (Includes Jig Capacitance)

● Timing Chart

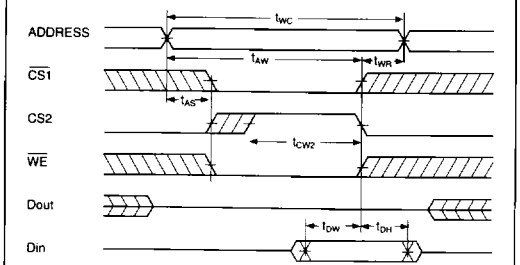
O Read Cycle *1



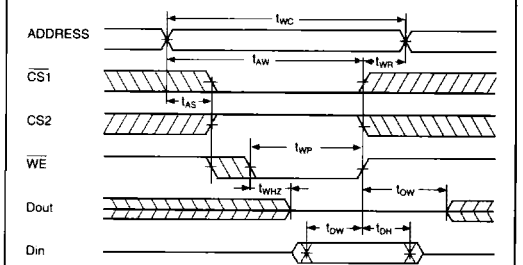
O Write Cycle 1 (CS1 Control) *2, *3



O Write Cycle 2 (CS2 Control) *2, *3



O Write Cycle 3 (WE Control) *2, *3



Note:
1. During read cycle time, WE should be "H" level.
2. During write cycle time that is controlled by CS1 or CS2, Output Buffer is in high impedance.
3. When I/O terminals are in output mode, be careful that opposite signals are not given to the I/O terminals.

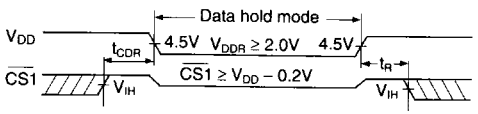
■ DATA RETENTION CHARACTERISTICS WITH LOW VOLTAGE POWER SUPPLY

(VSS=0V, Ta = 0 to 70°C)

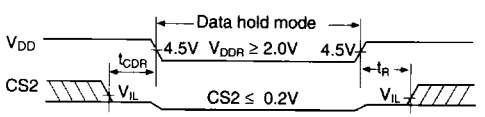
Parameter	Symbol	Conditions	Min	Typ*1	Max	Unit
Data retention supply voltage	VDDR		2.0	—	5.5	V
Data retention current	IDDR	VDDR=3V, CS2≤0.2V or CS1=CS2≥VDD-0.2V	—	1	50	µA
Chip select data hold time	tCDR		0	—	—	ns
Operation recovery time	tR		tRC*2	—	—	ns

*1 Typical values are measured at 25°C *2 tRC=Read cycle time

O Data Retention Timing 1 (CS1 Control)



O Data Retention Timing 2 (CS2 Control)



Note: During standby mode in which the data is retentive, the supply voltage (VDD) can be in low voltage until VDD=VDDR. At this mode data reading and writing are impossible.

■ FUNCTIONS

● Truth Table

$\overline{CS1}$	CS2	$\overline{WE}$	A0 to A14	DATA I/O	Mode	I_{DD}
H	X	X	X	Hi-Z	Standby	I_{DDS}, I_{DDS1}
X	L	X	X	Hi-Z	Standby	I_{DDS}, I_{DDS1}
L	H	L	Stable	D_{in}	Write	I_{DDA}, I_{DDA1}
L	H	H	Stable	D_{out}	Read	I_{DDA}, I_{DDA1}

X: "H" or "L"

● Read Mode

Data is read with setting addresses while holding $\overline{CS1}$="L", CS2="H" and $\overline{WE}$="H".

● Write Mode

There are following 4 ways of writing data into memory.

(1) Hold $\overline{CS1}$="L", $\overline{WE}$="L", set address, and give "H" pulse to CS2.
(2) Hold CS2="H", $\overline{WE}$="L", set address, and give "L" pulse to $\overline{CS1}$.
(3) Hold $\overline{CS1}$="L", CS2="H", set address and give "L" pulse to $\overline{WE}$.
(4) After setting addresses, give "L" pulse to both $\overline{CS1}$ and $\overline{WE}$, and also give "H" pulse to CS2.

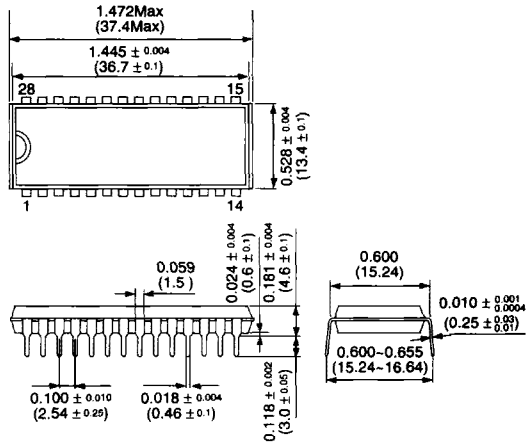
In the above cases, the data on the DATA I/O terminals are latched up into the SRM20257L10/12 when $\overline{CS1}$ and $\overline{WE}$ are in the positive-going of "L" pulse or CS2 are in the negative-going of "H" pulse. Since DATA I/O terminals are in high impedance, when $\overline{CS1}$="H" or CS2="L", bus contention between data driver and memory outputs can be avoided.

● Standby Mode

When $\overline{CS1}$ is "H" or CS2 is "L", the SRM20257L10/12 is in the standby mode. In this case data I/O terminals are in Hi-Z, so that all inputs of addresses, $\overline{WE}$ and data can be any value of "H" or "L". When $\overline{CS1}$ and CS2≥V_{DD} -0.2V, or CS2≤0.2V there is a small current in SRM20257L10/12 which flow through the high resistances of the memory cells only.

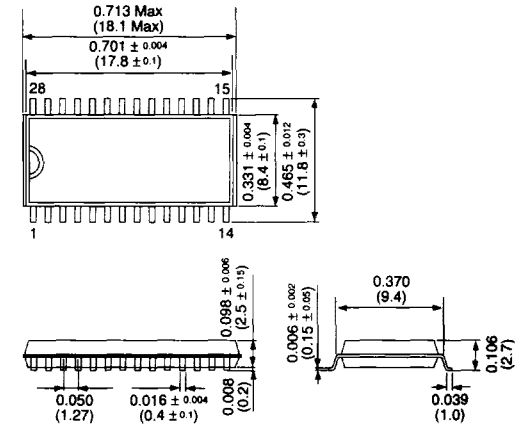
■ PACKAGE DIMENSIONS

Plastic DIP-28pin



unit : inch (mm)

Plastic SOP2-28pin

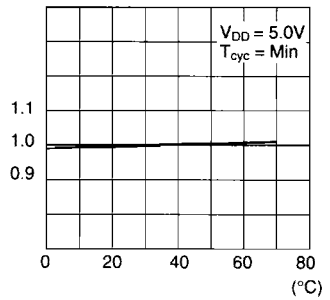


unit : inch (mm)

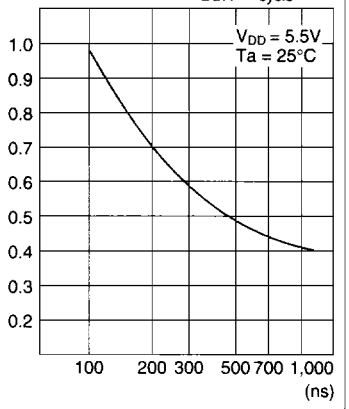
*1 SRM20257LM10/12 has the same electrical characteristics as SRM20257L10/12.

■ CHARACTERISTICS CURVES

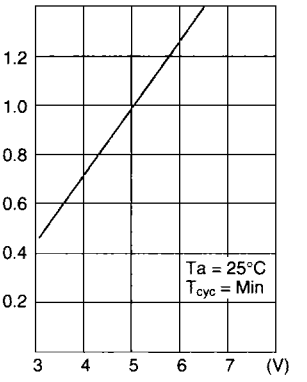
Normalized I_{DDA}—Ta



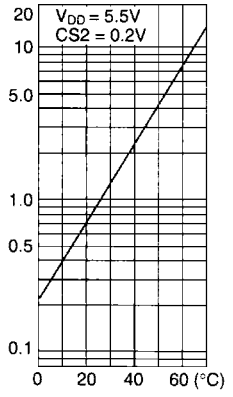
Normalized I_{DDA}—t_{cycle}



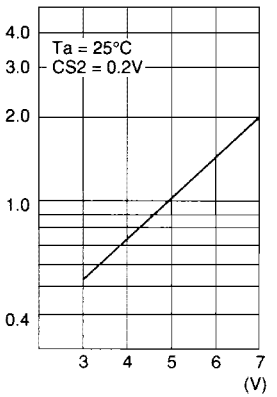
Normalized I_{DDA}—V_{DD}



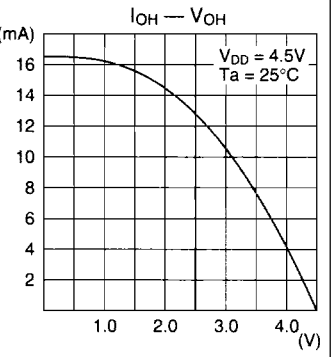
Normalized I_{DDS1}—Ta



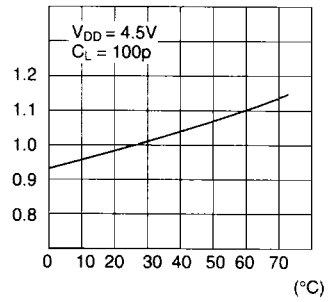
Normalized I_{DDS1}—V_{DD}



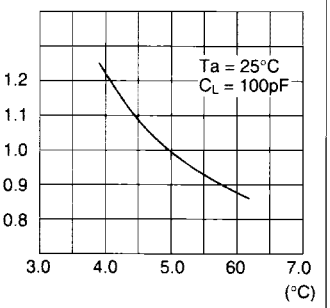
I_{OH} — V_{OH}



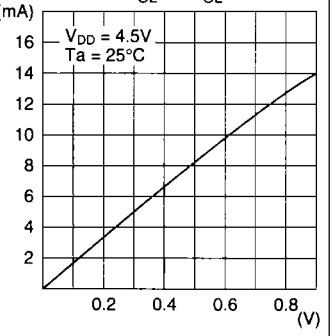
Normalized t_{ACC}·t_{ACS1},t_{ACS2}—Ta



Normalized t_{ACC}·t_{ACS1},t_{ACS2}—V_{DD}



I_{OL} — V_{OL}



THIS PAGE INTENTIONALLY BLANK