Semiconductor Corporation

CS5336 CS5338 CS5339

16-Bit, Stereo A/D Converters for Digital Audio

Features

- Complete CMOS Stereo A/D System
  - Delta-Sigma A/D Converters
  - Digital Anti-Alias Filtering
  - S/H Circuitry and Voltage Reference
- Adjustable System Sampling Rates including 32kHz, 44.1 kHz & 48kHz
- Low Noise and Distortion >90 dB S/(N+D)
- Internal 64X Oversampling
- Linear Phase Digital Anti-Alias Filtering
  - 0.01dB Passband Ripple
  - 80dB Stopband Rejection
- Low Power Dissipation: 400 mW
  - Power-Down Mode for Portable Applications
- Evaluation Board Available

General Description

The CS5336, CS5338 & CS5339 are complete analog-to-digital converters for stereo digital audio systems. They perform sampling, analog-to-digital conversion and anti-aliasing filtering, generating 16-bit values for both left and right inputs in serial form. The output word rate can be up to 50 kHz per channel.

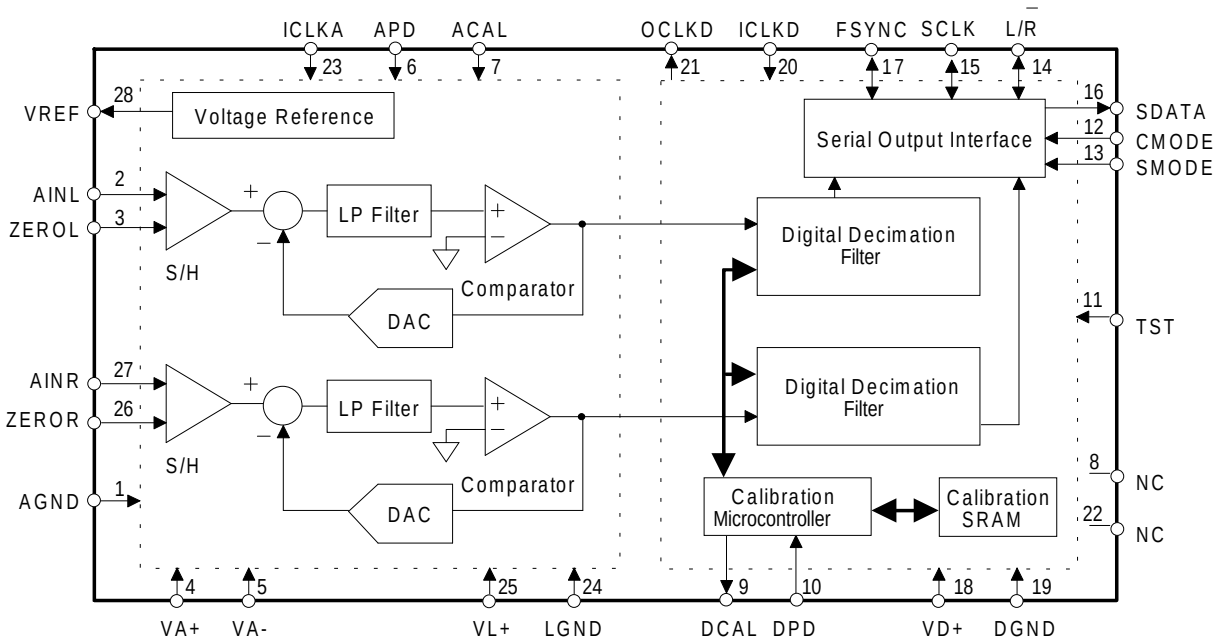
The ADCs use delta-sigma modulation with 64X over-sampling, followed by digital filtering and decimation, which removes the need for an external anti-alias filter.

The CS5336 & CS5338 have an SCLK which clocks out data on rising edges. The CS5339 has an SCLK which clocks out data on falling edges.

The CS5336 has a filter passband of dc to 22kHz. The CS5338 & CS5339 have a filter passband of dc to 24 kHz. The filters have linear phase, 0.01 dB passband ripple, and >80 dB stopband rejection.

The ADC's are housed in a 0.6" wide 28-pin plastic DIP, and also in a 0.3" wide 28-pin SOIC surface mount package. Extended temperature range versions of the CS5336 are also available.

ORDERING INFORMATION: See Page 3-59



ANALOG CHARACTERISTICS

(Logic 0 = GND; Logic 1 = VD+; K grade: T_A = 25°C; B and T grades: $T_A = T_{MIN}$ to T_{MAX}; VA+, VL+,VD+ = 5V; VA- = -5V; Full-Scale Input Sinewave, 1kHz; Output word rate = 48 kHz; SCLK = 3.072 MHz; Source Impedance = 50Ω with 10 nF to AGND; Measurement Bandwidth is 10 Hz to 20 kHz; unless otherwise specified.)

Parameter	Symbol	CS5336,8,9-K Min	Typ	Max	CS5336-B Min	Typ	Max	CS5336-T Min	Typ	Max	Units
Specified Temperature Range	T_A	0	to	70	-40	to	+85	-55	to	+125	°C
Resolution		16	-	-	16	-	-	16	-	-	Bits
Dynamic Performance											
Dynamic Range		92.7	95.7	-	90	93.5	-	84	92	-	dB
Signal-to-(Noise + Distortion); THD+N	S/(N+D)	90.7	92.7	-	85	89	-	82	86	-	dB
Signal to Peak Noise		-	96	-	-	95	-	-	94	-	dB
Total Harmonic Distortion	THD	.0025	.001	-	.005	.001	-	.013	.005	-	%
Interchannel Phase Deviation		-	.0001	-	-	.0001	-	-	.0001	-	°
Interchannel Isolation (dc to 20 kHz)		100	106	-	90	106	-	83	96	-	dB
dc Accuracy											
Interchannel Gain Mismatch		-	0.01	0.05	-	.01	.05	-	.01	0.1	dB
Gain Error (includes Vref tolerance)		-	±1	±5	-	±2	±5	-	±3	±6	%
Gain Drift (includes Vref drift, Note 1)		-	25	-	-	70	-	-	70	-	ppm/°C
Bipolar Offset Error (Note 2)		-	±5	±15	-	±10	±30	-	±16	±65	LSB
Offset Drift (Note1)		-	15	-	-	20	-	-	20	-	ppm/°C
Analog Input											
Input Voltage Range (±Full Scale)	VIN	±3.5	±3.68	-	±-3.5	±3.68	-	±3.5	±3.68	-	V
Input Impedance	ZIN	-	65	-	-	65	-	-	65	-	kΩ
Power Supplies											
Power Supply Current (VA+)+(VL+)	IA+	-	25	35	-	25	35	-	25	35	mA
with APD, DPD low VA-	IA-	-	-25	-35	-	-25	-35	-	-25	-35	mA
(Normal Operation) VD+	ID+	-	30	45	-	30	45	-	30	50	mA
Power Supply Current (VA+)+(VL+)	IA+	-	10	50	-	10	50	-	10	50	µA
with APD, DPD high VA-	IA-	-	-10	-50	-	-10	-50	-	-10	-50	µA
(Power-Down Mode) VD+	ID+	-	10	400	-	10	400	-	10	400	µA
Power Consumption (APD, DPD Low)	PDN	-	400	575	-	400	575	-	400	600	mW
(APD, DPD High)	PDS	-	0.15	2.5	-	0.15	2.5	-	0.15	2.5	mW
Power Supply (dc to 26 kHz)	PSRR	-	54	-	-	54	-	-	54	-	dB
Rejection Ratio (26 kHz to 3.046 MHz)		-	100	-	-	100	-	-	100	-	dB

Notes:
1. This parameter is guaranteed by design and/or characterization.
2. After calibration with DCAL connected to ACAL, and ZEROL & ZEROR terminated to AGND with an impedance matched to the AINR & AINL source impedance. Executing a calibration with ACAL tied low (See Power Down and Offset Calibration section) will yield an offset error of typically less than ± 5LSB.

Specifications are subject to change without notice.

DIGITAL FILTER CHARACTERISTICS

(T_A = 25 ° C; VA+, VL+ ,VD+ = 5V ± 5%; VA- = -5V ± 5%; Output word rate of 48 kHz)

Parameter			Symbol	Min	Typ	Max	Units
Passband	(-3 dB)	CS5336		0	to	22	kHz
	(-3 dB)	CS5338, CS5339		0	to	24	kHz
	(-0.01 dB)	CS5336		0	to	20	kHz
	(-0.01 dB)	CS5338, CS5339		0	to	22	kHz
Passband Ripple				-	-	± 0.01	dB
Stopband		CS5336		26	to	3046	kHz
		CS5338, CS5339		28	to	3044	kHz
Stopband Attenuation		(Note 3)		80	-	-	dB
Group Delay (OWR = Output Word Rate)			t_{gd}	-	18/OWR	-	s
Group Delay Variation vs. Frequency			$\triangle t_{gd}$	-	-	0.0	us

Notes: 3. The analog modulator samples the input at 3.072MHz for an output word rate of 48 kHz. There is no rejection of input signals which are multiples of the sampling frequency (that is: there is no rejection for n x 3.072MHz ±22kHz for the CS5338 & CS5339, or n x 3.072MHz ±20.0kHz for the CS5336, where n = 0,1,2,3...).

DIGITAL CHARACTERISTICS

(T_A = 25 °C; VA+, VL+ ,VD+ = 5V ± 5%; VA- = -5V ± 5%)

Parameter	Symbol	Min	Typ	Max	Units
High-Level Input Voltage	V_{IH}	70%VD+	-	-	V
Low-Level Input Voltage	V_{IL}	-	-	30% VD+	V
High-Level Output Voltage at Io = -20uA	V_{OH}	4.4	-	-	V
Low-Level Output Voltage at Io = 20uA	V_{OL}	-	-	0.1	V
Input Leakage Current	Iin	-	1.0	-	uA

ABSOLUTE MAXIMUM RATINGS (AGND, LGND, DGND = 0V, all voltages with respect to GND)

Parameter		Symbol	Min	Max	Units
DC Power Supplies:	Positive Analog	VA+	-0.3	+6.0	V
	Negative Analog	VA-	+0.3	-6.0	V
	Positive Logic	VL+	-0.3	(VA+) + 0.3	V
	Positive Digital	VD+	-0.3	+6.0	V
Input Current, Any Pin Except Supplies		I_{in}	-	± 10	mA
Analog Input Voltage (AIN and ZERO pins)		V_{INA}	(VA-)- 0.3	(VA+)+ 0.3	V
Digital Input Voltage		V_{IND}	-0.3	(VD+) + 0.3	V
Ambient Temperature (power applied)		T_A	-55	+125	°C
Storage Temperature		T_{stg}	-65	+150	°C

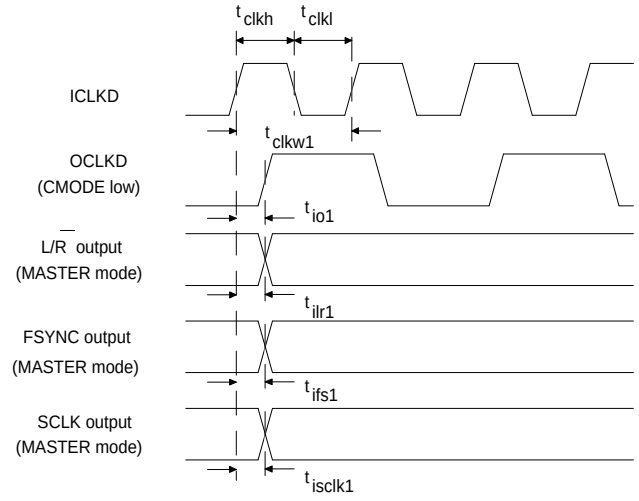
WARNING: Operation at or beyond these limits may result in permanent damage to the device. Normal operation is not guaranteed at these extremes.

SWITCHING CHARACTERISTICS

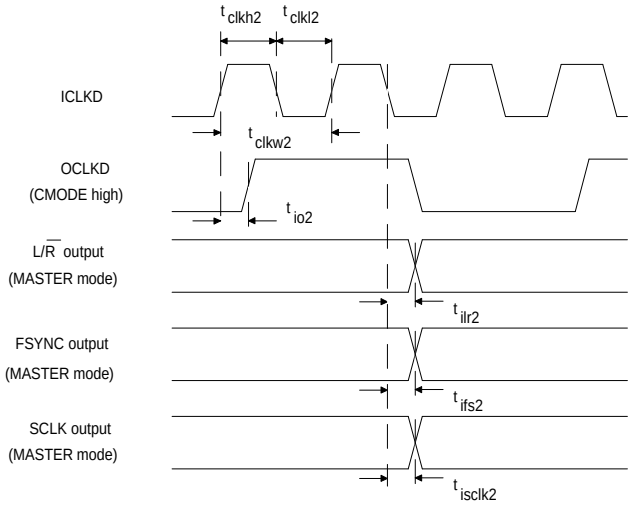
(T_A = 25 °C; VA+, VL+, VD+ = 5V ± 5%; VA- = -5V ± 5%; Inputs: Logic 0 = 0V, Logic 1 = VD+; C_L = 20 pF)

Parameter	Symbol	Min	Typ	Max	Unit
ICLKD Period (CMODE low) (Note 6)	t_{clkw1}	78	-	3906	ns
ICLKD Low (CMODE low)	t_{clkl1}	31	-	-	ns
ICLKD High (CMODE low)	t_{clkh1}	31	-	-	ns
ICLKD rising to OCLKD rising (CMODE low)	t_{io1}	5	-	40	ns
ICLKD Period (CMODE high)	t_{clkw2}	52	-	2604	ns
ICLKD Low (CMODE high)	t_{clkl2}	20	-	-	ns
ICLKD High (CMODE high)	t_{clkh2}	20	-	-	ns
ICLKD rising or falling to OCLKD rising (CMODE high, Note 4)	t_{io2}	5	-	45	ns
ICLKD rising to L/$\overline{R}$ edge (CMODE low, MASTER mode)	t_{ilr1}	5	-	50	ns
ICLKD rising to FSYNC edge (CMODE low, MASTER mode)	t_{ifs1}	5	-	50	ns
ICLKD rising to SCLK edge (CMODE low, MASTER mode)	t_{isclk1}	5	-	50	ns
ICLKD falling to L/$\overline{R}$ edge (CMODE high, MASTER mode)	t_{ilr2}	5	-	50	ns
ICLKD falling to FSYNC edge (CMODE high, MASTER mode)	t_{ifs2}	5	-	50	ns
ICLKD falling to SCLK edge (CMODE high, MASTER mode)	t_{isclk2}	5	-	50	ns
SCLK rising to SDATA valid (MASTER mode, Note 5)	t_{sdo}	0	-	50	ns
SCLK duty cycle (MASTER mode)		40	50	60	%
SCLK rising to L/$\overline{R}$ (MASTER mode, Note 5)	t_{mslr}	-20	-	20	ns
SCLK rising to FSYNC (MASTER mode, Note 5)	t_{msfs}	-20	-	20	ns
SCLK Period (SLAVE mode)	t_{sclkw}	155	-	-	ns
SCLK Pulse Width Low (SLAVE mode)	t_{sclkl}	60	-	-	ns
SCLK Pulse Width High (SLAVE mode)	t_{sclkh}	60	-	-	ns
SCLK rising to SDATA valid (SLAVE mode, Note 5)	t_{dss}	-	-	50	ns
L/$\overline{R}$ edge to MSB valid (SLAVE mode)	t_{lrdss}	-	-	50	ns
Falling SCLK to L/$\overline{R}$ edge delay (SLAVE mode, Note 5)	t_{slr1}	30	-	-	ns
L/$\overline{R}$ edge to falling SCLK setup time (SLAVE mode, Note 5)	t_{slr2}	30	-	-	ns
Falling SCLK to rising FSYNC delay (SLAVE mode, Note 5)	t_{sfs1}	30	-	-	ns
Rising FSYNC to falling SCLK setup time (SLAVE mode, Note 5)	t_{sfs2}	30	-	-	ns
DPD pulse width	t_{pdw}	2 x tclkw	-	-	ns
DPD rising to DCAL rising	t_{pcr}	-	-	50	ns
DPD falling to DCAL falling (OWR = Output Word Rate)	t_{pcf}	-	4096	-	1/OWR

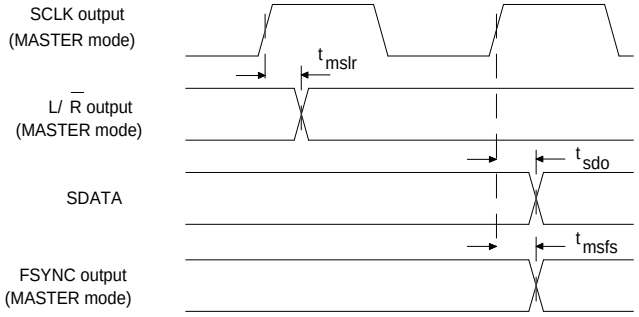
Notes: 4. ICLKD rising or falling depends on DPD to L/$\overline{R}$ timing (see Figure 2).
5. SCLK is shown for CS5336, CS5338. SCLK is inverted for CS5339.
6. Specifies minimum output word rate (OWR) of 1 kHz.



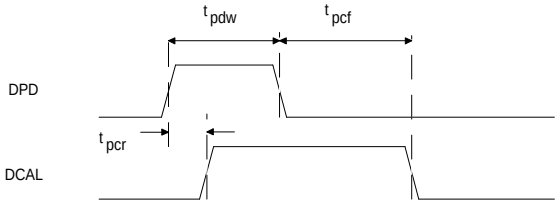
ICLKD to Outputs Propagation Delays (CMODE low)



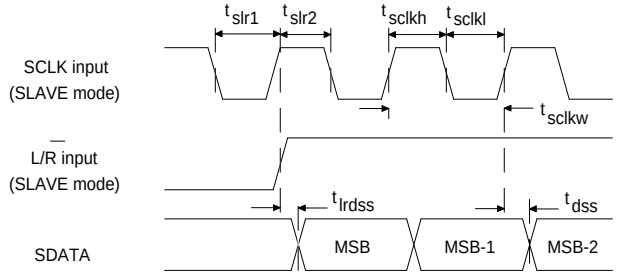
ICLKD to Outputs Propagation Delays (CMODE high)



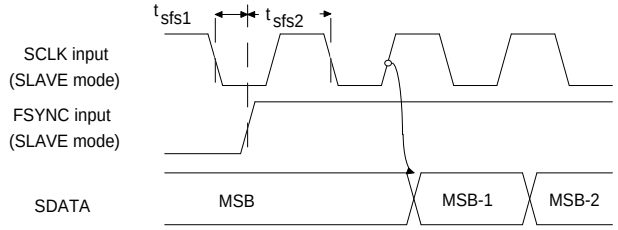
SCLK to SDATA, L/$\overline{R}$ & FSYNC - MASTER Mode



Power Down & Calibration Timing



SCLK to L/$\overline{R}$ & SDATA - SLAVE mode, FSYNC high



FSYNC to SCLK - SLAVE Mode, FSYNC Controlled.

RECOMMENDED OPERATING CONDITIONS

(AGND, LGND, DGND = 0V; all voltages with respect to ground)

Parameter		Symbol	Min	Typ	Max	Units
DC Power Supplies:	Positive Digital	VD+	4.75	5.0	VA+	V
	Positive Logic	VL+	4.75	5.0	VA+	V
	Positive Analog	VA+	4.75	5.0	5.25	V
	Negative Analog	VA-	−4.75	−5.0	−5.25	V
Analog Input Voltage	(Note 7)	V_{AIN}	−3.68	-	3.68	V

Notes: 7. The ADCs accept input voltages up to the analog supplies (VA+, VA-). They will produce a positive full-scale output for inputs above 3.68 V and negative full-scale output for inputs below -3.68 V. These values are subject to the gain error tolerance specification. Additional tag bits are output to indicate the amount of overdrive.

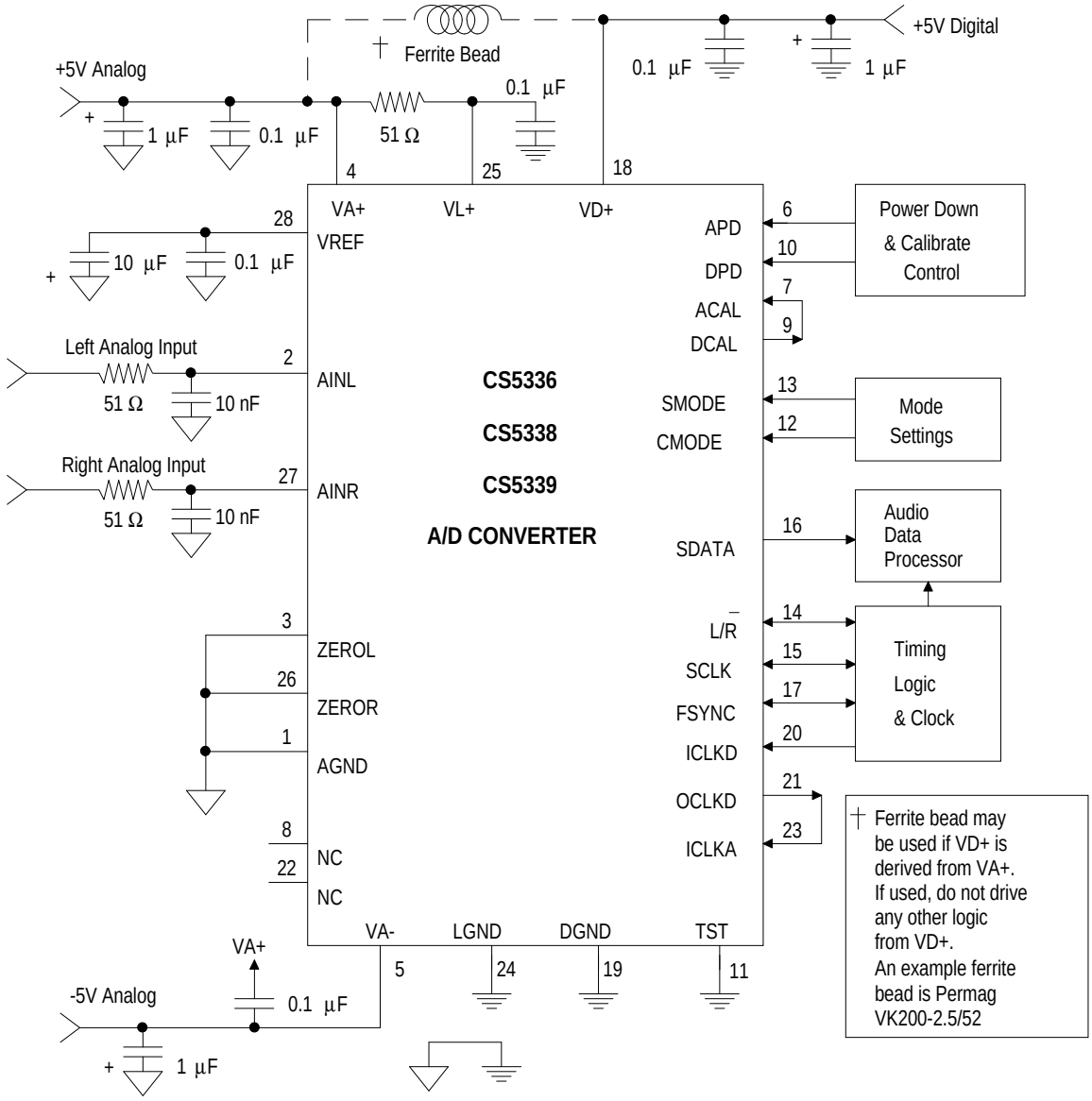


Figure 1. Typical Connection Diagram

GENERAL DESCRIPTION

The CS5336, CS5338, and CS5339 are 16-bit, 2-channel A/D converters designed specifically for stereo digital audio applications. The devices use two one-bit delta-sigma modulators which simultaneously sample the analog input signals at a 64 X sampling rate. The resulting serial bit streams are digitally filtered, yielding pairs of 16-bit values. This technique yields nearly ideal conversion performance independent of input frequency and amplitude. The converters do not require difficult-to-design or expensive anti-alias filters, and do not require external sample-and-hold amplifiers or a voltage reference.

An on-chip voltage reference provides for an input signal range of ± 3.68 volts. Any zero offset is internally calibrated out during a power-up self-calibration cycle. Output data is available in serial form, coded as 2's complement 16-bit numbers. Typical power consumption of only 400 mW can be further reduced by use of the power-down mode.

For more information on delta-sigma modulation and the particular implementation inside these ADCs, see the references at the end of this data sheet.

L/$\overline{R}$ (kHz)	CMODE	ICLKD (MHz)	OCLKD/ ICLKA (MHz)	SCLK (MHz)
32	low	8.192	4.096	2.048
32	high	12.288	4.096	2.048
44.1	low	11.2896	5.6448	2.8224
44.1	high	16.9344	5.6448	2.8224
48	low	12.288	6.144	3.072
48	high	18.432	6.144	3.072

Table 1. Common Clock Frequencies

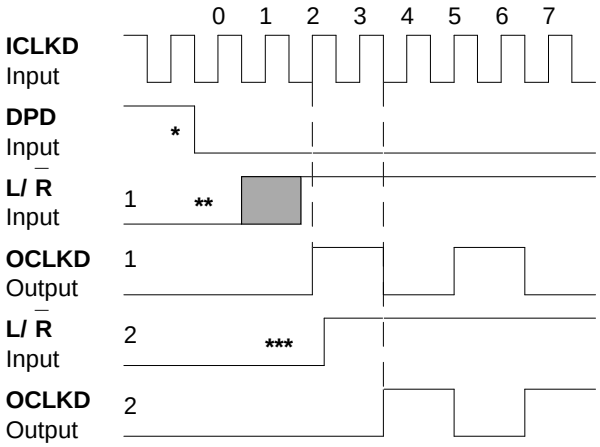
SYSTEM DESIGN

Very few external components are required to support the ADC. Normal power supply decoupling components, voltage reference bypass capacitors and a single resistor and capacitor on each input for anti-aliasing are all that's required, as shown in Figure 1.

Master Clock Input

The master input clock (ICLKD) into the ADC runs the digital filter, and is used to generate the modulator sampling clock. ICLKD frequency is determined by the desired Output Word Rate (OWR) and the setting of the CMODE pin. CMODE high will set the required ICLKD frequency to 384 X OWR, while CMODE low will set the required ICLKD frequency to 256 X OWR. Table 1 shows some common clock frequencies. The digital output clock (OCLKD) is always equal to 128 X OWR, which is always 2 X the input sample rate. OCLKD should be connected to ICLKA, which controls the input sample rate.

The phase alignment between ICLKD and OCLKD is determined as follows: when CMODE is



* DPD low is recognized on the next ICLKD rising edge (#0)
** L/$\overline{R}$ rising before ICLKD rising #2 causes OCLKD -1
*** L/$\overline{R}$ rising after ICLKD rising #2 causes OCLKD - 2

Figure 2. ICLKD to OCLKD Timing with CMODE high (384 X OWR)

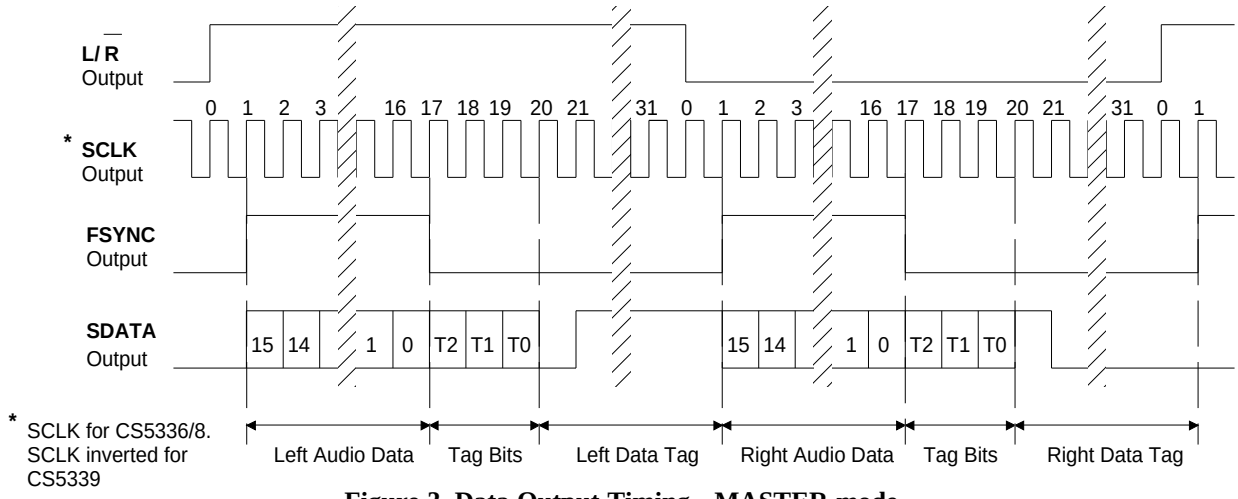


Figure 3. Data Output Timing - MASTER mode

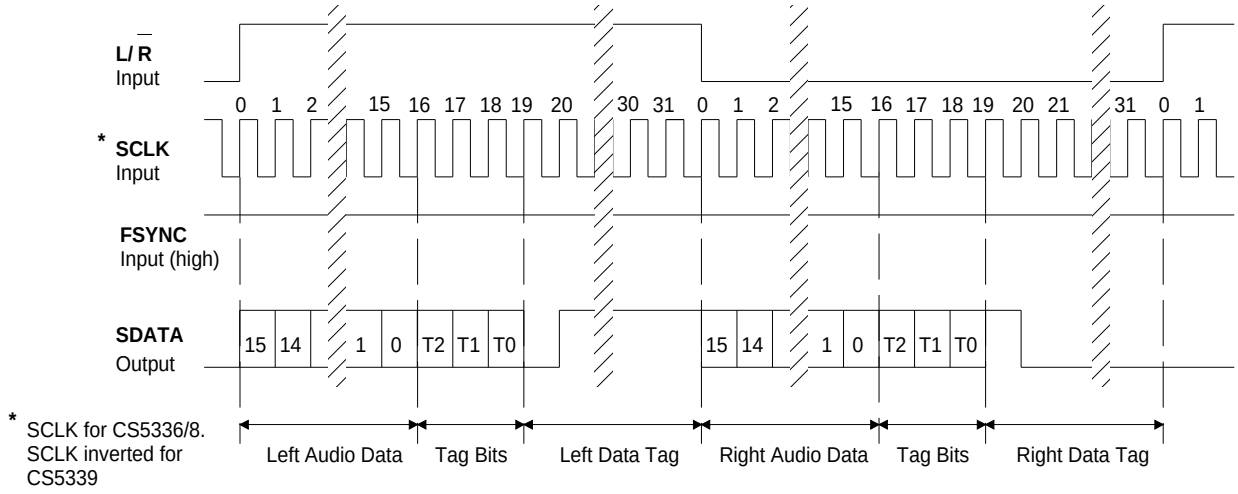


Figure 4. Data Output Timing - SLAVE Mode, FSYNC high

low, ICLKD is divided by 2 to generate OCLKD. The phase relationship between ICLKD and OCLKD is always the same, and is shown in the Switching Characteristics Timing Diagrams. When CMODE is high, OCLKD is ICLKD divided by 3. There are two possible phase relationships between ICLKD and OCLKD, which depend on the start-up timing between DPD and L/$\overline{R}$, shown in Figure 2.

Serial Data Interface

The serial data output interface has 3 possible modes of operation: MASTER mode, SLAVE mode with FSYNC high, and SLAVE mode with FSYNC controlled. In MASTER mode, the A/D converter is driven from a master clock (ICLKD) and outputs all other clocks, derived from ICLKD (see Figure 3). Notice the one SCLK cycle delay between L/$\overline{R}$ edges and FSYNC rising edges. FSYNC brackets the 16 data bits for each channel.

In SLAVE mode, L/$\overline{R}$ and SCLK are inputs. L/$\overline{R}$ must be externally derived from ICLKD, and should be equal to the Output Word Rate. SCLK should be equal to the input sample rate, which is equal to OCLKD/2. Other SCLK frequencies are possible, but may degrade dynamic range because of interference effects. Data bits are clocked out via the SDATA pin using the SCLK and L/$\overline{R}$ inputs. The rising edge of SCLK causes the ADC to

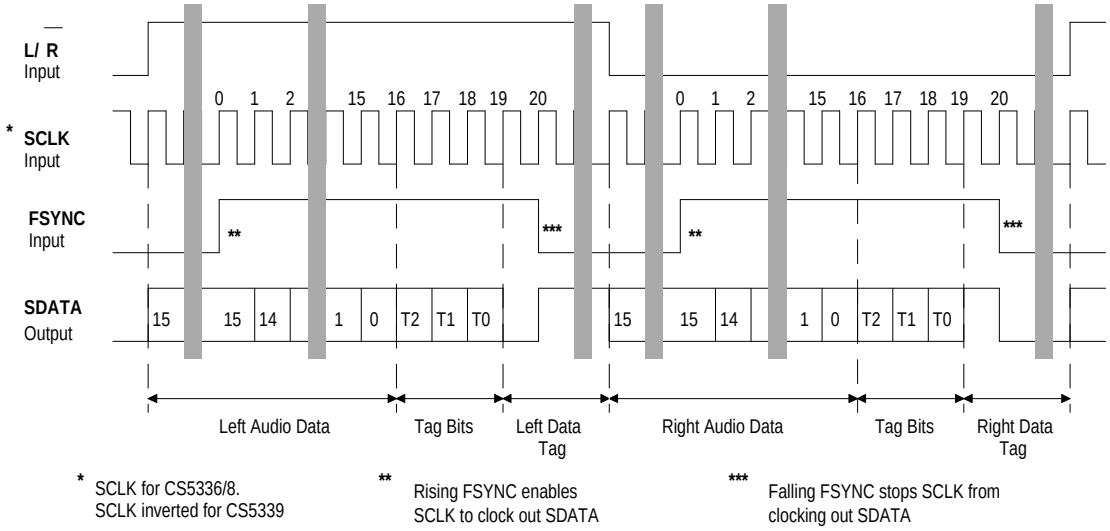


Figure 5. Data Output Timing - SLAVE Mode, FSYNC controlled

output each bit, except the MSB, which is clocked out by the L/$\overline{R}$ edge. As shown in Figure 4, when FSYNC is high, serial data bits are clocked immediately following the L/$\overline{R}$ edge.

In SLAVE mode with FSYNC controlled, as shown in Figure 5, when FSYNC is low, only the MSB is clocked out after the L/$\overline{R}$ edge. With FSYNC low, SCLK is ignored. When it is desired to start clocking out data, bring FSYNC high which enables SCLK to start clocking out data. Bringing FSYNC low will stop the data being clocked out. This feature is particularly useful to position in time the data bits onto a common serial bus.

The serial nature of the output data results in the left and right data words being read at different times. However, the words within an L/$\overline{R}$ cycle represent simultaneously sampled analog inputs.

In all modes, additional bits are output after the data bits: 3 tag bits and a left/right indicator. The tag bits indicate a near-to-clipping input condition for the data word to which the tag bits are attached. Table 2 shows the relationship between input level and the tag bit values. The serial bit immediately following the tag bits is 0 for the left channel, and 1 for the right channel. The remaining bits before the next L/$\overline{R}$ edge will be 1's for the left channel and 0's for the right channel. Normally, the tag bits are separated from the audio data by the digital signal processor. However, if the tag bits are interpreted as audio data, their position below the LSB would result as a very small dc offset.

In all modes, SCLK is shown for the CS5336 and CS5338, where data bits are clocked out on rising edges. SCLK is inverted for the CS5339.

Input Level	T2	T1	T0
1.375 x FS	1	1	1
1.250 x FS to 1.375 x FS	1	1	0
1.125 x FS to 1.250 x FS	1	0	1
1.000 x FS to 1.125 x FS	1	0	0
-1.006dB to 0.000dB	0	1	1
-3.060dB to -1.006dB	0	1	0
-6.000dB to -3.060dB	0	0	1
< -6.000dB	0	0	0

FS = Full Scale (0dB) Input

Table 2. Tag Bit Definition

Certain serial modes align well with various interface requirements. A CS5339 in MASTER mode, with an inverted L/$\overline{R}$ signal, generates I^2S (Philips) compatible timing. A CS5336 in MASTER mode, using FSYNC, interfaces well with a Motorola DSP56000. A CS5336 in SLAVE mode emulates a CS5326 style interface, and also links up to a DSP56000 in network mode.

Analog Connections

The analog inputs are presented to the modulators via the AINR and AINL pins. The analog input signal range is determined by the internal voltage reference value, which is typically -3.68 volts. The input signal range therefore is typically ± 3.68 volts.

The ADC samples the analog inputs at 3.072 MHz for a 12.288 MHz ICLKD (CMODE low). For the CS5336, the digital filter rejects all noise between 26 kHz and (3.072 MHz-26 kHz). For the CS5338 and CS5339, the digital filter rejects all noise between 28 kHz and (3.072 MHz-28 kHz). However, the filter will not reject frequencies right around 3.072 MHz (and multiples of 3.072 MHz). Most audio signals do not have significant energy at 3.072 MHz. Nevertheless, a 51 Ω resistor in series with the analog input, and a 10 nF NPO or COG capacitor to ground will attenuate any noise energy at 3.072 MHz, in addition to providing the optimum source impedance for the modulators. The use of capacitors which have a large voltage coefficient (such as general purpose ceramics) should be avoided since these can degrade signal linearity. If active circuitry precedes the ADC, it is recommended that the above RC filter is placed between the active circuitry and the AINR and AINL pins. The above example frequencies scale linearly with output word rate.

The on-chip voltage reference output is brought out to the VREF pin. A 10 µF electrolytic capacitor in parallel with a 0.1 µF ceramic capacitor attached to this pin eliminates the effects of high frequency noise. Note the negative value of VREF when using polarized capacitors. No load current may be taken from the VREF output pin.

The analog input level used as zero during the offset calibration period (described later) is input on the ZEROL and ZEROR pins. Typically, these pins are directly attached to AGND. For the ultimate in offset nulling, networks can be attached to ZEROR and ZEROL whose impedances match the impedances present on AINL and AINR.

Power-Down and Offset Calibration

The ADC has a power-down mode wherein typical consumption drops to 150 µW. In addition, exiting the power-down state initiates an offset calibration procedure.

APD and DPD are the analog and digital power-down pins. When high, they place the analog and digital sections in the power-down mode. Bringing these pins low takes the part out of power-down mode. DPD going low initiates a calibration cycle. If not using the power down feature, APD should be tied to AGND. When using the power down feature, DPD and APD may be tied together if the capacitor on VREF is not

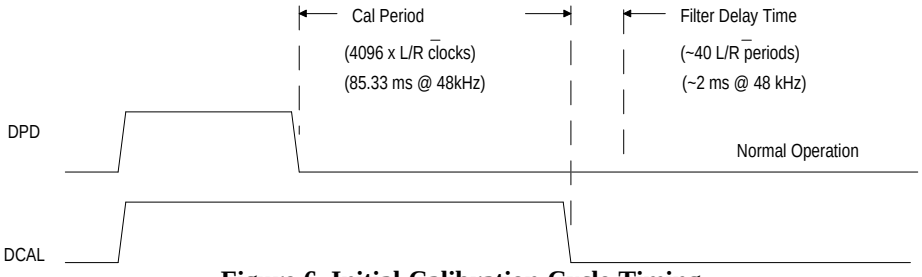


Figure 6. Initial Calibration Cycle Timing

greater than 10 µF, as stated in the "Power-Up Considerations" section.

During the offset calibration cycle, the digital section of the part measures and stores the value of the calibration input of each channel in registers. The calibration input value is subtracted from all future outputs. The calibration input may be obtained from either the analog input pins (AINL and AINR) or the zero pins (ZEROL and ZEROR) depending on the state of the ACAL pin. With ACAL low, the analog input pin voltages are measured, and with ACAL high, the zero pin voltages are measured.

As shown in Figure 6, the DCAL output is high during calibration, which takes 4096 L/$\overline{R}$ clock cycles. If DCAL is connected to the ACAL input, the calibration routine will measure the voltage on ZEROR and ZEROL. These should be connected directly to ground or through a network matched to that present on the analog input pins. Internal offsets of each channel will thus be measured and subsequently subtracted.

Alternatively, ACAL may be permanently connected low and DCAL utilized to control a multiplexer which grounds the user's front end. In this case, the calibration routine will measure and store not only the internal offsets but also any offsets present in the front end input circuitry.

During calibration, the digital output of both channels is forced to a 2's complement zero. Subtraction of the calibration input from conversions after calibration substantially reduces any power-on click that might otherwise be experienced. A short delay of approximately 40 output words will occur following calibration for the digital filter to begin accurately tracking audio band signals.

Power-up Considerations

Upon initial application of power to the supply pins, the data in the calibration registers will be indeterminate. A calibration cycle should always be initiated after application of power to replace potentially large values of data in these registers with the correct values.

The modulators settle very quickly (a matter of microseconds) after the analog section is powered on, either through the application of power, or by exiting the power-down mode. The voltage reference can take a much longer time to reach a final value due to the presence of large external capacitance on the VREF pin; allow approximately 5 ms/µF. The calibration period is long enough to allow the reference to settle for capacitor values of up to 10 µF. If a larger capacitor is used, additional time between APD going low and DPD going low should be allowed for VREF settling before a calibration cycle is initiated.

Grounding and Power Supply Decoupling

As with any high resolution converter, the ADC requires careful attention to power supply and grounding arrangements if its potential performance is to be realized. Figure 1 shows the recommended power arrangements, with VA+, VA- and VL+ connected to a clean ± 5 V supply. VD+, which powers the digital filter, may be run from the system +5V logic supply, provided that it is not excessively noisy (< ± 50 mV pk-to-pk). Alternatively, VD+ may be powered from VA+ via a ferrite bead. In this case, no additional devices should be powered from VD+. Analog ground and digital ground should be connected together near to where the supplies are brought onto the printed circuit board. Decoupling capacitors should be as near to the ADC as possible, with the low value ceramic capacitor being the nearest.

The printed circuit board layout should have separate analog and digital regions and ground planes,

with the ADC straddling the boundary. All signals, especially clocks, should be kept away from the VREF pin in order to avoid unwanted coupling into the modulators. The VREF decoupling capacitors, particularly the 0.1 µF, must be positioned to minimize the electrical path from VREF to Pin 1 AGND and to minimize the path between VREF and the capacitors. An evaluation board is available which demonstrates the optimum layout and power supply arrangements, as well as allowing fast evaluation of the ADC.

To minimize digital noise, connect the ADC digital outputs only to CMOS inputs.

Synchronization of Multiple CS5336/8/9

In systems where multiple ADC's are required, care must be taken to insure that the ADC internal clocks are synchronized between converters to insure simultaneous sampling. In the absence of this synchronization, the sampling difference could be one ICLKD period which is typically 81.4 nsec for a 48 kHz sample rate.

SLAVE MODE

Synchronous sampling in the slave mode is achieved by connecting all DPD and APD pins to a single control signal and supplying the same ICLKD and L/$\overline{R}$ to all converters.

MASTER MODE

The internal counters of the CS5336/8/9 are reset during DPD/APD high and will start simultaneously by insuring that the release of DPD/APD for all converters is internally latched on the same rising edge of ICLKD. This can be achieved by connecting all DPD/APD pins to the same control signal and insuring that the DPD/APD falling edge occurs outside a ±30 ns window either side of an ICLKD rising edge.

PERFORMANCE

FFT Tests

For FFT based tests, a very pure sine wave is presented to the ADC, and an FFT analysis is performed on the output data. The resulting spectrum is a measure of the performance of the ADC.

Figure 7 shows the spectral purity of the CS5336 with a 1 kHz, -10 dB input. Notice the low noise floor, the absence of any harmonic distortion, and the Dynamic Range value of 95.41 dB.

Figure 8 shows the CS5336 high frequency performance. The input signal is a -10 dB, 9 kHz sine wave. Notice the small 2nd harmonic at 110 dB down.

Figure 9 shows the low-level performance of the CS5336. Notice the lack of any distortion components. Traditional R-2R ladder based ADC's can have problems with this test, since differential non-linearities around the zero point become very significant. Figure 10 shows the same very low input amplitude performance, but at 9kHz input frequency.

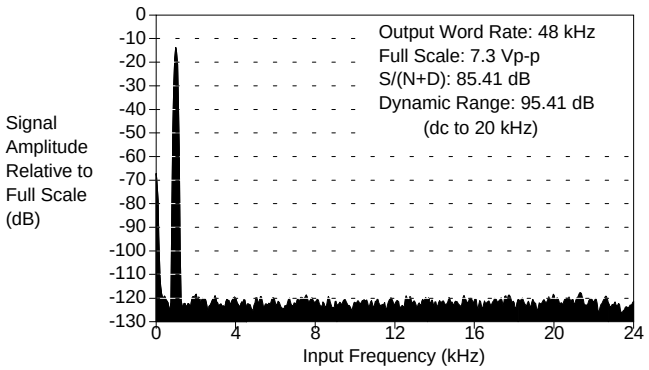


Figure 7. CS5336 FFT Plot with -10 dB, 1 kHz Input

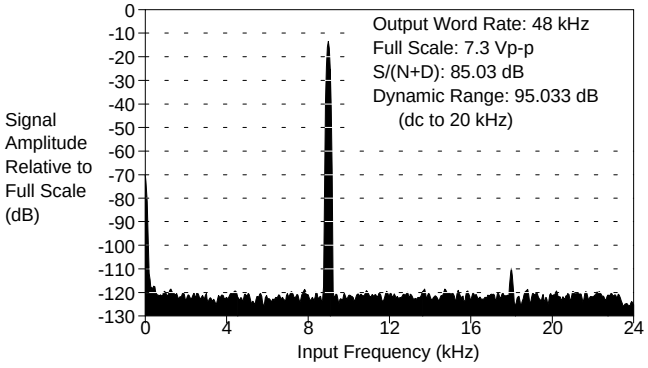


Figure 8. CS5336 FFT Plot with -10 dB, 9 kHz Input

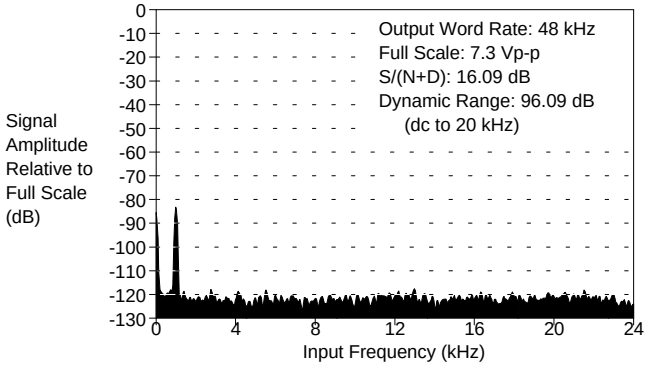


Figure 9. CS5336 FFT Plot with -80 dB, 1 kHz Input

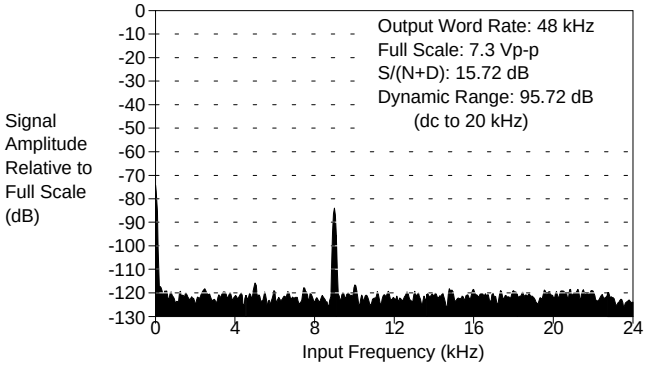


Figure 10. CS5336 FFT Plot with -80 dB, 9 kHz Input

DNL Tests

A Differential Non-Linearity test is also shown. Here, the converter is presented with a linear ramp signal. The resulting output codes are counted to yield a number which is proportional to the codewidth. A plot of codewidth versus code graphically illustrates the uniformity of the codewidths. Figure 11 shows the excellent Differential Non-Linearity of the CS5336. This plot displays the worst case positive and negative errors in each of 512 groups of 128 codes. Codewidths typically are within ± 0.2 LSB's of ideal. A delta-sigma modulator based ADC has no inherent mechanism for generating DNL errors. The residual small deviations shown in Figure 11 are a result of noise. Nevertheless, the performance shown is extremely good, and is superior to typical R-2R ladder based designs.

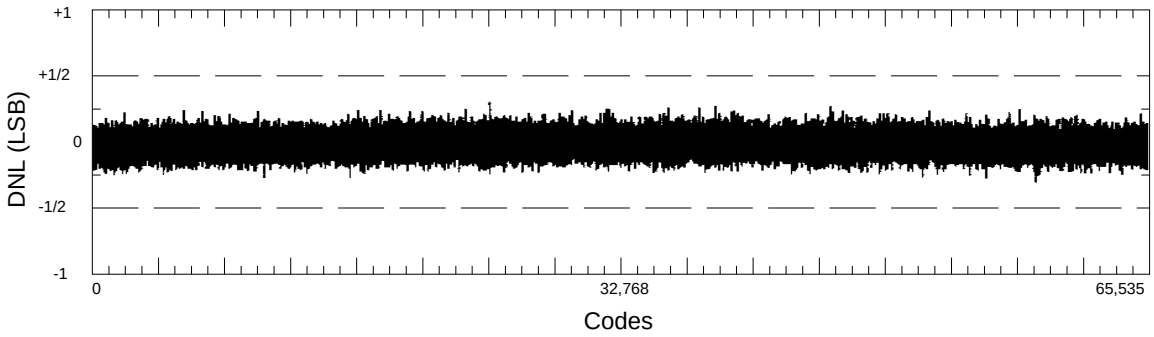


Figure 11. CS5336 Differential Non-Linearity Plot

Digital Filter

Figures 12 through 17 show the performance of the digital filter included in the ADC. All the plots assume an output word rate of 48 kHz. The filter frequency response will scale precisely with changes in output word rate. The passband ripple is flat to ± 0.01 dB maximum. Stopband rejection is greater than 80 dB.

Figures 12,14 &16 show the CS5338 and CS5339 filter characteristics. Figure 17 is an expanded view of the transition band.

Figures 13,15 & 17 show the CS5336 filter characteristics. Figure 17 is an expanded view of the transition band.

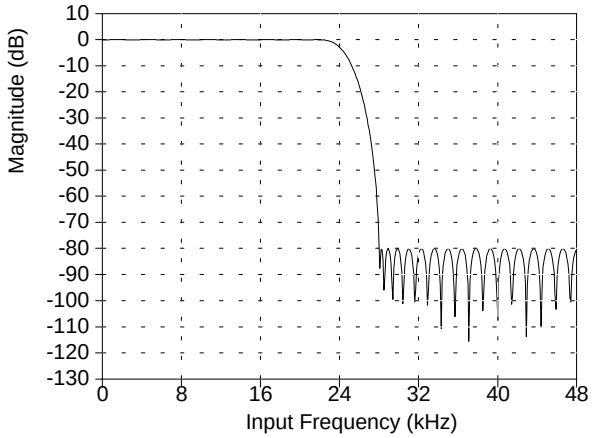


Figure 12. CS5338/9 Digital Filter Stopband Rejection

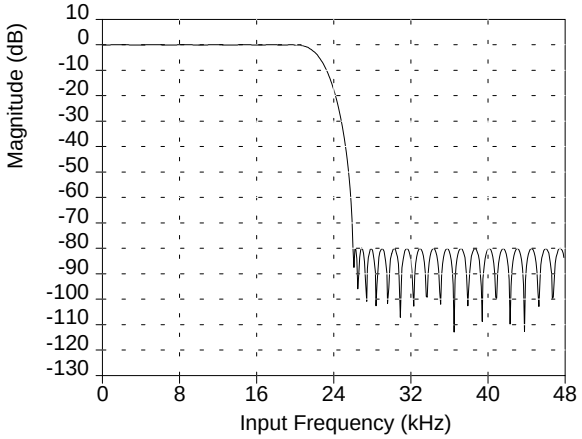


Figure 13. CS5336 Digital Filter Stopband Rejection

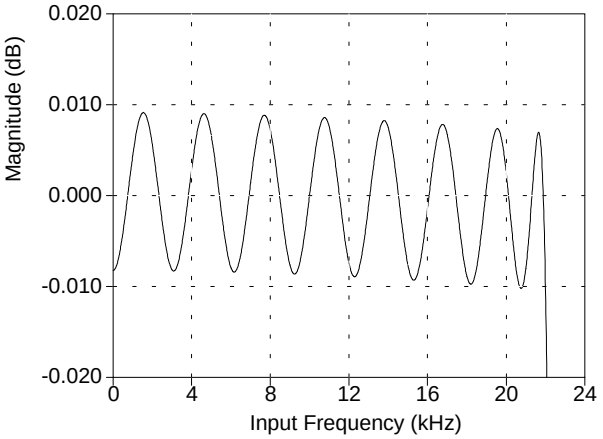


Figure 14. CS5338/9 Digital Filter Passband Ripple

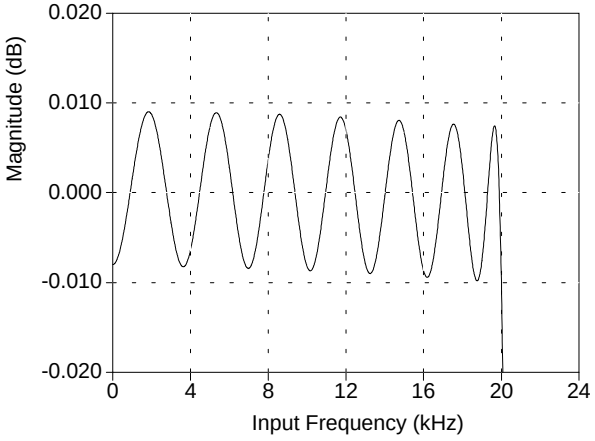


Figure 15. CS5336 Digital Filter Passband Ripple

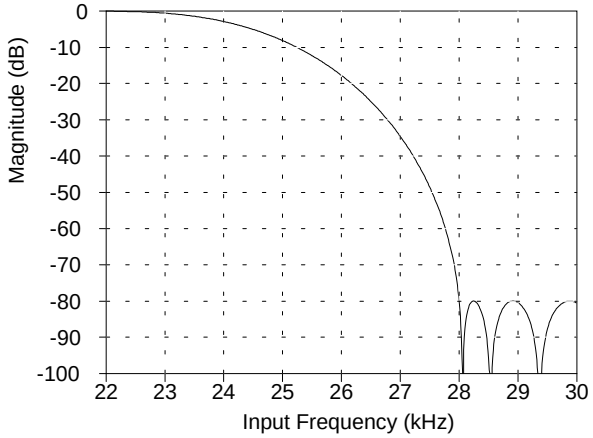


Figure 16. CS5338/9 Digital Filter Transition Band

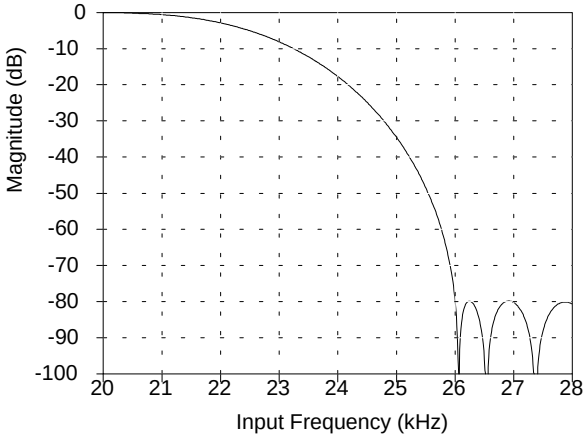
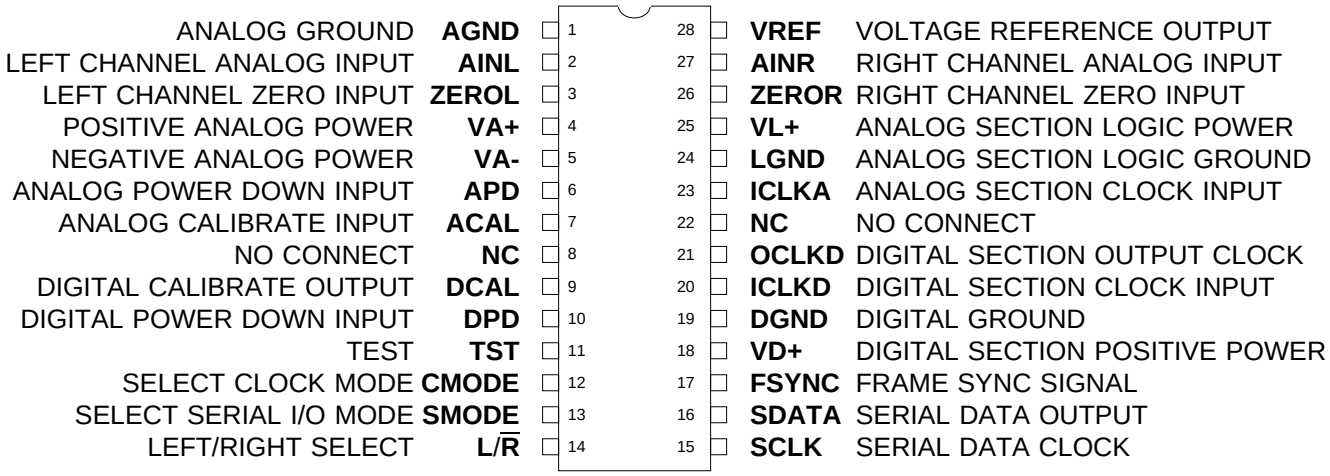


Figure 17. CS5336 Digital Filter Transition Band

PIN DESCRIPTIONS



Power Supply Connections

VA+ - Positive Analog Power, PIN 4.

Positive analog supply. Nominally +5 volts.

VL+ - Positive Logic Power, PIN 25.

Positive logic supply for the analog section. Nominally +5 volts.

VA- - Negative Analog Power, PIN 5.

Negative analog supply. Nominally -5 volts.

AGND - Analog Ground, PIN 1.

Analog ground reference.

LGND - Logic Ground, PIN 24

Ground for the logic portions of the analog section.

VD+ - Positive Digital Power, PIN 18.

Positive supply for the digital section. Nominally +5 volts.

DGND - Digital Ground, PIN 19.

Digital ground for the digital section.

Analog Inputs

AINL, AINR - Left and Right Channel Analog Inputs, PINS 2, 27

Analog input connections for the left and right input channels. Nominally ±3.68 volts full scale.

ZEROL, ZEROR - Zero Level Inputs for Left and Right Channels, PINS 3, 26.

Analog zero level inputs for the left and right channels. The levels present on these pins can be used as zero during the offset calibration cycle. Normally connected to AGND, optionally through networks matched to the analog input networks.

Analog Outputs

VREF - Voltage Reference Output, PIN 28.

Nominally -3.68 volts. Normally connected to a 0.1µF ceramic capacitor in parallel with a 10µF or larger electrolytic capacitor. Note the negative output polarity.

Digital Inputs

ICLKA - Analog Section Input Clock, PIN 23.

This clock is internally divided by 2 to set the modulators' sample rate. Sampling rates, output rates, and digital filter characteristics scale to ICLKA frequency. ICLKA frequency is 128 X the output word rate. For example, 6.144 MHz ICLKA corresponds to an output word rate of 48 kHz per channel. Normally connected to OCLKD.

ICLKD - Digital Section Input Clock, PIN 20.

This is the clock which runs the digital filter. ICLKD frequency is determined by the required output word rate and by the CMODE pin. If CMODE is low, ICLKD frequency should be 256 X the desired output word rate. If CMODE is high, ICLKD should be 384 X the desired output word rate. For example, with CMODE low, ICLKD should be 12.288 MHz for an output word rate of 48 kHz. This clock also generates OCLKD, which is always 128 X the output word rate.

APD - Analog Power Down, PIN 6.

Analog section power-down command. When high, the analog circuitry is in power-down mode. APD is normally connected to DPD when using the power down feature. If power down is not used, then connect APD to AGND.

DPD - Digital Power Down, PIN 10

Digital section power-down command. Bringing DPD high puts the digital section into power-down mode. Upon returning low, the ADC starts an offset calibration cycle. This takes 4096 $L/\overline{R}$ periods (85.33 ms with a 12.288 MHz ICLKD). DCAL is high during the calibrate cycle and goes low upon completion. DPD is normally connected to APD when using the power down feature. A calibration cycle should always be initiated after applying power to the supply pins.

ACAL - Analog Calibrate, PIN 7.

Analog section calibration command. When high, causes the left and right channel modulator inputs to be internally connected to ZEROL and ZEROR inputs respectively. May be connected to DCAL.

CMODE - Clock Mode Select, PIN 12.

CMODE should be tied low to select an ICLKD frequency of 256 X the output word rate. CMODE should be tied high to select an ICLKD frequency of 384 X the output word rate.

SMODE - Serial Interface Mode Select, PIN 13.

SMODE should be tied high to select serial interface master mode, where SCLK, FSYNC and L/$\overline{R}$ are all outputs, generated by internal dividers operating from ICLKD. SMODE should be tied low to select serial interface slave mode, where SCLK, FSYNC and L/$\overline{R}$ are all inputs. In slave mode, L/$\overline{R}$, FSYNC and SCLK need to be derived from ICLKD using external dividers.

Digital Outputs

SDATA - Serial Data Output, PIN 16.

Audio data bits are presented MSB first, in 2's complement format. Additional tag bits, which indicate input overload and left/right channel data, are output immediately following each audio data word.

DCAL - Digital Calibrate Output, PIN 9.

DCAL rises immediately upon entering the power-down state (DPD brought high). It returns low 4096 L/$\overline{R}$ periods after leaving the power down state (DPD brought low), indicating the end of the offset calibration cycle (which = 85.33 ms with a 12.288 MHz ICLKD). May be connected to ACAL.

OCLKD - Digital Section Output Clock, PIN 21.

OCLKD is always 128 X the output word rate. Normally connected to ICLKA.

Digital Inputs or Outputs

SCLK - Serial Data Clock, PIN 15.

Data is clocked out on the rising edge of SCLK for the CS5336 and CS5338. Data is clocked out on the falling edge of SCLK for the CS5339.

In master mode (SMODE high), SCLK is a continuous output clock at 64 X the output word rate.

In slave mode (SMODE low), SCLK is an input, which requires a continuously supplied clock at any frequency from 32 X to 128 X the output word rate (64 X is preferred). When FSYNC is high, SCLK clocks out serial data, except for the MSB which appears on SDATA when L/$\overline{R}$ changes.

L/$\overline{R}$ - Left/Right Select, PIN 14.

In master mode (SMODE high), L/$\overline{R}$ is an output whose frequency is at the output word rate. L/$\overline{R}$ edges occur 1 SCLK cycle before FSYNC rises. When L/$\overline{R}$ is high, left channel data is on SDATA, except for the first SCLK cycle. When L/$\overline{R}$ is low, right channel data is on SDATA, except for the first SCLK cycle. The MSB data bit appears on SDATA one SCLK cycle after L/$\overline{R}$ changes.

In slave mode (SMODE low), L/$\overline{R}$ is an input which selects the left or right channel for output on SDATA. The rising edge of L/$\overline{R}$ starts the MSB of the left channel data. L/$\overline{R}$ frequency must be equal to the output word rate.

Although the outputs of each channel are transmitted at different times, the two words in an L/$\overline{R}$ cycle represent simultaneously sampled analog inputs.

FSYNC - Frame Synchronization Signal, PIN 17.

In master mode (SMODE high), FSYNC is an output which goes high coincident with the start of the first SDATA bit (MSB) and falls low immediately after the last SDATA audio data bit (LSB).

In slave mode (SMODE low), FSYNC is an input which controls the clocking out of the data bits on SDATA. FSYNC is normally tied high, which causes the data bits to be clocked out immediately following L/$\overline{R}$ transitions. If it is desired to delay the data bits from the L/$\overline{R}$ edge, then FSYNC must be low during the delay period. Bringing FSYNC high will then enable the clocking out of the SDATA bits. Note that the MSB will be clocked out based on the L/$\overline{R}$ edge, independent of the state of FSYNC.

Miscellaneous

NC - No Connection, PINS 8, 22.

These two pins are bonded out to test outputs. They must not be connected to any external component or any length of PC trace.

TST -Test Input, PIN 11.

Allows access to the ADC test modes, which are reserved for factory use. Must be tied to DGND.

PARAMETER DEFINITIONS

Resolution - The total number of possible output codes is equal to $2^{N,}$ where N = the number of bits in the output word for each channel.

Dynamic Range - Full scale (RMS) signal to broadband noise ratio. The broadband noise is measured over the specified bandwidth, and with an input signal 60dB below full-scale. Units in decibels.

Signal-to-(Noise plus Distortion) Ratio - The ratio of the rms value of the signal to the rms sum of all other spectral components over the specified bandwidth (typically 10 Hz to 20 kHz), including distortion components. Expressed in decibels.

Total Harmonic Distortion - The ratio of the rms sum of all harmonics up to 20 kHz to the rms value of the signal. Units in percent.

Interchannel Phase Deviation - The difference between the left and right channel sampling times.

Interchannel Isolation - A measure of crosstalk between the left and right channels. Measured for each channel at the converter's output with the input under test grounded and a full-scale signal applied to the other channel. Units in decibels.

Interchannel Gain Mismatch - The gain difference between left and right channels. Units in decibels.

Gain Error - The deviation of the measured full scale amplitude from the ideal full scale amplitude value.

Gain Drift - The change in gain value with temperature. Units in ppm/°C.

Bipolar Offset Error - The deviation of the mid-scale transition (111...111 to 000...000) from the ideal (1/2 LSB below AGND). Units in LSBs.

REFERENCES

1) "A Stereo 16-bit Delta-Sigma A/D Converter for Digital Audio" by D.R. Welland, B.P. Del Signore, E.J. Swanson, T. Tanaka, K. Hamashita, S. Hara, K. Takasuka. Paper presented at the 85th Convention of the Audio Engineering Society, November 1988.

2) " The Effects of Sampling Clock Jitter on Nyquist Sampling Analog-to-Digital Converters, and on Oversampling Delta Sigma ADC's" by Steven Harris. Paper presented at the 87th Convention of the Audio Engineering Society, October 1989.

3) " An 18-Bit Dual-Channel Oversampling Delta-Sigma A/D Converter, with 19-Bit Mono Application Example" by Clif Sanchez. Paper presented at the 87th Convention of the Audio Engineering Society, October 1989.

Ordering Guide

Model	Resolution	Passband	SCLK	Temperature	Package
CS5336-KP	16-bits	22 kHz	↑ active	0°C to 70 °C	28-pin Plastic DIP
CS5336-BP	16-bits	22 kHz	↑ active	-40 to +85 °C	28-pin Plastic DIP
CS5338-KP	16-bits	24 kHz	↑ active	0°C to 70 °C	28-pin Plastic DIP
CS5339-KP	16-bits	24 kHz	↓ active	0°C to 70 °C	28-pin Plastic DIP
CS5336-KS	16-bits	22 kHz	↑ active	0°C to 70 °C	28-pin SOIC
CS5336-BS	16-bits	22 kHz	↑ active	-40 to +85 °C	28-pin SOIC
CS5338-KS	16-bits	24 kHz	↑ active	0°C to 70 °C	28-pin SOIC
CS5339-KS	16-bits	24 kHz	↓ active	0°C to 70 °C	28-pin SOIC
CS5336-TC	16-bits	22 kHz	↑ active	-55 to +125 °C	28-pin Sidebrazed Ceramic DIP

CDB5336	CS5336 Evaluation Board
CDB5338	CS5338 Evaluation Board
CDB5339	CS5339 Evaluation Board

Semiconductor Corporation

CDB5336
CDB5338 CDB5339

Evaluation Board for CS5336, CS5338 & CS5339

Features

- Demonstrates recommended layout and grounding arrangements
- CS8402 Generates AES/EBU, S/PDIF & CP-340 Compatible Digital Audio
- Buffered Serial Output Interface
- 16-Bit Parallel Output Interface
- Digital and Analog Patch Areas
- On-board or externally supplied system timing

General Description

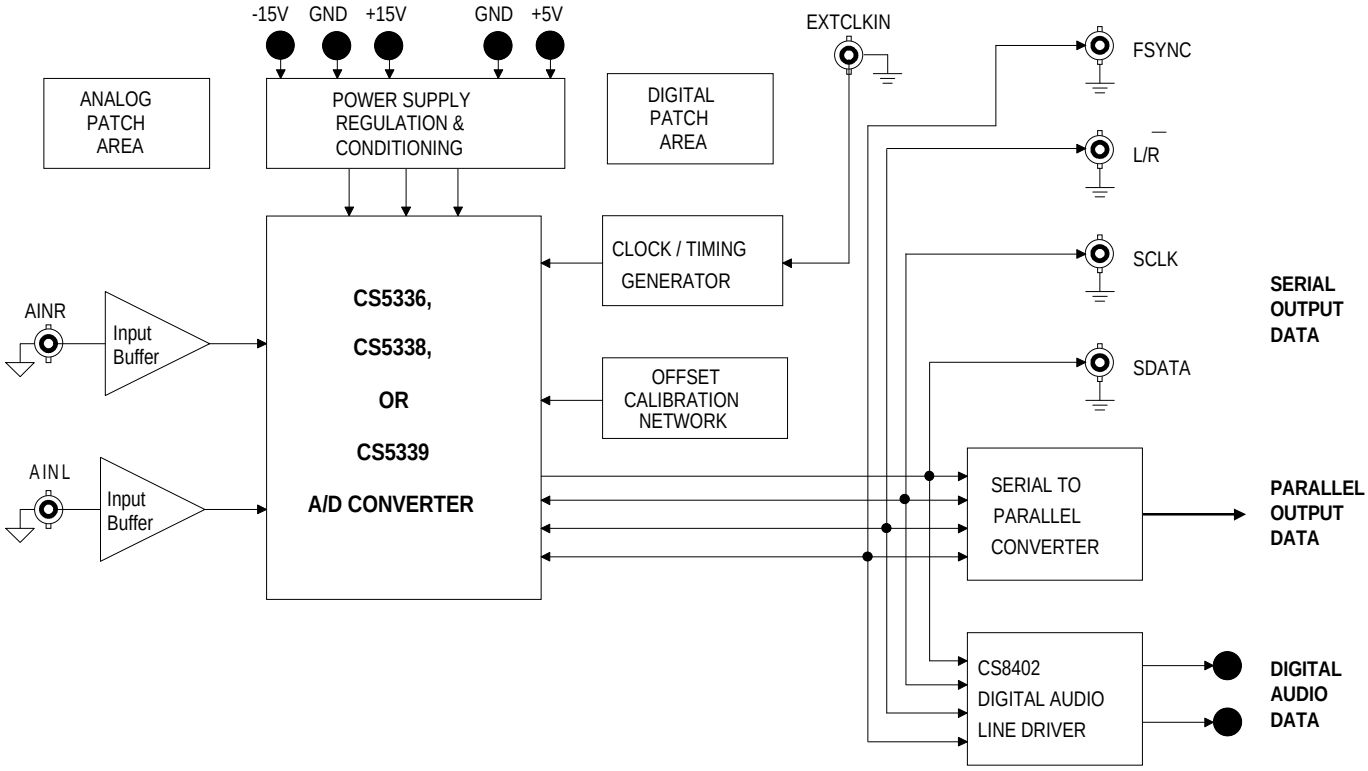
The CDB5336, CDB5338 & CDB5339 evaluation boards allow fast evaluation of the CS5336, CS5338 and CS5339 16-bit, stereo A/D converters. The boards generate all converter timing signals and provide both parallel and serial output interfaces. Evaluation requires a digital signal processor, a low-distortion signal source, and a power supply.

Also included is a CS8402 digital audio transmitter I.C., which can generate AES/EBU, S/PDIF & EIAJ CP-340 compatible audio data.

The evaluation boards may also be configured to accept external timing signals for operation in a user application during system development.

ORDERING INFORMATION:

CDB5336, CDB5338, CDB5339



Crystal Semiconductor Corporation
P.O. Box 17847, Austin, TX 78760
(512) 445 7222 FAX: (512) 445 7581

Power Supply Circuitry

The schematic diagram in Figure 1 shows the evaluation board power supply circuitry. Power is supplied to the evaluation board by five binding posts. The ±5 Volt analog power supply inputs of the converter are derived from ±15 Volts using the voltage regulators U10 and U11. The +5 Volt digital supply for the converter and the discrete logic on the board is provided by the +5V and DGND binding posts. D1, D2 and D4 are transient suppressors which also provide protection from incorrectly connected power supply leads. C25-C28, C30 and C31 provide general power supply filtering for the analog supplies. As shown in Figure 2, C10-C13 provide localized decoupling for the converter VA+ and VA- pins. Note that C13 is connected between VA- and VA+ and not VA- and AGND. Space for a ferrite bead inductor, L1, has been provided so that the board may be modified to power the converter's VD+ input directly from the VA+ supply. Note that the trace connecting the VD+ power to the VD+ of the converter must be broken before L1 may be installed. R5 and C7 low-pass filter the analog logic power supply pin, VL+. The evaluation board uses both an analog and a digital ground plane which are connected at a single point by J1. This ground plane arrangement isolates the board's digital logic from the analog circuitry.

Offset Calibration & Reset Circuit

Figure 1, shows the optional offset calibration circuit provided on the evaluation board. Upon power-up, this circuit provides a pulse on the Analog-to-Digital Converter's DPD pin initiating an offset calibration cycle. Releasing SW1 also initiates an offset calibration cycle. P6 (see Figure 2) selects the signal source used during offset calibration. In the "AIN" position, the AINL and AINR inputs are selected during calibration, while in the "ZERO" position, the ZEROL and ZEROR inputs are selected.

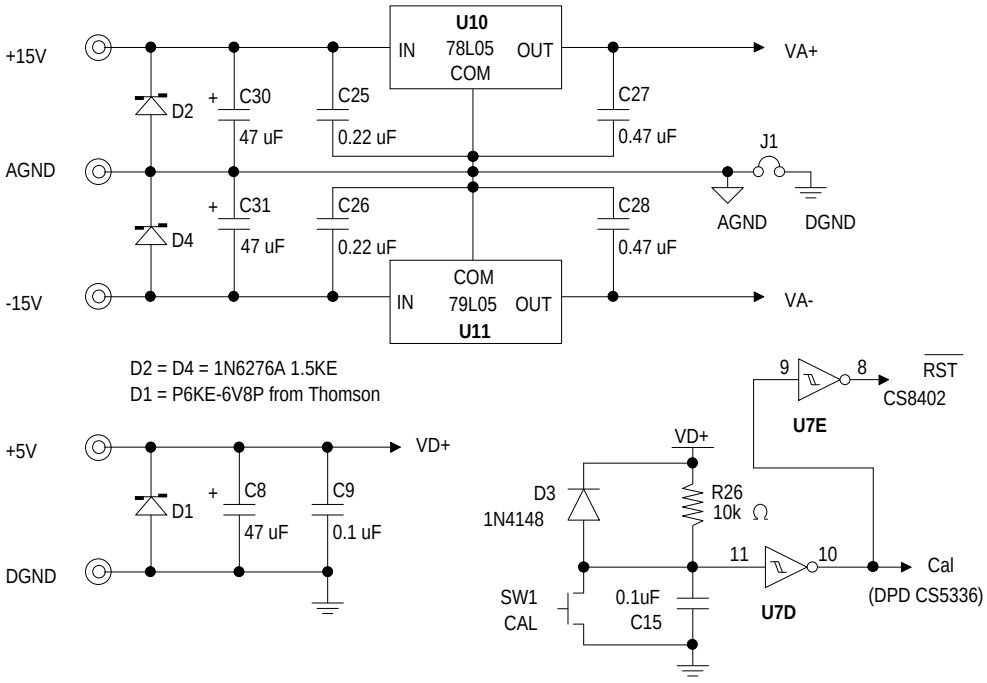


Figure 1. Power Supply and Reset Circuitry

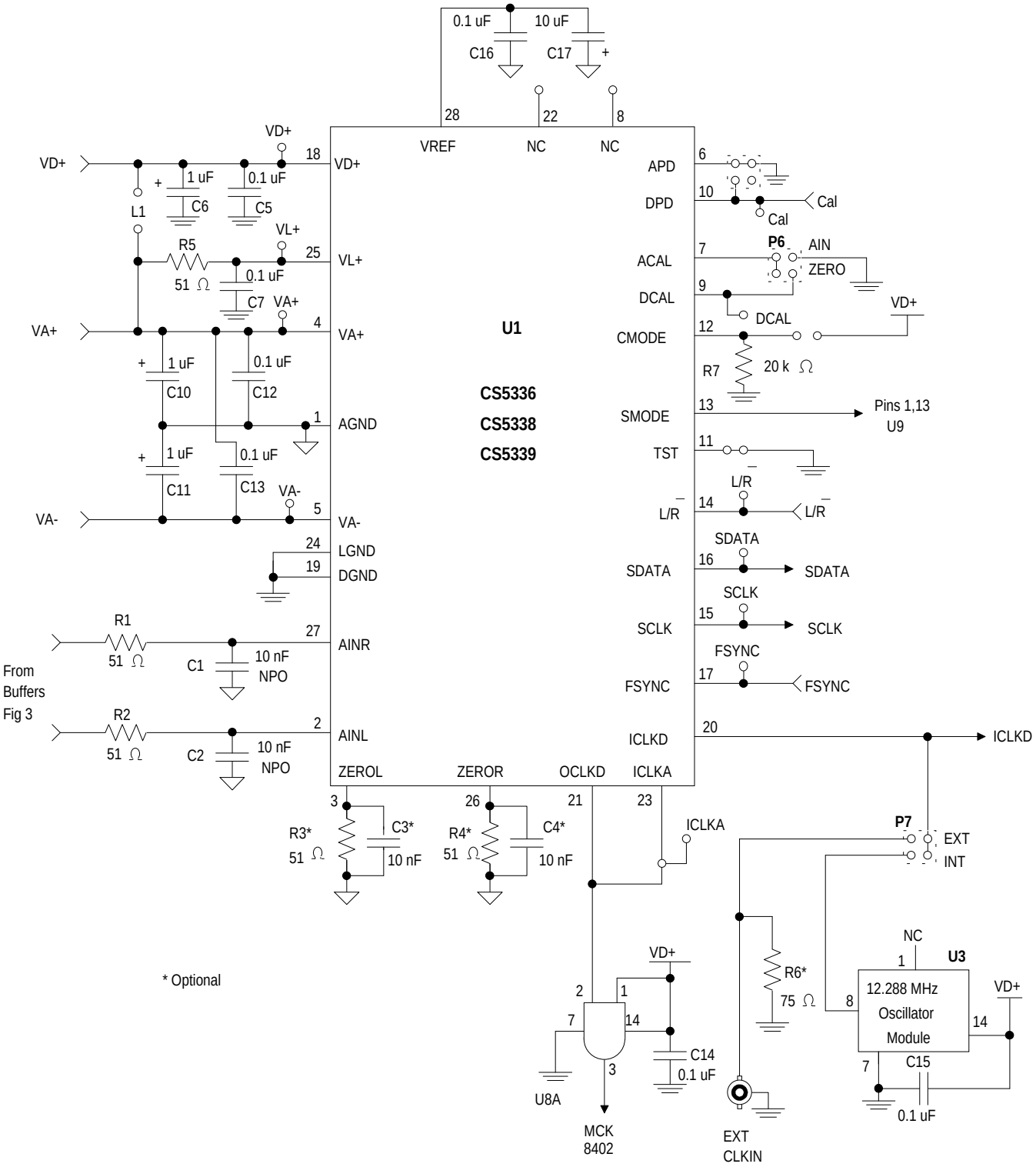


Figure 2 ADC Connections

Analog Inputs

As shown in Figure 2, the analog input signals are connected to the CS5336 via an RC network. R1 and C1 provide antialiasing and optimum source impedance for the right analog input channel while R2 and C2 do so for the left channel. The ZEROR and ZEROL inputs are tied to the analog ground plane on the board as shipped from the factory, but space is provided for an optional RC section on each. These RC sections may be added to model the output impedance of the analog signal source to minimize offset error during calibration.

Figure 3 shows the optional input buffer circuit. This can be used as an example input buffer circuit for your application. If the ADC is driven from a 50Ω source impedance signal generator, the input buffer amplifiers may be bypassed. Place P8 and P9 jumpers in the OUT position, and short circuit R1 and R2. This ensures that the ADC is driven from a 50Ω source resistance. Also remove U13 op-amp, to remove the 1kΩ load impedance.

Timing Generator

P7 selects the master clock source supplied to the ICLKD pin of the converter. As shipped from the factory, P7 is set to the "INT" position to select the 12.288 MHz clock signal provided by U3. An external master clock signal may be connected to the EXTCLKIN connector and selected by placing P7 in the "EXT" position. Note that R6, tied between EXTCLKIN and GND, is available for impedance matching an external clock source. The board is shipped with SMODE high, which selects MASTER timing mode. In this mode, SCLK, L/$\overline{R}$ and FSYNC are all outputs, generated by the converter from ICLKD.

Serial Output Interface

The serial output interface is provided by the SDATA, SCLK, FSYNC and L/$\overline{R}$ BNC connectors on the evaluation board. These out-

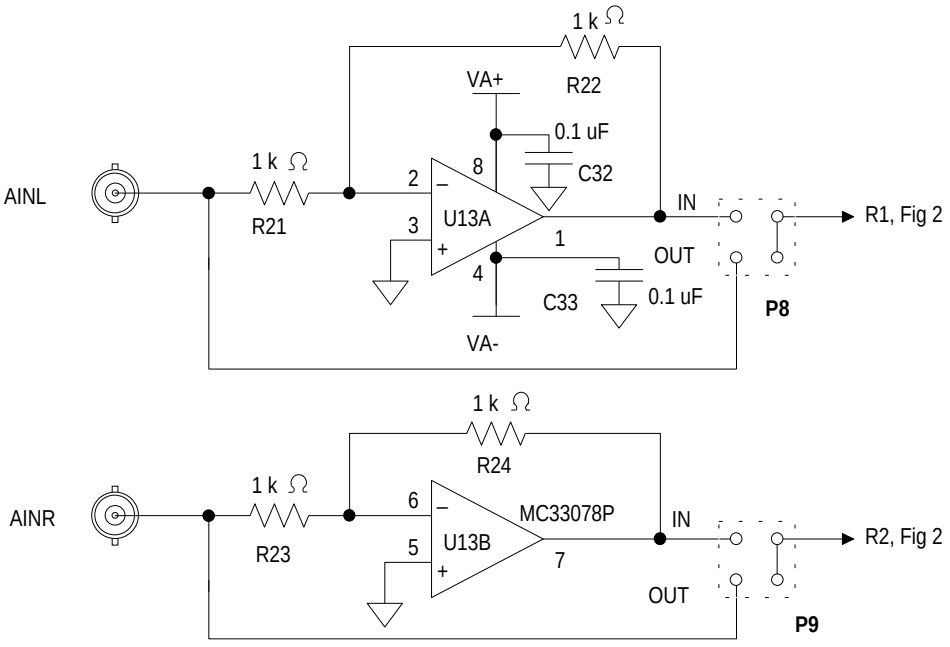


Figure 3. Input Buffer Circuit

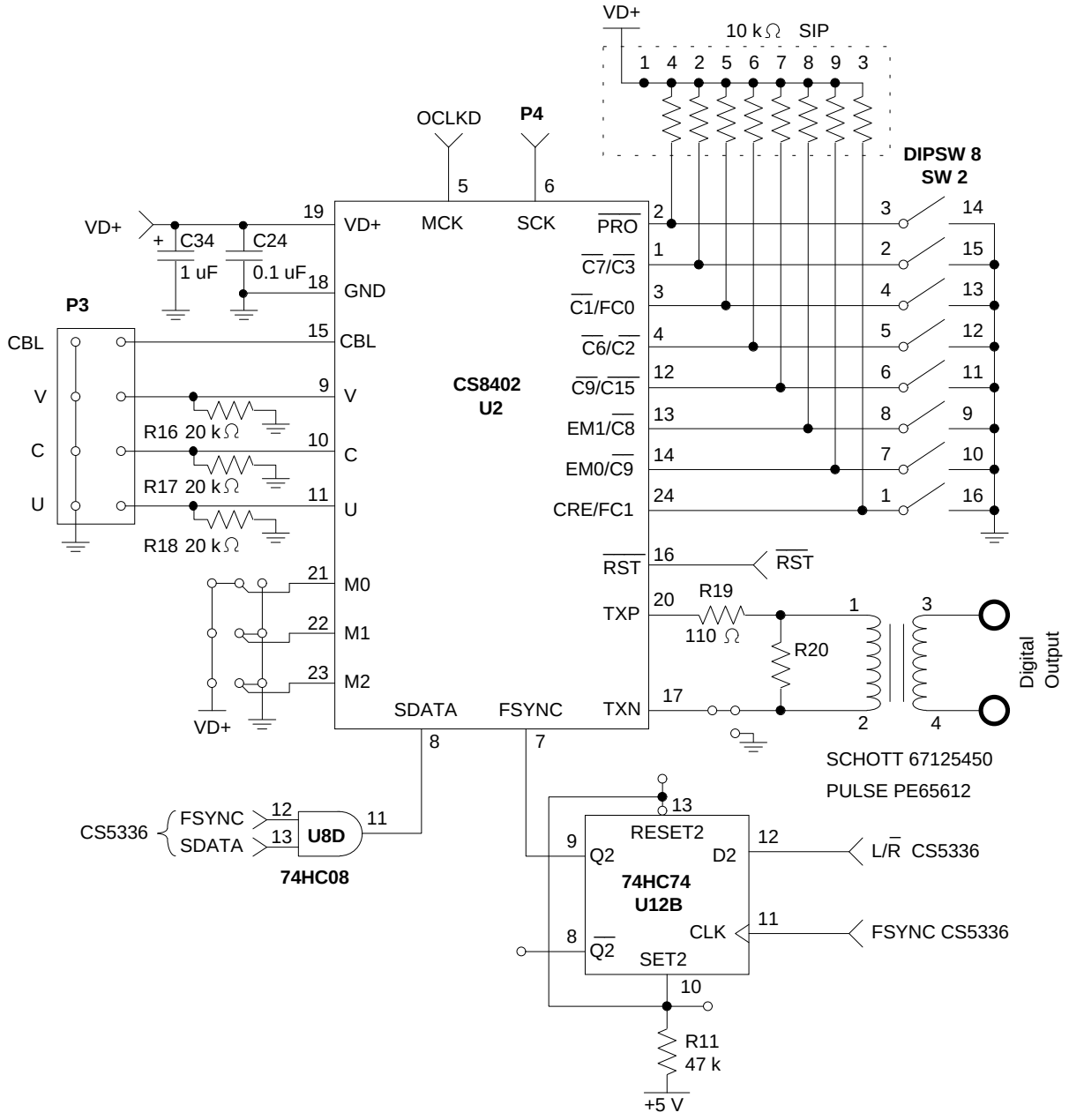


Figure 4. CS8402 Digital Audio Line Driver Connections

puts are buffered, as shown in Figure 5, in order to isolate the converter from the digital signal processor. If slave mode is selected by pulling SMODE low, then U9 (74HC243) will change to the opposite direction, and act as an input buffer. U9 is provided to protect against inadvertent external driving of SCLK, L/$\overline{R}$ and FSYNC while in MASTER mode. U9 is not necessary in your application circuit.

Jumper P4 allows the board to be configured for either the CS5336/38, or the CS5339, which have opposite polarities of SCLK.

Parallel Output Interface

Figure 6 depicts the parallel output interface on the evaluation board. 16-bit words are assembled from the serial data output of the converter. Each bit of serial data is clocked out of the converter

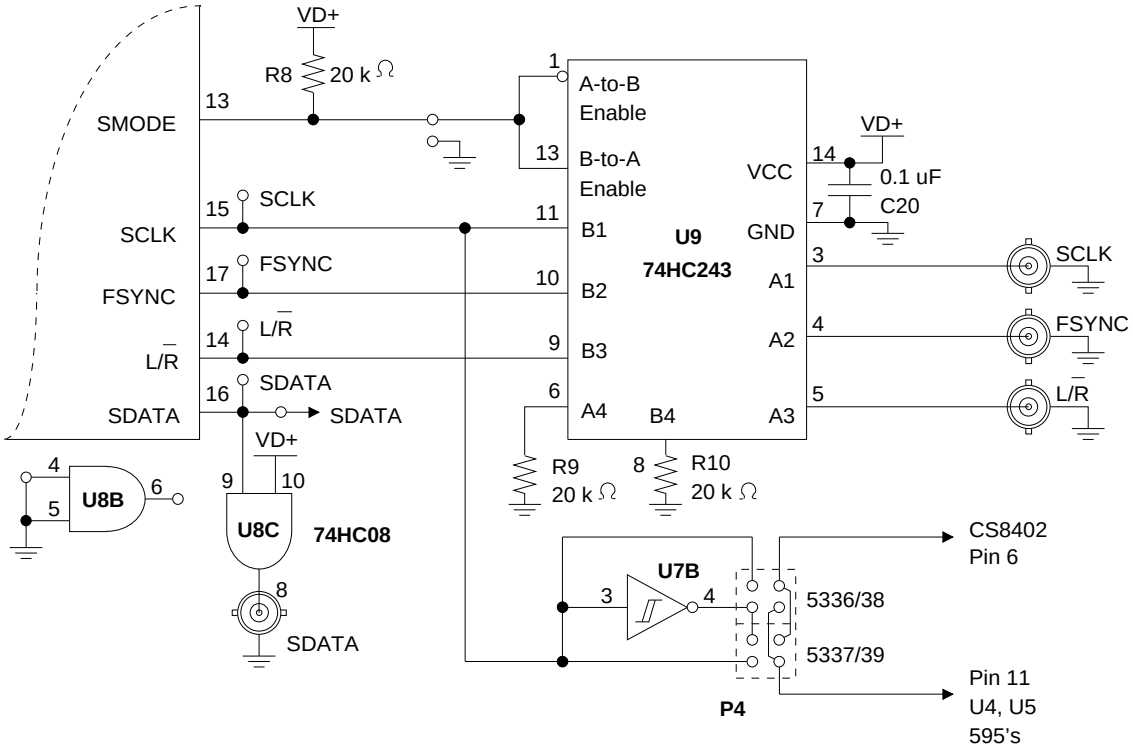


Figure 5. Serial Output Interface

on the rising edge of SCLK and shifted into the 16-bit shift register formed by U4 and U5 on SCLK's falling edge. After all data bits for the selected channel have been shifted into U4 and U5 the data is latched onto P1 by a delayed version of FSYNC.

P5 selects the channel whose output data will be converted to parallel form and presented on P1. With P5 in the "B" (both) position, parallel data from one channel will be presented first with data from the other channel presented subsequently. In the "L" (left) position, only left channel conversions will be presented, while in the "R" (right) position only right channel conversions are presented.

Two interface mechanisms are provided for reading the data from this port. With the first, the edges of L/$\overline{R}$ may be used to clock the parallel data into the digital signal processor. (Set jumper P2 into the L/$\overline{R}$ position.) Alternatively, a handshake protocol implemented with DACK and $\overline{DRDY}$ may be used to transfer data to the signal processor. (Set jumper P2 to the $\overline{DRDY}$ position.) The fall of $\overline{DRDY}$ informs the digital signal processor that a new data word is available. The processor then reads the port and acknowledges the transfer by asserting DACK. Note that $\overline{DRDY}$ will not be asserted again unless DACK is momentarily brought high although new data will continue to be latched onto the port.

Digital Audio Standard Interface

Included on the evaluation board is a CS8402 Digital Audio Line Driver. This device can implement AES/EBU, S/PDIF and EIAJ CP-340 interface standards. Figure 4 shows the schematic for the CS8402. P3 allows the C, U and V bits to be driven from external logic using the CBL output for block synchronization. SW2 provides 8 DIP switches to select various modes and bits for the CS8402. Table 3 lists the settings for the professional mode which is the default setting for the evaluation board from the factory. The third switch selects between professional

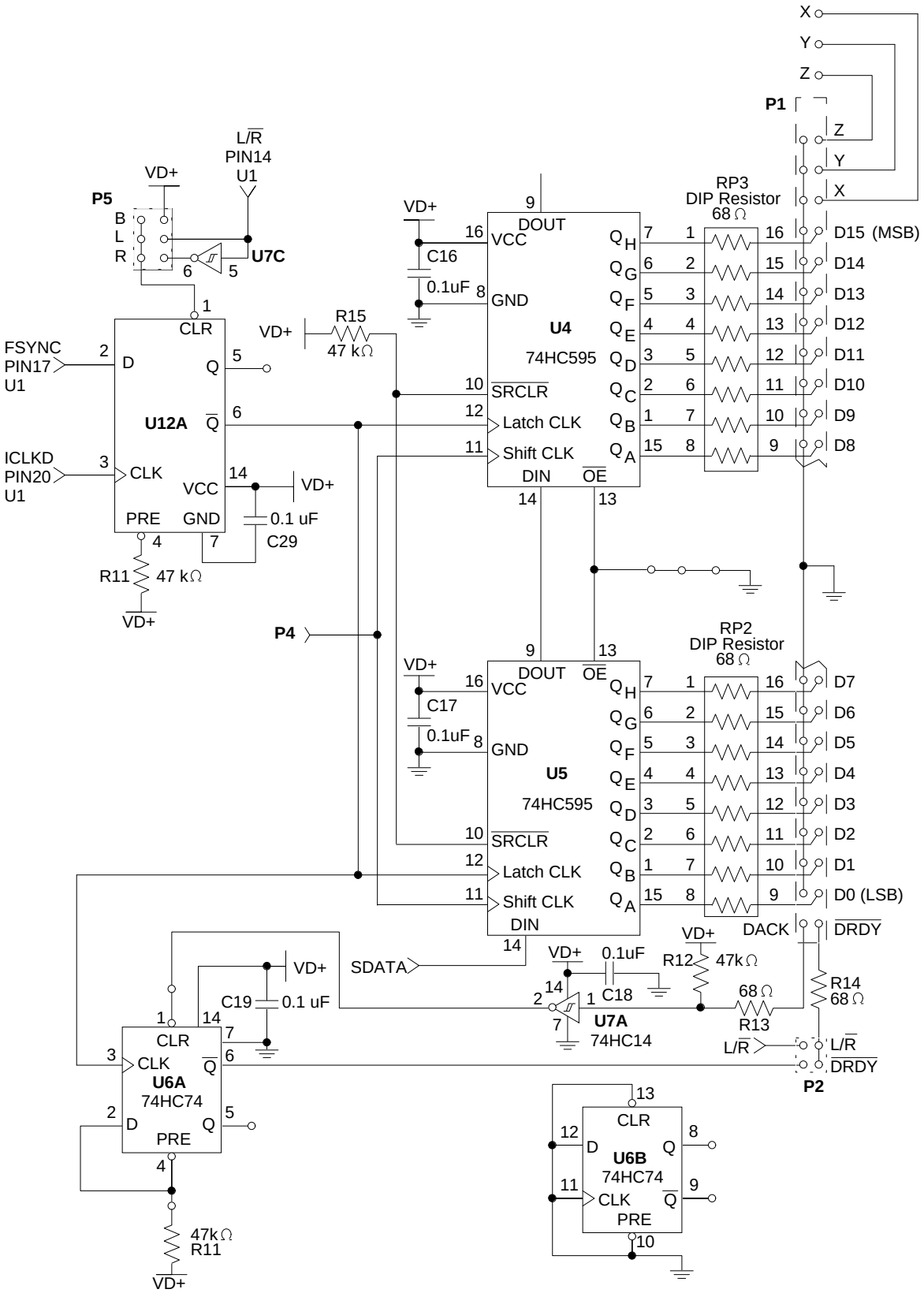


Figure 6. Parallel Output Interface

CONNECTOR	INPUT/OUTPUT	SIGNAL PRESENT
+15	input	+15 Volts from power supply
-15	input	-15 Volts from power supply
AGND	input	analog ground connection from power supply
+5	input	+5V for ADC VD+ and discrete logic
DGND	input	digital ground connection from power supply
AINL	input	left channel analog input
AINR	input	right channel analog input
EXTCLKIN	input	external master clock input
L/$\overline{R}$	output/input	left /right channel signal
SDATA	output	serial output data
SCLK	output/input	serial output clock
FSYNC	output/input	data framing signal
DIGITAL OUTPUT	output	CS8402 digital output via transformer
P3	output/input	CS8402 C,U,V inputs; CBL output
P1	output	parallel output data

Table 1. System Connections

JUMPER	PURPOSE	POSITION	FUNCTION SELECTED
P6	selects offset calibration input source	AIN	AINL and AINR selected during offset calibration
		*ZERO	ZEROL and ZEROR selected during offset calibration
P7	selects master clock source for CS5326 CLKIN	*INT	CLKIN provided by U3
		EXT	CLKIN provided by EXTCLKIN BNC
P5	selects channel for serial to parallel conversion	*L	left channel data presented on P1
		R	right channel data presented on P1
		B	left then right channel data alternately presented on P1
P2	selects L/$\overline{R}$ or $\overline{DRDY}$ as the output status signal presented on P1	*$\overline{DRDY}$	$\overline{DRDY}$ selected to signal the arrival of new data for the selected channel
		L/$\overline{R}$	L/$\overline{R}$ selected
P8, P9	selects optional input buffers	*IN	Buffer amplifier in circuit
		OUT	Buffer amplifier bypassed
P4	selects device type	5337/39	Correct SCLK for CS5337 & CS5339
		5336/38	Correct SCLK for CS5336 & CS5338

* Default setting from factory

Table 2. Jumper Selectable Options

Switch#	0=Closed, 1=Open	Comment
3	$\overline{PRO}$=0	Professional Mode, C0=1 (default)
1	CRE	Local Sample Address Counter & Reliability Flags
default	0 1	Disabled Internally Generated (channel status bytes 14-17 and byte 22)
5, 2	$\overline{C6}$, $\overline{C7}$	C6,C7 - Sample Frequency
default	1 1 1 0 0 1 0 0	00 - Not Indicated - Default to 48 kHz 01 - 48 kHz 10 - 44.1 kHz 11 - 32 kHz
4	$\overline{C1}$	C1 - $\overline{Audio}$
default	1 0	0 - Normal Audio 1 - Non-Audio
6	$\overline{C9}$	C8,C9,C10,C11 - Channel Mode (1 of 4 bits)
default	1 0	0000 - Not indicated - Default to 2-channel 0100 - Stereophonic
8, 7	EM1, EM0	C2,C3,C4 - Emphasis
default	1 1 1 0 0 1 0 0	000 - Not Indicated - default to none 100 - No emphasis 110 - 50/15 µs 111 - CCITT J.17

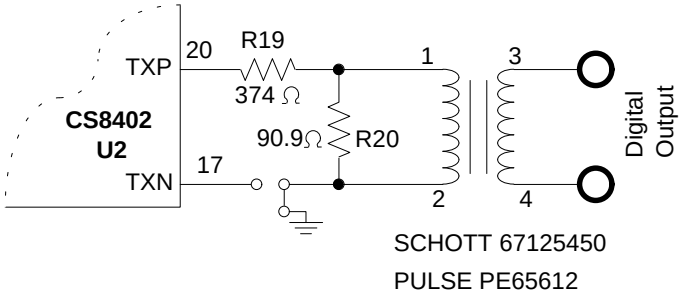
Table 3. CS8402 Switch Definitions - Professional Mode

and consumer modes; however, the CS8402 output to the transformer must be modified, as shown below Table 4, to be compatible with the consumer interface. Table 4 lists the switch settings for consumer mode. If the C input of connector P3 is used, the input bits are logically OR'ed with the appropriate DIP switch bits. In Tables 3 and 4, the 'C' bits listed in the comment section are taken from the Digital Audio Interface specifications. As an example, switch 6 in the professional mode (Table 3) controls $\overline{C9}$ which is the inverse of channel status bit 9 (also listed as byte 1, bit 1 in the CS8402 data sheet). Channel status bit 9 is one of four bits indicating channel mode. Therefore, using DIP switch 6, only two of the available channel modes may be selected. The C input port on connector P3 may be used to select other channel modes. See the CS8401 & CS8402 part data sheet for more information on the operation of the CS8402.

Switch#	0=Closed, 1=Open	Comment
3	$\overline{PRO}$=1	Consumer Mode, C0=0 (Note 1)
1, 4	FC1, FC0	C24,C25,C26,C27 - Sample Frequency (encoded 2 of 4 bits)
	0 0 0 1 1 0 1 1	0000 - 44.1 kHz 0100 - 48 kHz 1100 - 32 kHz 0000 - 44.1 kHz, CD Mode
2	$\overline{C3}$	C3,C4,C5 - Emphasis (1 of 3 bits)
	1 0	000 - None 100 - 50/15 µs
5	$\overline{C2}$	C2 - Copy/Copyright
	1 0	0 - Copy Inhibited/Copyright Asserted 1 - Copy Permitted/Copyright Not Asserted
6	$\overline{C15}$	C15 - Generation Status
	1 0	0 - Definition is based on category code. 1 - See CS8402 Data Sheet, Appendix A
8, 7	$\overline{C8}$, $\overline{C9}$	C8-C14 - Category Code (2 of 7 bits)
	1 1 1 0 0 1 0 0	0000000 - General 0100000 - PCM encoder/decoder 1000000 - Compact Disk - CD 1100000 - Digital Audio Tape - DAT

Note: 1. The evaluation board is shipped from the factory in the Professional mode. Changing switch 3 to open places the CS8402 in Consumer mode; however, the hardware is not set up for consumer mode. To modify the hardware for Consumer mode, change R19 to 374Ω and add R20 at 90.9Ω. Then, as shown in the figure below, cut the trace connecting TXN to the transformer, and connect the transformer side to the ground hole provided. For a full explanation of the consumer hardware interface, see the CS8402 data sheet, Appendix B.

Table 4. CS8402 Switch Definitions - Consumer Mode



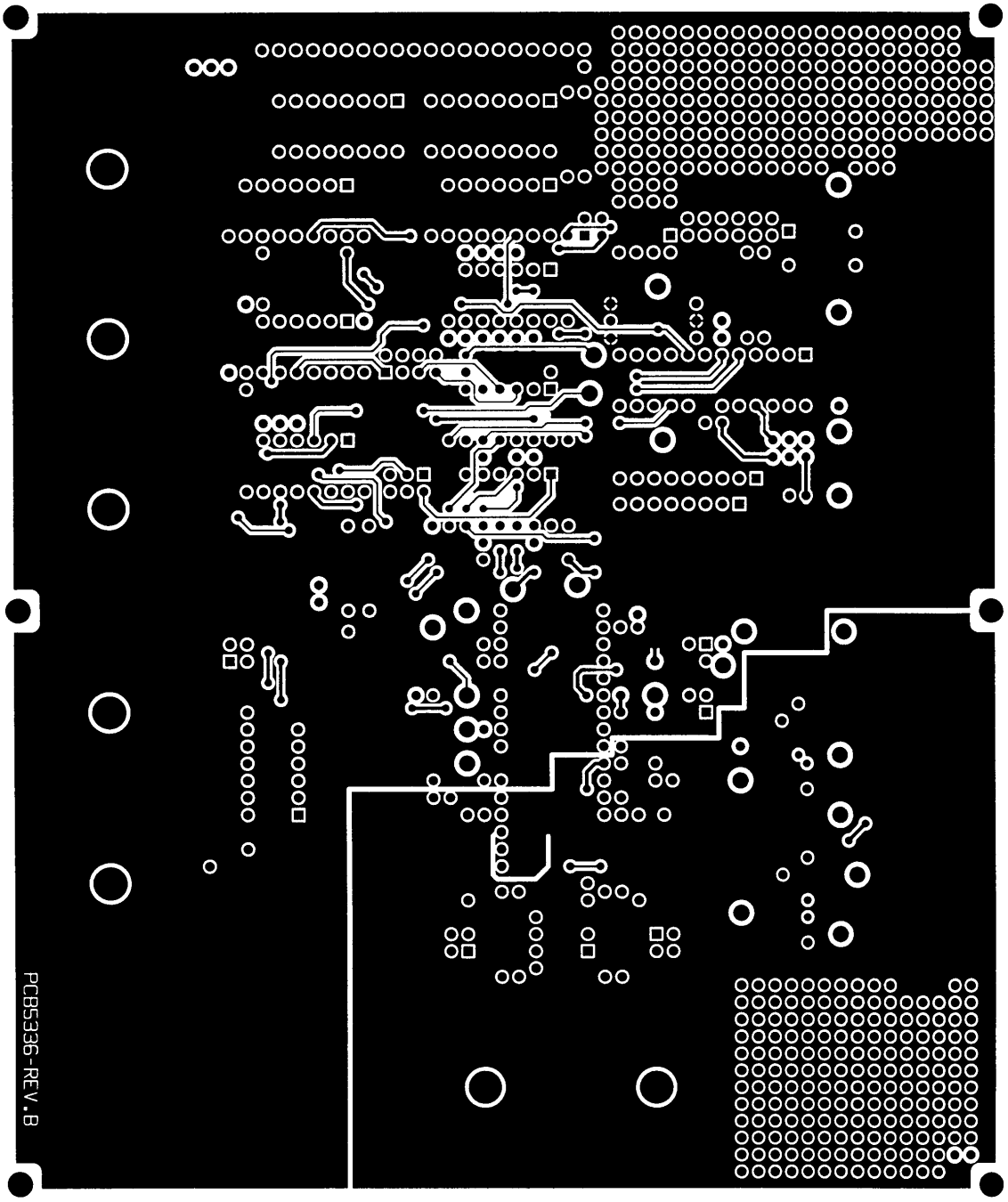


Figure 7. Top Ground Plane Layer (NOT TO SCALE)

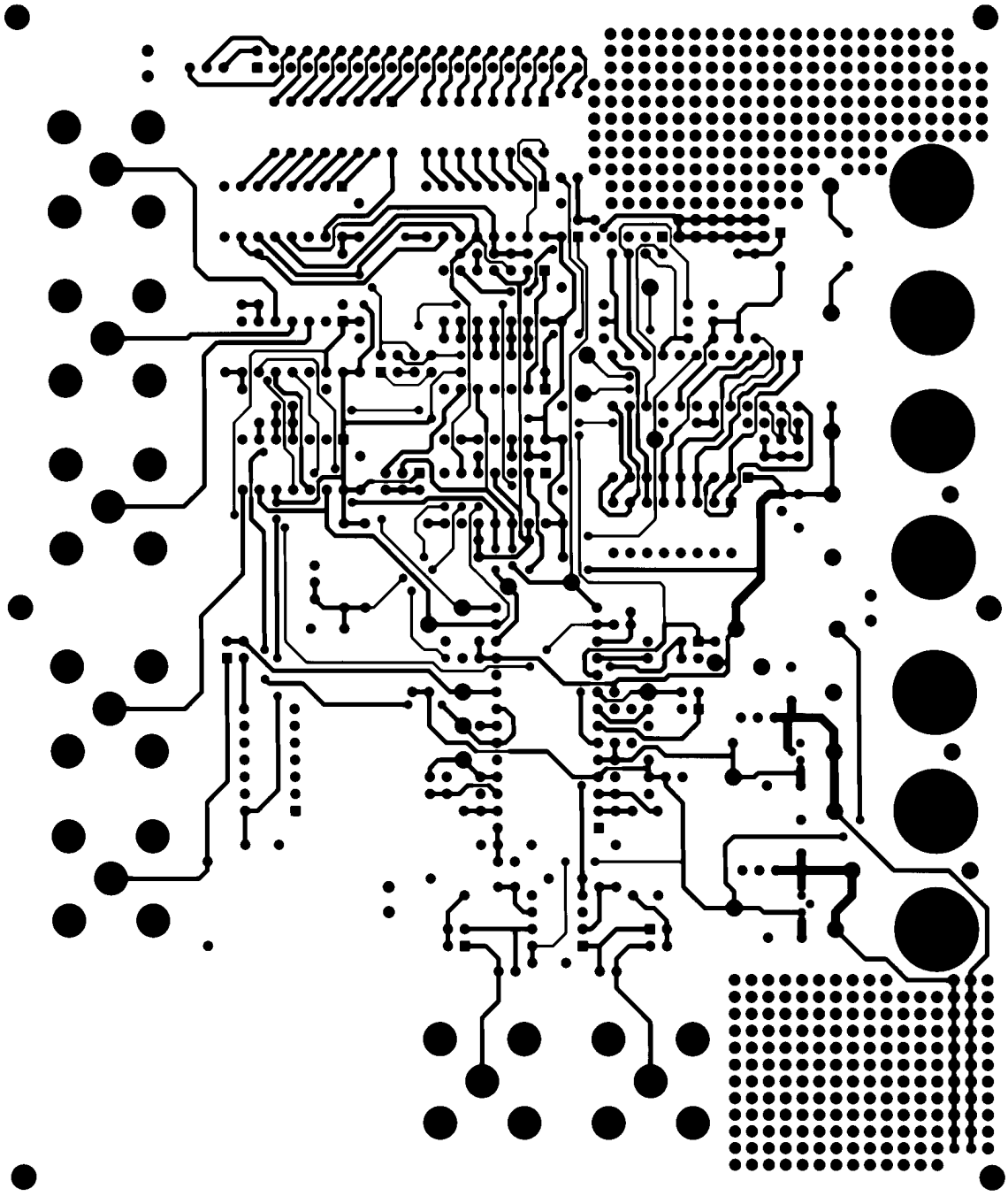


Figure 8. Bottom Trace Layer (NOT TO SCALE)

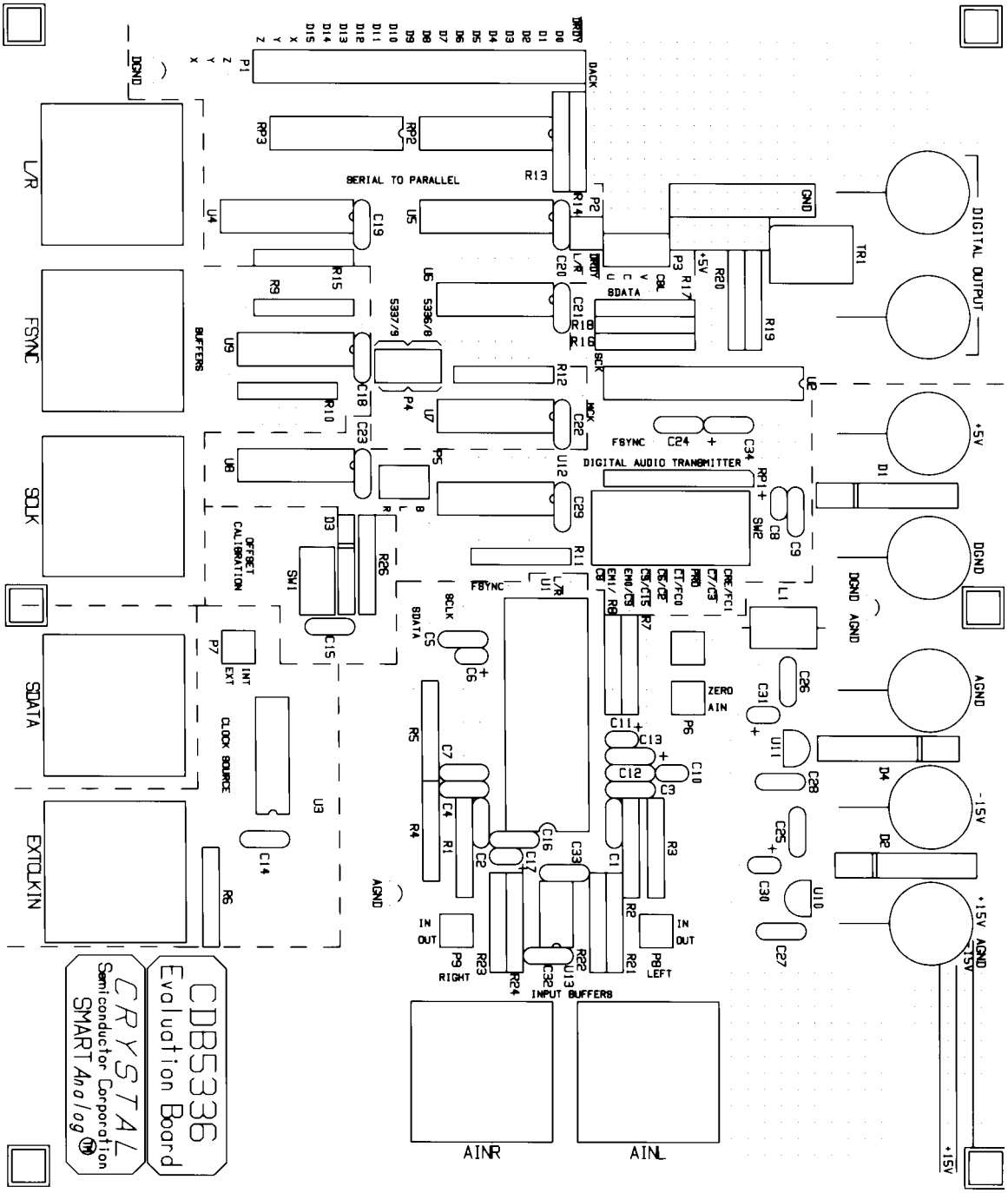


Figure 9. Component Layout (NOT TO SCALE)