CS8283 LeAPset-sx™ CHIPSet™ DATA BOOK

Revision 1.0

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CONVENTIONS

The following conventions are used throughout this document to refer to the configuration and diagnostics registers internal to the 82C841, 82C242, and 82C636 integrated circuits:

* REGnH denotes the internal register of index n in hexadecimal notation.
* REGnH<x:y> denotes the bit field from bit x to bit y with index n in hexadecimal notation.

The following methods are used to indicate an active low signal:

* a bar over the signal name
* an asterisk following the signal name

The following symbols are used to indicate the rising and falling edges of signals:

* ↑ - is a rising edge
* ↓ - is a falling edge

The following terms are used throughout the document:

* MB = megabyte
* Mb = megabit
* KB = kilobyte
* Kb = kilobit

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LeAPset (Low-Powered Enhanced AT Portable) CS8283 CHIPSets

- **100% IBM PC AT-compatible CHIPSet for 12, 16, and 20 MHz laptop computers**
- **Compatible with CHIPS' NEAT CHIPSet (CS8221)**
- **Power Control Unit (PCU) to control system power sources**
- **Special power saving features that accomodate laptop computer low power requirements:**

  Sleep mode
  Slow refresh DRAM support
  Suspend/Resume Support
  Selectable operating frequencies
  Auto power-off/on feature

- **Support for combining both video and system BIOS into a single ROM**
- **Support for ROM cartridges**
- **Support for three programmable I/O decodes**
- **Support for password/security EEPROMs**
- **Support for 80386sx microprocessors**
- **Two multipurpose, programmable parallel I/O ports**

The LeAPset CS8283 CHIPSet comprises highly integrated application specific integrated circuits that emulate the control logic of IBM PC AT-compatible computers. Additionally, this CHIPSet provides functions designed specifically for the laptop computer environment.

The CS8283 CHIPset, which supports the 386sx microprocessor, comprises the following devices:

- the 82C841. This device includes a CPU/bus, page/interleave, and EMS memory controller in addition to some laptop control features.
- the 82C242. This chip includes data/address buffers and bus conversion logic.
- the 82C636. This chip is the Power Control Unit. It controls system power and provides slow refresh DRAM support in standby mode.
- the 82C206. This device is an integrated peripheral controller.
- the 82C601. This is a multifunction controller that provides one parallel and two serial port interfaces.
- the 82C455. This is a VGA-compatible flat panel control that supports CRT, LCD, plasma and electro-luminescent displays.
- the 82C765. This is a floppy disk controller that is compatible with the uPD765A controller. It also contains a precision analog data separator.

The CS8283 CHIPSet, which is compatible with the NEAT CHIPSet, is designed specifically for use in laptop computers. However, it can be used as the basis for a small footprint desktop computer in which integration is the critical factor. Figure 1.1 is a block diagram of a typical implementation of the CS8283 in a laptop environment.

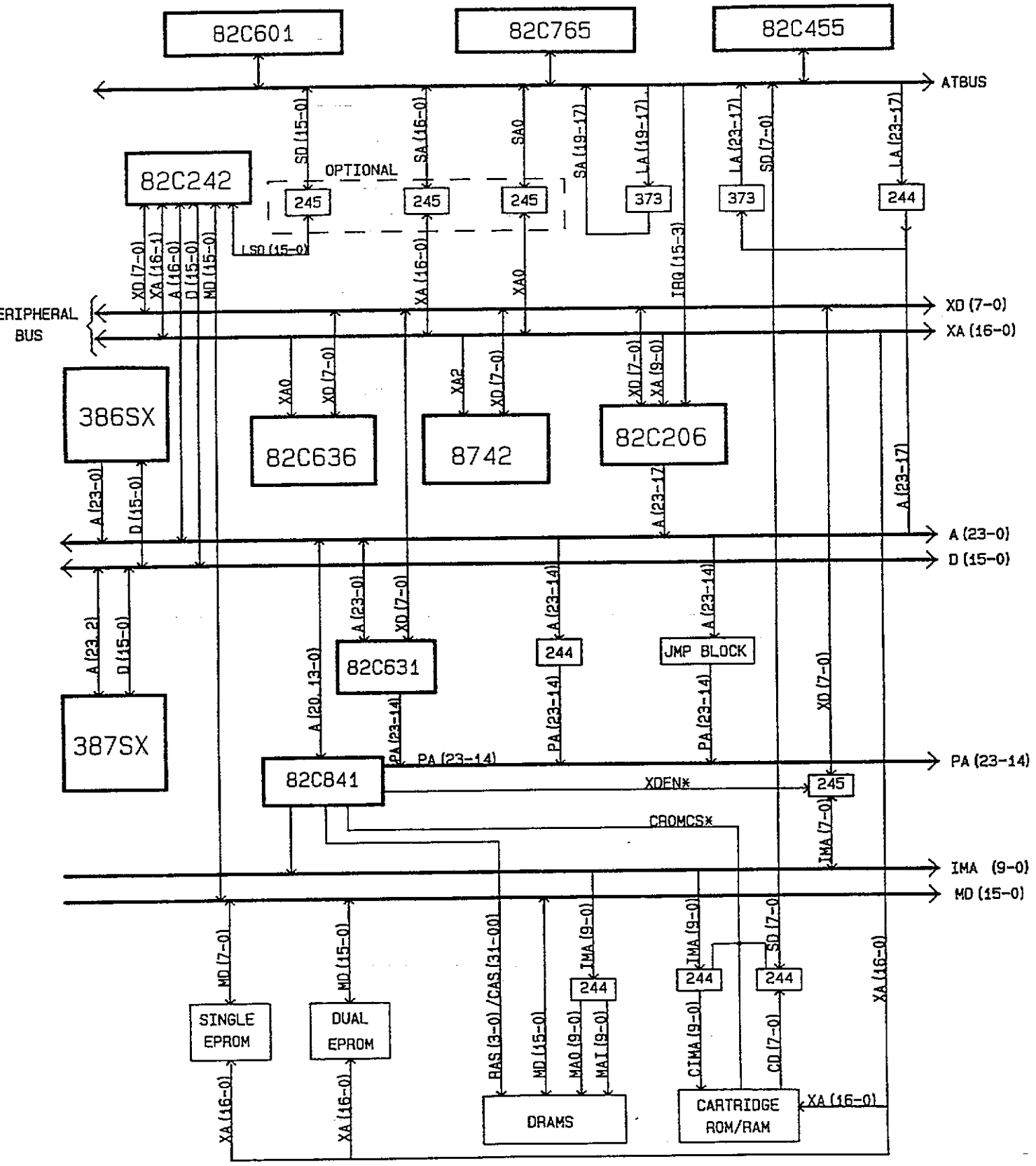


Figure 1.1 Block diagram of a Laptop System using CS8283

82C841 CPU/BUS/Memory System Controller

2.0 Features:

- CPU/BUS Bus control:
  - Clock generation with programmable speed selection
  - Optional independent AT-bus clock
  - CPU interface and bus control
  - Programmable command delays and wait state generation
  - Port B register and NMI logic
  - CPU state machine, AT-bus state machine and bus arbitration logic
  - Action code generation logic
  - DMA and refresh logic
  - Numeric coprocessor interface logic
  - Configuration registers

- Memory sub-system control:
  - Page mode access including single bank, odd number of banks, 2-way and 4-way page interleave, providing higher performance than conventional DRAM accessing schemes
  - 100ns DRAM support at 16MHz using page mode operation
  - Up to 8M of high speed local memory in four banks using 1M x 1 or 1M x 4 DRAMs
  - Remapping of DRAM resident in 640K to 1MB area above 1MB address space
  - LIM-EMS 4.0 support with four sets of EMS page registers on chip
  - Shadow RAM features for efficient system and video BIOS execution
  - OS/2 optimization features allow fast switching between protected and real mode
  - Staggered refresh to reduce power supply noise

- Laptop support:
  - Sleep mode to reduce power consumption by disabling or scaling down clock frequencies
  - Three programmable I/O chip select outputs to eliminate external decode circuitry
  - Combined system and video BIOS option
  - Support for both double EPROMs and single EPROM BIOS
  - Cartridge memory option
  - Suspend/resume mode support

2.1 Functional Description

The 82C841 CPU/Bus/Memory system controller consists of the following sub-modules as shown in Figure 2.1:

- Reset and shutdown logic
- Clock generation and sleep logic
- CPU state machine and timeout logic
- AT-bus state machine
- I/O decode logic
- Port B and NMI logic
- Numeric coprocessor interface
- Action code generation logic
- System control logic
- Memory control logic
- Refresh and bus arbitration logic
- Configuration registers

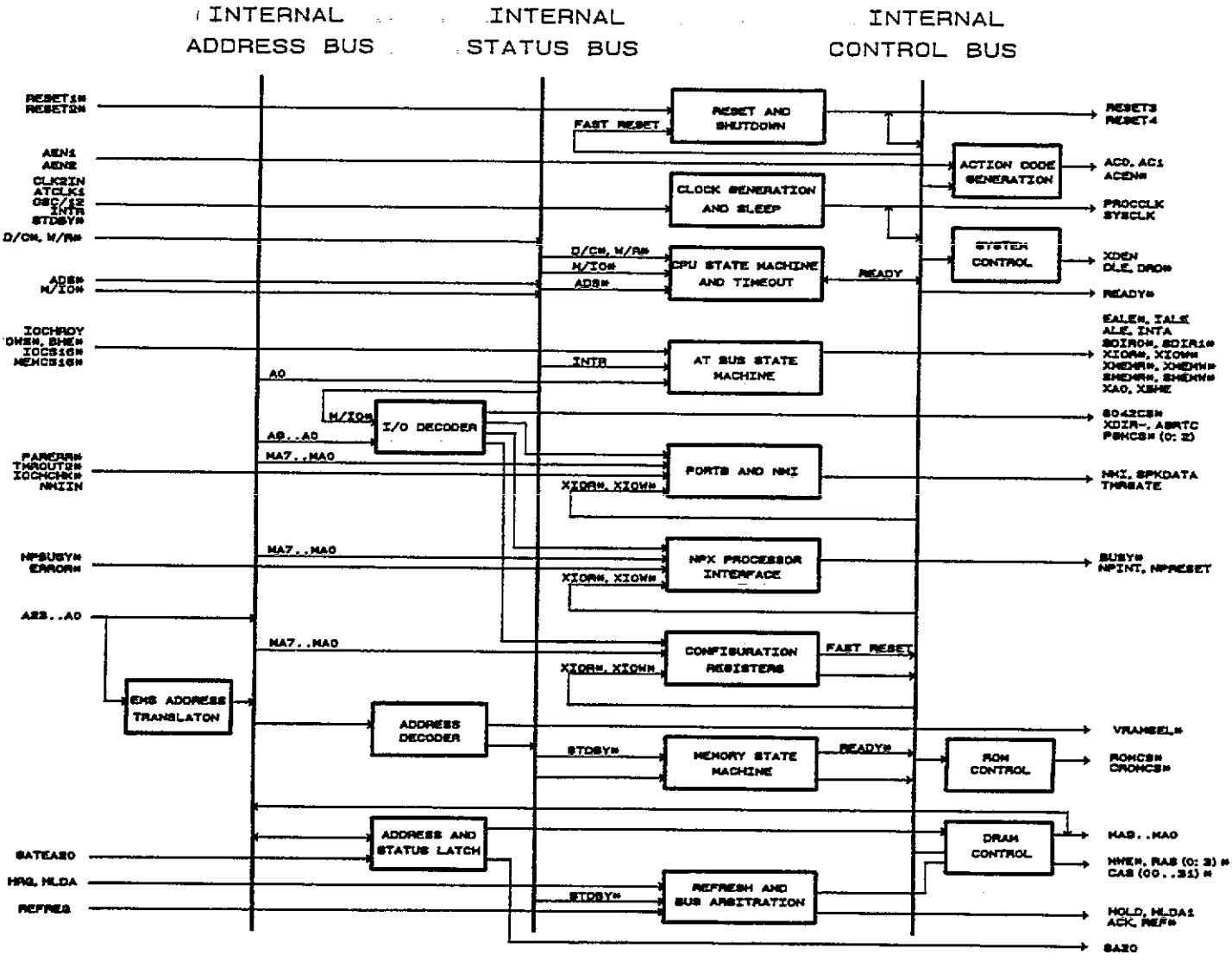


Figure 2.1 82C841 Internal Block Diagram

2.1.1 Reset and Shutdown Logic

The 82C841 has two reset inputs (RESET1* and RESET2*) as well as two reset outputs (RESET3 and RESET4). RESET1* can be derived from either the front panel push-button switch, the 82C636 Power Control Unit or a combination of both. When RESET1* is active, the 82C841 asserts both RESET3 and RESET4 to produce a system reset. RESET2* is generated by the 8042 (8742) keyboard controller when a "warm reset" (RESET3 only) is required. The RESET3 output should be used to reset the CPU, while the RESET4 output should be used to reset the keyboard controller, the 82C206, and any other peripherals that use the RESET signal on the AT-BUS. Both RESET3 and RESET4 are held active an additional 64 PROCCLK cycles after their input stimuli are deasserted (ie: RESET3 lasts at least 64 PROCCLK cycles beyond the rising edge of RESET1*). RESET3 and RESET4 are synchronized with the PROCCLK signal, and both meet the setup and hold times of the 386sx CPU.

Additionally, RESET3 can be activated by two other conditions. The first condition is when a shutdown cycle is detected on the CPU status lines. RESET3 is generated synchronously with the PROCCLK signal and lasts for at least 64 PROCCLK cycles. This synchronization with PROCCLK assures proper CPU operation. The second condition is when a one is written to chipset index REG60H<5> (a low to high transition). This software generated fast reset causes RESET3 to remain active for at least 64 PROCCLK cycles.

2.1.2 Clock Generation and Sleep Logic

Writing to the appropriate 82C841 chipset registers provides a flexible way of selecting clock frequencies for both the CPU and the AT-bus. Figure 2.2 shows a block diagram of the internal clock selection scheme. The 82C841 has two input clocks, CLK2IN and ATCLK. CLK2IN is driven from a TTL crystal oscillator, running at a maximum of twice the rated processor clock frequency. ATCLK is also driven from a TTL crystal oscillator and is typically lower in frequency than CLK2IN. The 82C841 generates the processor clock, PROCCLK, for driving the CPU interface and state machine. BCLK is an internal clock and is used to synchronize the the AT-bus interface logic. SYSCLK is the AT-bus system clock and is derived from BCLK. In non-sleep mode, its frequency is always BCLK/2. In sleep mode, both PROCCLK and SYSCLK can be programmed to run at slower frequencies. This is discussed in the Sleep Mode section.

Both PROCCLK and BCLK (and in turn SYSCLK) can be derived from either CLK2IN or from ATCLK. In the synchronous mode, both PROCCLK and BCLK are derived from CLK2IN, thereby making the processor state machine and the AT-bus state machine run synchronously to each other. In the asynchronous mode, PROCCLK is derived from CLK2IN and BCLK is derived from ATCLK, thereby making the processor state machine and AT-bus state machine run asynchronously to each other. Possible clock selections in the two modes are:

Synchronous mode:

1. PROCCLK = CLK2IN
   BCLK = CLK2IN
   SYSCLK = BCLK/2 = CLK2IN/2
2. PROCCLK = CLK2IN
   BCLK = CLK2IN/2
   SYSCLK = BCLK/2 = CLK2IN/4

Asynchronous Mode:

1. PROCCLK = CLK2IN
   BCLK = CLK2IN/3
   SYSCLK = BCLK/2 = CLK2IN/6
2. PROCCLK = CLK2IN
   BCLK = CLK2IN/4
   SYSCLK = BCLK/2 = CLK2IN/8
3. PROCCLK = CLK2IN
   BCLK = CLK2IN/8
   SYSCLK = BCLK/2 = CLK2IN/16
4. PROCCLK = CLK2IN
   BCLK = ATCLK
   SYSCLK = BCLK/2 = ATCLK/2
5. PROCCLK = BCLK
   BCLK = ATCLK
   SYSCLK = BCLK/2 = ATCLK/2

Although other combinations can be selected, system performance cannot be guaranteed due to SYSCLK becoming too slow or too fast.

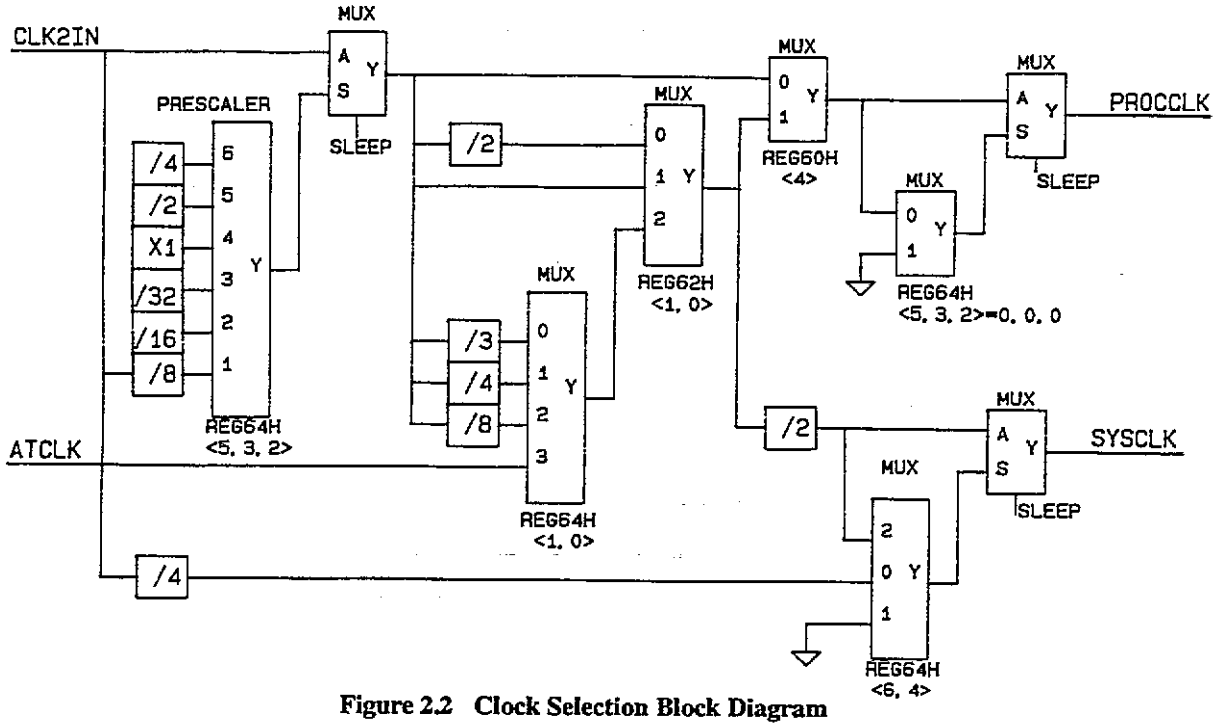


Figure 2.2 Clock Selection Block Diagram

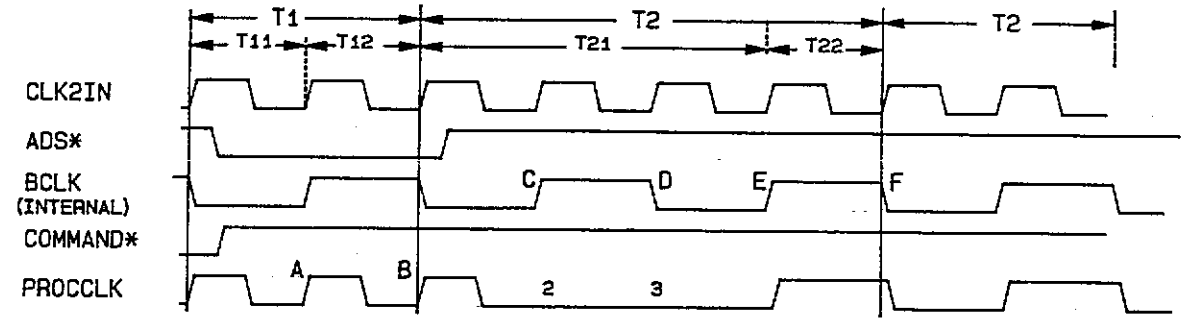


Figure 2.3 Sequence Diagram for High- to Low-Frequency Transition

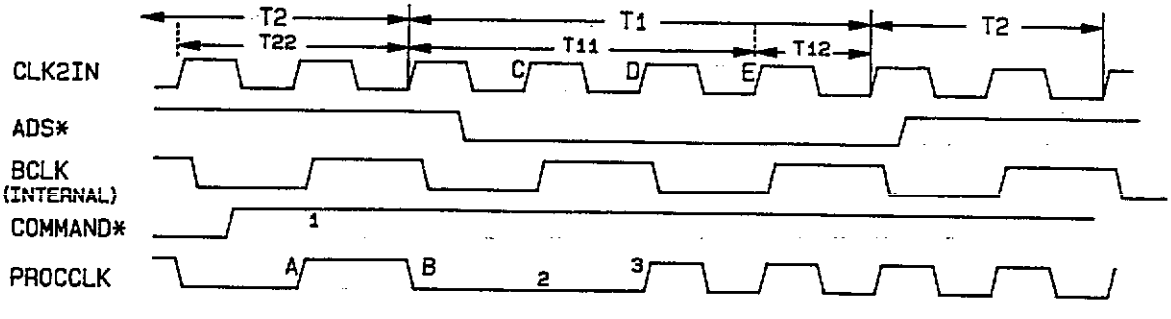


Figure 2.4 Sequence Diagram for low to High Frequency Transition

PROCCLK	REG60H <4>	REG62H <1>	REG62H <0>	REG64H <1>	REG64H <0>
CLK2IN	0	X	X	X	X
CLK2IN/2	1	0	0	X	X
CLK2IN/3	1	1	0	0	0
CLK2IN/4	1	1	0	0	1
CLK2IN/8	1	1	0	1	0
ATCLK	1	1	0	1	1

(a) PROCCLK selection - Awake Mode

SYSCLK	REG60H <4>	REG62H <1>	REG62H <0>	REG64H <1>	REG64H <0>
CLK2IN/2	X	0	1	X	X
CLK2IN/4	X	0	0	X	X
CLK2IN/6	X	1	0	0	0
CLK2IN/8	X	1	0	0	1
CLK2IN/16	X	1	0	1	0
ATCLK/2	X	1	0	1	1

(b) SYSCLK selection - Awake Mode

Table 2.1 System Clocks Selection

Under normal operation, CLK2IN should be selected as the processor clock (PROCCLK) to allow the processor to run at full speed. BCLK can either be a submultiple of CLK2IN or the external ATCLK itself. ATCLK may be selected to generate PROCCLK when it is desirable to slow down the processor for timing dependent code execution. Once the options for clock switching are set, the switching transitions occur cleanly in either the asynchronous or synchronous mode. During clock switching, both phases of PROCCLK meet the minimum and maximum values specified for the 386sx CPU. Special programming note: if BCLK is selected to be the source of PROCCLK (by setting REG60H<4>), then REG62H cannot be changed. In this case, first select PROCCLK to be CLK2IN, make the necessary speed changes in REG62H<1,0> and REG64H<1,0>, and then change REG60H<4>. Table 2.1 shows the various register settings for different choices of PROCCLK and SYSCLK respectively.

Figures 2.3 and 2.4 illustrate the sequence of events that switch PROCCLK from high- to low-speed and from low- to high-speed caused by programming the configuration registers. In Figure 2.3, the rising edge (A) of PROCCLK is used to latch the command inactive condition (1). On the rising edge (B), CLK2IN is disabled on the PROCCLK line. This ensures that clock switching occurs when PROCCLK is low. Once CLK2IN is disabled, the first rising edge (C) of BLCK latches this condition as denoted by sequence (2). BCLK then enables itself on the PROCCLK line on the falling edge (D) as denoted by sequence (3). This ensures a glitch free transition between the two clocks. It also does not violate the minimum and maximum 386sx CPU clock specifications. If BCLK is asynchronous with respect to CLK2IN, it is possible that sequence (2) could violate setup time requirements with respect to edge (C). In this case edge (D) registers the state of PROCCLK as still being high in sequence (3). Hence, edge (E) samples PROCCLK to be low and edge (F) enables BCLK on the PROCCLK line. This case does not violate the minimum and maximum 386sx CPU clock specifications.

In Figure 2.4, the rising edge (A) of PROCCLK latches command inactive as denoted by sequence (1). Edge (B) disables BCLK on the PROCCLK line. In sequence (2), edge (C) of CLK2IN latches PROCCLK low. Edge (D) then enables CLK2IN on the PROCCLK line as denoted by sequence (3). If sequence (2) does not meet setup time requirements fo edge (C), then the state of PROCCLK is sampled as being high in sequence (2). In this case, edge (D) samples PROCCLK low, and edge (E) enables CLK2IN on the PROCCLK line. PROCCLK does not violate the minimum and maximum 386sx clock specifications.

Note that during sleep mode clock switching, PROCCLK and SYSCLK transition between awake and sleep frequencies while their phase is high. This is opposite to awake frequency scaling, which only switches frequencies during PROCCLK's low phase.

Sleep Mode:

Sleep mode is a power saving feature in the 82C841. It is used to reduce the system clock frequencies when an application program is waiting for an external event such as an input from the keyboard or an I/O operation. PROCCLK and SYSCLK can be turned off or scaled down by programming the appropriate chipset registers in the 82C841. This reduces the overall power consumption of the system, as devices connected to the clocks tend to consume less power at lower frequencies (e.g., the CPU, a coprocessor, etc.). However, these devices must be able to recover without re-initialization when the original clock frequency is restored. The 82C841 implements this ability via programming options in REG64H<6,5,4,3,2>.

Three options are available for SYSCLK during sleep mode. Its frequency can be programmed to shut off (remain low), to equal CLK2IN/4, or to follow BCLK/2 (which can also be reduced - see below). Chipset REG64<6,4> accomplishes this. During sleep mode, the frequency from CLK2IN is directly reduced by the value programmed into the CLK2IN prescaler (REG64<5,3,2>. The following CLK2IN reductions are possible: CLK2IN (no change), CLK2IN/2, CLK2IN/4, CLK2IN/8, CLK2IN/16, CLK2IN/32, static CLK2IN (held low). This means that if CLK2IN is programmed to generate PROCCLK or BCCLK, then PROCCLK or BCCLK (or both) also have their frequency reduced by the same factor as CLK2IN. The static CLK2IN has a special property in that it also shuts off PROCCLK regardless of the source of PROCCLK. If PROCCLK is already operating at a reduced CLK2IN frequency (such as CLK2IN/3 while in awake mode), the sleep frequency further reduces PROCCLK by the CLK2IN prescaler factor. Care must be taken in choosing frequencies during sleep mode to guarantee that PROCCLK does not fall below the minimum required 386sx CPU frequency. Once the desired values are programmed into these bits (typically by the BIOS upon power up), they remain unaltered until a RESET1* occurs. See section 2.5 for details on programming these bits.

The procedure for entering sleep mode (after the sleep mode clock frequencies have been programmed) is to set the Sleep Mode Enable bit (REG70H<7>) and the Sleep Mode Request bit (REG70H<6>), and then issue a HLT instruction. Sleep mode is not entered until the HLT instruction is executed. Immediately after executing the HLT instruction, sleep mode is entered, and PROCCLK and SYSCLK transition to their sleep mode frequencies. The system remains in sleep mode until the next hardware interrupt occurs. However, sleep is temporarily exited during a refresh cycle, a DMA cycle, or a master cycle. During these cycles, PROCCLK temporarily returns to its awake frequency. It returns to its sleep frequency at the completion of the cycle.

In the case of an interrupt, sleep mode is exited, PROCCLK and SYSCLK return to their awake frequencies, and the interrupt acknowledge cycle proceeds normally. The Sleep Mode Enable bit (REG70<7>) remains unaltered, but the Sleep Mode Request bit (REG70H<6>) is cleared by hardware to prevent the system from entering sleep mode again on the next HLT instruction. To re-enter sleep mode, the Sleep Mode Request bit must again be set (REG70<6>) and a new HLT instruction executed.

One way to implement this feature is through an INT function call to the BIOS. This permits having a centralized control for this feature. A typical application waiting for an event can enter sleep mode through the INT function. Upon wake up by an interrupt, the event occurrence can be verified. If the event did not occur, sleep mode can be re-entered. On the other hand, if the event did occur, an IRET from the interrupt routine brings the application back to the point where the request for sleep mode was made.

The sleep status output signal from the 82C841 can be used by peripherals that take advantage of knowing when the processor is in sleep mode. This output is active high and tracks the sleep status of the CPU. This pin is multiplexed with the PGMCS2* (programmable chip select 2) signal. Applications wishing to use this signal must program REG79H<6> to a one, otherwise this pin will function as a chip select signal instead.

2.1.3 CPU State Machine

The CPU state machine and timeout control logic interpret the signals ADS*, M/IO*, D/C*, and W/R* from the 386sx processor to determine when a CPU cycle is starting and what type it is. The 82C841 generates IALE in response to a new cycle and generates READY* to the CPU at the completion of the cycle. The CPU state machine typically runs using the CLK2IN, however it can also run using the ATCLK as discussed in section 2.1.2.

IALE is issued in response to the beginning of a new cycle during the first T_2 for non-pipelined cycles or T_{1P} for pipelined cycles (Figure 2.5). The memory control block decides if the current cycle is a local memory cycle. If the current cycle is not a local memory cycle, it is assumed to be an AT-bus cycle and control is handed over to the AT-bus state machine. The CPU state machine then waits for the completion of the AT-bus cycle before generating a READY* to the CPU. If the cycle is a local memory cycle, the CPU state machine waits for the memory control block to internally signal that it has completed the cycle. Upon completion of the cycle, the CPU state machine generates READY* for the CPU. For a local memory cycle, if the memory control block does not return the completion signal within 128 clocks, the CPU state machine generates READY* for the CPU and sets the Bus Timeout Flag (REG60H<0>). Additionally, if the Local bus Ready Timeout NMI Enable (REG60H<2>) is set, an NMI is generated.

2.1.4 AT-bus State Machine

The AT-bus state machine gains control when the current cycle is not a local memory cycle. It uses BCLK, an internal clock, which is twice the frequency of SYSCLK, the AT system clock. When asynchronous modes are selected, the 82C841 performs the necessary synchronization of control and status signals between the AT-bus and the processor. The AT-bus state machine supports both 8- and 16-bit transactions between the processor and the AT-bus.

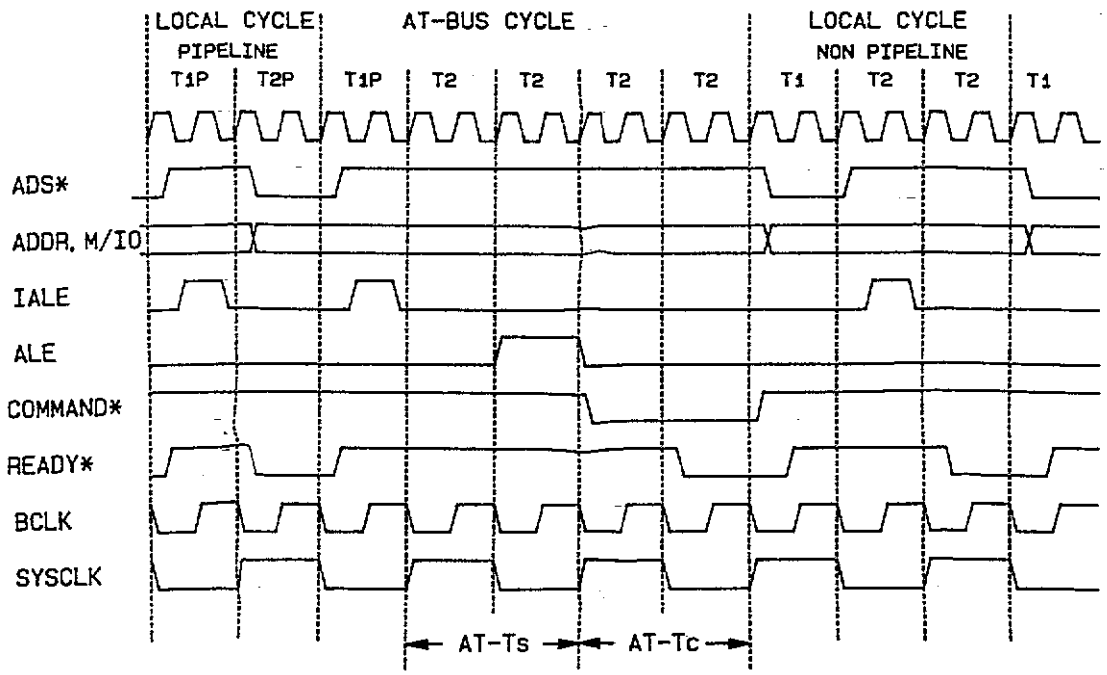


Figure 2.5 Local and AT-bus Cycles

An AT-bus cycle is initiated by asserting ALE for one BCLK cycle during AT-T_{s1} (Figure 2.5). For memory cycles, MEMCS16* is sampled on the falling edge of ALE to determine whether the data bus size is 8- or 16-bits. For I/O cycles, IOCS16* is sampled and must remain active for the duration of the cycle. After a programmed number of command delays, the memory or I/O command goes active (AT-T_C). The sequencing and timing signals for the AT-bus are provided by the 82C841. The command signals remain active until the programmed number of wait states have been executed. At this point, IOCHRDY is sampled. If IOCHRDY is active, the command terminated after the next SYSCLK cycle. If IOCHRDY is not active, one more wait state is added and IOCHRDY is again be sampled. This process repeats indefinitely until IOCHRDY becomes active.

AT-bus wait states and command delays are software programmable by writing to the chipset registers. Providing command delays causes the commands XMEMR*, XMEMW*, XIOR*, XIOW*, SMEMR*, and SMEMW* to be delayed from the falling edge of ALE in BLCK increments. Providing wait states causes the command to remain active for additional AT command cycles (AT-T_C). The minimum AT command cycle is equal to one SYSCLK cycle. A command active for one AT-wait-state is two SYSCLKs long (one SYSCLK for the original command cycle T_C and one SYSCLK for the wait state T_W).

2.1.5 I/O Decode Logic

This sub-module decodes the address and status lines from the CPU and generates various chip select signals. Some of these chipset signals are used to access registers internal to the 82C841, while others are available at output pins. The chip selects decoded and used internally are for accesses to Port B, the numeric processor ports at system I/O address F0H-FFH, and chipset configuration registers accessed at system I/O address 22H and 23H. Those that are decoded and available at output pins include 8042CS* (decoded for the keyboard controller's address range) and ASRTC (for the real-time clock address range). This I/O sub-module also generates XDIR to control the direction of data buffers during these I/O cycles.

Additionally, there are three programmable I/O decode selects, PGMCS0*, PGMCS1*, and PGMCS2*, available in the 82C841, eliminating the need for external I/O decode circuitry Each programmable chip select has its own chipset registers associated with it and each chip select can be individually programmed for read only, write only, or both read/write access rights. Mask bits can also be set to allow the programmable decode to respond to a range of I/O addresses. The registers used are REG71H through REG79H. (PGMCS2* is available as long as REG79<6> is zero, otherwise this output will function as a sleep status indicator - refer to the sleep mode section). Section 2.5 shows the details of the implementation of these registers.

2.1.6 Port B and NMI generation logic

The 82C841 implements the Port B defined for the PC-AT system at system I/O address 61H. Refer to section 2.5 for details of bit assignments. The NMI sub-module performs latching and enabling of both I/O channel check error and parity error conditions. If the corresponding NMIs are enabled in Port B, a non-maskable interrupt is generated for the CPU, and the source is also recorded in Port B. Reading Port B indicates the source of the error condition. The 82C841 also accepts an NMI from the 82C636 (power control unit) if the PCU NMI Recognition bit is set (REG70H<2>). When enabled, an NMI from the 82C636 generates a non-maskable interrupt for the CPU, and the 82C841 records the event by setting the PCU NMI Status flag (REG70H<3>).

The master enable for NMI recognition as defined for PC-AT systems is at I/O address 70H, bit 7, and is implemented internally in the 82C841. If this bit is set to one, all NMIs are disabled; if set to zero, NMIs are enabled. Although bit 7 of port 70H is contained in the 82C841, port 70H is also used by the 80C206 to access the real-time clock. Care should be taken when programming this port to insure that bit 7 is not accidentally turned on or off when accessing the real-time clock's CMOS RAM.

2.1.7 Numeric Coprocessor Interface

The 82C841 also includes the necessary circuitry to interface a 387sx numeric coprocessor with the 386sx with minimum external logic. This internal circuitry handles the decoding required for selecting and resetting the 387sx, handling the NPBUSY* and ERROR* signals from the 387sx to the 386sx, and generating the interrupt signals for error handling.

During a system reset, the 82C841 determines whether an 387sx is installed by monitoring the ERROR* signal from the coprocessor. If a 387sx is installed, the 82C841 sets the Coprocessor Installed flag (REG62H<7>). A coprocessor cycle is terminated by a READY* signal which can be generated from either the 387sx itself (via its READYO* line) or by the 82C841 READY* (after the programmed number of I/O wait-states). The choice of which device generates READY* is programmable by setting or clearing the Coprocessor Ready Generation control bit (REG62H<6>). This bit has no effect on the system if a coprocessor is not installed. Note that having the 387sx generate its own ready results in higher performance than having the 82C841 generate READY*, but it also requires external gates to tristate the READYO* line and actively pull it up at the completion of a cycle.

The system designer should make his own analysis as to which device will source the coprocressor ready signal in his system. (ie: trade off between higher integration with the '82C841 generating ready or slightly higher performance at the cost of external logic if the '387sx generates the coprocessor ready signal). If the '387sx is chosen to provide the ready signal, then REG62<6> must be set correctly or else the potential exists for both the 82C841 and the '387sx to generate a ready signal for the same cycle which could result in loss of synchronization between the CPU and the 82C841.

Coprocessor cycles are decoded by the 82C841 for the I/O ranges 0F0H, 0F1H, and 8000F8H-8000FFH. While executing a task, the 387sx issues an NPBUSY* signal to the 82C841. Under normal operation, this is passed out to the CPU as BUSY*. If during this busy period, a numeric coprocessor error occurs, the ERROR* input to the 82C841 becomes active, resulting in latching of the BUSY* output to the CPU and NPINT is asserted. Both BUSY* and NPINT stay active until cleared by an I/O write to address 0F0H or 0F1H or until cleared by a system reset. The 387sx is reset through the NPRESET output, which is activated by either a system reset or by performing a write operation to I/O port 0F1H.

2.1.8 Action Code Generation

The AT state machine performs data conversion for CPU accesses to devices not on the CPU or local memory bus. These conversions are performed for 8- and 16-bit read or write operations. 16-bit transfers are broken into smaller 8-bit AT-bus or peripheral bus transfers. To do this, it generates action codes AC0, AC1, and the ACEN* signals in response to MEMCS16* and IOCS16*. These control signals are used by the 82C242 to perform the necessary conversions. Bus conversions are also performed for DMA transfers.

Table 2.2 shows the combinations of ACEN*, AC0, and AC1 that are generated for various accesses. For local bus accesses, AC0 and AC1 are not used, thus ACEN* is not generated. On the other hand, for both AT-bus cycles and DMA cycles, ACEN* is active, and AC0 and AC1 indicate the needed conversion.

Figure 2.6 shows a sequence diagram for data conversion cycle. ALE is issued on the AT-bus in sequences 1 and 2. MEMCS16* from the external device is sampled high by the 82C841 in sequence 3, initiating a bus conversion cycle. The first command also goes active at this point for the first byte transaction and is terminated in sequence 4. In order to provide sufficient back-to-back time between the two 8-bit cycles, the second byte command is issued two PROCCLKs later in sequence 5 and terminated in sequence 6. Note that no ALE is issued for the second byte since only address line XA0 changes from zero to one. READY* is asserted low in sequence 7 and is sampled by the processor in sequence 8 to terminate the current cycle. ACEN*, AC0, and AC1 are also issued appropriately to control the bus conversion.

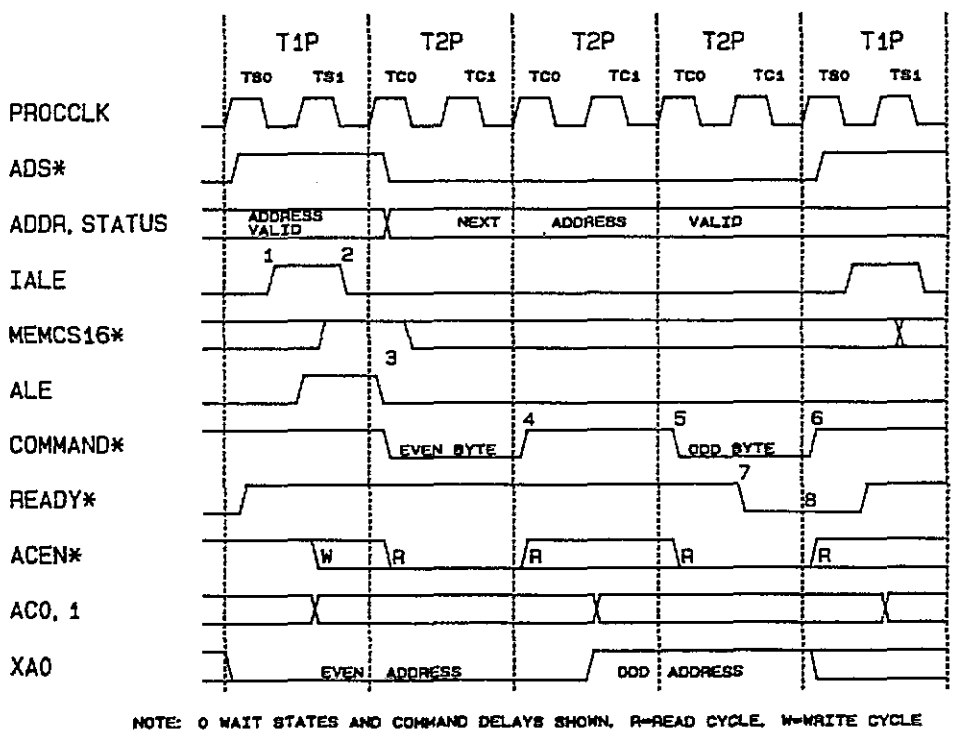


Figure 2.6 Bus Conversion Cycle (Quick Mode shown)

Operation	ACEN*
DMA/MASTER	0
CPU (local)	1
CPU (AT-bus)	0 for write 0 qualified by command for read and interrupt acknowledge cycles
REFRESH	1 qualified by REF

ACEN* generation

AC<10>	Operation
0 0	16-bit write and 8-bit write (low byte)
0 1	16-bit read and 8-bit read (low byte)
1 0	8-bit write (high byte)
1 1	8-bit read (high byte)

AC0 and AC1 for AT-bus CPU cycles (HLDA1 = 0)

AC<10>	Operation
0 0	MD bus tristated from the 82C242 for 16-bit and 8-bit read/write operations
0 1	Reserved
1 0	High memory write MD0-7 to MD8-15
1 1	High memory read MD8-15 to MD0-7

AC0 and AC1 for DMA/MASTER cycles (HLDA1 = 1)

Table 2.2 - Action Code Generation

2.1.9 System Control Logic

This sub-module generates some of the signals used to simplify external system implementation. At the start of a new cycle, the status signals and addresses from the CPU are interpreted and a decision is made whether the cycle is an AT-bus cycle or a local cycle. This module also generates DLE and DRD signals for enabling and controlling the direction of data buffers between the CPU data bus and the memory data bus in the 82C242 Address/Data Buffer Controller.

The 82C841 does not have pins that can be connected directly to the I/O data bus (XD bus). Instead, during I/O accesses to registers inside the 82C841, the MA0-MA7 lines are multiplexed to become the associated I/O data lines for the internal registers. Therefore, in a standard system implementation, the system XD bus is connected to the MA bus through an external buffer. Whenever an I/O access is made to any of the internal registers of the 82C841, XDEN* is generated. XDEN* is used to enable the external buffer, which provides the path between XD bus and the MA bus for the cycle. For all other cycles XDEN* is high and MA0-MA7 are used as local DRAM address lines.

2.1.10 Memory Controller Logic

The local memory controller module consists of the following sub-modules:

- Address latches
- Address decoder
- EMS address translation logic
- Memory state machine
- ROM control logic
- DRAM control logic

The address latches store the address from the CPU at the start of a new cycle. This address is decoded by the address decoder to determine if the cycle is a local DRAM cycle, local ROM cycle, video RAM cycle, or video ROM cycle. If it is determined that the address is an access to the video RAM memory area (A0000H-BFFFFH), control is passed to the AT-bus state machine and VRAMSEL* is generated to indicate this. VRAMSEL* is used by the 82C636 to monitor accesses to the display buffer for power control purposes. If the access is to the video ROM (C0000H-C7FFFH) and if the combined ROM option (both system and video BIOS in the same physical ROM modules) is disabled (REG70H<5>), control is transferred to the AT-bus state machine. On the other hand, if combined ROM option is enabled, the cycle is treated as a local ROM access. The chipset configuration registers specify the address ranges that are considered local memory space and also define the local DRAM, local ROM, and cartridge memory address ranges. If the access is to either the local ROM or local DRAM, the memory control state machine takes control to complete the cycle. If EMS or cartridge memory is enabled, the EMS/CROM address translation logic translates the CPU addresses for the address decoders. For accesses to local ROM area or cartridge memory area, the ROM control logic generates all the required signals; for accesses to local DRAM area, the DRAM control logic generates all the required signals. In either case, the memory control state machine generates READY* for the CPU upon completion of the desired memory operation. The number of programmed wait-states are automatically inserted.

The DRAM control logic interprets the programmed chipset registers information for page mode, interleave mode, bank size, number of banks, shadow DRAM, etc. It is then responsible for generating the RAS*, CAS*, and MWE* signals. Each RAS* line drives one 16-bit DRAM bank and each CAS* line drives one byte in that bank. The DRAM row and column addresses are put out on the MA9-MA0 address pins.

The ROM control logic generates ROMCS* for EPROM cycles and CROMCS* for cartridge memory cycles. During a cartridge ROM cycle, MA9-MA0 provide the address lines A23-A14 for the cartridge ROM access. Table 2.5 shows the relationship between the MA9-MA0 address lines and A23-A14 addresses.

2.1.11 Bus Arbitration and Refresh

The 82C841 controls all bus activity and provides the arbitration between the CPU, DMA/Master devices, and DRAM refresh requests. On HRQ or REFREQ*, HOLD to the CPU is generated and arbitration among these requests is in a non-preemptive manner. After arbitration, HOLD becomes active and the CPU relinquishes the bus by issuing HLDA. The 82C841 in turn responds by issuing REF* or HLDA1 depending upon which request prevailed in the arbitration. During a refresh cycle, the refresh logic has control of the bus until REF* goes inactive. MWE* is held high for the entire cycle. XMEMR* is asserted low after the refresh address is provided on the MA9-MA0 lines (local memory) and the A9-A0 lines (AT-bus memory). All four RAS* lines are asserted during a refresh cycle. RAS0* and RAS3* are activated first, followed by RAS1* and RAS2* after a small delay. Staggering of the RAS* lines helps reduce switching noise on the power supply. Prior to a refresh cycle, all RAS* lines are pulled high to ensure RAS* precharge. RAS0*/RAS3* and RAS1*/RAS2* bundling is provided so that staggering is effective for both a minimal 2-bank or a full 4-bank configuration.

During a DMA cycle, the DMA controller has control of the bus until HRQ goes inactive. The 82C841 is still responsible for generating action codes for bus sizing based on AEN1 and AEN2. ACEN, ALE, and EALE remain active throughout a DMA cycle.

Figure 2.7 shows refresh and DMA cycles. The refresh request signal, REFREQ, is internally latched by SYSCLK. On the first rising edge of SYSCLK, HOLD is output to the processor (sequence 1). After the processor finishes its current activity, the CPU issues its hold acknowledge signal, HLDA, and relinquishs control of the bus (sequence 2). The 82C841 responds with REF* active (sequence 3). The refresh addresses are activated on A9-A0 and MA9-MA0 (sequence 4) followed by XMEMR* active and MWE* high (sequence 5). The RAS lines are then asserted (sequence 6 and 7). XMEMR* goes inactive (sequence 8) and the RAS lines are de-asserted (sequence 9 and 10). HOLD goes inactive (sequence 11) and control is transferred to the CPU after HLDA goes inactive (sequence 12).

A DMA device requests control of the bus by asserting hold request one, HRQ1, to the 82C841. The 82C841 then generates the HOLD signal to the CPU. After a DMA latency, the CPU relinquishes the bus by asserting HLDA. The 82C841 then issues HLDA1 to the requesting device (sequence 14). HLDA1 is held active as long as HRQ1 is active. Once HRQ1 is de-asserted, HOLD to the CPU is de-asserted. After the CPU deactivates HLDA, HLDA1 is de-asserted (sequence 15) and control is returned to the processor.

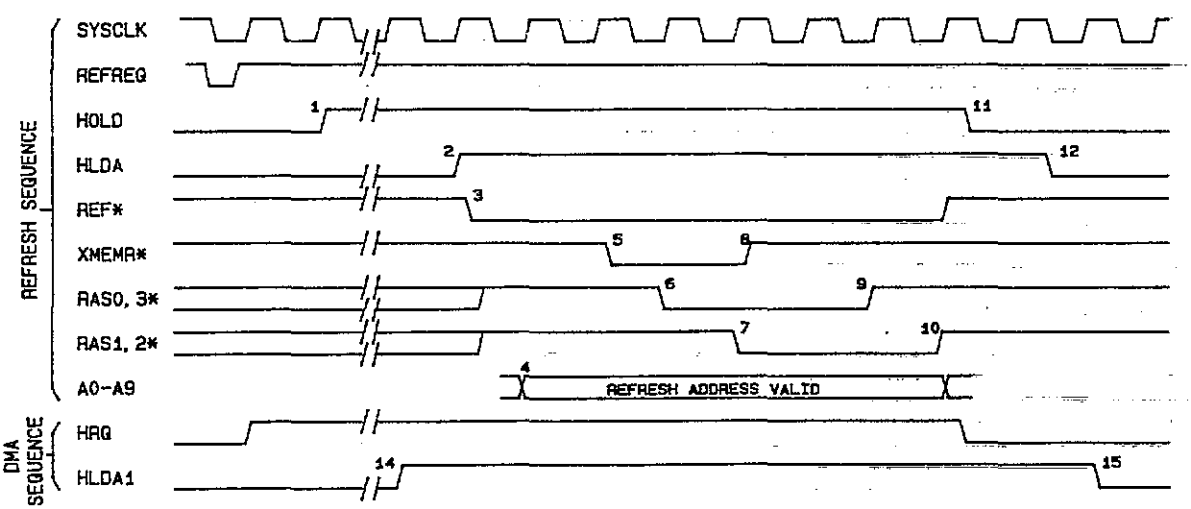


Figure 2.7 Refresh/DMA Cycle

2.1.12 Configuration Registers

The 82C841 contains a number of chipset configuration registers. By programming these registers, the various system configuration options and special chipset features can be selected. These registers are accessed by an indexing scheme, whereby the index value of the register to be accessed is written to I/O port 22H, followed by the data transaction at I/O port 23H. All reserved bits are set to zero by default, and when written to, should be set to zero. Section 2.5 describes the details of implementation and features of these registers.

2.2 Memory System Overview

The 82C841 performs memory system control functions utilizing either page mode or non-page mode access DRAMs. The various possible memory array configurations, page/interleave mode, shadow RAM, EMS system, and cartridge memory system are discussed in this section.

2.2.1 DRAM Array Configuration

The 82C841 organizes memory as local ROM and local DRAM systems. It also supports local EMS RAM memory and cartridge ROM memory. These two systems are discussed in later sections. Only the local DRAM system is discussed here.

Local memory is organized as four memory banks of DRAMs as shown in Figure 2.8. Each bank consists of 18 bits, with 16 bits of data and 2 bits of parity information. These 18 bits are split into high- and low-order bytes, with one parity bit associated with each byte. This configuration can be implemented using eighteen 1-bit wide DRAMs or four 4-bit wide DRAMs for data, and two 1-bit wide DRAMs for parity or two 9-bit wide SIMM modules. The minimum configuration can be a single bank operating in either non-page mode or single bank page mode. The maximum configuration can be four banks of identical size DRAMs operating in 4-way interleave mode.

The 82C841 generates a set of four RAS* lines for accessing each of the four banks. Each RAS* has two corresponding CAS* lines that provide access to each of the high and low bytes of data and parity. The four banks can be implemented using 1Mb or 256Kb (and in one case 64Kb) DRAMs. Table 2.3 shows the various possible configurations for the four banks.

DRAM Type in Bank				Total	EMS
0	1	2	3	mem	range
0	0	0	0	disable	0
256K	0	0	0	512Kb	0
1M	0	0	0	2Mb	1Mb to 2Mb
256K	64K	0	0	640Kb	0
256K	256K	0	0	1Mb	1Mb to 1.384Mb
1M	1M	0	0	4Mb	1Mb to 4Mb
256K	256K	256K	0	1.5Mb	1Mb to 1.5Mb
256K	256K	1M	0	3Mb	1Mb to 3Mb
1M	1M	1M	0	6Mb	1Mb to 6Mb
256K	64K	256K	256K	1.64Mb	1Mb to 1.64Mb
256K	256K	256K	256K	2Mb	1Mb to 2Mb
256K	64K	1M	1M	4.64Mb	1Mb to 4.64Mb
256K	256K	1M	1M	5Mb	1Mb to 5Mb
1M	1M	1M	1M	8Mb	1Mb to 8Mb

Table 2.3 - Memory Bank Configurations

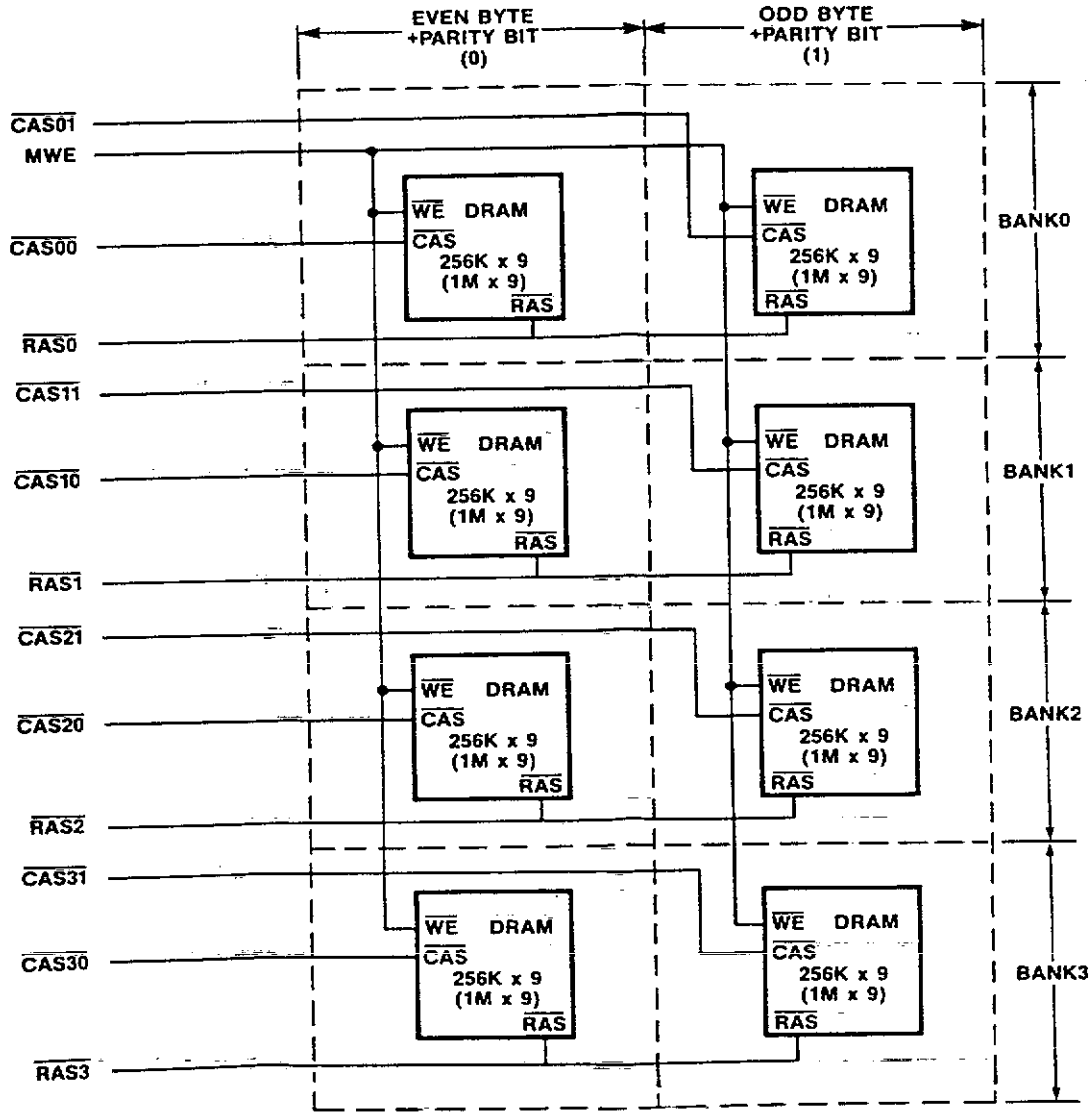


Figure 2.8 Local DRAM Memory Organization

2.2.2 Page/Interleave Operation

The 82C841 uses a page/interleaved design that is superior to most common interleaved memory designs. Typical 2-way interleaving schemes use two banks of DRAMs with even word addresses on one bank and odd word addresses on the other bank. If memory accesses are sequential, the RAS* precharge time of one bank overlaps the access time of the other bank. Figure 2.9 shows a sequence for a two bank memory design that only uses interleaving. The RAS* signals of the two banks are interleaved so that the RAS* active time in one bank is used for the RAS* precharge time (T_{RP}) of the other bank. For non-sequential accesses, wait states can occur if two consecutive accesses are made to the same bank.

In paged mode memory organization (Figure 2.10), once a row access has been made, it is possible to access subsequent column addresses within that row without a RAS* precharge penalty. However, RAS* must eventually be pulled high, typically every 10 microseconds (slow refresh DRAMS have a longer RAS* active limit). Since the CAS* precharge time, T_{CP}, is small, it is possible to make zero wait-state fast random accesses within a selected row (also referred to as a page). Typically, page mode access times are half the normal DRAM access times. For 256K x 1 DRAMs, each row has 512 bits. If eighteen of these are used to implement a bank, a page would have 512 x 2 bytes = 1KB (excluding the two parity bits).

The 82C841 combines logic from both of the previous memory architectures to provide bank interleaving and page mode access at the same time. Thus, page mode DRAMs can be interleaved at 1KB boundaries rather than two byte boundaries as in the regular interleaved mode operation. Any access to a currently active RAS* page occurs in a short page access time, and any subsequent access within the page will not incur any penalty due to RAS* precharge penalty. Memory configured this way renders significant performance benefits over normal interleaving because:

1. Page mode access time is shorter than normal DRAM access time. This allows more time in DRAM critical paths, to achieve penalty free accesses or hits.
2. The possibility of the next access being fast is significantly higher than in the regular interleaving scheme because instructions and data tend to cluster together by principle of locality of reference.

Figure 2.11 shows a 2-way page/interleaved scheme using page mode DRAMs. As indicated, it is possible to make zero wait-state accesses between the two banks by overlapping the CAS* precharge time of one bank with the CAS* active time of the other bank. The DRAM RAS* lines for both banks can be held active until the RAS* active timeout period, at which time a RAS* precharge for that bank is required. Typical hit ratios higher than 80% are possible using this scheme and 150ns access time DRAMs can be used at 12MHz and 100ns access time DRAMs can be used at 16MHz.

The 82C841 supports both 2-way and 4-way interleaved modes. 2-way interleaving uses pairs of banks, with Bank 0 and Bank 1 forming one pair and Bank 2 and Bank 3 forming the other pair. Each pair of banks can be of different types. For 2-way interleaving, banks within a pair must contain identical DRAMs. For 4-way interleaving, the DRAMs used in all four banks must be identical. Table 2.4 shows the 0 wait-state hit space for various bank configurations.

Physical memory locations in page mode are different from those of non-page mode. The physical address locations in non-page mode are linear, starting from Bank 0, Bank 1, Bank 2, and Bank 3. Figure 2.12 shows the physical memory arrangement for non-page mode, 2-way interleaved mode and 4-way interleaved mode.

DRAM Type		Interleave Mode	
Bank 0/1	Bank 2/3	2-way	4-way
256K	0	2K	-N/A-
256K	256K	2K	4K
256K	1M	3K	-N/A-
1M	0	4K	-N/A-
1M	1M	4K	8K

Table 2.4 - Average 0 Wait-state Hit Space

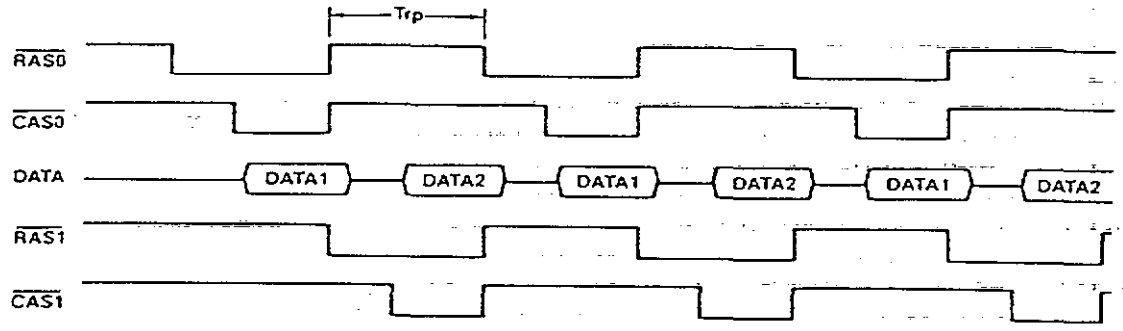


Figure 2.9 DRAM Interleaved Mode Operation

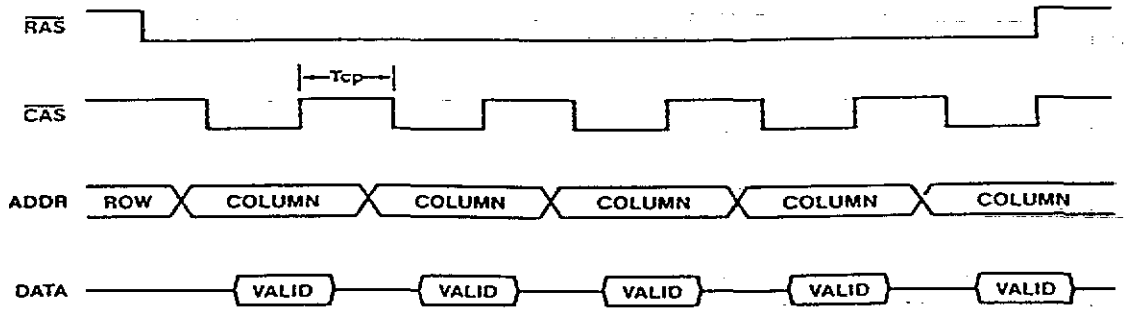


Figure 2.10 DRAM Page Mode Operation

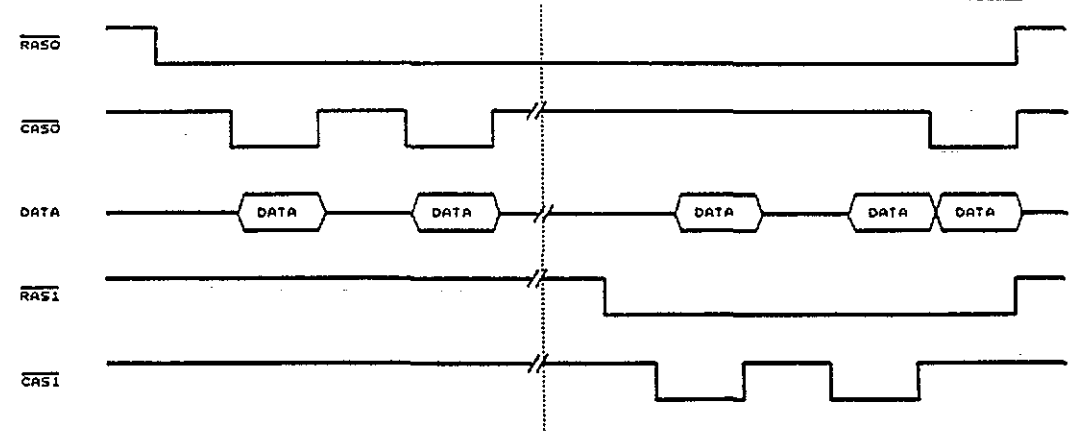
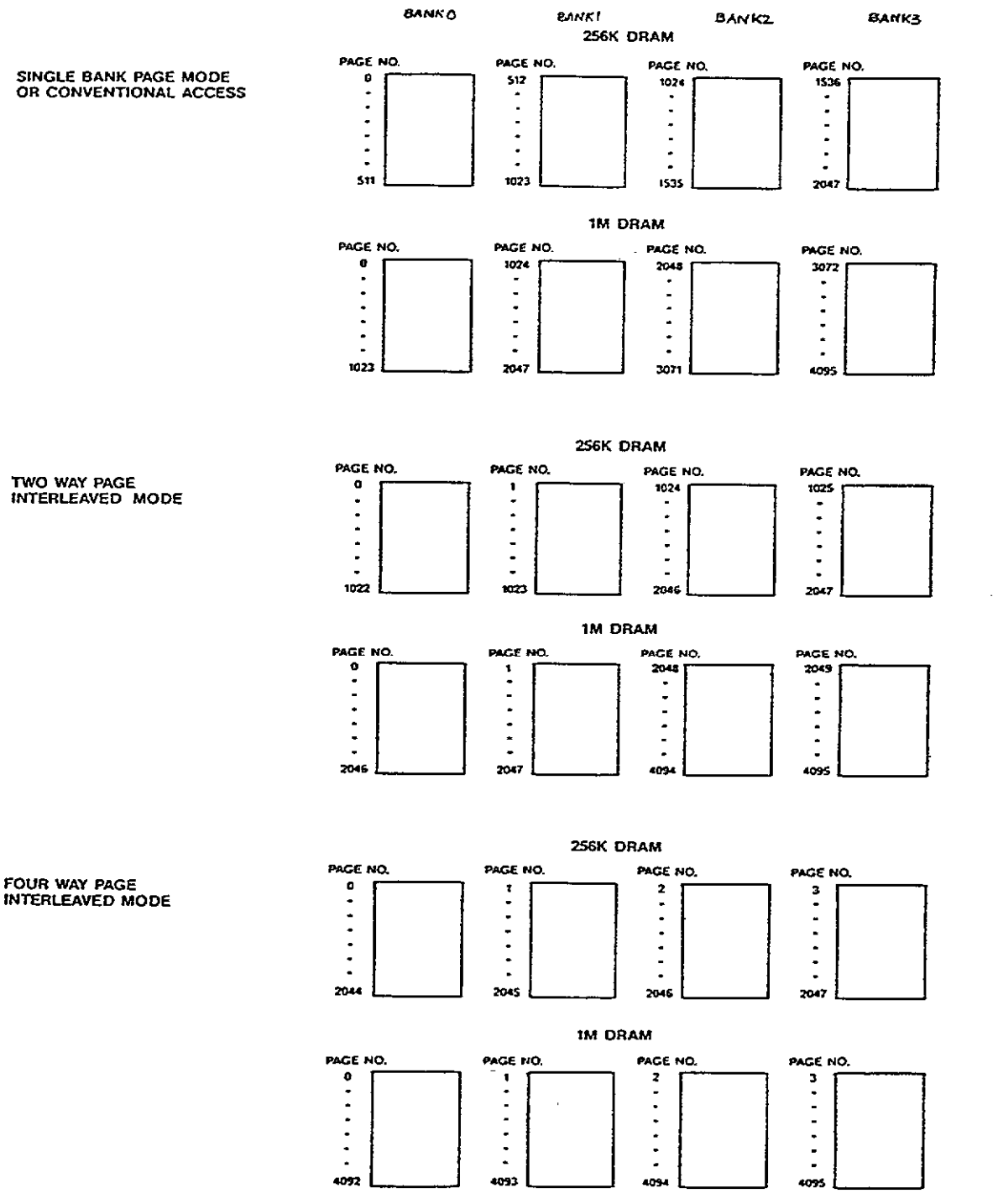


Figure 2.11 DRAM Page/Interleave Mode Operation



256K DRAM PAGE SIZE = 1Kb

1M DRAM PAGE SIZE = 2Kb

Figure 2.12 Local DRAM Memory Page Organization

2.2.3 Memory Mapping Scheme

Because of the memory mapping scheme used by an AT system, only the first 640KB of memory is treated as system DRAM. The remaining 384KB address range is reserved for the video buffer, the video ROM, add-on ROMs, and system BIOS ROMs. Through the memory mapping logic in the 82C841, it is possible to logically map the 384KB of DRAM that would normally be lost in a 1MB system to the area immediately above 1MB as shown in Figure 2.13. Hence, with 1MB of on-board DRAM, the software can address DRAM from 0 to 640KB and from 1MB to 1.384MB. The 640KB to 1MB area reserved for the system can still be addressed in the normal way. This feature is only possible in a configuration in which the total on board system DRAM memory is exactly 1MB.

Note on Pipelined vs. non Pipelined addressing: The '841 supports both pipelined and nonpipelined addressing from the '386sx. When running in nonpipelined mode, a wait state is added at the beginning of a cycle in order to provide sufficient address and status setup time. This wait state is removed as soon as the system enters into pipelined mode. ie: true 0 wait state can only be achieved in pipeline mode.

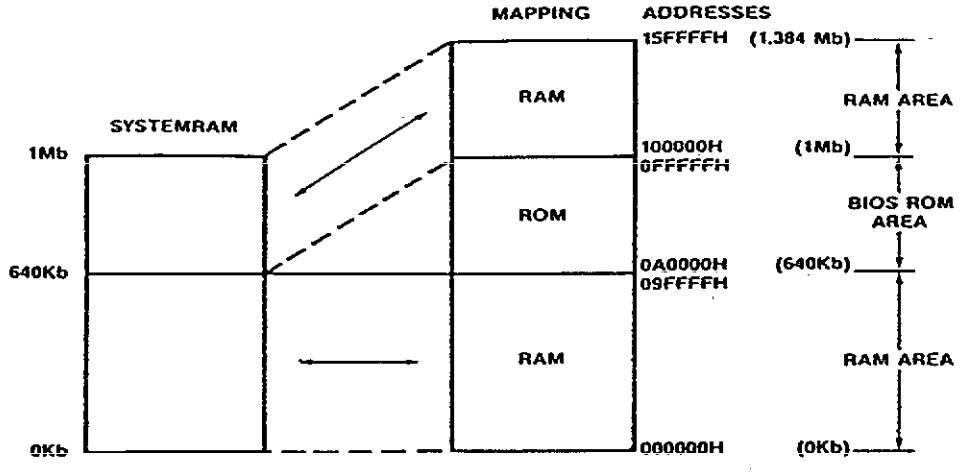


Figure 2.13 System RAM/ROM Mapping for 1MB System RAM

2.2.4 Shadow RAM Operation

To improve performance, it is preferable to execute BIOS code from DRAM rather than from slower EPROMs. The 82C841 provides the shadow RAM support which allows the BIOS code to be executed from system DRAM, resident at the same physical address as the BIOS EPROM. This feature significantly improves the performance in applications making frequent BIOS calls. Performance improvements as high as 300% to 400% have been observed in benchmark tests on shadow RAM. The BIOS code should first be copied into the corresponding DRAM area before enabling this feature. The 82C841 supports shadow RAM ability for the entire C0000H-FFFFFH (256KB) address range, thereby including video BIOS also. A typical way to establish shadow RAM is as follows:

First, the required BIOS is copied to a temporary location in the lower system DRAM. ROMCS* generation for the BIOS address range is disabled by programming the appropriate bits in REG65H. The DRAM area in the BIOS address range is then enabled by writing to the appropriate registers REG67H through REG69H. Access to this enabled DRAM is made read/write by programming REG65H. The copied BIOS is then moved to its DRAM location. This DRAM BIOS area is then write-protected by again programming the bits REG65H that control its access rights. The shadow RAM is now established. Note that to implement this feature, a minimum of 1MB of system DRAM is required.

If more than 1MB of system DRAM exists and shadow RAM feature is not invoked, DRAM is mapped as shown in Figure 2.14(a). This means that DRAM in the 640KB to 1MB area cannot be accessed. If the shadow RAM feature is used, then DRAM is mapped as shown in Figure 2.14(b), overlapping or shadowing the EPROM area. In both cases, accesses beyond the 1MB address range can be made only in the protected mode of the 386sx.

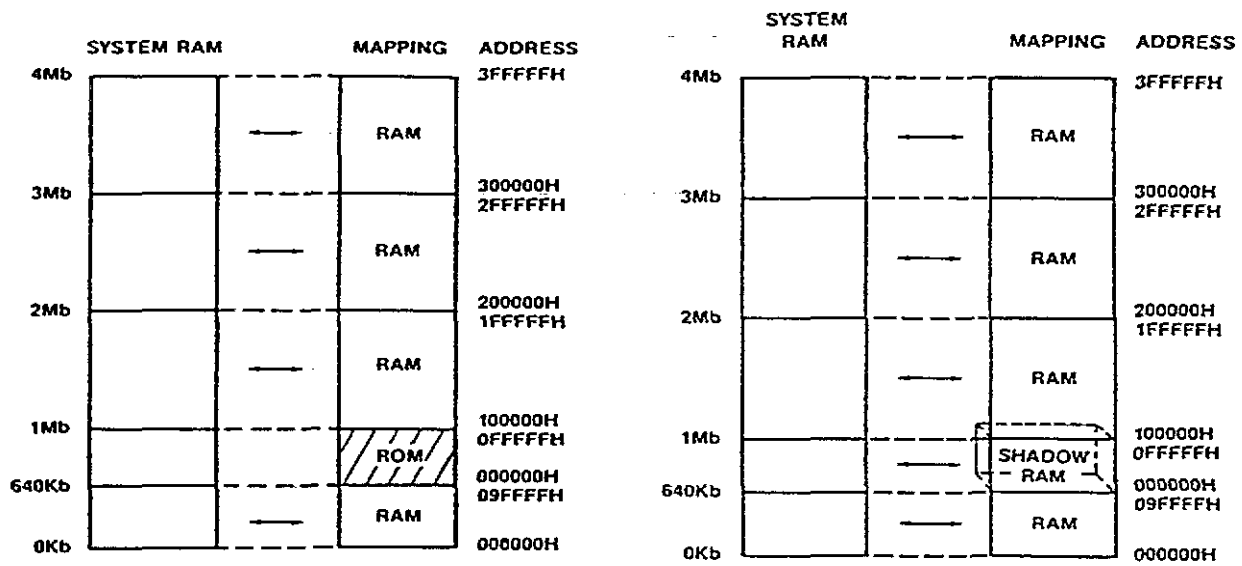


Figure 2.14 RAM/ROM mapping (a) without Shadow RAM (b) with Shadow RAM

2.2.5 EMS Support and Address Translation

The 82C841 provides internal EMS mapping hardware. This allows a 64KB area in the C0000H-EFFFF region to be used as a window (called a page frame) into a larger memory map. The page frame is divided into four 16KB blocks (pages) which can be independently redirected through a translation table to anywhere in the 82C841's memory map between 1MB and 8MB. However, the pages cannot be redirected to locations on the AT-bus.

Since the 82C841 uses a translation technique, address lines A14 to A22 are translated by the appropriate page base address register pairs. The full set of page base address registers is implemented at address 2x8 and 2x9 (see Section 2.5 for details). The I/O addresses for these registers are programmable and so is the choice of the 64KB block. Figure 2.15 shows the EMS organization along with a sample translation scheme. Although it is possible for the 82C841 to map this 64KB block to anywhere in the 0 to 8MB area, it is desirable to map it above 1MB in order to preserve the DRAM space in the 0 to 640KB area. Each of the 16KB pages can be individually enabled or disabled. For an EMS address cycle, a local DRAM cycle is performed thereby giving all advantages of the local DRAM access.

Memory that is used as expanded memory must be reserved as such, and must not be accessible as extended memory. The EMS memory size field (REG6FH<7, 6, 5>) is used for that purpose. It allows a section of extended memory to be hidden from the system. This prevents software from accessing that memory as both extended memory and expanded memory. For example, if a system has 4MB of RAM and the EMS size is set to 2MB, the upper 2MB of memory is only accessible as expanded memory, leaving 1MB of extended memory and 1MB of conventional memory and shadow RAM.

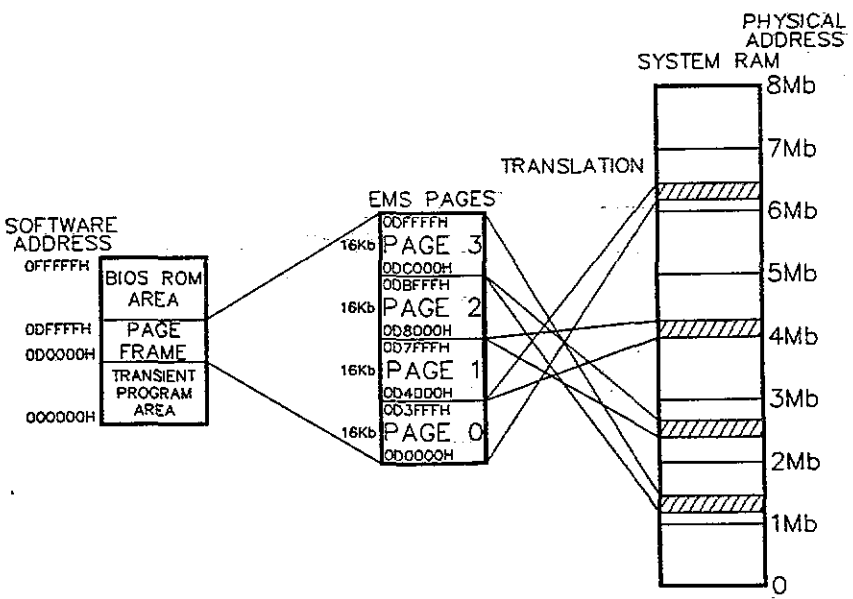


Figure 2.15 EMS Memory Mapping

2.2.6 Cartridge Memory Support

The 82C841 provides the capability to support up to 8MB of ROM cartridges. These cartridges provide a way of implementing fast access, transportable, application programs. Power consumption is reduced as disk accesses are eliminated. Cartridge memory space resides in the address range of 8MB to 16MB. The access to this memory is always byte wide. This area is accessed similarly to accesses to EMS space, and it shares the same window and page address registers as the EMS system. Thus, if the cartridge ROM is enabled, EMS has to be disabled. As the EMS address range is from 0 to 8MB, the two can co-exist physically on the system, but functionally exist only one at a time. The cartridge memory option is enabled by setting REG6BH<2>. Once enabled, access to the 16KB page generates the CROMCS* and MEMR* signals. The upper address of CA14-CA23 are provided on the MA0-MA9 address lines of the 82C841. Table 2.5 shows the address assignments on the MA address lines during cartridge memory accesses.

MA0	-	CA14	MA5	-	CA19
MA1	-	CA15	MA6	-	CA20
MA2	-	CA16	MA7	-	CA23
MA3	-	CA17	MA8	-	CA21
MA4	-	CA18	MA9	-	CA22

Table 2.5 **Cartridge memory address assignments on MA lines.**

2.2.7 Single ROM and Combined ROM

The 82C841 supports the option of using either two ROMs congigured as 16-bits wide, or a single 8-bit wide ROM for the system BIOS. If a 16-bit wide ROM data bus configuration is used (two ROMs), then the SGLROM input to the 82C841 must be strapped low and if the 8-bit wide ROM data bus option is chosen (single ROM), then the SGLROM input must be strapped high. The 82C841 interprets this input and performs the necessary bus conversions for accesses to 8-bit ROM. Single ROM cycles are treated by the 82C841 as 8 bit AT-cycles and follow the programmed number of wait states defined for 8 bit devices in REG62H<3,2> while the double ROM configuration always treats ROM accesses as local memory cycles.

The 82C841 also provides the capability of combining the video BIOS into the same physical ROM as the system BIOS. The video BIOS is located at the physical beginning of the ROM. To enable this feature, REG70H<5> must be set to one and to enable the ROMCS* generation for video ROM address range of C0000H-C8000H, REG65H<3> must be set to zero. Upon doing so, whenever the video BIOS ROM area is accessed, the 82C841 automatically generates local memory cycles for double combined ROM. This allows for faster video BIOS code execution. (Single combined ROM follows the programmed number of 8-bit AT wait states as described in the previous paragraph).

2.3 OS/2 Optimization

The 82C841 supports features that aid in OS/2 optimization. Whenever OS/2 makes DOS calls, the 386sx CPU has to switch from protected mode to real mode. Typical PC-AT architectures require the processor to issue two commands to the keyboard controller: one to reset the CPU and return to real mode, and the other to activate GATEA20. FAST RESET and FAST GATEA20 features are included in the 82C841. Since these functions are implemented directly in the 82C841 hardware rather than the keyboard controller firmware, they operate very fast. In an OS/2 environment, where the 386sx switches out of protected mode frequently, a significant performance improvement is realized.

The FAST RESET is performed by setting REG60H<5> from a zero to a one. This generates the RESET3 to reset the CPU. The FAST GATEA20 feature in REG6FH<1> is used to control A20 from the CPU. By setting this bit to zero, A20 is allowed to propagate through to the system buses. By setting this bit to a one, A20 is forced low if GATEA20 from the keyboard controller is also forcing A20 low.

2.4 Modes of Operation

The 82C841 has four modes: Normal mode, Quick mode, Delayed mode, and External mode. Each of these modes uses different CPU and AT clocks. They are discussed in the following sections.

2.4.1 Normal Mode

This is the default mode of the 82C841. During this mode the following clock selections are made:

PROCCLK	=	CLK2IN
BCLK	=	CLK2IN/2
SYSCLK	=	CLK2IN/4

Since the CPU state machine clock and the AT-bus state machine clock are derived from CLK2IN, this is a synchronous mode. ALE and commands (SMEMR*, SMEMW*, MEMR*, MEMW*, IOR*, and IOW*) are issued only for AT-bus cycles and not for local cycles. By default, I/O cycles have one command delay, 8-bit AT memory cycles have five wait-states, and 16-bit AT memory cycles have three wait-states.

Figure 2.16 shows the sequence diagram of a Normal mode local cycle followed by an AT-bus cycle with zero wait-states (0 W.S.) and zero command delays (0 C.D.). In sequences 1 and 2, IALE is generated from CLK2IN. ALE and commands (SMEMR*, SMEMW*, MEMR*, MEMW*, IOR*, and IOW*) are not generated since it is a local cycle. For a zero wait-state cycle, READY* is sampled low by the 386sx CPU in sequence 3 and the cycle is terminated. For the AT-bus cycle, again IALE is generated in sequence 4 and control is transferred to the AT-bus state machine. BCLK then generates the AT-bus states. ALE is generated in sequences 5 and 6 and AT-bus commands are generated in sequences 6 and 7 after the programmed zero command delays. For a zero wait-state cycle, READY is asserted low as shown in sequences 8 and 9, to be sampled by the CPU in sequence 7 and the cycle is terminated.

On the AT-bus, certain slow peripherals require between 50 and 60 nanoseconds between commands going inactive to the next ALE going active to provide sufficient data recovery time. Figure 2.17 shows a Normal mode AT-bus cycle with additional hold time. The dotted IALE and READY* signal shows the normal IALE being generated with no additional hold time. Instead, IALE is delayed by one T_c state of the processor by asserting READY* one T_c cycle later. The 82C841 also extends DLE to the 82C242, so that data is available to the CPU during read cycles. This feature is enabled by programming REG61H<7>.

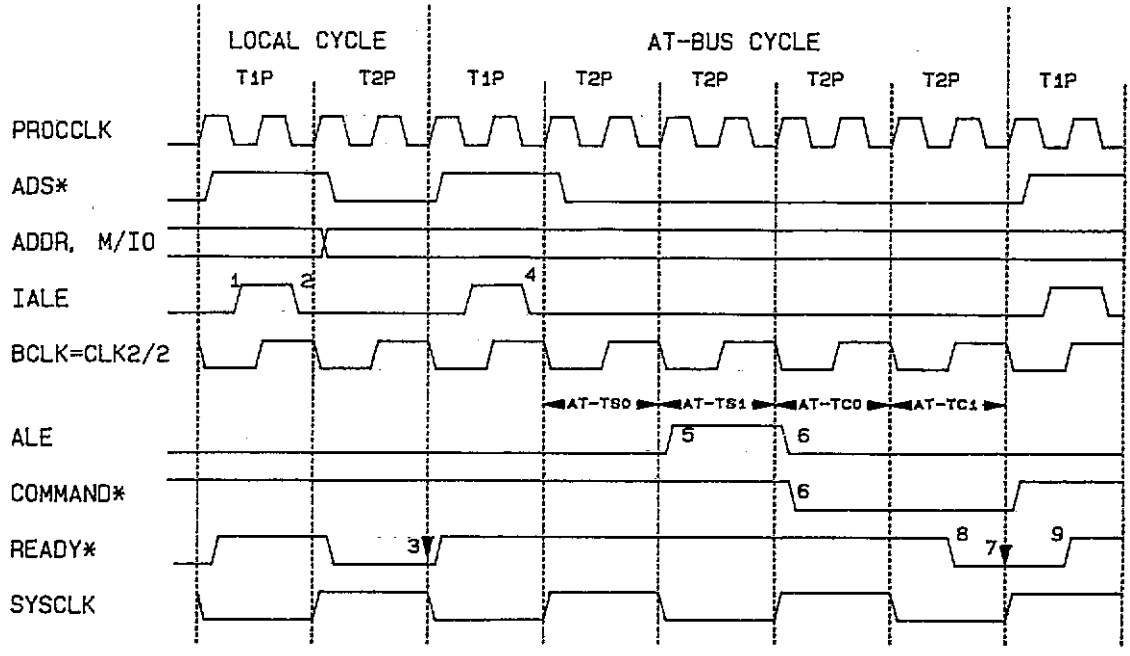


Figure 2.16 Normal Mode Local Cycle Followed by AT-bus Cycle (0WS, 0CD)

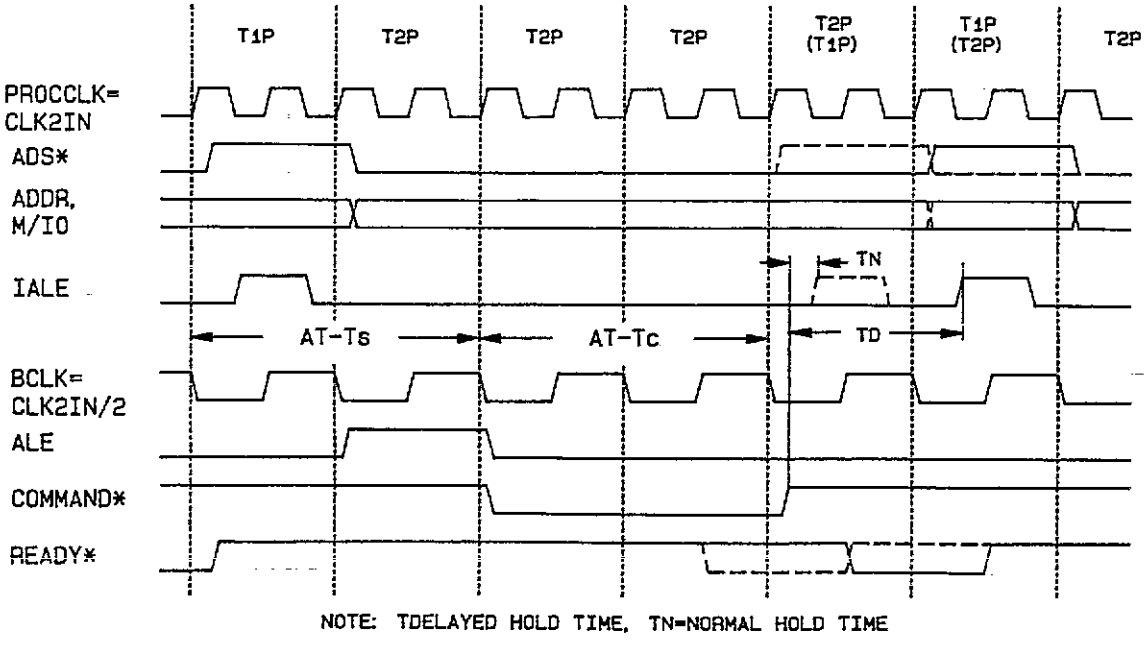


Figure 2.17 Normal Mode AT-bus Cycle with Additional Hold Time(0WS, 0CD)

2.4.2 Quick Mode

This mode is also a synchronous mode. It is enabled by writing a zero to REG61H<6> and making the following clock selections:

PROCCLK	=	CLK2IN
BCLK	=	CLK2IN
SYSCLK	=	CLK2IN/2

In Quick mode, an ALE signal is generated on the AT-bus for both AT-bus and local bus cycles. However, the commands SMEMR*, SMEMW*, MEMR*, MEMW*, IOR*, and IOW* are not issued for local bus cycles.

The sequence diagram for a Quick mode local cycle followed by an AT-bus cycle is shown in Figure 2.18. In this mode, both IALE and ALE are generated in sequences 1 and 2 for the local bus cycle, thereby issuing an ALE for local cycles also. The local cycle is terminated when READY* is sampled low by the 386sx in sequence 3. For the AT-bus cycle, the command is issued in sequence 5. For write cycles, ACEN* is activated in sequence 4 and for read cycles, it is activated in sequence 5. If the next cycle is not an AT-bus write cycle, then ACEN* is deactivated in sequence 6. READY* is sampled low in sequence 7 and the cycle is terminated. As seen, the AT-bus states coincide with the CPU states for AT-bus cycles. Hence, Quick mode is more efficient when switching between local and AT-bus cycles and is useful for high speed AT-bus devices.

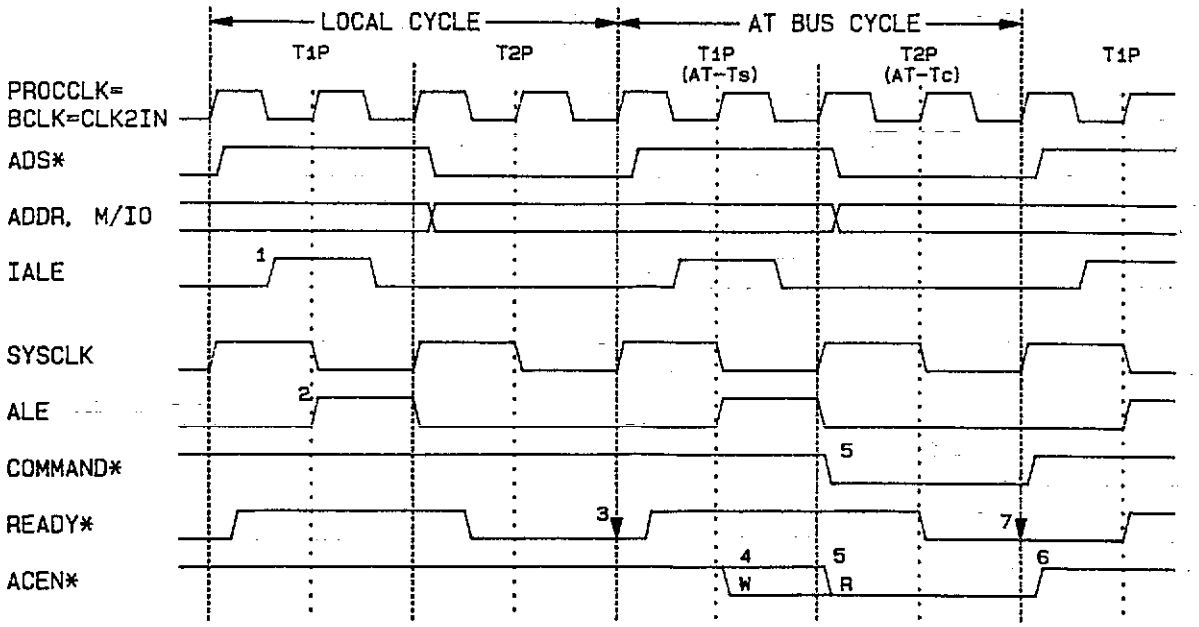


Figure 2.18 Quick Mode Local Cycle Followed by AT-bus Cycle (0WS, 0CD)

2.4.3 Delayed Mode

This mode is another synchronous mode. It is enabled when Quick mode is disabled and the following clock selections are made:

PROCCLK	=	CLK2IN
BCLK	=	CLK2IN
SYSCLK	=	CLK2IN/2

In Delayed mode, ALE and commands SMEMR*, SMEMW*, MEMR*, MEMW*, IOR*, and IOW* are issued only for AT-bus cycles as in Normal mode and are not issued for local cycles. Fig 2.19 shows a Delayed mode AT-bus cycle. IALE is generated in sequences 1 and 2. ALE is asserted in sequence 3 and is de-asserted in sequence 4. Therefore, although the AT-bus states are synchronous, they are delayed with respect to the processor states. Figure 2.19 is an example with two command delays and three wait-states. The dotted lines A and B show commands going active for zero and one command delays. Sequence 5 shows command going active for programmed two command delays. Dotted lines D, E, and F show commands going inactive for zero, one, and two wait-states. Sequence 6 shows commands going inactive for programmed three wait-states. READY* is sampled low by 386sx in sequence 6 to terminate the current cycle. Since AT-bus states are delayed with respect to the processor states, local address lines LA17-LA23 (typically unlatched) are not valid when ALE is active. In order to have these lines valid when ALE is active, they can be latched by EALE* as shown in sequence 7. Sequence 8 and 9 show when ACEN* is asserted for AT-bus write and read cycles respectively. ACEN* is de-asserted in sequence 10. This mode is useful for slow peripherals on the AT-bus.

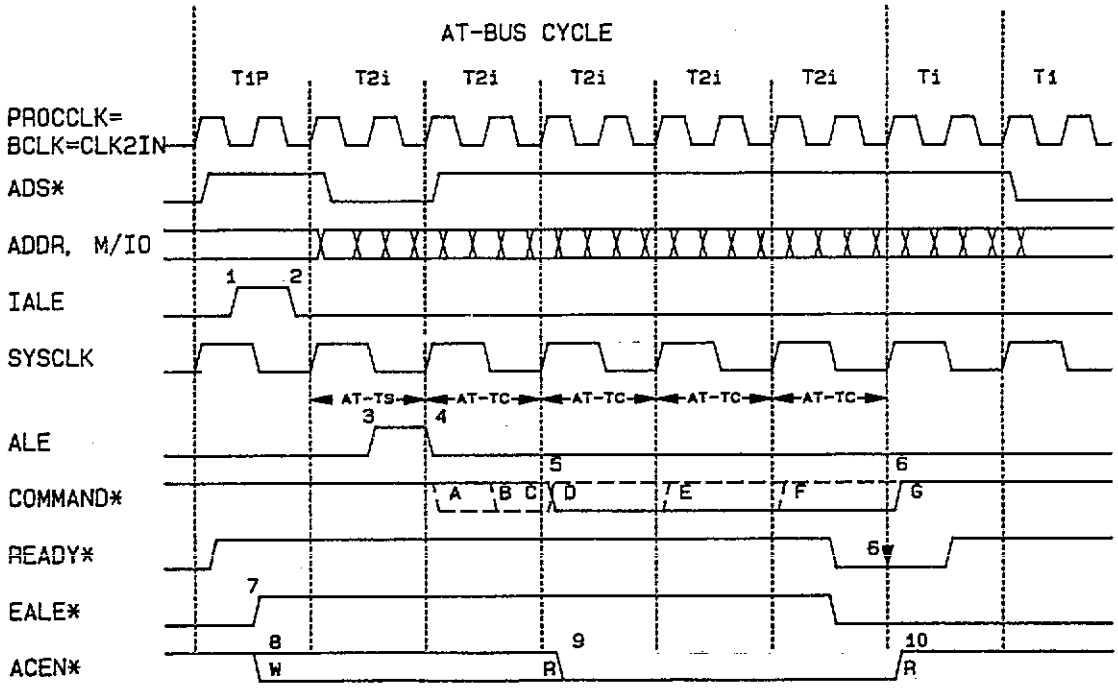


Figure 2.19 Delayed Mode AT-bus Cycle (3WS, 2CD)

2.4.4 External Mode

This is an asynchronous mode. It is enabled when the ATCLK is selected as the source for BCLK and the following clock selections are made:

PROCCLK	=	CLK2IN
BCLK	=	ATCLK
SYSCLK	=	ATCLK/2

Since ATCLK is asynchronous to CLK2IN, the CPU state machine runs asynchronously to the AT-bus state machine. ALE and commands SMEMR*, SMEMW*, MEMR*, MEMW*, IOR*, and IOW* are issued only for AT-bus cycles. Figure 2.20 shows a sequence diagram for an External mode AT-bus cycle. IALE is issued in sequences 1 and 2. ALE is issued in sequences 3 and 4. For a zero command delay and zero wait-states cycle, the command is issued on the AT-bus in sequences 4 and 6, synchronized with BCLK. For write cycles, ACEN* is asserted in sequence 1 and for read cycles, it is asserted in sequence 7. The command inactive state is sampled on every rising edge of CLK2IN. In this case, edge D of CLK2IN samples command high in sequence 8. READY* is asserted in sequence 9, synchronized with CLK2IN which samples in sequence 10 and terminates the cycle.

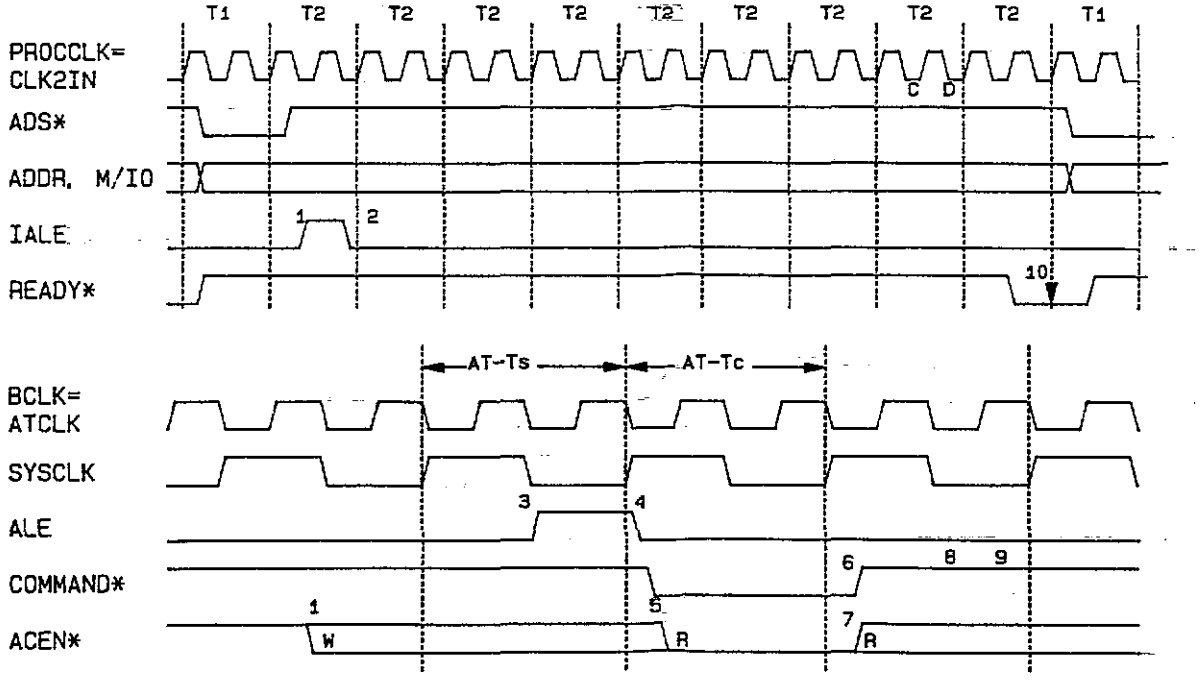


Figure 2.20 External Mode AT-bus Cycle (0WS, 0CD)

2.5 82C841 Configuration/Control Registers:

The 82C841 provides access to Port B defined for the PC AT and bit 7 of the CMOS RAM access port 70H in the system I/O address space.

System I/O Port 61H **Port B**

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PCHK	CHK	T20	RFD	EIC	ERP	SPK	T2G

Bits	Access	Default	Function
7	R	0	PCK - System memory parity check
6	R	0	CHK - System I/O Channel check
5	R	X	T2O - Timer 2 Output
4	R	0	RFD - Refresh Detect
3	R/W	0	EIC - Enable I/O channel check
2	R/W	0	ERP - Enable system parity check
1	R/W	0	SPK - Speaker data
0	R/W	0	T2G - Timer 2 Gate (speaker gate)

System I/O Port 70H **CMOS RAM access Port 70H**

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
NMIEN	....implemented in 80C206....						

Bits	Access	Default	Function
7	R/W	0	System NMI enable
6..0	R/W	X..X	Implemented in 82C206

The 82C841 incorporates bit 7 of the CMOS RAM access port 70H in the system I/O address space.

The following registers are accessed by an indexing scheme, whereby the index value of the register to be accessed is written to I/O port 22H, *followed by the data transaction at I/O* port 23H.

Index: 60H **PROCCLK Register**

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Ver 1	Ver 0	CPU RESET	PCLK SEL	--	RDYNMI EN	--	RDY NMI

Bits	Access	Default	Function
7, 6	R	X, X	82C841 Revision Number
5	R/W	0	Alternate CPU Reset. A low-to-high transition in this bit activates a CPU reset.
4	R/W	0	Processor clock selection 0 = PCLK = CLK2IN 1 = PCLK = BCLK
3	R/W	1	Reserved
2	R/W	0	Local bus READY timeout NMI enable 0 = Disable 1 = Enable
1	R/W	1	Reserved
0	R	0	Local bus READY timeout status 0 = READY timeout has not occurred 1 = READY timeout has occurred 128 cycles after AF16/ has been asserted

Index: 61H **AT BUS Command Delay Register**

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
HOLD TIME DELAY	QUICK MODE	16-BIT CMD DELAY		8-BIT CMD DELAY		I/O CMD DELAY	

Bits	Access	Default	Function
7	R/W	0	Extra address hold time 0 = Disable 1 = Enable
6	R/W	1	Quick Mode 0 = Enable 1 = Disable
5, 4	R/W	0, 0	AT bus 16-bit memory cycles command delay 0 0 = 0 BCLK cycles 0 1 = 1 BCLK cycles 1 0 = 2 BCLK cycles 1 1 = 3 BCLK cycles
3, 2	R/W	0, 1	AT bus 8-bit memory cycles command delay 0 0 = 0 BCLK cycles 0 1 = 1 BCLK cycles 1 0 = 2 BCLK cycles 1 1 = 3 BCLK cycles
1, 0	R/W	0, 1	AT bus I/O cycles command delay 0 0 = 0 BCLK cycles 0 1 = 1 BCLK cycles 1 0 = 2 BCLK cycles 1 1 = 3 BCLK cycles

*** In general, extra address hold time should be set (REG61H<7> = 1) in order to allow sufficient MA bus recovery time after an I/O access to an '841 register.

Index: 62H **AT BUS Wait-state Register**

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
387sx. INST	387sx. RDY	16-BIT		8-BIT WAIT-STATES		BCLK SEL WAIT-STATES	

Bits	Access	Default	Function
7	R	X	387sx Detection Status Flag 0 = No Coprocessor detected 1 = Coprocessor detected
6	R/W	X	Coprocessor READY* source 0 = 82C841 generates READY* 1 = 387sx generates its own READY*
5, 4	R/W	1, 1	AT bus 16-bit wait-state selection 0 0 = 0 wait-states 0 1 = 1 wait-states 1 0 = 2 wait-states 1 1 = 3 wait-states
3, 2	R/W	1, 1	AT bus 8-bit wait-state selection 0 0 = 2 wait-states 0 1 = 3 wait-states 1 0 = 4 wait-states 1 1 = 5 wait-states
1, 0	R/W	0, 0	Bus Clock (BCLK) source selection 0 0 = BCLK = CLK2IN/2 0 1 = BCLK = CLK2IN 1 0 = BCLK = Follow REG. 64H 1 1 = Reserved

*** Bits<1, 0> of index register 62H cannot be written if PROCCLK = BLCK, i.e., if bit 4 of index register 60 is one.

Index: 63H **Reserved**

Index: 64H **ASYNC and Sleep mode Clock Select Register**

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
--	SYSCLK SLEEP	CLK2IN SCALE	SYSCLK SLEEP	CLK2IN SCALE		BCLK SEL	

Bits	Access	Default	Function
7	R/W	1	Reserved
6,4	R/W	0,0	Sleep mode SYSCLK selection 00 = CLK2IN/4 01 = Static (held low) 10 = BCLK/2 11 = Reserved
5,3, 2	R/W	0,0,0	Sleep mode CLK2IN scaling factor 000 = Static (held low) 001 = PROCCLK/8 010 = PROCCLK/16 011 = PROCCLK/32 100 = PROCCLK (no change) 101 = PROCCLK/2 110 = PROCCLK/4 111 = Not used
1, 0	R/W	0, 0	Bus clock (BCLK) source selection 00 = CLK2IN/3 01 = CLK2IN/4 10 = CLK2IN/8 11 = Asynchronous clock (ATCLK)

NOTE: The order of bit fields for this register are assigned to maintain compatibility with earlier versions of the 82C841. Also note that the sleep mode CLK2IN scaling factor only affects PROCCLK if PROCCLK is derived from CLK2IN (except for the static selection 000).

Index: 65H **ROM Configuration Register**

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
WP768	WP832	WP 896	WP 960	SD768	SD832	SD896	SD960

Bits	Access	Default	Function
7	R/W	0	Shadow RAM at C0000H-CFFFFH access rights 0 = Read/Write 1 = Read Only (write protected)
6	R/W	0	Shadow RAM at D0000H-DFFFFH access rights 0 = Read/Write 1 = Read Only (Write protected)
5	R/W	0	Shadow RAM at E0000H-EFFFFH access rights 0 = Read/Write 1 = Read Only (Write protected)
4	R/W	0	Shadow RAM at F0000H-FFFFFH access rights 0 = Read/Write 1 = Read Only (Write protected)
3	R/W	1	ROMCS* for address C0000h-CFFFFH 0 = ROMCS* generated (Shadow RAM disabled) 1 = ROMCS* not generated (Shadow RAM enabled)
2	R/W	1	ROMCS* for address D0000h-DFFFFH 0 = ROMCS* generated (Shadow RAM disabled) 1 = ROMCS* not generated (Shadow RAM enabled)
1	R/W	1	ROMCS* for address E0000h-EFFFFH 0 = ROMCS* generated (Shadow RAM disabled) 1 = ROMCS* not generated (Shadow RAM enabled)
0	R/W	0	ROMCS* for address F0000h-FFFFFH 0 = ROMCS* generated (Shadow RAM disabled) 1 = ROMCS* not generated (Shadow RAM enabled)

Index: 66H **Memory Enable Register 1**

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
512K - 640K	256K - 512K	0K - 256K	--	--	--	--	--

Bits	Access	Default	Function
7	R/W	0	Map RAM address 80000H-9FFFFH on to system board 0 = address is on I/O channel 1 = address is on system board
6	R/W	0	Map RAM address 40000H-7FFFFH on to system board 0 = address is on system board 1 = address is on I/O channel
5	R/W	0	Map RAM address 00000H-3FFFFH on to system board 0 = address is on system board 1 = address is on I/O channel
4..0	R/W	1..1	Reserved

Index: 67H **Memory Enable Register 2**

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
640EN	656EN	672EN	688EN	704EN	720EN	736EN	752EN

Bits	Access	Default	Function
7	R/W	X	Shadow RAM at AC000H-AFFFFH area 0 = Disable 1 = Enable
6	R/W	X	Shadow RAM at A8000H-ABFFFH area 0 = Disable 1 = Enable
5	R/W	X	Shadow RAM at A4000H-A7FFFH area 0 = Disable 1 = Enable
4	R/W	X	Shadow RAM at A0000H-A3FFFH area 0 = Disable 1 = Enable
3	R/W	X	Shadow RAM at BC000H-BFFFFH area 0 = Disable 1 = Enable
2	R/W	X	Shadow RAM at B8000H-BBFFFH area 0 = Disable 1 = Enable
1	R/W	X	Shadow RAM at B4000H-B7FFFH area 0 = Disable 1 = Enable
0	R/W	X	Shadow RAM at B0000H-B3FFFH area 0 = Disable 1 = Enable

Index: 68H **Memory Enable Register 3**

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
880EN	864EN	848EN	832EN	816EN	800EN	784EN	768EN

Bits	Access	Default	Function
7	R/W	X	Shadow RAM at DC000H-DFFFFH area 0 = Disable 1 = Enable
6	R/W	X	Shadow RAM at D8000H-DBFFFH area 0 = Disable 1 = Enable
5	R/W	X	Shadow RAM at D4000H-D7FFFH area 0 = Disable 1 = Enable
4	R/W	X	Shadow RAM at D0000H-D3FFFH area 0 = Disable 1 = Enable
3	R/W	X	Shadow RAM at CC000H-CFFFFH area 0 = Disable 1 = Enable
2	R/W	X	Shadow RAM at C8000H-CBFFFH area 0 = Disable 1 = Enable
1	R/W	X	Shadow RAM at C4000H-C7FFFH area 0 = Disable 1 = Enable
0	R/W	X	Shadow RAM at C0000H-C3FFFH area 0 = Disable 1 = Enable

Index: 69H **Memory Enable Register 4**

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
1008EN	992EN	976EN	960EN	944EN	928EN	912EN	896EN

Bits	Access	Default	Function
7	R/W	X	Shadow RAM at FC000H-FFFFFH area 0 = Disable 1 = Enable
6	R/W	X	Shadow RAM at F8000H-FBFFFH area 0 = Disable 1 = Enable
5	R/W	X	Shadow RAM at F4000H-F7FFFH area 0 = Disable 1 = Enable
4	R/W	X	Shadow RAM at F0000H-F3FFFH area 0 = Disable 1 = Enable
3	R/W	X	Shadow RAM at EC000H-EFFFFH area 0 = Disable 1 = Enable
2	R/W	X	Shadow RAM at E8000H-EBFFFH area 0 = Disable 1 = Enable
1	R/W	X	Shadow RAM at E4000H-E7FFFH area 0 = Disable 1 = Enable
0	R/W	X	Shadow RAM at E0000H-E3FFFH area 0 = Disable 1 = Enable

Index: 6AH **Memory Bank 0/1 Enable Register**

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
DRAM TYPE		NO. OF BANKS	--	--	--	--	--

Bits	Access	Default	Function
7, 6	R/W	1, 0	DRAM types used on system board for banks 0 and 1 0 0 = Disabled 0 1 = 256K and 64K DRAMs (for 640KB combination only) 1 0 = 256Kb DRAMs 1 1 = 1Mb DRAMs
5	R/W	0	Number of DRAM banks used 0 = bank one only 1 = banks one AND two
4..0	R/W	1..1	Reserved

Index: 6BH **DRAM Configuration Register**

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PAGE MODE	MEM RELEC	WAIT STATE	EMS EN	EMS WAIT	CMEM EN	ROM WAIT-STATES	

Bits	Access	Default	Function
7	R/W	1	Page Mode control 0 = Non-page Mode 1 = Page Mode
6	R/W	0	384KB DRAM from A0000H-FFFFFH relocation to 100000H-15FFFFH (for a total memory of 1MB only) 0 = Disable 1 = Enable
5	R/W	1	RAM access wait-states 0 = 0 wait-state 1 = 1 wait-state
4	R/W	0	EMS control 0 = Disable 1 = Enable
3	R/W	0	EMS access wait-states 0 = 0 wait-state 1 = 1 wait-state
2	R/W	0	Cartridge memory access control 0 = Disable 1 = Enable
1, 0	R/W	1, 1	ROM access wait-states 0 0 = 0 wait-state 0 1 = 1 wait-states 1 0 = 2 wait-states 1 1 = 3 wait-states

*** Note: For systems operating at 16 MHz and above, the EMS Wait state option must be configured for 1 EMS Wait State (REG6B<3>=1) for any EMS cycle. This is true regardless of whether the internal EMS registers are being accessed or whether an external EMS chip such as the 82C631 is used.

Index: 6CH **Memory Bank 2/3 Enable Register**

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
DRAM TYPE		NO. OF BANKS	4-WAY	--	--	--	--

Bits	Access	Default	Function
7, 6	R/W	0, 0	DRAM types used on the system board for banks 2 and 3 0 0 = Disabled 0 1 = Reserved 1 0 = 256Kb DRAMs 1 1 = 1Mb DRAMs
5	R/W	0	Number of DRAM banks used 0 = bank two only 1 = banks two and three
4	R/W	0	Page interleaving mode 0 = Enable 2-way page interleave mode 1 = Enable 4-way page interleave mode if all four banks are of same type
3..0	R/W	1..1	Reserved

Index: 6DH **EMS Base Address Register**

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
EMBAS3	EMBAS2	EMBAS1	EMBAS0	EMIO3	EMIO2	EMIO1	EMIO0

Bits	Access	Default	Function
7..4	R/W	X..X	These bits are used for selecting the EMS base addresses (if EMS is enabled) or cartridge ROM memory base addresses (if cartridge is enabled). They are encoded as follows with unused combinations reserved: 0 0 0 0 = C0000H, C4000H, C8000H, CC000H 0 0 0 1 = C4000H, C8000H, CC000H, D0000H 0 0 1 0 = C8000H, CC000H, D0000H, D4000H 0 0 1 1 = CC000H, D0000H, D4000H, D8000H 0 1 0 0 = D0000H, D4000H, D8000H, DC000H 0 1 0 1 = D4000H, D8000H, DC000H, E0000H 0 1 1 0 = D8000H, DC000H, E0000H, E4000H 0 1 1 1 = DC000H, E0000H, E4000H, E8000H 1 0 0 0 = E0000H, E4000H, E8000H, EC000H
3..0	R/W	X..X	These bits are used for the EMS or CROM page registers I/O base address. They are encoded as follows with unused combinations reserved: 0 0 0 0 = 208H/209H 0 0 0 1 = 218H/219H 0 1 0 1 = 258H/259H 0 1 1 0 = 268H/269H 1 0 1 0 = 2A8H/2A9H 1 0 1 1 = 2B8H/2B9H 1 1 1 0 = 2E8H/2E9H

Index: 6EH **Reserved**

Index: 6FH **Miscellaneous Register**

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
EMSIZ2	EMSIZ1	EMSIZ0	EXTEMS	--	RASTIMO DIS	FAST GA20	--

Bits	Access	Default	Function
7..5	R/W	X..X	These bits are used to set the EMS memory size. Memory is allocated from the top of available system memory. 0 0 0 : < 1 MB (for total of 384KB) 0 0 1 : 1MB 0 1 0 : 2MB 0 1 1 : 3MB 1 0 0 : 4MB 1 0 1 : 5MB 1 1 0 : 6MB 1 1 1 : 7MB
4	R/W	0	External EMS mapper existence 0 = Absent 1 = Present
3	R/W	1	Reserved
2	R/W	0	RAS timeout counter for page operation 0 = Enabled 1 = Disabled
1	R/W	1	Address line A20 control 0 = Enable CPUA20 onto A20 1 = GATEA20 input controls CPUA20 onto A20
0	R/W	0	Reserved

Index:70H **Sleep Mode Control Register**

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
SLEEP EN	ENTER SLEEP	COMBO ROM	16-BIT VIDEO	PCU NMI	PCU NMI EN	INT DLY LN	ADDR TO CAS DLY

Bits	Access	Default	Function
7	R/W	0	Sleep mode enable 0 = Disable 1 = Enable
6	R/W	0	Sleep mode request - if sleep mode is enabled, setting this bit will generate PROCCLK at the prescaled sleep frequency following a HLT instruction.
5	R/W	0	Combined system and video BIOS 0 = Separate 1 = Combined
4	R/W	0	16-bit video RAM access mode 0 = Disable 16-bit access and interpret MEMCS16* signal 1 = Enable 16-bit access and ignore MEMCS16* signal
3	R/W	0	PCU NMI status 0 = NMI did not occur 1 = NMI did occur
2	R/W	0	PCU NMI recognition 0 = Disable 1 = Enable
1	R/W	0	Delay Line source for non-page mode operation 0 = External 1 = Internal
0	R/W	0	Column address setup time to CAS 0 = 1/2 CLK2IN cycle 1 = 1 CLK2IN cycle

Index:71H **Programmable I/O decode PORT0 Register 1**

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PDA115	PDA114	PDA113	PDA112	PDA111	PDA110	PDA109	PDA108

Bits	Access	Default	Function
7..0	R/W	X..X	A15-A8 of programmable I/O decode for PORT0

Index:72H **Programmable I/O decode PORT0 Register 2**

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PDA107	PDA106	PDA105	PDA104	PDA103	PDA102	PDA101	PDA100

Bits	Access	Default	Function
7..0	R/W	X..X	A7-A0 of programmable I/O decode for PORT0

Index:73H **Programmable I/O decode PORT0 Enable Register**

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
--	--	RDEN	WREN	MASKA3	MASKA2	MASKA1	MASKA0

Bits	Access	Default	Function
7, 6	R/W	1, 1	Reserved
5	R/W	0	Decode for I/O read operation 0 = Disabled 1 = Enabled
4	R/W	0	Decode for I/O Write operation 0 = Disabled 1 = Enabled
3..0	R/W	0..0	Mask bits for A3-A0. 0 = Disable mask 1 = Enable mask (corresponding address is a don't care)

Index:74H **Programmable I/O decode PORT1 Register 1**

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PDA215	PDA214	PDA213	PDA212	PDA211	PDA210	PDA209	PDA208

Bits	Access	Default	Function
7..0	R/W	X..X	A15-A8 of programmable I/O decode for PORT1

Index:75H **Programmable I/O decode PORT1 Register 2**

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PDA207	PDA206	PDA205	PDA204	PDA203	PDA202	PDA201	PDA200

Bits	Access	Default	Function
7..0	R/W	X..X	A7-A0 of programmable I/O decode for PORT1

Index:76H **Programmable I/O decode PORT1 Enable Register**

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
--	--	RDEN	WREN	MASKA3	MASKA2	MASKA1	MASKA0

Bits	Access	Default	Function
7, 6	R/W	1, 1	Reserved
5	R/W	0	Decode for I/O read operation 0 = Disabled 1 = Enabled
4	R/W	0	Decode for I/O write operation 0 = Disabled 1 = Enabled
3..0	R/W	0..0	Mask bits for A3-A0. 0 = Disable mask 1 = Enable mask (corresponding address is a don't care)

Index:77H **Programmable I/O decode PORT2 Register 1**

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PDA315	PDA314	PDA313	PDA312	PDA311	PDA310	PDA309	PDA308

Bits	Access	Default	Function
7..0	R/W	X..X	A15-A8 of programmable I/O decode for PORT2

Index:78H **Programmable I/O decode PORT2 Register 2**

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PDA307	PDA306	PDA305	PDA304	PDA303	PDA302	PDA301	PDA300

Bits	Access	Default	Function
7..0	R/W	X..X	A7-A0 of programmable I/O decode for PORT2

Index:79H **Programmable I/O decode PORT2 Enable Register**

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
--	SLP CTL	RDEN	WREN	MASKA3	MASKA2	MASKA1	MASKA0

Bits	Access	Default	Function
7	R/W	1	Reserved
6	R/W	0	PGMCS2 output pin as Sleep status pin control 0 = output as PGMCS2* 1 = output as sleep indicator defined as follows: 0 = awake mode 1 = sleep mode
5	R/W	0	Decode for I/O read operation 0 = Disabled 1 = Enabled
4	R/W	0	Decode for I/O write operation 0 = Disabled 1 = Enabled
3..0	R/W	0..0	Mask bits for A3-A0. 0 = Disable mask 1 = Enable mask (corresponding address is a don't care)

The 82C841 (82C841) also provides access to the EMS/cartridge ROM page registers located in system I/O space. If EMS is enabled A23 is zero, thereby always mapping it below 8MB. If cartridge ROM is enabled, A23 is one, thereby always mapping it above 8MB.

Page 0 : 2X8H ; Page 1 : 42X8H ; Page 2 : 82X8H; Page 3 : C2X8H

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PE	A20	A19	A18	A17	A16	A15	A14

Bits	Access	Default	Function
7	R/W	0	EMS/Cartridge ROM page access 0 = Disable 1 = Enable
6..0	R/W	X..X	EMS/cartridge ROM page address A20 to A14

Page 0 : 2X9H ; Page 1 : 42X9H ; Page 2 : 82X9H; Page 3 : C2X9H

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
--	--	--	--	--	--	A22	A21

Bits	Access	Default	Function
7..2	R/W	X..X	Reserved
1, 0	R/W	X..X	EMS/cartridge ROM page address A22 and A21 If EMS is enabled base address selected will be: 0 0 = 0 to 2MB 0 1 = 2 to 4MB 1 0 = 4 to 6MB 1 1 = 6 to 8MB If cartridge ROM is enabled base address selected will be: 0 0 = 8 to 10MB 0 1 = 10 to 12MB 1 0 = 12 to 14MB 1 1 = 14 to 16MB

NOTE: Default values which are shown as "X" are unpredictable values. The BIOS should initialize them to desired values during CHIPSet initialization.

2.6 82C841 Pin Assignments

Type	Symbol	Description
Clocks:		
I	CLK2IN	CLOCK 2 input from a TTL crystal oscillator having a maximum of twice the rated frequency of the 386sx processor clock.
I	ATCLK	EXTERNAL AT CLOCK input from a TTL oscillator, used for the AT-bus operation. It is required only if the AT-bus clock (SYSCLK) is not programmed to be derived from CLK2IN. It should be lower than CLK2IN in frequency and tied low when not used.
I	OSC/12	1/12 of 14.3818 MHz oscillator frequency.
O	PROCCLK	PROCESSOR CLOCK output for the 386sx. It can be programmed to be a derivative of CLK2IN or ATCLK.
O	SYSCLK	AT SYSTEM CLOCK, buffered to drive the SYSCLK line on the AT-bus I/O channel. It is half the frequency of BCLK (an internal clock) and should be between 6 MHz and 8 MHz for maintaining correct AT I/O bus timing compatibility with the IBM PC-AT. It can be programmed to be derived from CLK2IN or ATCLK.
Control Signals		
I	P9*	Processor type selection input, should be tied low.
I	RESET1*	RESET1* is an active low, cold reset input generated by either the power good signal from the power supply or the reset from the power control unit (82C636). It is latched internally and when low activates RESET3 and RESET4.
I	RESET2*	RESET2* is an active low, warm reset input generated from the keyboard controller for a warm reset of the CPU. It forces a CPU reset by activating RESET3, but does not generate RESET4.
O	RESET3	RESET3 is an active high output used to reset the CPU and is active when either RESET1* or RESET2* is active. It is also activated when a shut-down condition in the CPU is detected and when REG60H<5> is programmed for a FAST RESET. RESET3 stays active for at least 64 PROCCLK cycles and is synchronized with PROCCLK.
O	RESET4	RESET4 is an active high signal used to reset the AT-bus, the keyboard controller, the 80C206 IPC, and other peripherals. It is synchronized with the processor clock.

2.6 82C841 Pin Assignments (contd.)

Type	Symbol	Description
CPU Interface		
I/O	READY*	READY is the system ready signal to the CPU used to terminate the current bus cycle after a requested I/O or memory transfer is completed. It is an output for local memory, I/O and AT-bus cycles. It is generated after the chosen number of wait-states for local cycles and after IOCHRDY is high, 0WS* is high, or bus "time out" (if programmed) for AT cycles. It can be programmed as an input for a coprocessor cycle. It is an open collector output requiring an external pull-up resistor of 10K and is connected to the Cpus READY* pin.
I	ADS*	ADDRESS STATUS is an input signal from the CPU indicating that a valid bus cycle definition and address are being driven by the CPU.
I	M/IO*	MEMORY I/O is an input signal from the CPU indicating the type of access for the current cycle. When high it indicates a memory access and when low it indicates an I/O access. A 10Kohm pull-up resistor should be used on this line.
I	D/C*	DATA/CONTROL is an input signal from the CPU that distinguishes data cycles, either memory or I/O from control cycles. When high, it indicates a data cycle, when low it indicates a control cycle. A 10K pull-up resistor is recommended.
I	W/R*	WRITE/READ is an input signal from the CPU that distinguishes write cycles from read cycles. When high, it indicates a write cycle, when low it indicates a read cycle. A 10K pull-up resistor is recommended.
O	HOLD	CPU HOLD REQUEST is an active high output to the CPU and is activated during DMA, Master and refresh cycles.
I	HLDA	HOLD ACKNOWLEDGE is an active high input from the CPU and is generated to indicate that the bus has been relinquished for the requesting master's use. When active it forces all commands (IOR*, IOW*, MEMR*, MEMW*, SMEMR*, SMEMW* and INTA*) to be tri-stated.
I/O	BHE*	BYTE HIGH ENABLE is an active low signal indicating data transfer on the upper byte of the data bus. With A0, it is an input during CPU cycles and is an output during DMA and MASTER cycles. A pull-up resistor of 10K is required on this line.
I/O	XBHE*	X BYTE HIGH ENABLE is an active low signal indicating that the high byte of the data bus is valid. It is an output during CPU and DMA cycles, and an input during MASTER cycles. A 10K pull-up resistor is required on this line.
O	NMI	NON MASKABLE INTERRUPT is an active high output connected to the CPU and is generated by the 82C841.

2.6 82C841 Pin Assignments (contd.)

Type	Symbol	Description
O	IALE	INTERNAL ADDRESS LATCH ENABLE is an active high output synchronous to the PROCCLK and is used to control address latches during bus cycles.
I	IOCHRDY	I/O CHANNEL READY is an active high input from the AT-bus. When low it indicates a not ready condition on the bus and 82C841 inserts wait-states into the AT cycles. When high and after the programmed number of wait-states, the cycle is terminated. A series damping resistor of 33ohms at the AT-bus connector is recommended to limit the negative under shoot. Also a 10K pullup resistor is needed on this line.
I	IOCHCK*	I/O CHANNEL CHECK is an active low input from the AT-bus indicating an error condition on the bus. If enabled, an NMI is generated to signal this error condition to the CPU. A 10K pull-up resistor is needed on this line.
I	PARERR*	PARITY ERROR is an active low input from the 82C242 indicating a memory parity error in the local memory system. It causes an NMI to the CPU if the feature is enabled.
O	ALE	ADDRESS LATCH ENABLE is an active high output to the AT-bus and is synchronous with the AT-bus state machine clock. It is used to latch the addresses in the address latches during AT-bus cycles. This signal should be buffered before driving it to the AT-bus.
O	EALE*	EXTENDED ADDRESS LATCH ENABLE is an active low output used to latch the CPU extended address lines A17-A23 during AT-bus cycles.
I	STANDBY*	STANDBY is an active low signal from the 82C636 indicating that the system is in standby mode. For normal operation, this signal should be high and when low the 82C841 performs only the standby mode functions.
DMA Interface		
I	HRQ	HOLD REQUEST is an active high input when DMA/Master is requesting a bus cycle. For an AT compatible architecture, it should be connected to the HOLD REQUEST signal from DMA1 and DMA2.
O	HLDA1	HOLD ACKNOWLEDGE 1 is an active high output generated during a DMA cycle to indicate that the bus has been granted in response to the HOLD REQUEST.
I	AEN1*	ADDRESS ENABLE 1 is an active low input from one of the two DMA controllers enabling the address latches for 8 bit DMA transfers.

2.6 82C841 Pin Assignments (contd.)

Type	Symbol	Description
I	AEN2*	ADDRESS ENABLE 2 is an active low input from one of the two DMA controllers enabling the address latches for 16 bit DMA transfers.
BUS Input		
I	MEMCS16*	MEMORY CHIP SELECT 16 is an active low input from the AT-bus, indicating a 16 bit memory transfer. If high, it implies an 8 bit memory transfer. A pull-up resistor of 330 ohms is required on this line.
I	IOCS16*	I/O CHANNEL SELECT 16 is an active low input from the AT-bus, indicating a 16 bit I/O transfer. If high, it implies an 8 bit I/O transfer. A pull-up resistor of 330 ohms is required on this line.
I	0WS*	ZERO WAIT-STATE is an active low input from the AT-bus, causing immediate termination of the current AT-bus cycle. Memories requiring zero wait-states use this line to speed up memory cycles. A pull-up of 330 ohms is required on this line.
Device Decode		
O	8042CS*	8042 CHIP SELECT is an active low output for the keyboard controller chip select. It is generated whenever the ports on the keyboard controller are accessed for I/O operations.
O	ASRTC	ADDRESS STROBE TO RTC is an active high signal used to select the real-time clock registers on the 82C206. It is generated whenever the ports on the real-time clock are accessed for I/O operations.
O	PGMCS*<0:2>	PROGRAMMABLE CHIP SELECTs 0:2 are active low signals and can be generated on I/O accesses to any I/O port address or range. This signal generation can be controlled by programming the associated chipset registers where the addresses and access rights can be programmed. PGMCS2* can also function as a sleep status indicator.
O	VRAMSEL*	VIDEO RAM SELECT is an active low signal indicating that the current cycle is accessing the video RAM area. This is used by the 82C636 for controlling the power to the video subsystem.
Refresh		
I	REFREQ	REFRESH REQUEST from 82C636 is an input signal initiating a DRAM refresh sequence. It is active low for normal mode and active high for stand-by mode. It indicates that a refresh to the DRAMs is to be performed. The refresh rate is controlled by the timer in the 82C206 during normal mode and by the 82C636 during the stand-by mode..

2.6 82C841 Pin Assignments (contd.)

Type	Symbol	Description
I/O	REF*	REFRESH is an active low signal. As an open-drain output, it indicates a refresh cycle is in progress. As an input, it can be used to force a refresh cycle from an external source. A pull-up of 10K is required on this line.
AT-BUS Interface		
I/O	MEMR*	AT-BUS MEMORY READ is an active low signal used to control the memory read cycle on the AT-bus. It is an output when the CPU is controlling the bus and is an input when a DMA controller is controlling the bus.
I/O	MEMW*	AT-BUS MEMORY WRITE is an active low signal used to control the memory write cycle on the AT-bus. It is an output when the CPU is controlling the bus and is an input when a DMA controller is controlling the bus.
O	SMEMR*	LOW 1MEG AT-BUS MEMORY READ is an active low output signal used to control the memory read cycle on the AT-bus. It is generated for a write cycle to memory below 1 Mb.
O	SMEMW*	LOW 1MEG AT-BUS MEMORY WRITE is an active low output signal used to control the memory write cycle on the AT-bus. It is generated for a read cycle from memory below 1 Mb.
I/O	IOR*	AT-bus I/O READ is an active low signal directing an I/O port on the AT-bus to place data on the AT-bus. It is an output if the CPU is controlling the bus and is an input if a DMA controller is controlling the bus.
I/O	IOW*	AT-bus I/O WRITE is an active low signal directing an I/O port on the AT-bus to accept data from the AT-bus. It is an output if the CPU is controlling the bus and is an input if a DMA controller is controlling the bus.
O	TMRGATE	TIMER GATE is an active high output to enable the 8254 compatible counter timer in the 82C206 to generate the tone signal for the speaker.
I	TMROUT2	TIMER OUT 2 is an active high input from the 8254 compatible counter timer in the 82C206 that can be read from the system PORT B on the 82C841.
O	SPKDATA	SPEAKER DATA is an active high output used to gate the tone signal from the 8254 compatible timer on the 82C206 to the speaker.
O	INTA*	INTERRUPT ACKNOWLEDGE is an active low output to the 82C206 interrupt controller indicating that the current cycle is an interrupt acknowledge cycle.

2.6 82C841 Pin Assignments (contd.)

Type	Symbol	Description
I	INTR	INTERRUPT REQUEST is an active high input from the interrupt controller in the 82C206 indicating that an interrupt has occurred. This signal is also driven into the interrupt pin on the CPU.
Buffer Control		
O	SDIR0	SYSTEM BUS DIRECTION 1 is an output to control the low byte data path between the SD bus and the MD bus. When low it sets the data path from the SD bus to MD bus and when high the data path is set from MD bus to SD bus.
O	SDIR1	SYSTEM BUS DIRECTION 0 is an output to control the high byte data path between the SD bus to the MD bus. When low it sets the data path from the SD bus to MD bus and when high the data path is set from MD bus to SD bus.
O	ACEN*	ACTION CODE ENABLE is an active low output that validates the action code signals AC<1, 0> and is used by the 82C242 in bus sizing and byte assembly control. This signal is also used to latch the data from the AT-bus.
O	AC<1, 0>	ACTION CODE 1 and 0 is a two bit encoded output command used by the 82C242 for bus sizing and byte assembly operations.
O	XDEN*	X DATA BUFFER ENABLE is an active low output asserted during I/O accesses to port 22H and to port 23H when the index register chosen lies within the 82C841's range of 60H-7FH. This signal is also generated for accesses to system PORT 61H and 70H, which are incorporated within the 82C841. This signal is used to enable the buffers between the XD bus and MA bus during accesses to the 82C841 internal registers.
Memory Control		
I	A<23:10>	ADDRESS input lines A23 through A10 from the CPU local bus
I/O	A<9:0>	ADDRESS lines A9 through A0. During CPU cycles they are inputs from the CPU local bus. During refresh cycles, they are outputs containing the refresh addresses. A1 is also used to detect halt and shutdown conditions of the CPU and A0 is used to generate the enable signal for the data bus transceivers.
I/O	SA0	AT-BUS ADDRESS 0 is an output during CPU, 16 bit DMA and refresh cycles, and is an input during 8 bit DMA and MASTER cycles.
I	GATEA20	GATE ADDRESS 20 is an input from the keyboard controller used control propagation of A20 from CPU on to the bus. When high, it propagates Cpus A20 line to the bus on the GA20 line. When low, it will force bus GA20 line only if the Fast Gate A20 is also trying to force it low.

2.6 82C841 Pin Assignments (contd.)

Type	Symbol	Description
I/O	GA20	GATED ADDRESS 20 is the Address 20 output gated by the GATEA20 signal or internal Fast GATEA20 bit during CPU cycles. During DMA/Master cycles it is an input from the bus.
O	ROMCS*	ROM CHIP SELECT is an active low chip select output to the BIOS EPROM. It is generated for accesses to the BIOS ROM area, whose address ranges are programmable.
O	CROMCS*	CARTRIDGE MEMORY CHIP SELECT is an active low chip select output and is generated whenever an access is made to the cartridge memory area. The exact address range for which this is generated is programmable within the 82C841.
Numeric Coprocessor (NPX) Interface		
I	NPBUSY*	NUMERIC CO-PROCESSOR BUSY is an active low input from the NPX, indicating that it is currently executing a command. A 10Kohm pull-up resistor is required on this line.
O	BUSY*	BUSY is an active low output to the CPU initiated by the NPX, indicating that the NPX is busy. A 10Kohm pull-up resistor is required on this line.
I	ERROR*	ERROR FROM NUMERIC CO-PROCESSOR is an active low input from the NPX indicating that an error condition has occurred within the NPX. A 10Kohm pull-up resistor is required on this line.
O	NPINT	NUMERIC CO-PROCESSOR INTERRUPT is an active high output interrupt request generated due to an NPX error condition. It is connected to the IRQ13 on the 82C206 in a PC-AT environment. A 10Kohm pull-up resistor is required on this line.
O	NPRESET	NUMERIC CO-PROCESSOR RESET is an active high reset output to the NPX. It is active when RESET4 is active or when a write operation is made to system Port 0F1H. In the later case, it is active for the period of the command.
DRAM Interface		
O	RAS<3:0>*	ROW ADDRESS STROBES 3 to 0 are active low outputs used as RAS signals to the DRAMs for selecting different banks. RAS3* selects the highest bank and RAS0* selects the lowest bank. These signals should be terminated before driving the DRAM RAS lines with 33 ohm series resistors to reduce ringing.
O	CAS00*	COLUMN ADDRESS STROBE 00 is an active low output used to select the low byte DRAMS of bank 0. This signal should be terminated before driving the DRAM CAS line with a 33 ohm series resistor to reduce ringing.

2.6 82C841 Pin Assignments (contd.)

Type	Symbol	Description
O	CAS01*	COLUMN ADDRESS STROBE 01 is an active low output used to select the high byte DRAMS of bank 0. This signal should be terminated before driving the DRAM CAS line with a 33 ohm series resistor to reduce ringing.
O	CAS10*	COLUMN ADDRESS STROBE 10 is an active low output used to select the low byte DRAMS of bank 1. This signal should be terminated before driving the DRAM CAS line with a 33 ohm series resistor to reduce ringing.
O	CAS11*	COLUMN ADDRESS STROBE 11 is an active low output used to select the high byte DRAMS of bank 1. This signal should be terminated before driving the DRAM CAS line.with a 33 ohm series resistor to reduce ringing.
O	CAS20*	COLUMN ADDRESS STROBE 20 is an active low output used to select the low byte DRAMS of bank 2. This signal should be terminated before driving the DRAM CAS line with a 33 ohm series resistor to reduce ringing.
O	CAS21*	COLUMN ADDRESS STROBE 21 is an active low output used to select the high byte DRAMS of bank 2. This signal should be terminated before driving the DRAM CAS line with a 33 ohm series resistor to reduce ringing.
O	CAS30*	COLUMN ADDRESS STROBE 30 is an active low output used to select the low byte DRAMS of bank 3. This signal should be terminated before driving the DRAM CAS line with a 33 ohm series resistor to reduce ringing.
O	CAS31*	COLUMN ADDRESS STROBE 30 is an active low output used to select the high byte DRAMS of bank 3. This signal should be terminated before driving the DRAM CAS line with a 33 ohm series resistor to reduce ringing.
O	MWE*	MEMORY WRITE ENABLE is an active low output to enable writes to the DRAM. It should be buffered and terminated with a 33 ohm series resistor before driving the WE* lines on the DRAMs.
O	DLE	DATA LATCH ENABLE is an active high output used to latch the local memory in the 82C242.
O	DRD*	DATA READ is an active low output used to transfer data from the memory bus to the local CPU bus in the 82C242. If high it sets the data path from the local CPU bus to the memory bus and if low it sets the data path from the memory bus to the local CPU data bus.
O	DLYOUT	DELAY LINE OUT is an active high output to the external delay line used for DRAM control.

2.6 82C841 Pin Assignments (contd.)

Type	Symbol	Description
I	DLY<2:0>	DELAY IN 0, 1 and 2 are active high inputs from the first three taps on the external delay line used to generate DRAM control signals in non-page mode.
O	XDIR	X BUS DIRECTION is an output used to control the drivers between the X bus and SD bus. The driver should be used such that when high data path is from SD bus to X bus and when low data path is from the X bus to SD bus.
O	MA<9:8>	DRAM ADDRESS 9 and 8 are address lines 9 and 8 outputs for the DRAMs. These lines should be buffered and terminated with 33 ohm series resistors before driving the DRAM address lines. During a cartridge memory cycle, these lines provide address 22 and 21 respectively.
I/O	MA<7:0>	MULTIPLEXED DRAM ADDRESS lines MA7 to MA0. These bi-directional lines are used to drive the addresses 7 through 0 to the DRAMs during a DRAM cycle. They should be buffered and terminated with 33 ohm series resistors before driving the DRAM address lines. These lines also act as the 8-bit data path during accesses to the 82C841 internal registers. They act as inputs when the registers are read, and as outputs when the registers are written. An external buffer should be used to isolate this data path during normal DRAM cycles and the buffer should be enabled using XDEN*. During a cartridge memory cycle, MA6:0 provide the address 20:14 and MA7 provides address 23.
Miscellaneous		
I	SGLROM	SINGLE ROM is an input to indicate the data path width of the BIOS EPROM. A high at this input is interpreted as an 8-bit data path indicating only one ROM is used. A low is interpreted as a 16-bit data path, indicating a pair of ROMS are used with odd and even byte split. This input should be tied high or low depending on the ROM data width.
I	NMIIN	NMI INPUT from PCU is an active high signal from the 82C636 indicating that an NMI condition exists in the system.
I	XEMS*	EXTERNAL EMS is an active low input indicating that an external mapper chip address translation is in progress for an EMS access.
I	CPTEST	CHIPs TEST is an input pin used for test purposes only. For normal operations this pin should be tied low on the system.
I	VCC	+5V is the power input to the 82C841. If the system implements the suspend and resume function, this input should be tied to the power plane on which the local memory DRAMs reside.
I	GND	GROUND

2.7 Pinout List

Pin	Name	Pin	Name	Pin	Name
1	GA20	49	DLE	97	INTA*
2	D/C*	50	XEMS*	98	INTR
3	W/R*	51	NMIIN	99	CPTEST
4	NPCS*	52	HLDA1	100	MWE*
5	GATEA20	53	XDIR*	101	GND
6	HOLD	54	VCC	102	RAS0*
7	HLDA	55	GND	103	RAS1*
8	VCC	56	SYSCLK	104	RAS2*
9	BHE*	57	SGLROM	105	RAS3*
10	XBHE*	58	XDEN*	106	DLYOUT
11	NMI	59	MA9	107	DLY2
12	IALE	60	MA8	108	DLY1
13	GND	61	MA7	109	DLY0
14	READY*	62	MA6	110	NPRESET
15	P9*	63	MA5	111	NPINT
16	M/IO*	64	MA4	112	ERROR*
17	CLK2IN	65	GND	113	NPBUSY*
18	VCC	66	MA3	114	BUSY*
19	GND	67	MA2	115	CROMCS*
20	PROCCLK	68	MA1	116	ROMCS*
21	PGMCS0*	69	MA0	117	SA0
22	PCMCS1*	70	VCC	118	A0
23	PGMCS2*	71	ASRTC	119	A1
24	VRAMSEL*	72	STANDBY*	120	A2
25	RESET3	73	GND	121	A3
26	RESET4	74	CAS00*	122	A4
27	SDIR0	75	CAS01*	123	A5
28	SDIR1	76	CAS10*	124	A6
29	ACEN*	77	CAS11*	125	A7
30	AC0	78	CAS20*	126	VCC
31	AC1	79	CAS21*	127	GND
32	GND	80	CAS30*	128	OSC/12
33	SPKDATA	81	CAS31*	129	A8
34	TMRGATE	82	GND	130	A9
35	IOR*	83	IOCHRDY	131	A10
36	IOW*	84	IOCHK*	132	A11
37	TMROUT2	85	PARERR*	133	A12
38	SMEMR*	86	ALE	134	A13
39	SMEMW*	87	EALE*	135	A14
40	MEMR*	88	RESET2*	136	A15
41	MEMW*	89	HRQ	137	A16
42	REF*	90	VCC	138	A17
43	REFREQ	91	GND	139	A18
44	RESET1*	92	AEN1*	140	A19
45	GND	93	AEN2*	141	A20
46	ATCLK	94	MEMCS16*	142	A21
47	8042CS*	95	IOCS16*	143	A22
48	DRD*	96	0WS*	144	A23

Name-	Pin	Name	Pin	Name-	Pin
0WS*	96	DLE	49	MWE*	100
P9*	15	DLY0	109	NMI	11
8042CS*	47	DLY1	108	NMIIN	51
A0	118	DLY2	107	NPBUSY*	113
A1	119	DLYOUT	106	NPCS*	4
A10	131	DRD*	48	NPINT	111
A11	132	EALE*	87	NPRESET	110
A12	133	ERROR*	112	OSC/12	128
A13	134	GA20	1	PARERR*	85
A14	135	GATEA20	5	PCMCS1*	22
A15	136	GND	13	PGMCS0*	21
A16	137	GND	19	PGMCS2*	23
A17	138	GND	32	PROCCLK	20
A18	139	GND	45	RAS0*	102
A19	140	GND	55	RAS1*	103
A2	120	GND	65	RAS2*	104
A20	141	VCC	70	RAS3*	105
A21	142	GND	73	READY*	14
A22	143	GND	82	REF*	42
A23	144	GND	91	REFREQ	43
A3	121	GND	101	RESET1*	44
A4	122	GND	127	RESET2*	88
A5	123	HLDA	7	RESET3	25
A6	124	HLDA1	52	RESET4	26
A7	125	HOLD	6	ROMCS*	116
A8	129	HRQ	89	D/C*	2
A9	130	IALE	12	W/R*	3
AC0	30	INTA*	97	SA0	117
AC1	31	INTR	98	SDIR0	27
ACEN*	29	IOCHK*	84	SDIR1	28
AEN1*	92	IOCHRDY	83	SGLROM	57
AEN2*	93	IOCS16*	95	SMEMR*	38
ALE	86	IOR*	35	SMEMW*	39
ASRTC	71	IOW*	36	SPKDATA	33
ATCLK	46	M/IO*	16	STANDBY*	72
BHE*	9	MA0	69	SYSCLK	56
BUSY*	114	MA1	68	TMRGATE	34
CAS00*	74	MA2	67	TMROUT2	37
CAS01*	75	MA3	66	VCC	18
CAS10*	76	MA4	64	VCC	54
CAS11*	77	MA5	63	VCC	90
CAS20*	78	MA6	62	VCC	8
CAS21*	79	MA7	61	VCC	126
CAS30*	80	MA8	60	VRAMSEL*	24
CAS31*	81	MA9	59	XBHE*	10
CLK2IN	17	MEMCS16*	94	XDEN*	58
CPTEST	99	MEMR*	40	XDIR*	53
CROMCS*	115	MEMW*	41	XEMS*	50

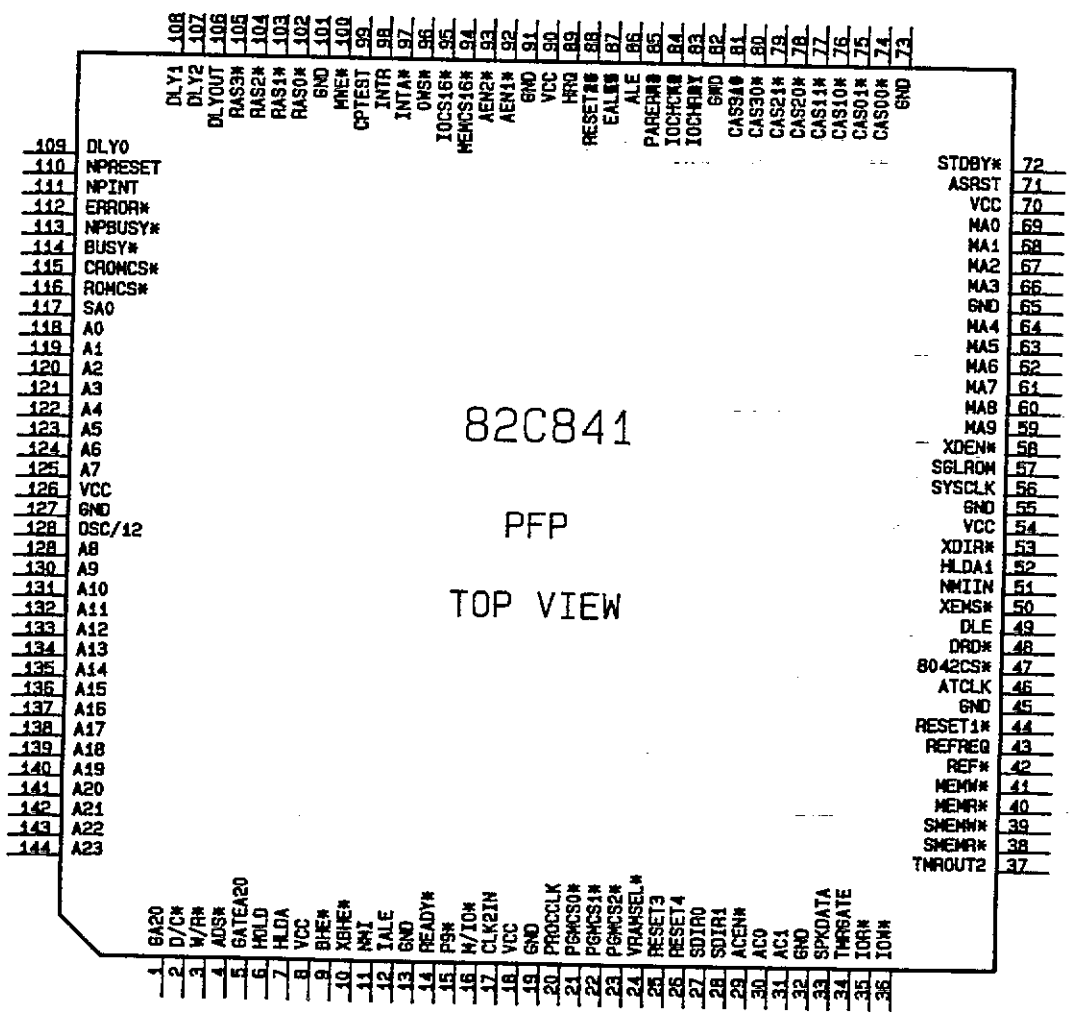
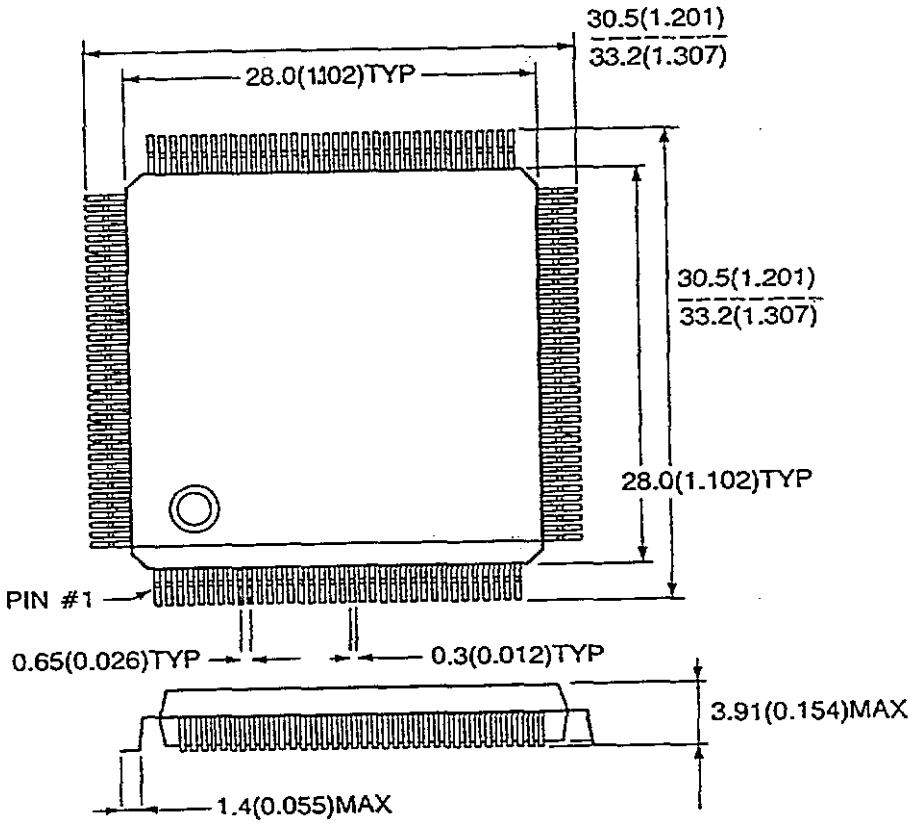


Figure 2.21 82C841 Pin Diagram

2.8 Physical Dimensions

144-Pin Plastic Flat Package (Square) Dimensions: mm(in)



2.9 82C841 Absolute Maximum Ratings

Parameter	Symbol	Min.	Max.	Units
Supply Voltage	V_{CC}	-	7.0	V
Input Voltage	V_I	-0.5	5.5	V
Output Voltage	V_O	-0.5	5.5	V
Operating Temperature	T_{OP}	-25°	85°	C
Storage Temperature	T_{STG}	-40°	125°	C

NOTE: Permanent device damage may occur if Absolute Maximum Ratings are exceeded. Functional operation should be restricted to the conditions described under Operating Conditions.

2.10 82C841 Operating Conditions

Parameter	Symbol	Min.	Max.	Units
Supply Voltage	V_{CC}	4.75	5.25	V
Ambient Temperature	T_A	0°	70°	C

2.11 82C841 DC Characteristics (T_A = 0C to 70C; V_{CC} = 5V +/- 5%)

Parameter	Symbol	Min.	Max.	Units
Input Low Voltage	V_{IL}	-	0.8	V
Input High Voltage	V_{IH}	2.0	-	V
Output Low Voltage	V_{OL}	-	0.45	V
Output High Voltage	V_{OH}	2.4	-	V
Input Low Current ($0 < V_{IN} < V_{CC}$)	I_{IL}	-	±10	mA
Power Supply Current @ 16MHz	I_{CC}			mA
Output High-Z Leakage Current ($0 < V_{IN} < V_{CC}$)	I_{OZI}	-	±10	uA
Static Power Supply Current	I_{CCSB}			mA

I_{OH} and I_{OL} - Output drive capability (for both V_{OH} and V_{OL})

$I_{OL}=I_{OH}$=4mA: HOLD, NMI, IALE, PGMCS2*-PGMCS0*, VRAMSEL*, RESET3, RESET4, SDIR1, SDIR0, ACEN*, AC0, AC1, SPKDATA, TMRGATE, SMEMR*, SMEMW*, 8042CS*, DRD*, DLE, XDIR, HLDA1, SYSCLK, XDEN*, MA9, MA8, ASRTC, ALE, EALE*, MWE*, INTA*, DLYOUT, NPRESET, BUSY*, NPINT, CROMCS*, ROMCS*.

$I_{OL}=I_{OH}$=8mA: GA20, XBHE*, BHE*, READY*, PROCCLK, IOR*, IOW*, MEMR*, MEMW*, REF*, MA7-MA0, CAS31*-CAS00*, RAS3*-RAS0*, SA0, A9-A0.

Power Supply Current I_{cc}

Mode	16 MHz		20 MHz		Units
	Typ	Max	Typ	Max	
Normal	82	115	-	130	mA
Sleep mode	18	33	-	39	mA
Stand-by	120	260	-	260	uA

Note:
1. Power consumption measured using 2 MB of local DRAM and double ROMs.
2. Normal mode measurements made at DOS prompt.
3. Sleep mode measurements made at DOS prompt and using Chips and Technology BIOS for LeAPSet and the smart sleep feature.

2.12 82C841 AC Characteristics

(T_A = 0°C to 70°C, V_{CC} = 5V ± 5%, C_L = 75pF)
(Min and Max values in nanoseconds)

Sym	Description	16 MHz		20 MHz	
		Min	Max	Min	Max
t1	ALE active delay from $SYSCLK_L$	-10	10	-10	10
t2	ALE inactive delay from $SYSCLK_H$	-10	12	-10	12
t3	COMMAND active delay from SYSCLK	-10	16	-10	16
t4	COMMAND inactive delay from $SYSCLK_H$	-14	15	-14	15
t5	EALE* active delay from $SYSCLK_L$	0	31	0	25
t5a	EALE* inactive delay from $PROCCLK_L$	1	18	1	15
t6	MEMCS16* set-up time to $SYSCLK_H$	12	-	12	-
t7	MEMCS16* hold time to $SYSCLK_H$	4	-	4	-
t8	IOCS16* set-up time to $SYSCLK_L$	10	-	10	-
t9	IOCS16* hold time to $SYSCLK_H$	10	-	10	-
t10	0WS* set-up time to $SYSCLK_L$	15	-	15	-
t11	0WS* hold time to $SYSCLK_L$	2	-	2	-
t12	IOCHRDY set-up time to $SYSCLK_H$	11	-	11	-
t13	IOCHRDY hold time to $SYSCLK_H$	4	-	4	-
t14	IALE active delay from $PROCCLK_L$	1	15	1	12
t15	IALE inactive delay from $PROCCLK_L$	2	12	2	10
t20	RESET3 active delay from $PROCCLK_H$	3	17	0	13
t21	RESET3 inactive delay from $PROCCLK_L$	3	17	0	13
t22	RESET4 active delay from $PROCCLK_H$	3	17	0	13
t23	RESET4 inactive delay from $PROCCLK_L$	3	17	0	13
t24	SDIR<1:0> active delay from $SYSCLK_L$	0	40	0	40
t25	SDIR<1:0> inactive delay from $SYSCLK_H$	-14	15	-14	15
t26	ACEN* active delay from $SYSCLK_L$	0	30	0	30
t27	ACEN* inactive delay from $SYSCLK_H$	-16	13	-16	13
t32	AC0 active delay from $PROCCLK_H$	5	35	5	35
t33	AC0 inactive delay from $PROCCLK_H$	5	35	5	35
t34	AC1 active delay from $PROCCLK_H$	5	35	5	35
t35	AC1 inactive delay from $PROCCLK_H$	5	35	5	35
t38	HOLD active delay from $SYSCLK_H$	-50	50	-50	50
t39	HOLD inactive delay from $SYSCLK_H$	-10	50	-10	50
t40	REF* active delay from $HLDA_H$	0	50	0	50
t43	REF* inactive delay from $SYSCLK_H$	0	25	0	25
t44	MEMR* active delay from $SYSCLK_H$	-10	16	-10	16
t45	MEMR* inactive delay from $SYSCLK_H$	-10	12	-10	12
t46	HRQ set-up time to $SYSCLK_H$	40	-	40	-
t47	HRQ hold time to $SYSCLK_H$	4	-	4	-
t49	HLDA1 active delay from $HLDA_H$	2	35	2	35
t51	HLDA1 inactive delay from $HLDA_L$	0	26	0	24
t52	NPCS* active delay from $PROCCLK_H$	-	45	-	45
t53	Overlap of NPBUSY* and ERROR* (both low)	50	-	50	-

2.12 82C841 AC Characteristics (continued)

(T_A = 0°C to 70°C, V_{CC} = 5V ± 5%, C_L = 75pF)
(Min and Max values in nanoseconds)

Sym	Description	16 MHz Min	16 MHz Max	20 MHz Min	20 MHz Max
t54	NPINT delay from NPBUSY*, ERROR* low	-	32	-	25
t55	NPINT inactive delay from ERROR*$_H$	-	32	-	25
t60	BUSY* active delay from NPBUSY*$_L$	-	18	-	18
t61	BUSY* inactive delay from NPBUSY*$_H$	-	15	-	15
t62	BUSY* inactive delay from IOW*	-	20	-	20
t63	NPRESET active delay from IOW*	-	20	-	20
t64	NPRESET inactive delay from IOW*	-	20	-	20
t66	Address set-up time to PROCCLK$_H$	19	-	3	-
t67	Address hold time to PROCCLK$_L$	17	-	12	-
t68	CLK2IN$_L$ to PROCCLK$_L$ delay	-	32	-	25
t69	CLK2IN$_H$ to PROCCLK$_H$ delay	-	32	-	25
t70	PROCCLK$_H$ to SYSCLK$_H$ delay (normal mode)	0	20	0	16
t71	PROCCLK$_H$ to SYSCLK$_L$ delay (normal mode)	0	20	0	16
t72	PROCCLK$_H$ to SYSCLK$_H$ delay (1/3 mode)	-	24	-	20
t73	PROCCLK$_H$ to SYSCLK$_L$ delay (1/3 mode)	-	20	-	20
t74	ATCLK$_H$ to PROCCLK$_H$ delay	0	30	0	30
t75	ATCLK$_L$ to PROCCLK$_L$ delay	0	30	0	30
t76	ATCLK$_H$ to SYSCLK$_H$ delay	0	30	0	30
t77	ATCLK$_H$ to SYSCLK$_L$ delay	0	30	0	30
t80	ADS-setup time to PROCCLK$_H$	19	-	19	-
t81	ADS- hold time from PROCCLK$_H$	6	-	6	-
t82	M/IO -setup time to PROCCLK$_H$	19	-	19	-
t83	M/IO- hold time from PROCCLK$_H$	9	-	9	-
t85	PROCCLK$_H$ to SYSCLK$_H$ delay (quick mode)	0	20	0	20
t86	PROCCLK$_H$ to SYSCLK$_L$ delay (quick mode)	0	20	0	20
t101	RAS$_i$* active delay from PROCCLK$_H$ (non-page)	5	18	5	18
t102	RAS$_i$* inactive delay from PROCCLK$_H$ (non-page)	5	28	5	28
t103	DLYOUT active delay from RAS$_{i\,L}$*	0	5	0	5
t104	DLYOUT inactive delay from RAS$_{i\,H}$*	0	8	0	8
t105	Column address stable from DLY0$_H$	5	20	5	20
t106	Column address hold from DLY0$_L$	0	22	0	22
t107	CAS$_i$* active delay from DLY1$_H$	5	15	5	15
t108	CAS$_i$* inactive delay from DLY1$_L$	6	17	6	17
t111	READY* active delay from PROCCLK$_L$	5	28	5	22
t112	READY* inactive delay from PROCCLK$_H$	6	30	6	25
t113	DRD* active delay from PROCCLK$_H$	10	19	10	19
t114	DRD* hold time from DLE$_L$	13	-	13	-
t115	DLE active delay from DLY1$_H$	0	30	0	22

2.12 82C841 AC Characteristics (continued)

(T_A = 0°C to 70°C, V_{CC} = 5V ± 5%, C_L = 75pF)
(Min and Max values in nanoseconds)

Sym	Description	16 MHz Min	16 MHz Max	20 MHz Min	20 MHz Max
t116	DLE inactive delay from $PROCCLK_H$	0	24	0	20
t119	GA20 valid delay from CPUA20 valid	0	25	0	20
t120	GA20 invalid delay from CPUA20 invalid	0	25	0	20
t122	MWE* active delay from $PROCCLK_H$	0	30	0	25
t123	MWE* inactive delay from $PROCCLK_H$	0	20	0	15
t126	CAS_i* active delay from $PROCCLK_H$	6	21	6	17
t127	CAS_i* inactive delay from $PROCCLK_H$	5	21	5	17
t128	DRD* inactive delay from $PROCCLK_H$	5	24	5	24
t129	CAS_i* inactive delay from DLE inactive	-	5	-	5
t130	RAS_i* active delay from $PROCCLK_H$ (page-mode)	5	20	5	17
t131	Row address set-up time to $RAS_i{}^*{}_L$	8	-	8	-
t132	Row address hold time from $PROCCLK_H$	6	28	6	25
t133	RAS_i* inactive delay from $PROCCLK_H$ (page-mode)	0	32	0	28
t134	RAS_i* precharge time (page mode)		4 X PROCCLK		
t135	ROMCS* active delay from $PROCCLK_H$	0	30	0	25
t136	ROMCS* inactive delay from $PROCCLK_H$	0	30	0	20
t137	DLE hold time from DRD^*_H	0	10	0	8
t138	RAS<0-3>* inactive from REF^*_L	0	24		24
t139	RAS<0-3>* active from $MEMR^*_L$	5	24	5	24
t140	RAS<0-3>* inactive from $MEMR^*_H$	5	30	5	30
t141	RAS<1,2>* active from $RAS<0,3>^*_L$		1 X PROCCLK		
t142	RAS<1,2>* inactive from $RAS<0,3>^*_H$		1 X PROCCLK		
t143	Address set-up time to $MEMR^*_L$	10	-	10	-
t144	Address hold time from REF^*_H	-	50	-	50
t145	Refresh address delay	-	10	-	10
t149	RAS<0-3>* inactive from $HLDA1_H$	0	40	0	40
t150	RAS_i* active from COMMAND active	-	25	-	25
t151	RAS_i* inactive from COMMAND inactive	-	25	-	25
t154	Column address stable from $DLY0_H$ (for DMA)	-	18	-	18
t155	CAS_i* active delay from $DLY1_H$ (for DMA)	-	22	-	22
t156	CAS_i* inactive from COMMAND inactive (for DMA)	-	22	-	25
t160	XEMS* set-up time from $PROCCLK_L$	13	-	7	-
t161	XEMS* hold time from $PROCCLK_L$	10	-	10	-
t168	GA20 valid from REF^*_H	-	30	-	25
t169	GA20 valid from $HLDA1_L$	-	30	-	25
t170	XDEN* active delay from $XIOR^*_L$ or $XIOW^*_L$	4	25	4	25
t171	XDEN* inactive delay from $XIOR^*_H$ or $XIOW^*_H$	4	20	4	20

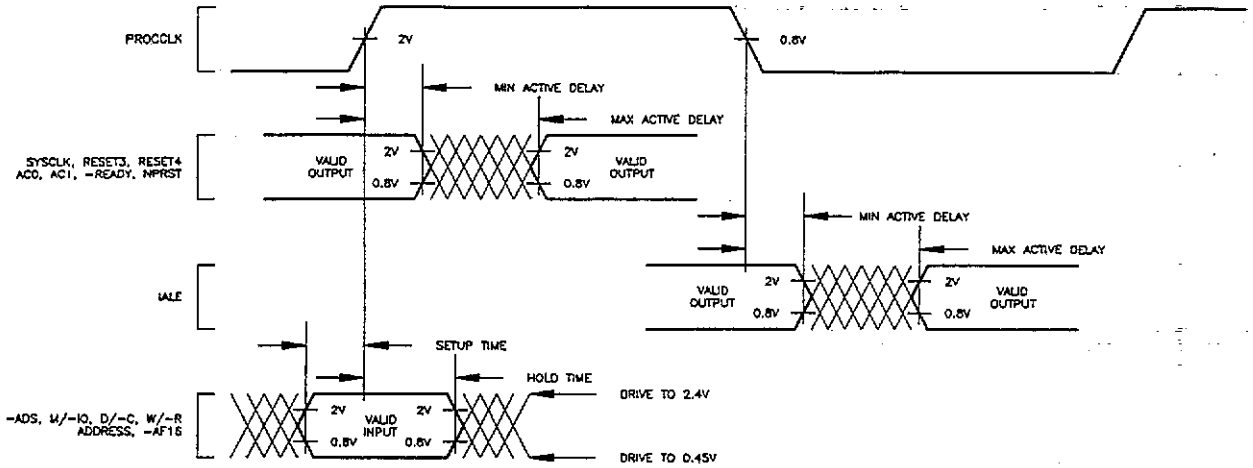
2.12 82C841 AC Characteristics (continued)

(T_A = 0°C to 70°C, V_{CC} = 5V ± 5%, C_L = 75pF)
(Min and Max values in nanoseconds)

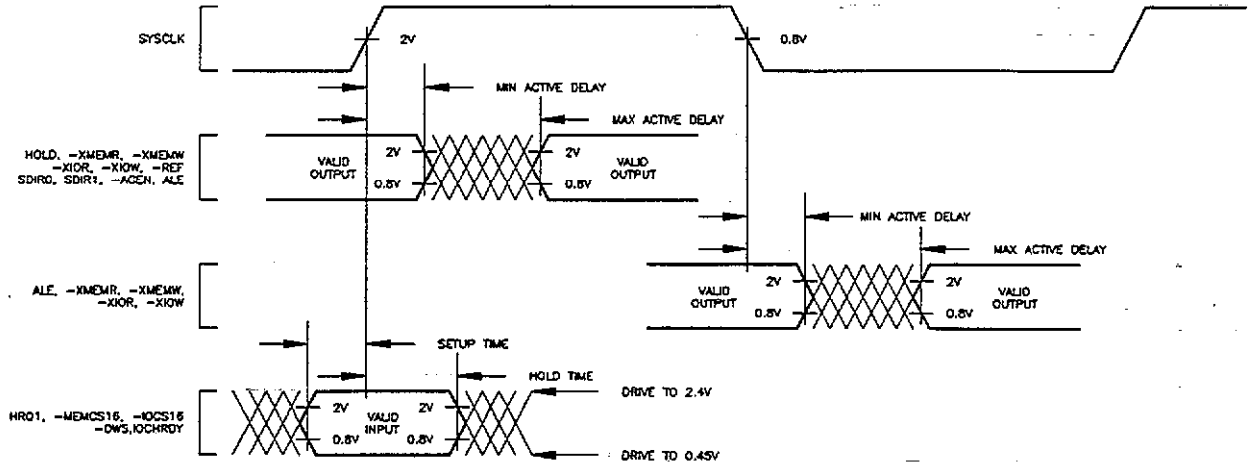
Sym	Description	16 MHz Min	16 MHz Max		20 MHz Min	20 MHz Max
t172	XDIR* active delay from $XIOR*_L$	4	25		4	25
t173	XDIR* inactive delay from $XIOR*_H$	4	20			20
t174	XBHE* active delay from $PROCCLK_H$	-	32	-	-	28
t175	XBHE* inactive delay from $PROCCLK_H$	-	32	-	-	28
t176	SA0 active delay from $PROCCLK_H$	-	40		-	35
t177	SA0 inactive delay from $PROCCLK_H$	-	40		-	35
t200	8042CS* active delay from $PROCCLK_L$	-	30		-	25
t201	8042CS* inactive delay from $PRCOCLK_L$	-	30		-	25
t202	ASRTC active delay from $XIOW*_L$	-	15		-	15
t203	ASRTC inactive delay from $XIOW*_H$	-	15		-	15
t204	PGMCS<0:2>* active delay from $PROCCLK_H$	0	40		0	35
t205	PGMCS<0:2>* inactive delay from $PROCCLK_H$	0	16		0	13
t206	CROMCS* active delay from $PROCCLK_H$	0	30		0	25
t207	CROMCS* inactive delay from $PROCCLK_H$	0	25		0	20
t208	VRAMSEL* active delay from $PROCCLK_H$	-	30		-	25
t209	VRAMSEL* inactive delay from $PROCCLK_H$	-	30		-	25

NOTES: - Signal names with a subscript of 'L' refers to low going edge and 'H' refers to high going edge.
- COMMAND refers to IOR*, IOW*, MEMR*, MEMW*, SMEMR* and SMEMW*

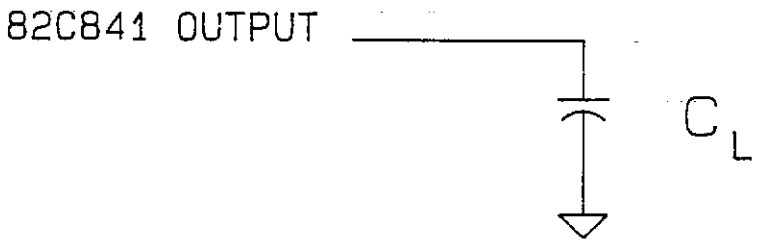
2.13 82C841 AC Timing Diagrams



82C841 Setup, Hold and Active Delay Timings Relative to PROCCLK

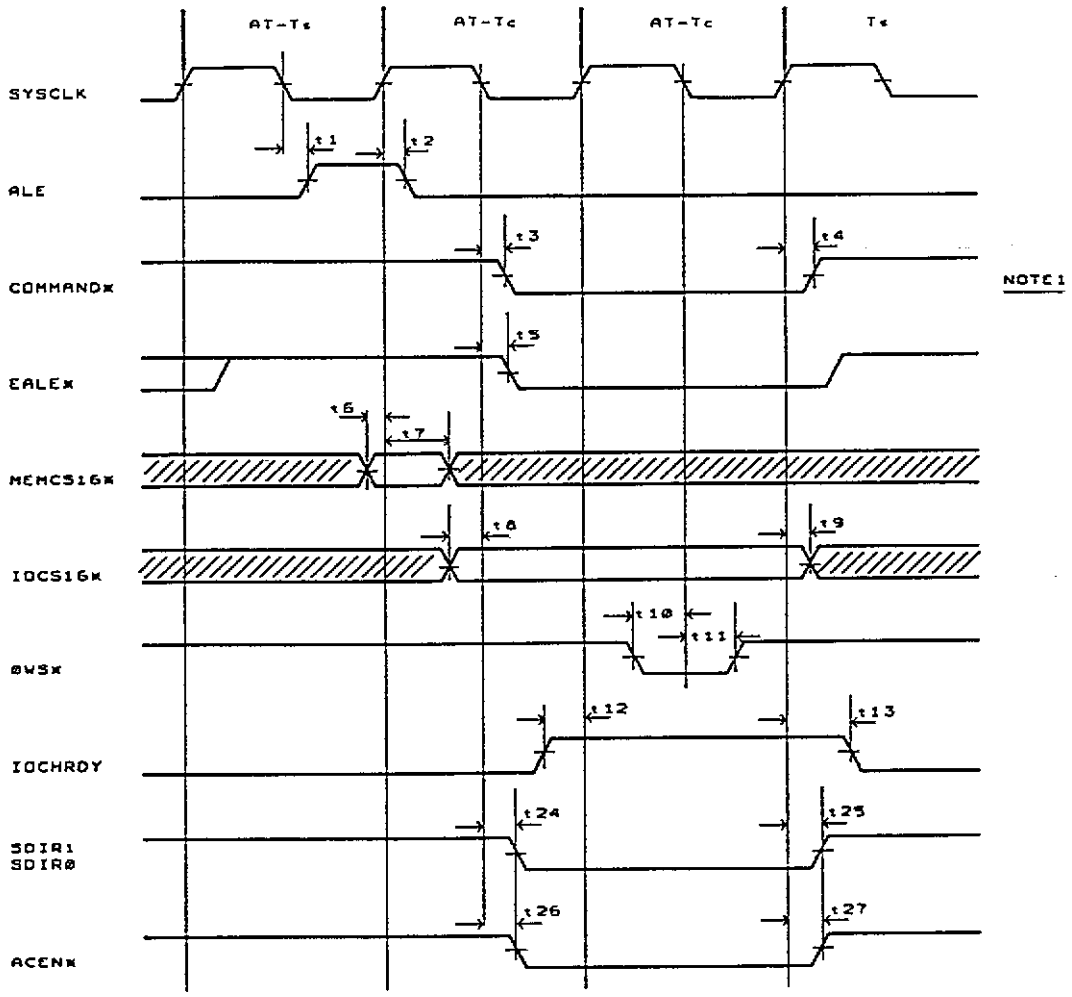


82C841 Setup, Hold and Active Delay Timings Relative to SYSCLK



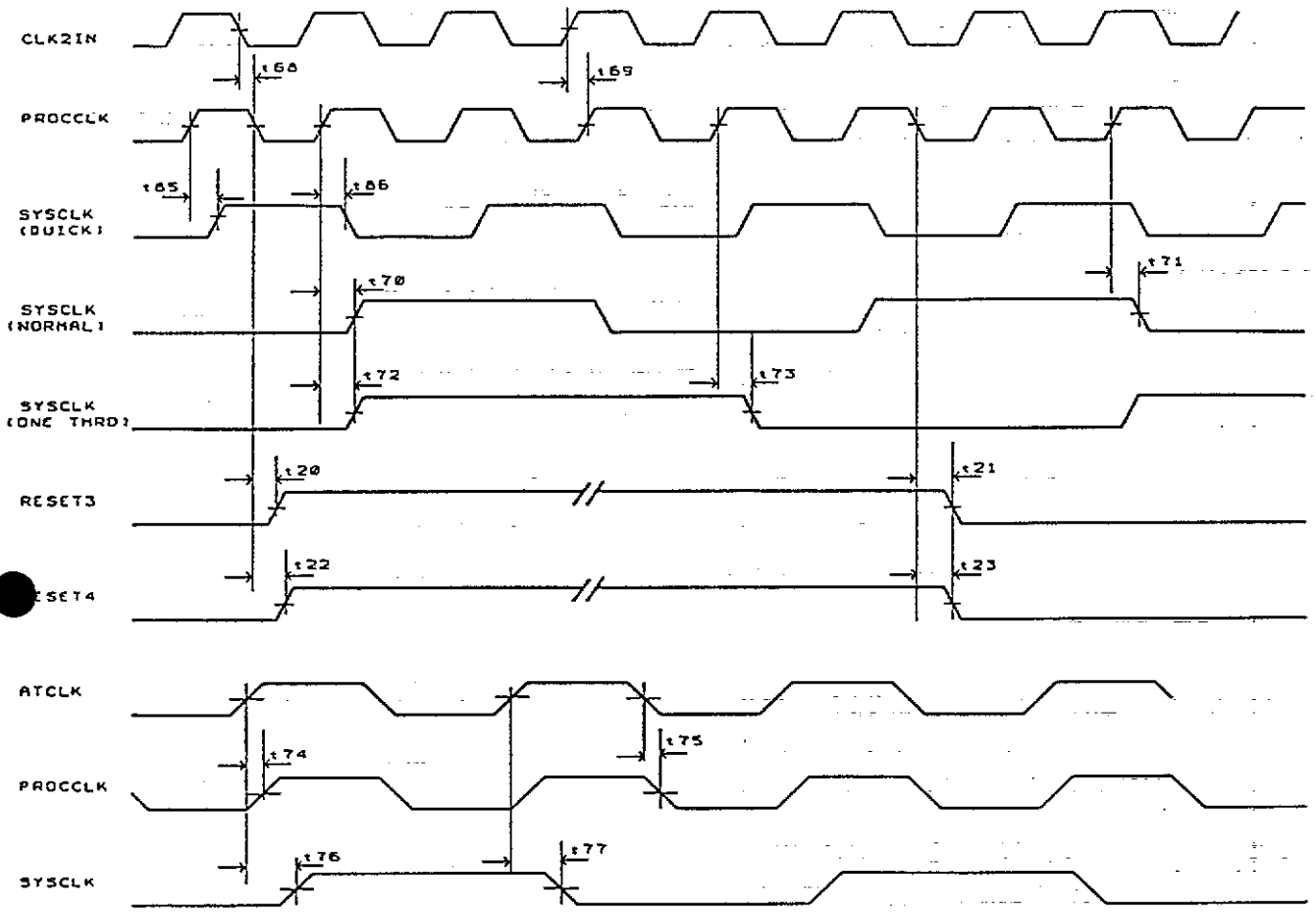
82C841 Test Load

2.13 82C841 AC Timing Diagrams (continued)



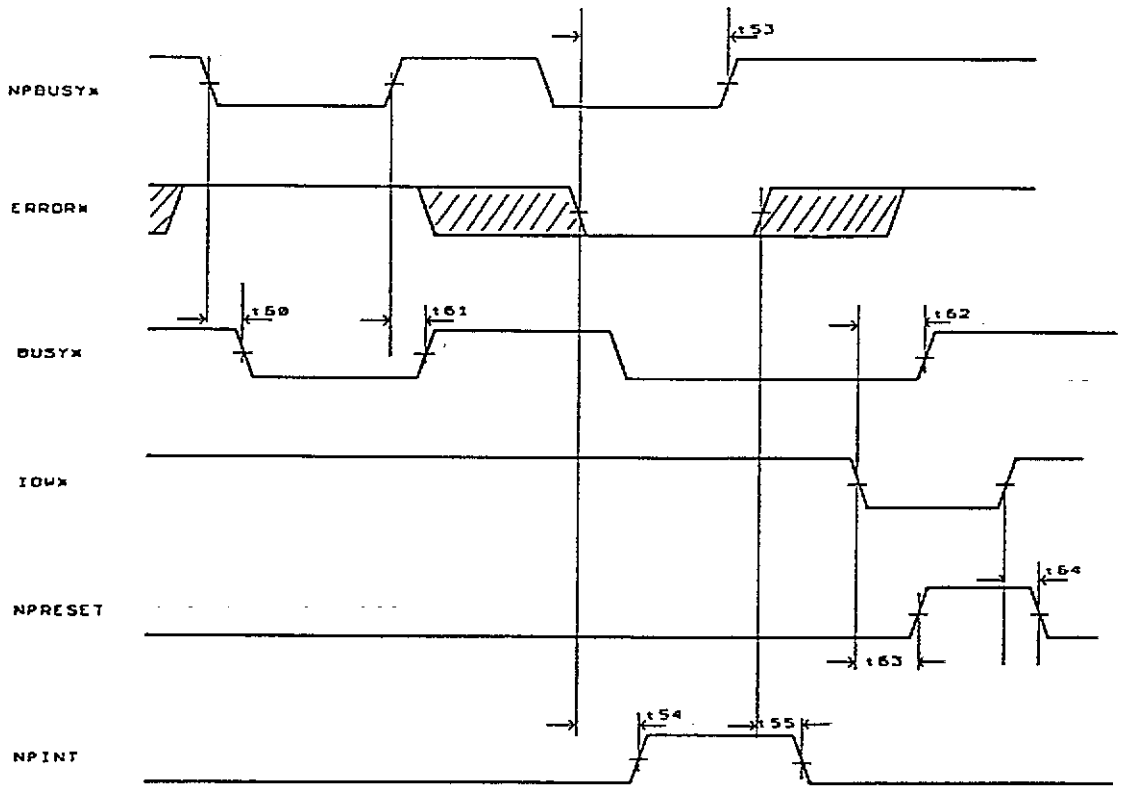
AT bus timing

2.13 82C841 AC Timing Diagrams (continued)



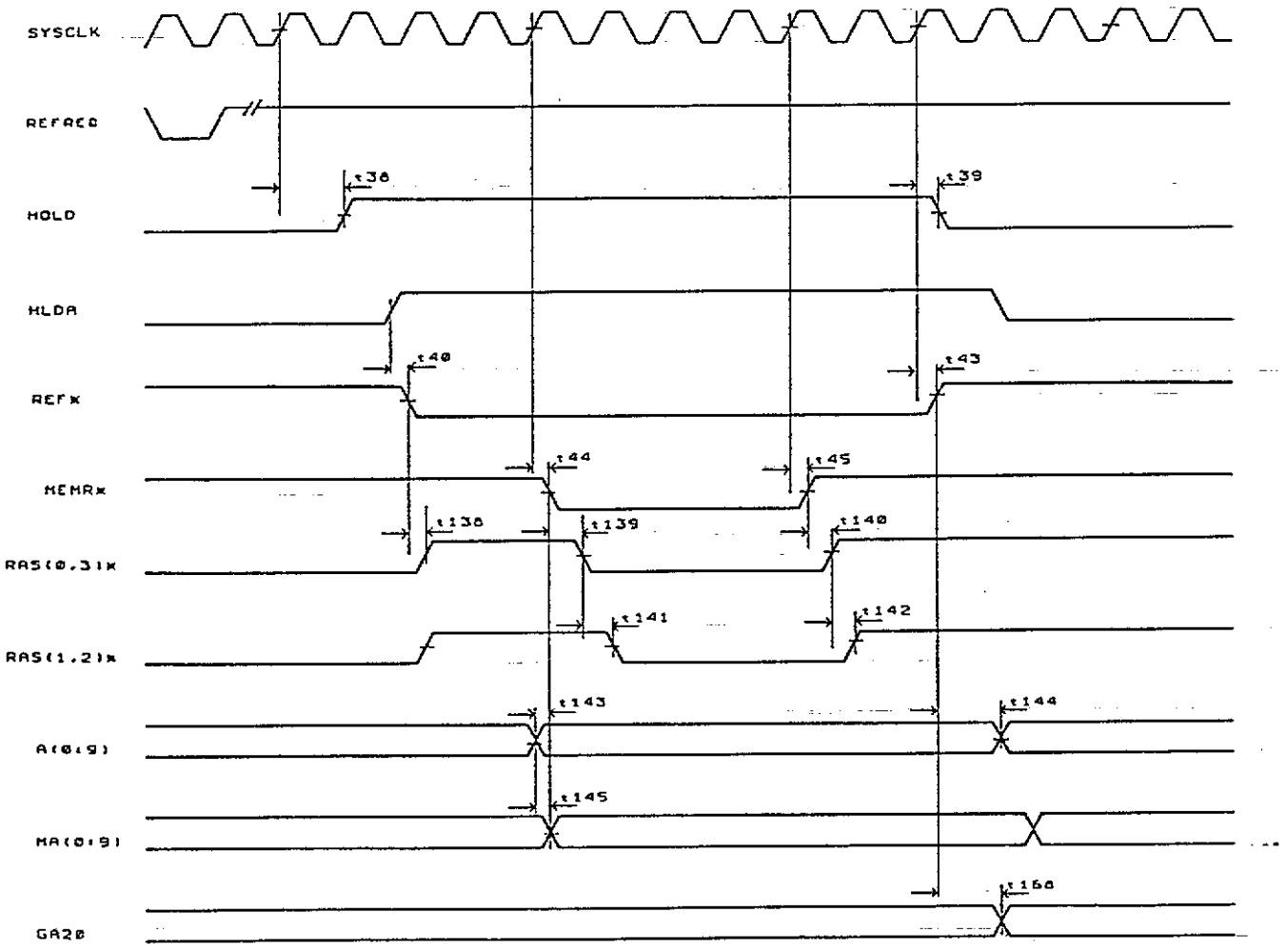
Sytem Clocks and Reset signals

2.13 82C841 AC Timing Diagrams (continued)



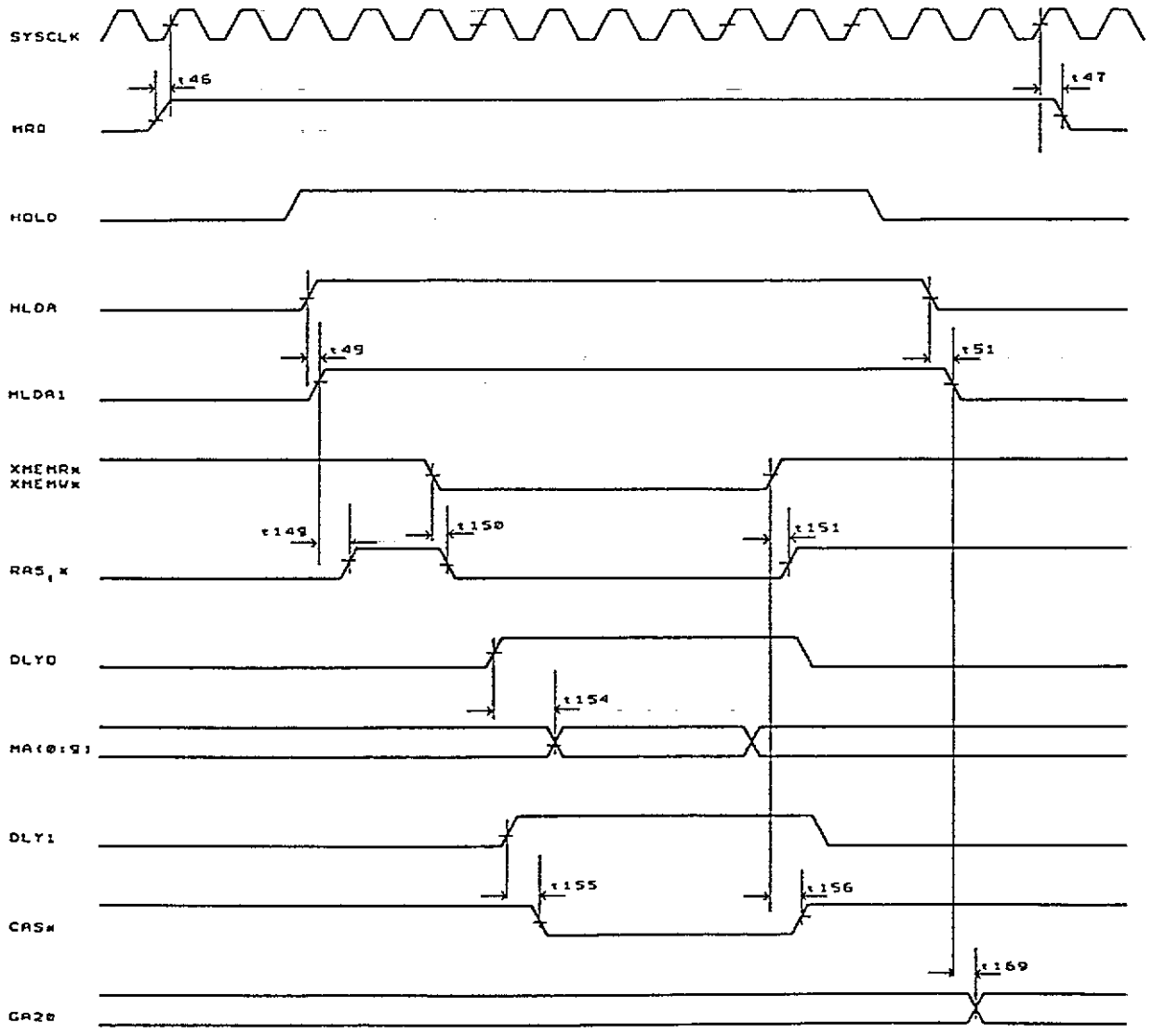
Numeric Processor Interface

2.13 82C841 AC Timing Diagrams (continued)



Refresh cycle

2.13 82C841 AC Timing Diagrams (continued)



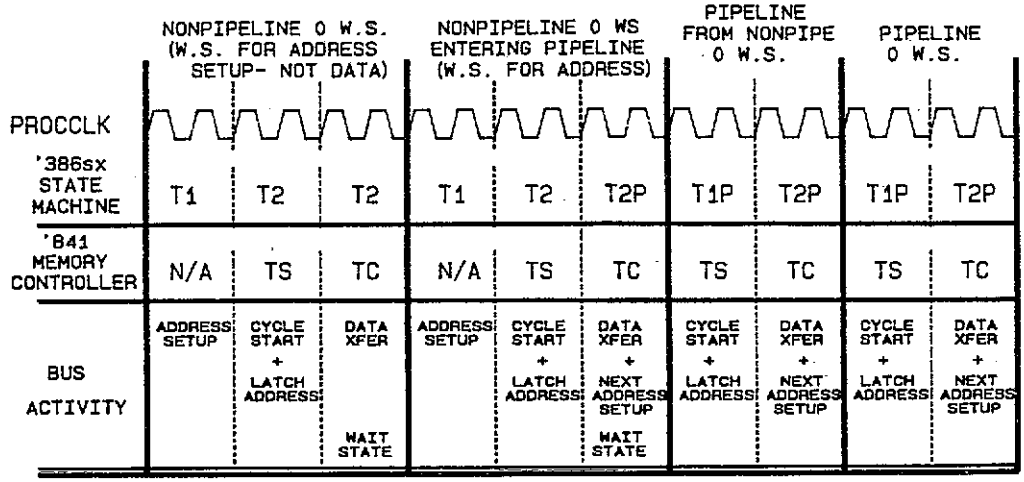
DMA cycle

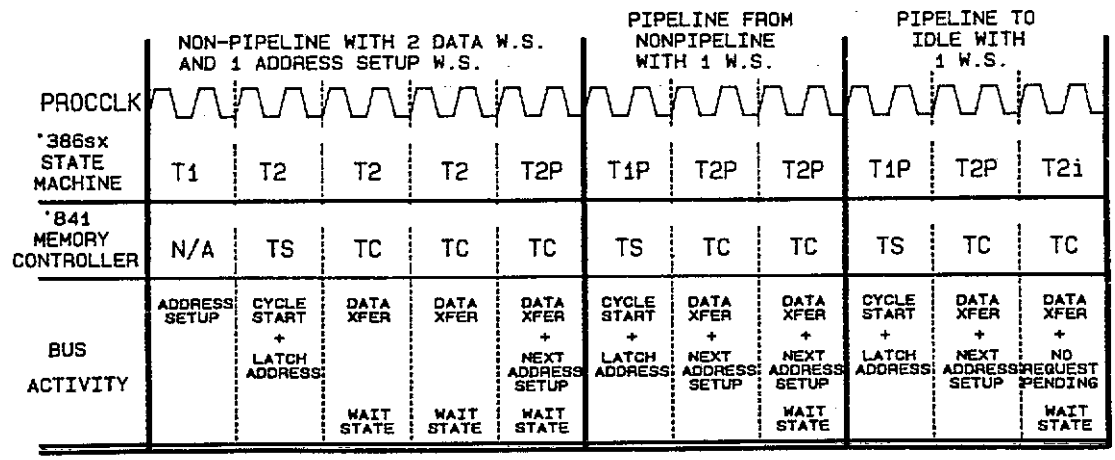
2.13 82C841 AC Timing Diagrams (continued)

'286 TO '386sx CONVERSION CHART FOR INTERPRETING MEMORY TIMING DIAGRAMS			
'286 EQUIVALENT	'386sx NON-PIPELINE EQUIVALENT	'386sx PIPELINE EQUIVALENT	GENERAL BUS ACTIVITY
N/A	T1	N/A	NONPIPELINE ADDRESS SETUP
TS	FIRST T2	T1P	LATCH ADDRESS
FIRST TC	SECOND T2	FIRST T2P	DATA XFER
SUBSEQUENT TC	SUBSEQUENT T2	SUBSEQUENT T2P	WAIT STATES

TYPICAL EXAMPLES:

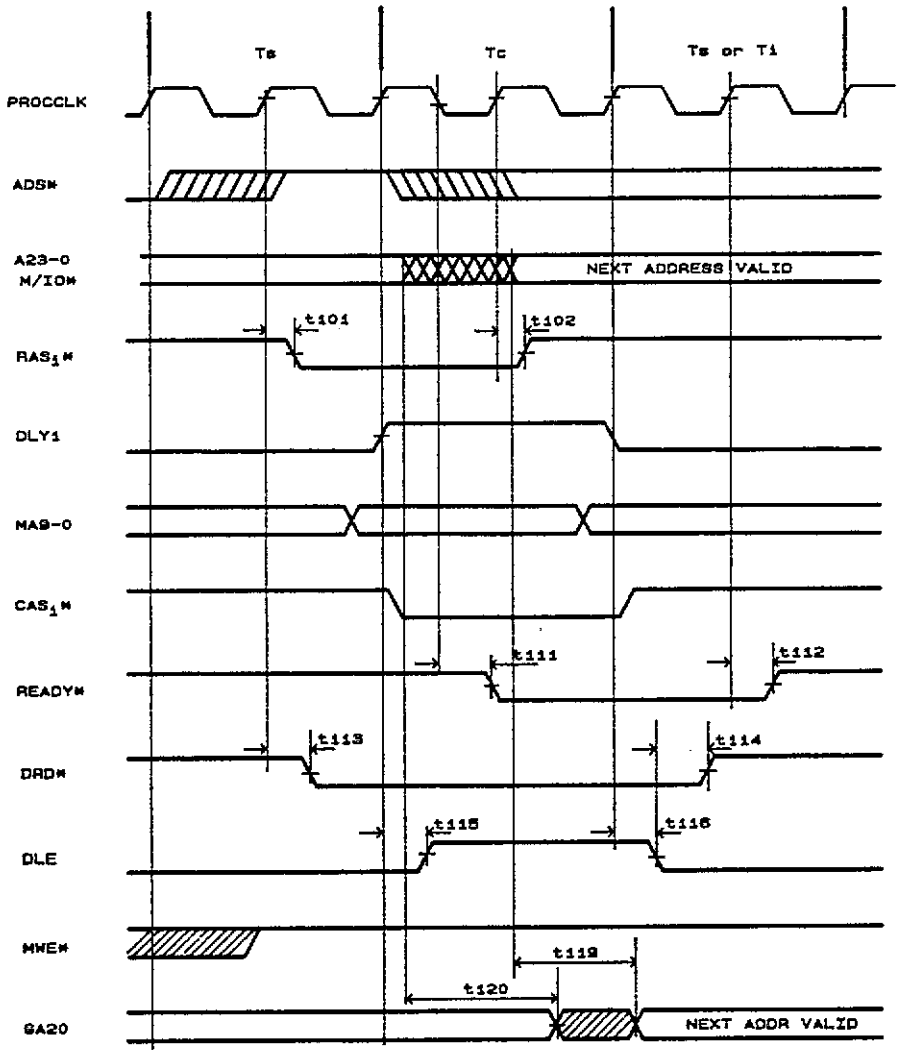
CYCLES ARE SHOWN IN ORDER TO COMPARE '386SX Tx NUMBERS WITH '841 MEMORY CONTROLLER ('286 TYPE) Tx NUMBERS. WAIT STATES HAVE BEEN ARBITRARILY ADDED FOR ILLUSTRATION ONLY.





'386sx T State to '841 T State Conversion

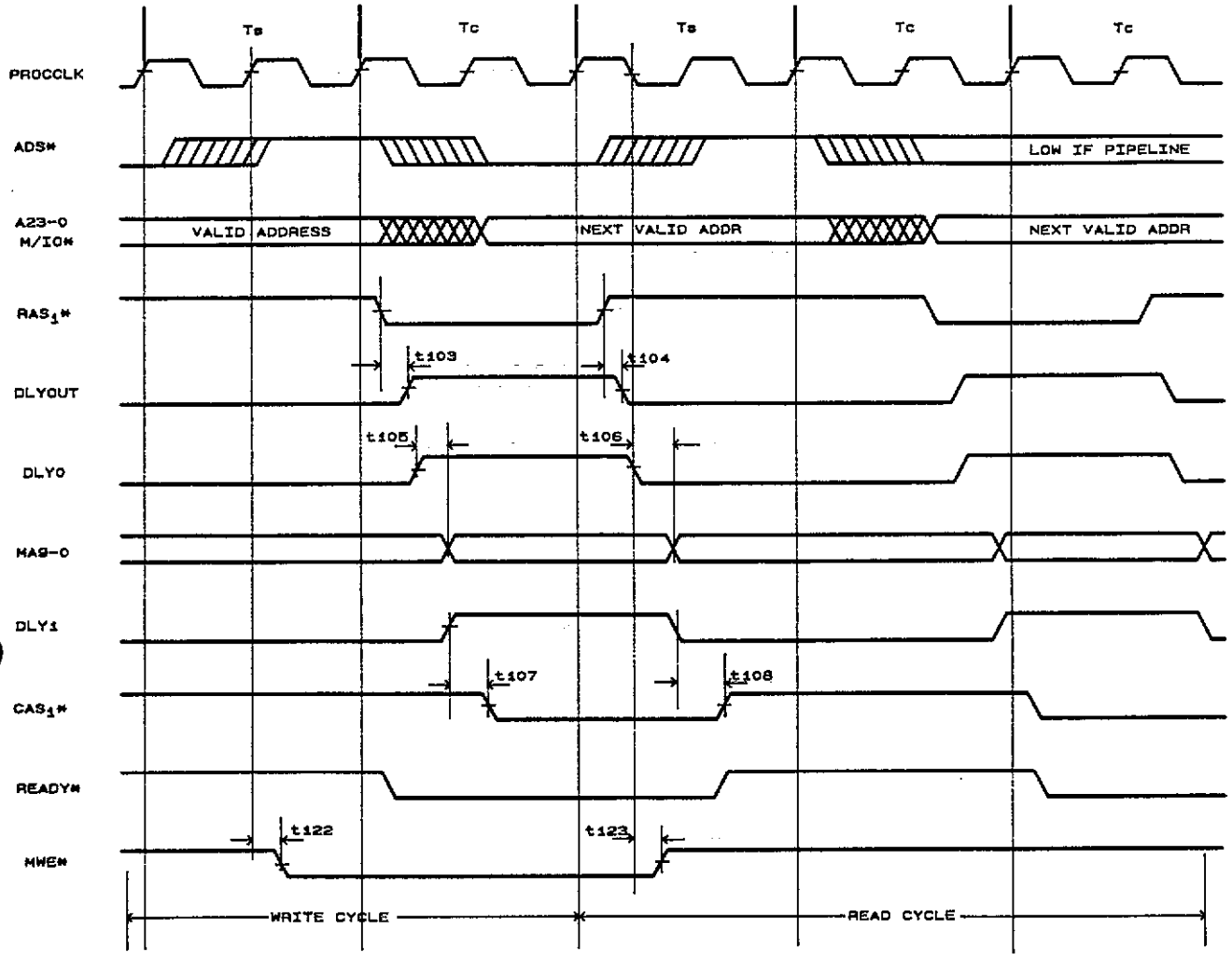
2.13 82C841 AC Timing Diagrams (continued)



ADS SHOWN ASSUMING PIPELINE CYCLES

Non-Page Mode - Read, 0WS

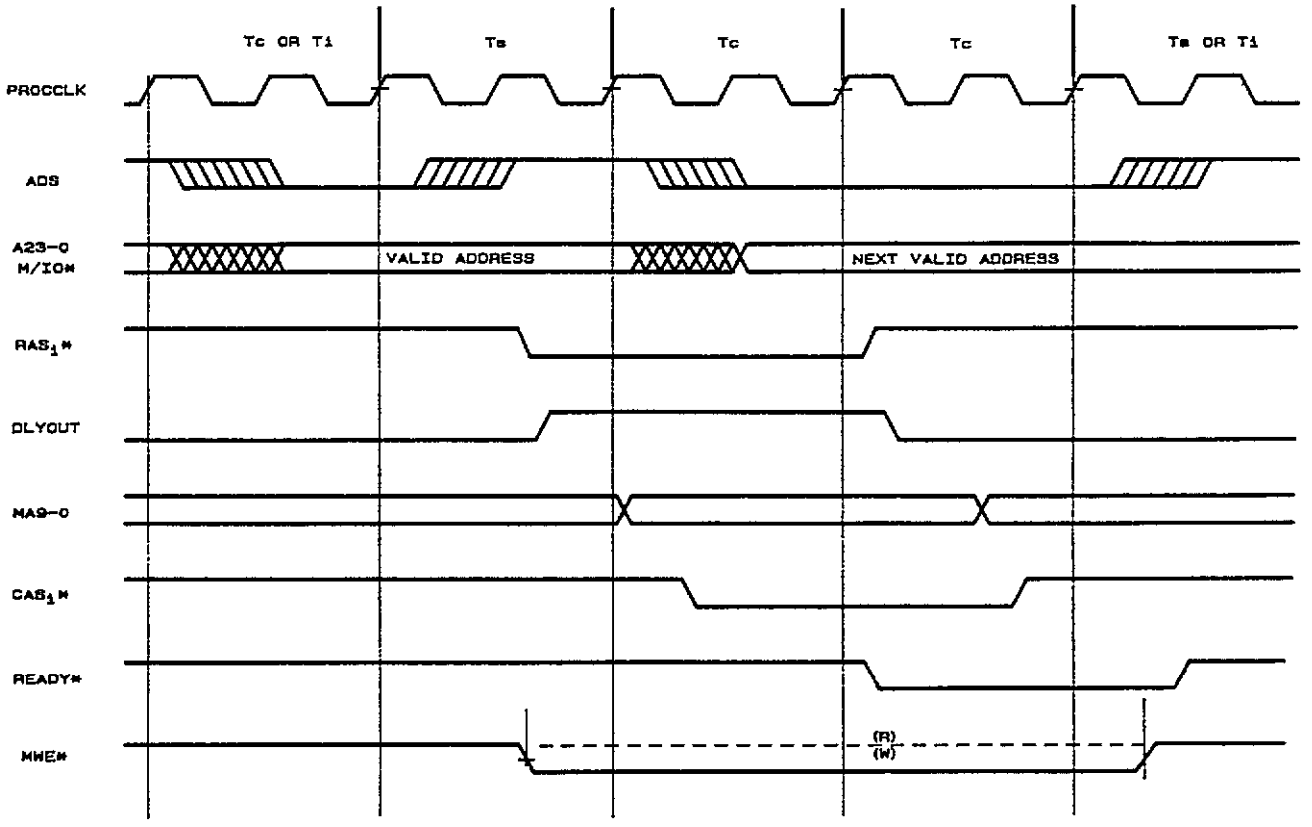
2.13 82C841 AC Timing Diagrams (continued)



ADS SHOWN ASSUMING PIPELINE CYCLES

Non-Page Mode - Write Followed by Read, 0WS

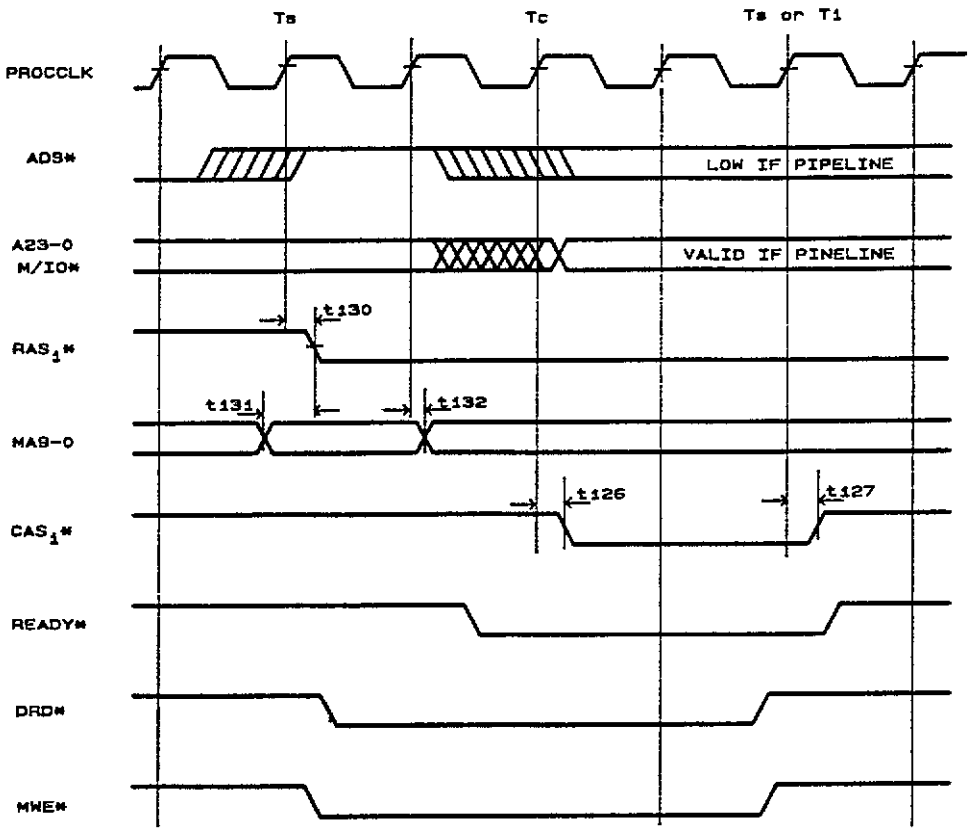
2.13 82C841 AC Timing Diagrams (continued)



ADS SHOWN ASSUMING PIPELINE CYCLES

Non-Page Mode - 1WS, Read, Write

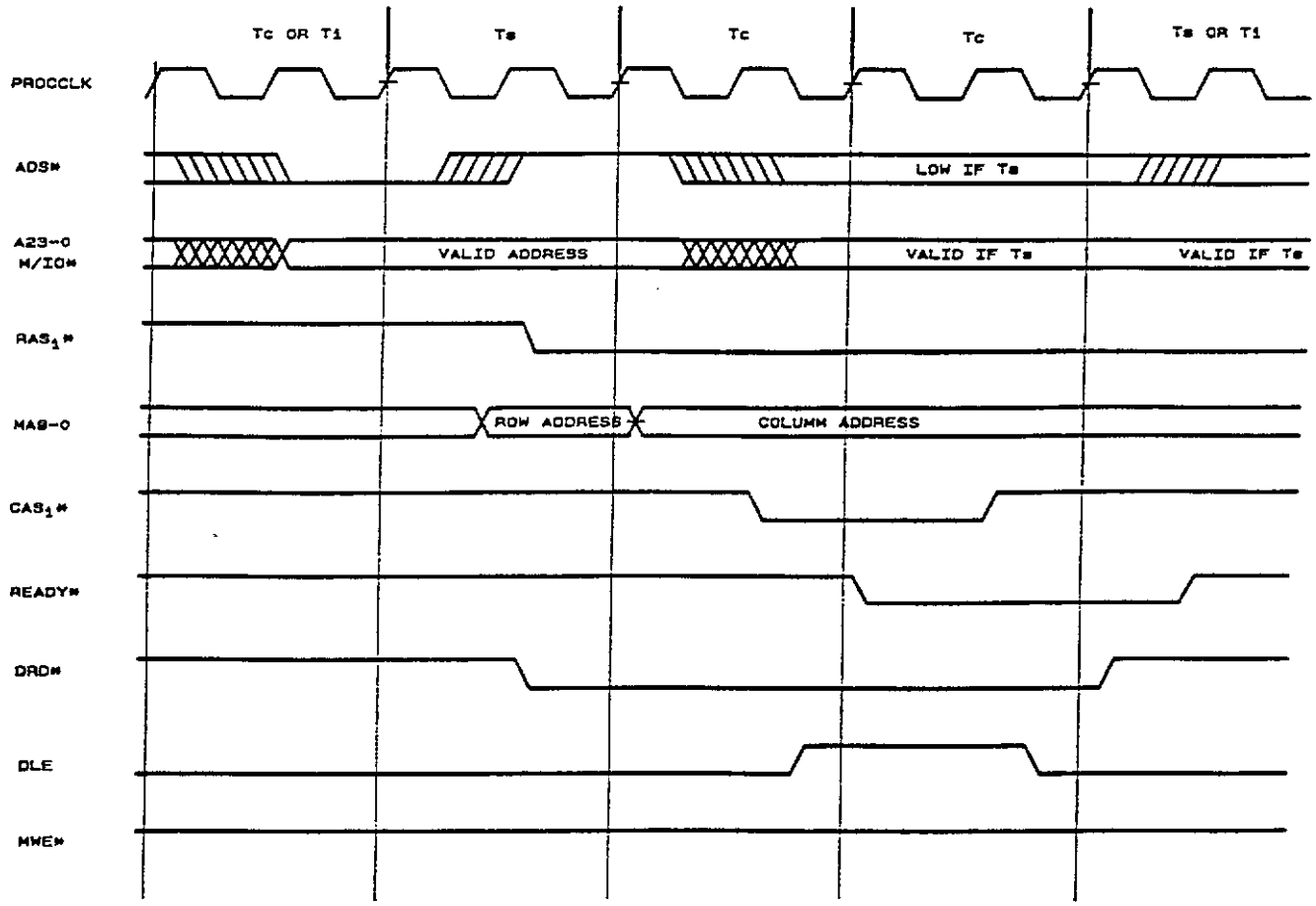
2.13 82C841 AC Timing Diagrams (continued)



ADS SHOWN ASSUMING PIPELINE CYCLES

Page Mode - Write Cycle with RAS Inactive, 0WS

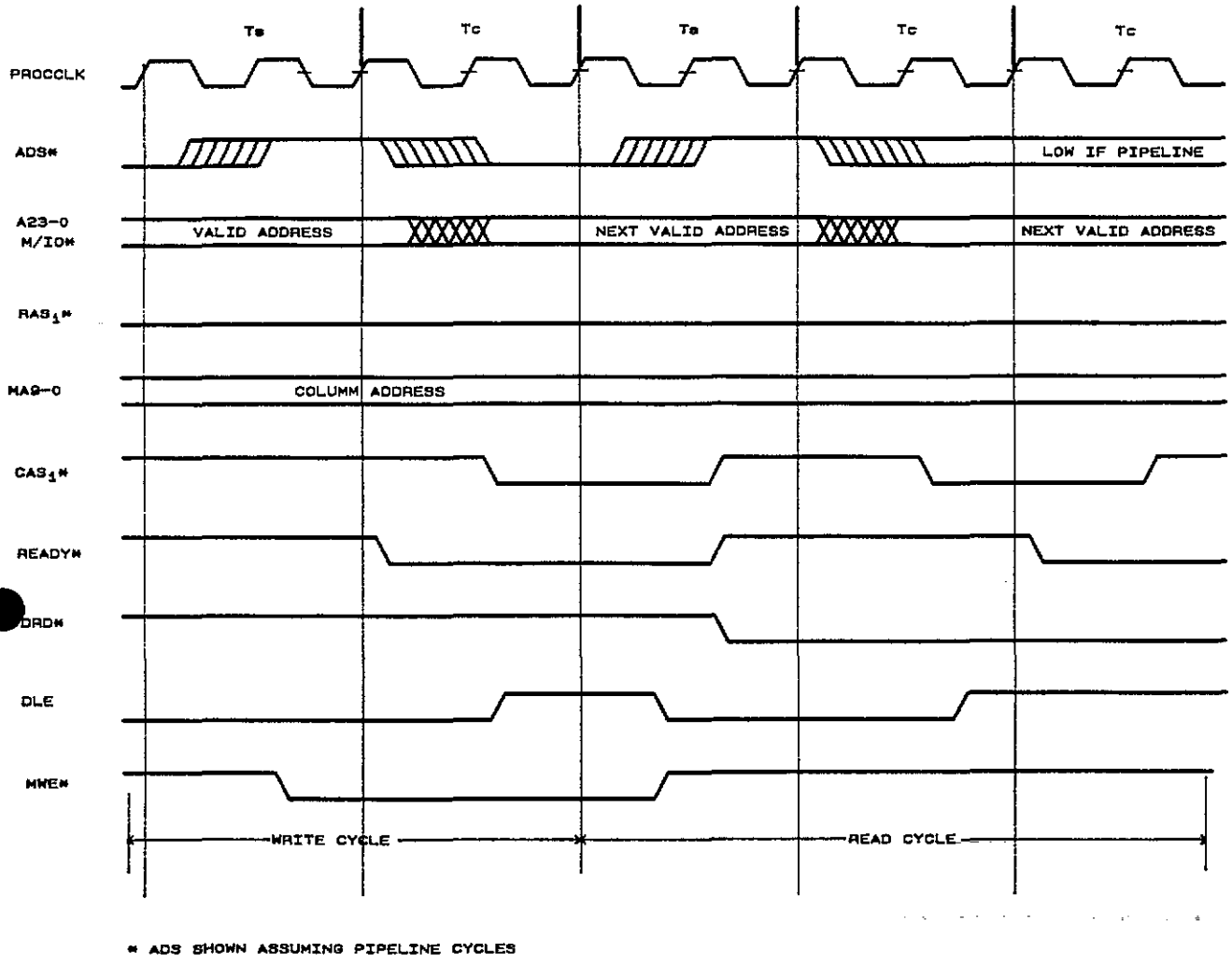
2.13 82C841 AC Timing Diagrams (continued)



ADS SHOWN ASSUMING PIPELINE CYCLES

Page Mode - Read Cycle with RAS Inactive, 0 WS

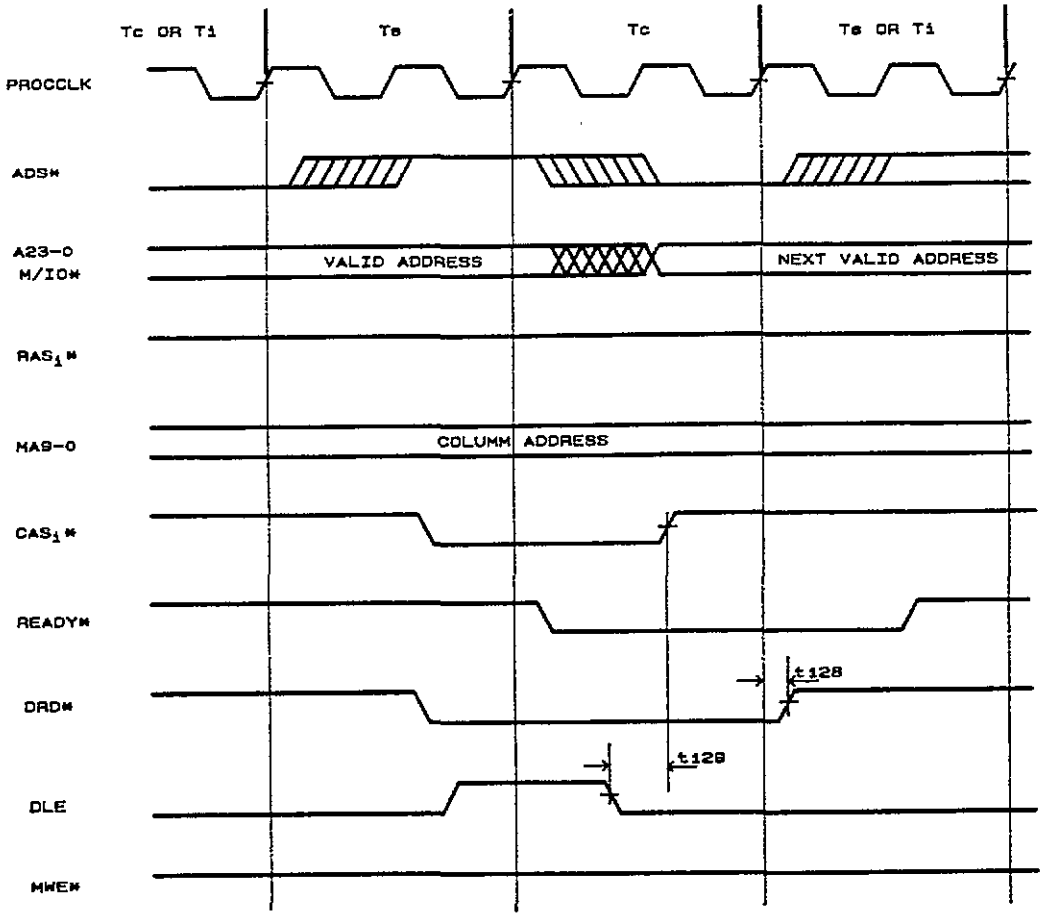
2.13 82C841 AC Timing Diagrams (continued)



ADS SHOWN ASSUMING PIPELINE CYCLES

Page Mode - Read after Write with RAS Active, 0 WS

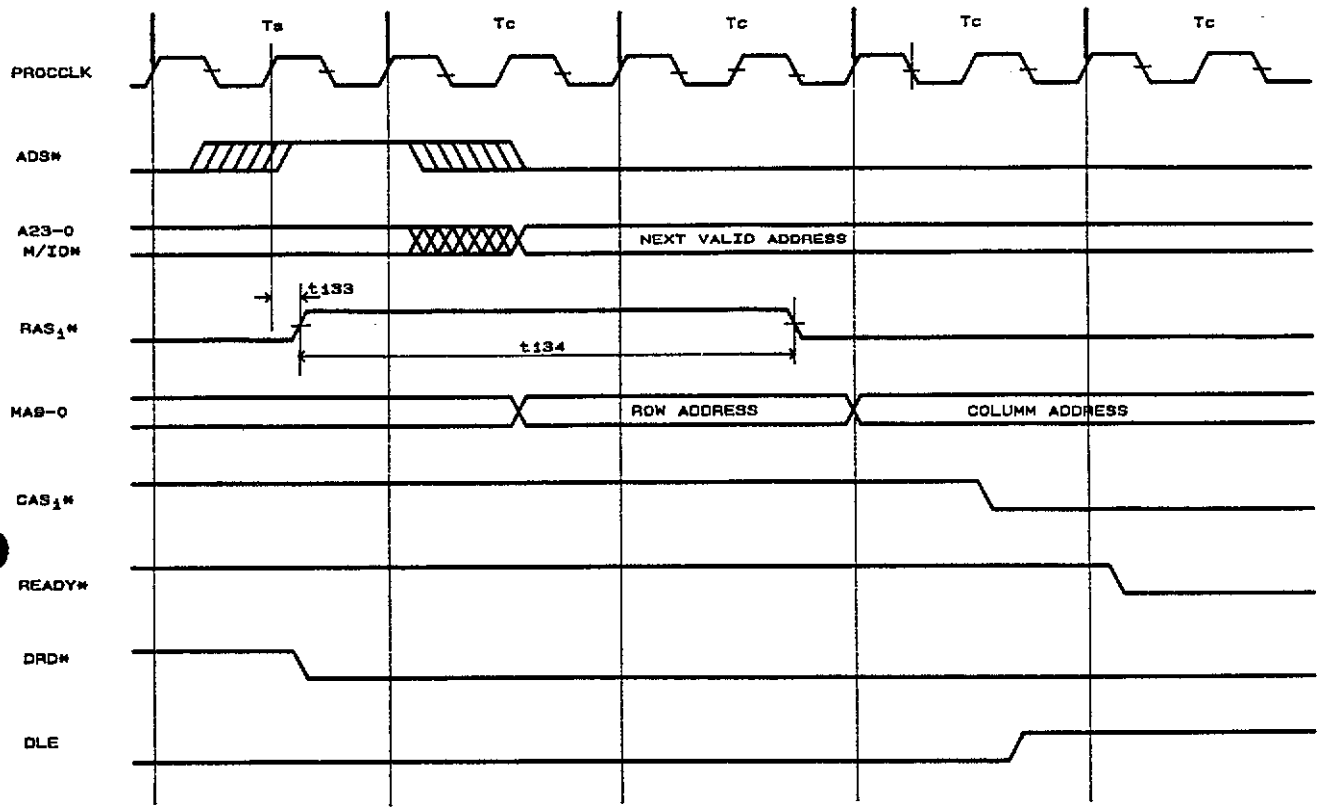
2.13 82C841 AC Timing Diagrams (continued)



ADS SHOWN ASSUMING PIPELINE CYCLES

Page Mode - Read with RAS Active, 0WS

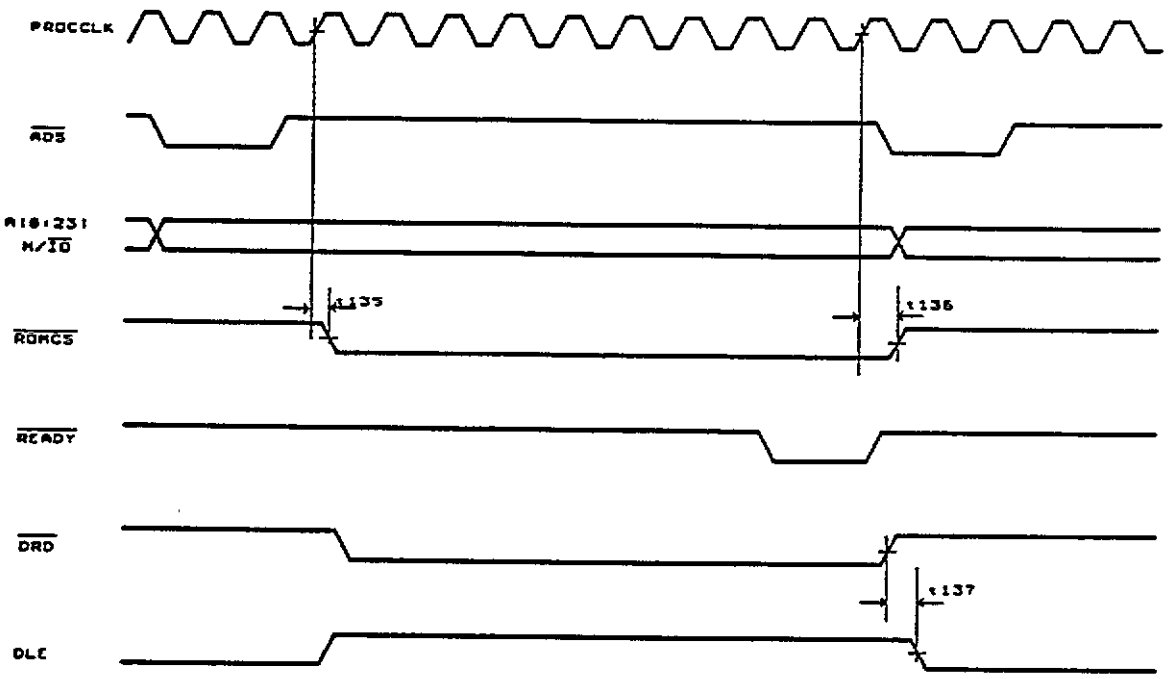
2.13 82C841 AC Timing Diagrams (continued)



* ADS SHOWN ASSUMING PIPELINE CYCLES

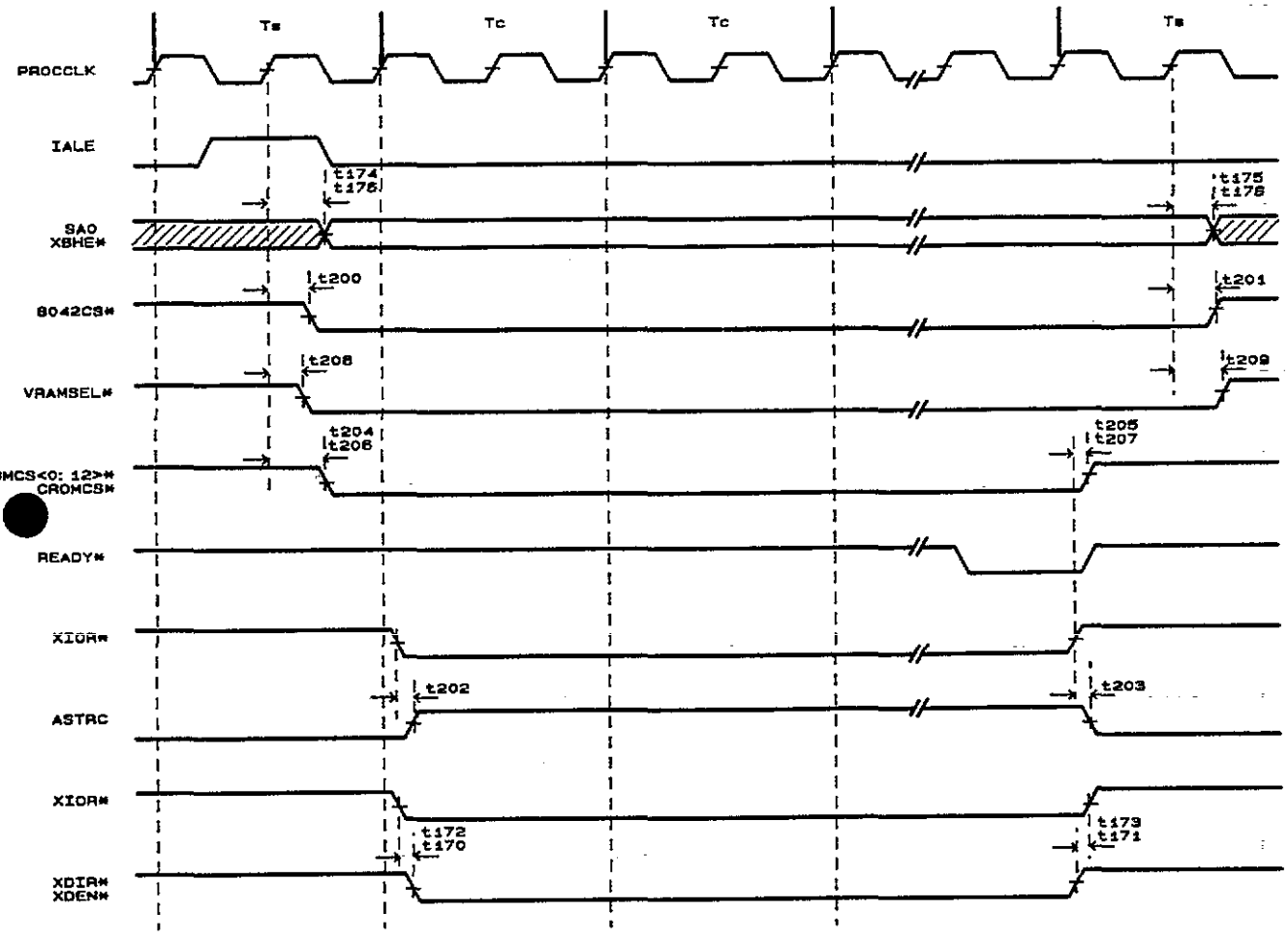
Page Mode - Read Miss Cycle

2.13 82C841 AC Timing Diagrams (continued)



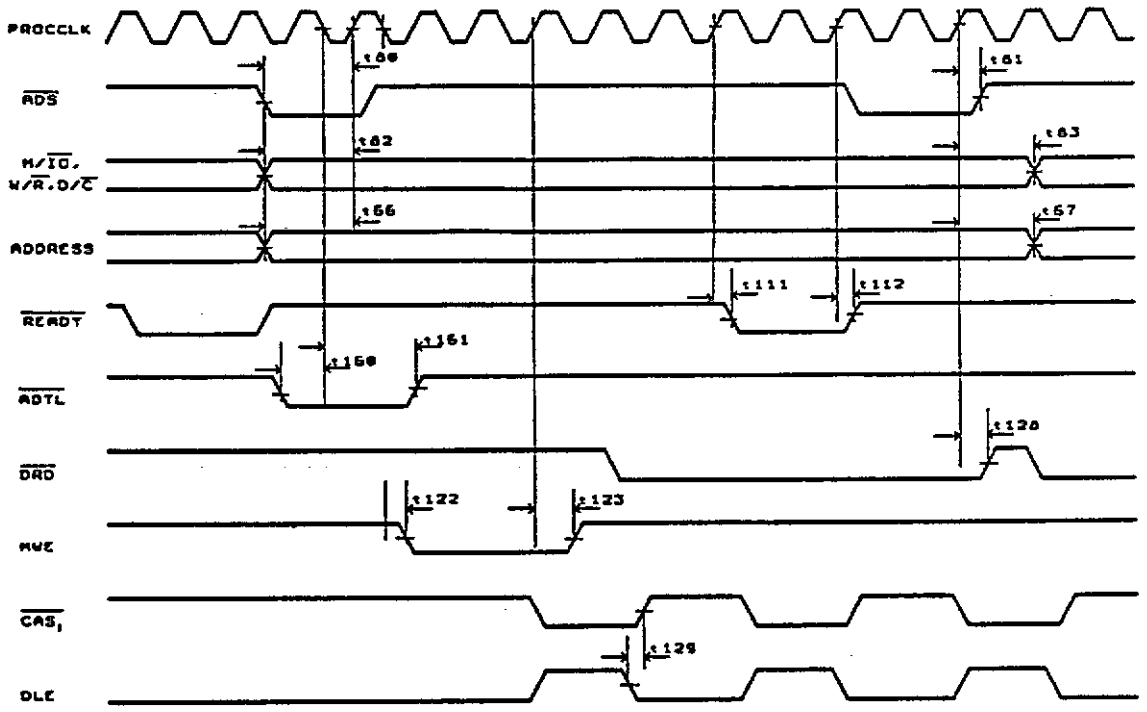
ROM read cycle

2.13 82C841 AC Timing Diagrams (continued)



Miscellaneous timing 1

2.13 82C841 AC Timing Diagrams (continued)



Miscellaneous timing 2

82C242 Address/Data Buffers and Bus Conversion Logic

3.0 Features:

- CPU and DMA address latches and buffers
- CPU data buffers and latches
- Bus conversion logic for 16-bit to 8-bit transfers
- Parity generation/detection logic
- Data buffers for local memory bus and local I/O bus
- Data buffers for external AT bus
- Oscillator circuit support for 14.31818MHz crystal

3.1 Functional Description:

The 82C242 Data/Address buffer chip consists of the following sub-modules as shown in Figure 3.1:

- Oscillator logic
- I/O decode logic
- Address buffers
- Data buffers
- Parity logic

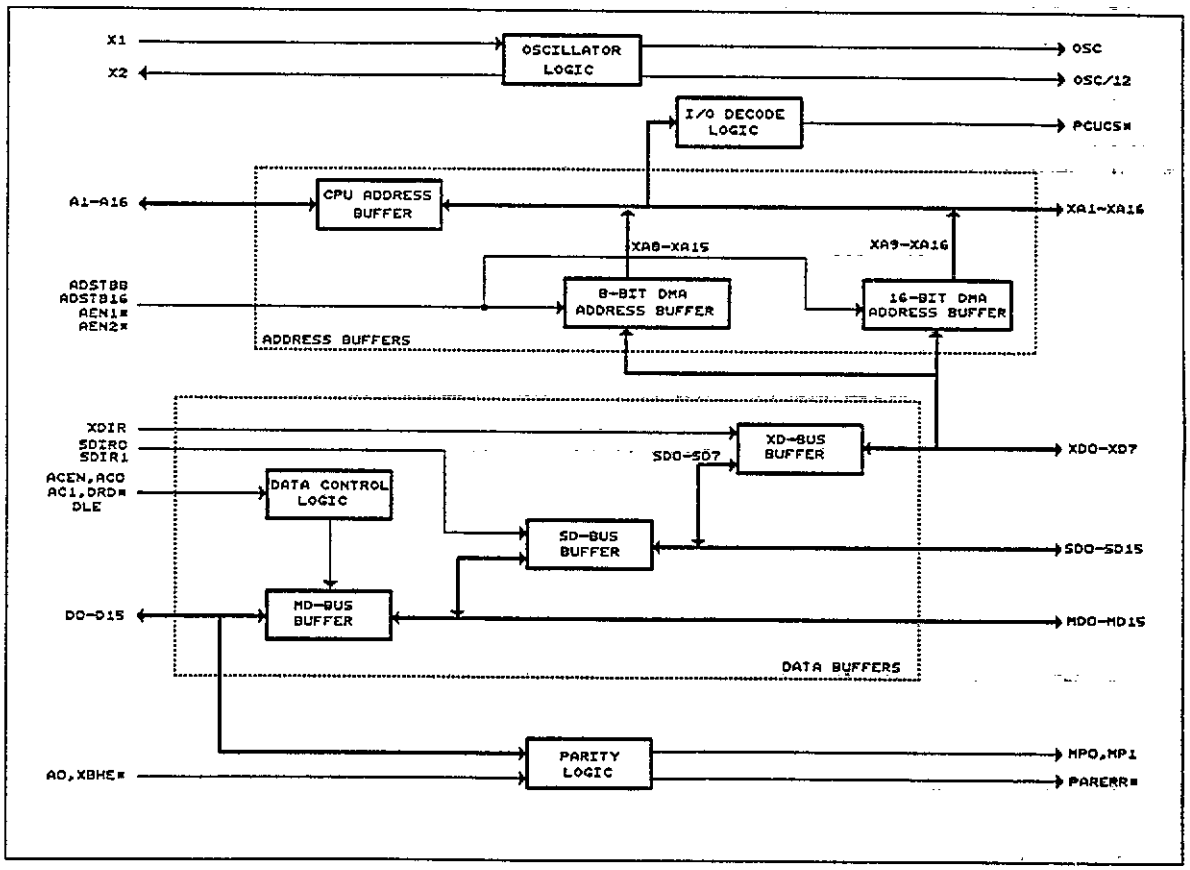


Figure 3.1. 82C242 Block Diagram

3.1.1 Oscillator Support Logic

The 82C242 generates the system clock, ATOSC from a crystal oscillator of 14.31818MHz at the X1 and X2 pins. The 14.31818MHz clock at the OSC output can be buffered and used for the AT bus. Also, it divides this clock by twelve to generate OSC/12 at 1.19MHz clock, which is used as the time base for the timers in the 80C206, Integrated Peripheral Controller.

3.1.2 I/O decode Logic

The 82C242 provides the decoding of the I/O addresses 22H and 23H, which are used to access the CHIPSet registers in the 82C636 Power Control Unit. The PCUCS* signal is activated for all I/O accesses to addresss 22H and 23H. The 82C636 uses this signal with the XA0 address line to distinguish between the two I/O addresses.

3.1.3 Address Buffers

The 82C242 provides the address buffers between the CPU address lines A1-A16 and the XA bus address lines, XA1-XA16. It also provides the buffering between the DMA address lines from the XD bus and the XA or CPU address lines. For normal CPU operations, the CPU address lines are latched by IALE to generate the XA address lines, whenever HLDA is not active. During DMA accesses, the upper addresses which are present on the XD bus are latched by ADSTB8 and ADSTB16 signals from the 82C206. ADSTB8 with AEN1* enables the addresses XA8-XA15 for 8-bit DMA accesses and ADSTB16 with AEN2* enables the addresses XA9-XA16 for 16-bit DMA accesses.

3.1.4 Data Buffers

The 82C242 provides data buffers needed to implement the various data buses in a typical AT compatible system. The various buffers provided are the CPU data bus to local memory data bus, the MD data bus to SD data bus and the SD data bus to XD data bus

The MD Bus Buffer shown in Figure 3.1 provides the buffering between the CPU data bus, D0-D15 and the local memory data bus, MD0-MD15. For data flow between the MD bus and the D bus, the enable for the latches is controlled by DLE. The direction is controlled by DRD*. The Data Control Logic block controls the necessary bus conversion, when the 16-bit CPU reads from or writes to 8-bit devices. This block also provides the conversion for Master/DMA cycles. The various possible data paths for this bus conversion is shown in Figure 3.2 and Table 3.1. Bus conversion process is controlled by the action codes, AC0 and AC1 which are qualified by the ACEN* signal from the 82C241 (82C841).

The 82C242 also provides the buffering between the MD bus and the SD bus in the system as shown by the SD Bus Buffer block in Figure 3.1. SDIR0 and SDIR1 control the direction of these buffers. The path is from MD bus to SD bus, when SDIR0 and SDIR1 are high, and from SD bus to MD bus, when they are low.

The XD bus buffering is supported by the 82C242 as shown by the XD Bus Buffer in Figure 3.1. The direction of this buffer is controlled by the XDIR* signal from the 82C241 (82C841). The path is from SD bus to XD bus, when XDIR is high, and from XD bus to SD bus, when it is low.

3.1.4 Parity Logic

The 82C242 generates even parity for each of the two bytes of the data word for all local RAM write cycles. These valid even parity bits are written to the parity bits MP0 and MP1 in the local DRAMs. During all local memory read cycles, the 82C242 checks even parity for each of the MD data byte. Anytime an odd parity is detected on either of the two MD data bytes, the 82C242 flags a parity error on the PARERR* output line. The 82C241 (82C841) samples this PARERR* line for local RAM cycles only, and generates an NMI to the CPU if a parity error is detected and the NMI generation due to this is enabled.

AC1	AC0	Cycle	Operation	Data path
0	0	CPU	16-bit write	A-B-D-E-F-G and H-J-L-M-N-P
0	0	CPU	8-bit LO write	H-J-L-M-N-P
0	1	CPU	16-bit read	G-F-E-D-B-A and P-N-M-L-J-H
0	1	CPU	8-bit LO read	P-N-M-L-J-H
1	0	CPU	8-bit HI write	A-B-C-K-L-M-N-P
1	1	CPU	8-bit HI read	P-N-M-L-K-C-B-A
1	0	DMA/MASTER	8-bit HI write	P-N-M-L-K-C-D-E-F-G
1	1	DMA/MASTER	8-bit HI read	G-F-E-D-C-K-L-M-N-P

Table 3.1. Table of the 82C242 Bus Conversion Data Paths

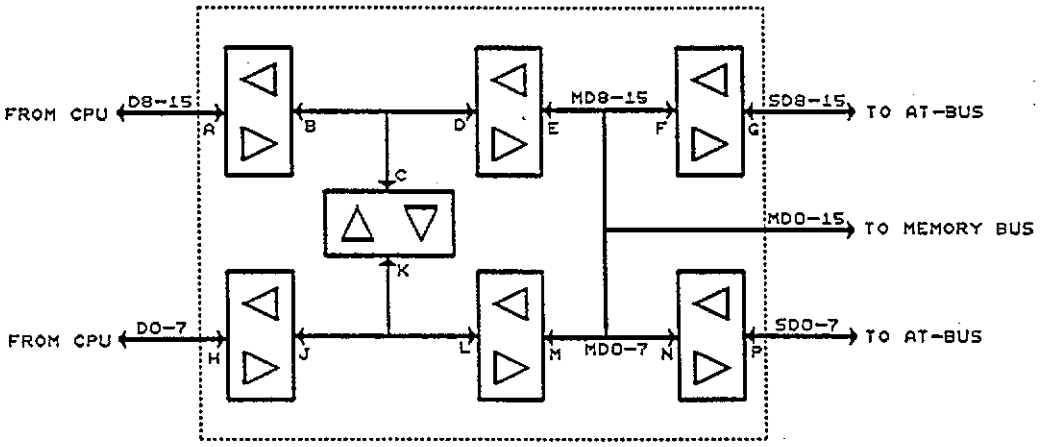


Figure 3.2. 82C242 Bus Conversion Data Paths

3.2 82C242 Pin Assignments

Type	Symbol	Description
I	ACEN*	ACTION CODE ENABLE is an active low input from the 82C241 (82C841) that validates the action codes AC0 and AC1 and is used for bus sizing and byte assembly control.
I	AC<1:0>	ACTION CODES 1 and 0 are inputs from 82C241 (82C841) used for bus sizing, conversion and byte assembly operations.
I	DLE	DATA LATCH ENABLE is an active high input from 82C241 (82C841) used to enable the local memory data buffer latch.
I	DRD*	DATA READ is an input from 82C241 (82C841) used to control the direction of data transfer from MD bus to CPU data bus. If low, transfer is from MD data bus to CPU data bus and if high, transfer is from CPU data bus to MD data bus.
I	HLDA1	HOLD ACKNOWLEDGE 1 is an active high input from the 82C241 (82C841) used for address and data direction control during DMA and MASTER cycles.
I	IALE	INTERNAL ADDRESS LATCH ENABLE is an active high input from the 82C241 (82C841) used to latch the CPU address lines on to the XA address bus.
I	XBHE*	BYTE HIGH ENABLE is an active low input from the CPU and is used to enable high byte parity checking.
I	A0	ADDRESS line A0 is an input from the CPU and when low, it enables low byte parity checking.
I	X1	CRYSTAL 1 input from the 14.31818MHz crystal.
O	X2	CRYSTAL 2 output to the 14.31818MHz crystal.
O	OSC	OSCILLATOR output for the system clock at 14.31818MHz.
O	OSC/12	OSCILLATOR divided by 12 output with a clock frequency of 1.19MHz (equal to 1/12 of 14.31818MHz).
I	AEN1*	ADDRESS ENABLE 1 is an active low input from one of the two DMA controllers or the 82C206 and is used to enable the address latches for 8-bit DMA transfers.
I	AEN2*	ADDRESS ENABLE 2 is an active low input from one of the two DMA controllers or the 82C206 and is used to enable the address latches for 16-bit DMA transfers.
I	ADSTB8	Address strobe used during DMA transfers to latch XD0-7 into the upper addresses XA8-15 for 8-bit peripherals.
I	ADSTB16	Address strobe used during DMA transfers to latch XD0-7 into the upper addresses XA9-16 for 16-bit peripherals.

3.2 82C242 Pin Assignments(continued)

Type	Symbol	Description
I	SDIR(1,0)	SYSTEM BUS DIRECTION control inputs from 82C241 (82C841) used to control the direction of data path from SD bus to MD bus. If low, the path is from SD bus to MD bus and if high, the path is from MD bus to SD bus. SDIR1 is for the high byte and SDIR0 is for low byte control.
I	XDIR*	XD BUS DIRECTION is an input from the 82C241 (82C841) used to control the direction of the buffers between XD bus and SD bus. If low, the path is from XD bus to SD bus and if high, the path is from SD bus to XD bus.
I/O	MP<0:1>	Memory Parity bits 0 and 1 are the parity bits associated with the lower data byte (MD0:7) and upper data byte (MD8:15) respectively.
O	PARERR*	Parity error is an active low signal indicating that a parity error has occurred during a data transaction2 in either the upper or lower byte.
I/O	D<0:15>	D0-D15 data bus from the CPU are inputs for write operations and are outputs for read operations.
I/O	SD<0:15>	SD0-SD15 data bus to the AT bus are outputs for write operations to the AT bus and are inputs for read operations from the AT bus.
I/O	XD<0:7>	XD0-7 data bus for the on-board peripherals are outputs for write operations and are inputs for read operations.
I/O	MD<0:15>	MD0-MD15 memory data bus for the on-board local memory which includes the RAMs and the double EPROMs. These pins are outputs for write operations and are inputs for read operations.
I/O	A<1:16>	A1-16 address bus from the CPU are inputs if the CPU is in control and are outputs if a bus master is in control and have a drive capability of 4mA.
I/O	XA<1:16>	XA1-XA16 address bus to the AT bus are outputs for cycles in which the CPU is in control and are inputs if a bus master is in control.
I	REF*	Refresh in progress from 82C241 (82C841)
I	MASTER*	Indicates AT bus device mastership.
O	ACK*	Acknowledge indicates that a refresh DMA or MASTER cycle is in progress.
O	PCUCS*	82C636 Power Control Unit chip select is an active low signal generated whenever an I/O operation to port 22H and 23H is performed to access any of the 82C636 CHIPSet registers.
I	VCC	+5V
I	GND	GROUND

3.3 Pinout List

Pin	Name	Pin	Name	Pin	Name
1	VCC	49	MD1	97	SD10
2	A11	50	MD2	98	SD11
3	A12	51	MD3	99	SD12
4	A13	52	MD4	100	SD13
5	A14	53	N.C	101	SD14
6	A15	54	VCC	102	SD15
7	A16	55	GND	103	GND
8	GND	56	MD5	104	X1
9	XA1	57	MD6	105	X2
10	XA2	58	MD7	106	OSC
11	XA3	59	MD8	107	OSC/12
12	XA4	60	MD9	108	GND
13	XA5	61	MD10	109	GND
14	XA6	62	MD11	110	XDIR*
15	XA7	63	MD12	111	HLDA1
16	XA8	64	MD13	112	MASTER*
17	N.C	65	MD14	113	REF*
18	VCC	66	MD15	114	ACK*
19	GND	67	GND	115	GND
20	XA9	68	VCC	116	IALE
21	XA10	69	SDIR1	117	XD0
22	XA11	70	SDIR0	118	XD1
23	XA12	71	ACEN*	119	XD2
24	XA13	72	VCC	120	XD3
25	XA14	73	VCC	121	XD4
26	XA15	74	AC0	122	XD5
27	XA16	75	AC1	123	XD6
28	GND	76	DRD*	124	XD7
29	D0	77	DLE	125	N.C
30	D1	78	A0	126	VCC
31	D2	79	XBHE*	127	GND
32	D3	80	PARERR*	128	PCUCS*
33	D4	81	MP0	129	AEN2*
34	D5	82	MP1	130	AEN1*
35	D6	83	GND	131	ADSTB16
36	GND	84	SD0	132	ADSTB8
37	GND	85	SD1	133	GND
38	D7	86	SD2	134	A1
39	D8	87	SD3	135	A2
40	D9	88	SD4	136	A3
41	D10	89	N.C	137	A4
42	D11	90	VCC	138	A5
43	D12	91	GND	139	A6
44	D13	92	SD5	140	A7
45	D14	93	SD6	141	A8
46	D15	94	SD7	142	A9
47	GND	95	SD8	143	A10
48	MD0	96	SD9	144	VCC

Name	Pin	Name	Pin	Name	Pin
A0	78	GND	8	SD15	102
A1	134	GND	55	SD2	86
A10	143	GND	67	SD3	87
A11	2	GND	83	SD4	88
A12	3	GND	91	SD5	92
A13	4	GND	103	SD6	93
A14	5	GND	108	SD7	94
A15	6	GND	109	SD8	95
A16	7	GND	115	SD9	96
A2	135	GND	127	SDIR0	70
A3	136	GND	133	SDIR1	69
A4	137	HLDA1	111	VCC	1
A5	138	IALE	116	VCC	18
A6	139	MASTER*	112	VCC	54
A7	140	MD0	48	VCC	68
A8	141	MD1	49	VCC	72
A9	142	MD10	61	VCC	73
AC0	74	MD11	62	VCC	90
AC1	75	MD12	63	VCC	126
ACEN*	71	MD13	64	VCC	144
ACK*	114	MD14	65	X1	104
ADSTB16	131	MD15	66	X2	105
ADSTB8	132	MD2	50	XA1	9
AEN1*	130	MD3	51	XA10	21
AEN2*	129	MD4	52	XA11	22
D0	29	MD5	56	XA12	23
D1	30	MD6	57	XA13	24
D10	41	MD7	58	XA14	25
D11	42	MD8	59	XA15	26
D12	43	MD9	60	XA16	27
D13	44	MP0	81	XA2	10
D14	45	MP1	82	XA3	11
D15	46	N.C	17	XA4	12
D2	31	N.C	53	XA5	13
D3	32	N.C	89	XA6	14
D4	33	N.C	125	XA7	15
D5	34	OSC	106	XA8	16
D6	35	OSC/12	107	XA9	20
D7	38	PARERR*	80	XBHE*	79
D8	39	PCUCS*	128	XD0	117
D9	40	REF*	113	XD1	118
DLE	77	SD0	84	XD2	119
DRD*	76	SD1	85	XD3	120
GND	19	SD10	97	XD4	121
GND	28	SD11	98	XD5	122
GND	36	SD12	99	XD6	123
GND	37	SD13	100	XD7	124
GND	47	SD14	101	XDIR*	110

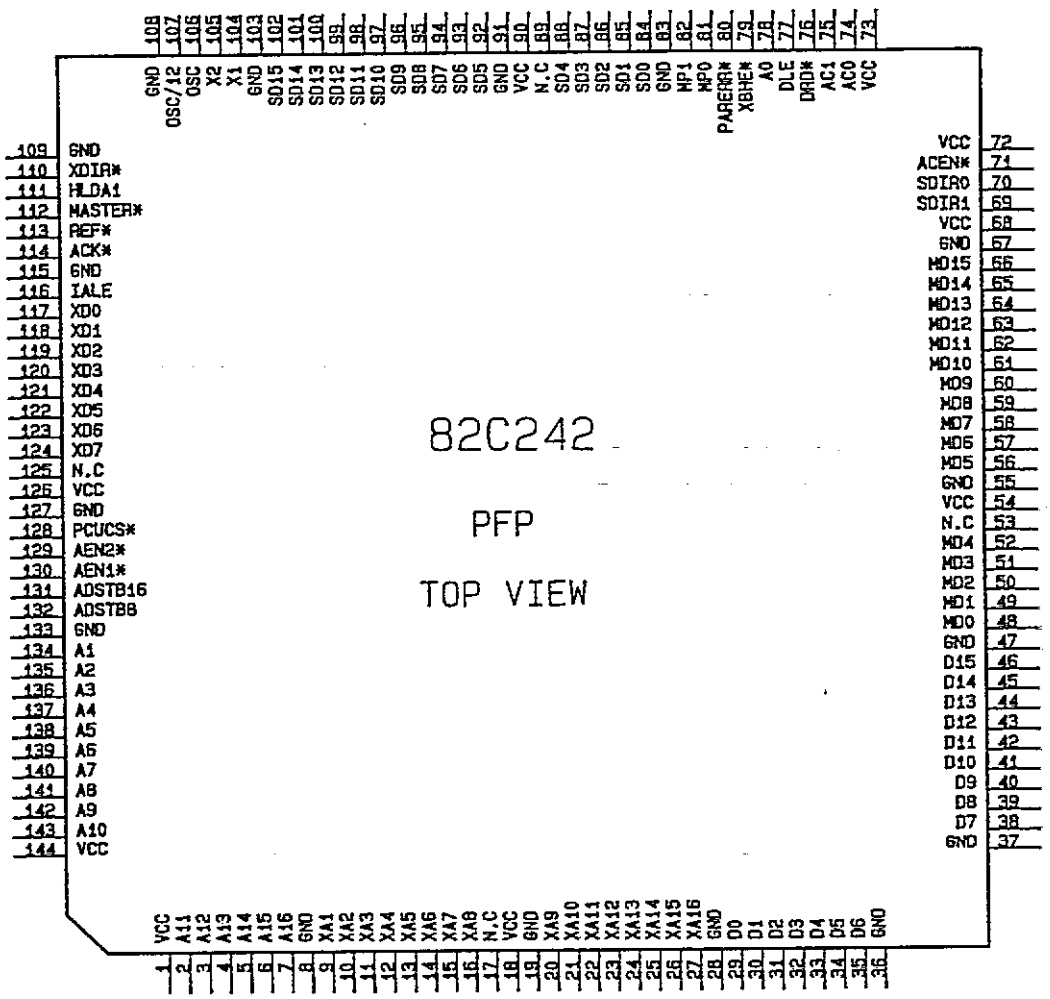
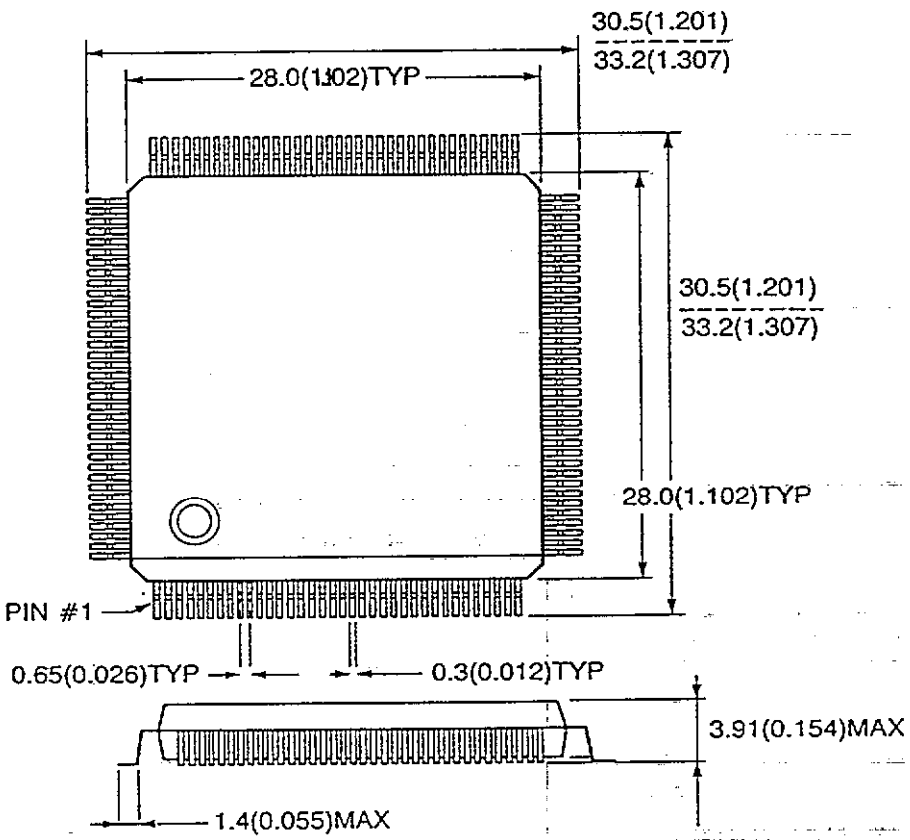


Figure 3.3. 82C242 Pin Diagram

3.4 Physical Dimensions

144-Pin Plastic Flat Package (Square) Dimensions: mm(in)



3.5 82C242 Absolute Ratings

Parameter	Symbol	Min.	Max.	Units
Supply Voltage	V_{CC}	-	7.0	V
Input Voltage	V_I	-0.5	5.5	V
Output Voltage	V_O	-0.5	5.5	V
Operating Temperature	T_{OP}	-25°	85°	C
Storage Temperature	T_{STG}	-40°	125°	C

NOTE: Permanent device damage may occur if Absolute Maximum Ratings are exceeded. Functional operation should be restricted to the conditions described under Operating Conditions.

3.6 82C242 Operating Conditions

Parameter	Symbol	Min.	Max.	Units
Supply Voltage	V_{CC}	4.75	5.25	V
Ambient Temperature	T_A	0°	70°	C

3.7 82C242 DC Characteristics

Parameter	Symbol	Min.	Max.	Units
Input Low Voltage	V_{IL}	-	0.8	V
Input High Voltage	V_{IH}	2.0	-	V
Output Low Voltage	V_{OL}	-	0.2	V
Output High Voltage	V_{OH}	3.84	-	V
Input Low Current ($0 < V_{IN} < V_{CC}$)	I_{IL}	-	± 10	mA
Output High-Z Leakage Current ($0 < V_{IN} < V_{CC}$)	I_{OZ1}	-	± 10	uA
Static Power Supply Current	I_{CCSB}	-	1	mA

I_{OH} and I_{OL} - Output drive capability

4mA: D15-D0, PARERR*, X2, OSC/12, ACK*, PCUCS*, A16-A1, XA16-XA1

8mA: MD15-MD0, MP0, MP1, SD15-SD0, OSC, XD7-XD0

Power Supply Current I_{cc}

Mode	12 MHz		16 MHz		20 MHz		Units
	Min	Max	Min	Max	Min	Max	
Normal	-	52	-	60	-	68	mA
Sleep mode	-	11	-	12	-	13	mA
Stand-by	-	0	-	0	-	0	uA

Note:
1. Power consumption measured using 2 MB of local DRAM and double ROMs.
2. Normal mode measurements made at DOS prompt.
3. Sleep mode measurements made at DOS prompt and using Chips and Technology BIOS for LeAPSet and the smart sleep feature.
4. 82C242 is powered off during stand-by.

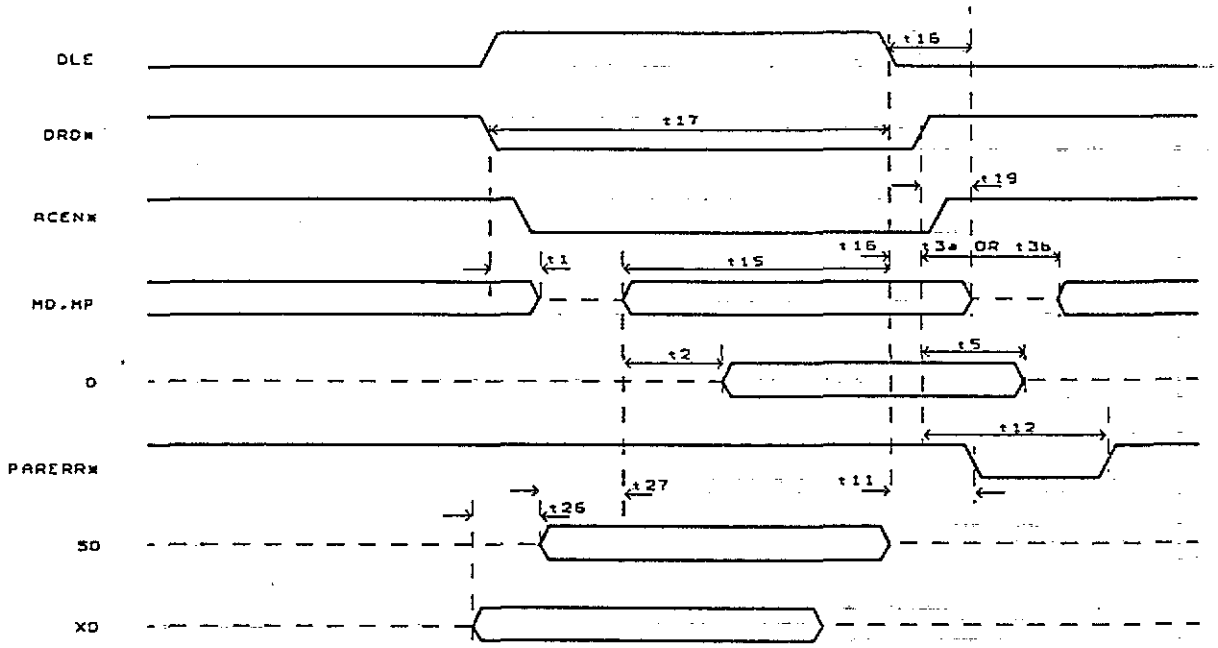
3.8 82C242 AC Characteristics

(T_A = 0°C to 70°C, V_{CC} = 5V ± 5%, C_L = 75pF)
(Min and Max values in nanoseconds)

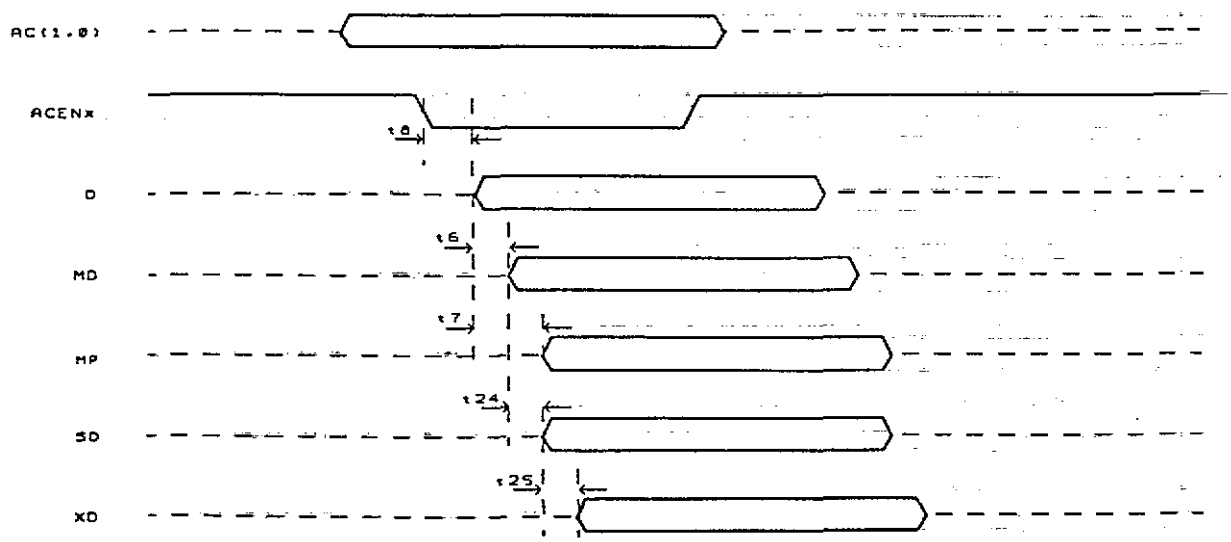
Sym	Description	12 MHz		16 MHz		20 MHz	
		Min	Max	Min	Max	Min	Max
t1	MD bus tri-stated after DRD* active	-	24	-	24	-	24
t2	MD bus valid to D bus valid	-	18	-	18	-	18
t3a	MD bus being driven after DRD* inactive	-	28	-	28	-	28
t3b	MP being driven after DRD* inactive	-	23	-	23	-	23
t5	D bus tri-stated after DRD* inactive	-	15	-	15	-	15
t6	D bus valid to MD bus valid	-	35	-	30	-	27
t7	D bus valid to MP valid	-	35	-	30	-	27
t8	ACEN* active to D bus valid	-	40	-	40	-	40
t9	AC code valid to MD bus valid	-	40	-	35	-	20
t10	AC code invalid to MD bus invalid	-	40	-	30	-	20
t11	DLE inactive to PARERR* enabled	-	45	-	40	-	35
t12	DRD* inactive to PARERR* disabled	-	45	-	40	-	35
t13	IALE active to XA bus valid	-	50	-	45	-	40
t14	XA bus valid to A bus valid	-	40	-	40	-	40
t15	MD, MP setup time to DLE_L	0	-	0	-	0	-
t16	MD, MP hold time from DLE_L	7	-	7	-	7	-
t17	DRD* setup time to DLE_L	30	-	30	-	30	-
t19	MD bus hold from $ACEN*_H$	9	-	9	-	9	-
t20	MD bus valid to MP valid during DMA write	-	30	-	30	-	30
t21	MD high byte valid to MD low byte valid during DMA high memory read cycle	-	30	-	30	-	30
t22	AC code valid to MD high byte valid during DMA high memory write cycle	-	25	-	25	-	25
t23	AC code valid to MP valid during DMA high memory write cycle	-	30	-	30	-	30
t24	MD bus valid to SD bus valid	-	30	-	25	-	20
t25	SD bus valid to XD bus valid	-	15	-	10	-	5
t26	XD bus valid to SD bus valid	-	25	-	20	-	15
t27	SD bus valid to MD bus valid	-	25	-	20	-	15

NOTES: - Signal names with a subscript of "L" refers to low going edge and "H" refers to high going edge.

3.9 82C242 AC Timing Diagrams

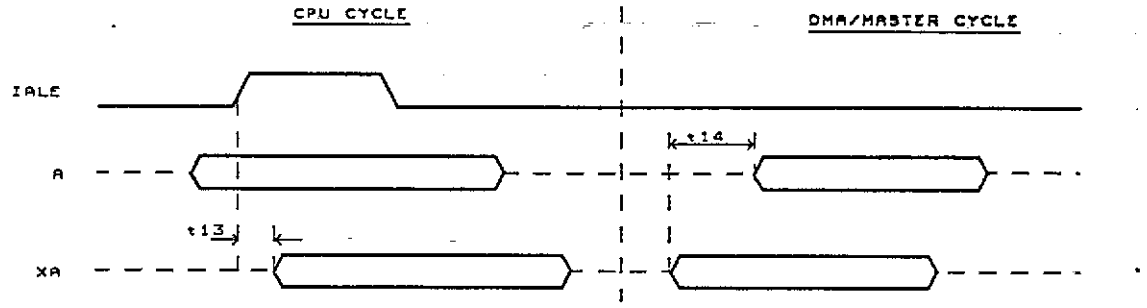


READ OPERATION

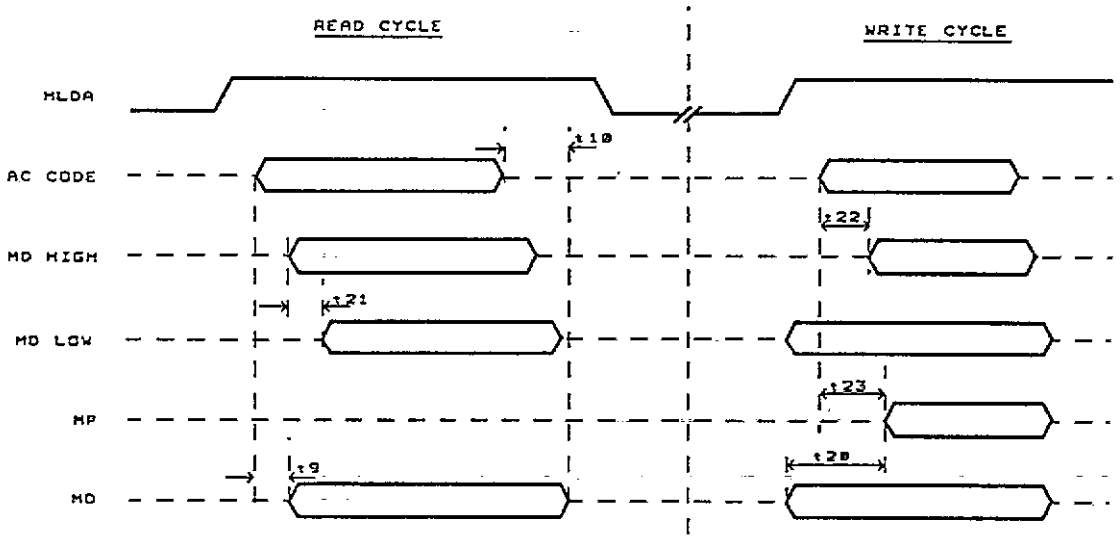


WRITE OPERATION

3.9 82C242 AC Timing Diagrams (continued)



ADDRESS LATCHING



DMA/MASTER CYCLE

82C636 Power Control Unit

4.0 Features:

- Power control for CPU, memory, serial ports, modem, display panel backlight, keyboard and disk drive powers.
- Stand-by mode support.
- Manual Power on capability.
- Programmable auto power on by modem rings.
- Programmable Scheduled Power on.
- Slow and Normal Refresh DRAMs support.
- Auto Power Saving capability with built in programmable timeout counters.
- Two multipurpose programmable parallel I/O ports.

4.1 Functional Description:

The 82C636 Power Control Unit consists of the following sub-modules as shown in Figure 4.1.

- Timers and counters
- System interface
- NMI handler
- Programmable I/O block
- Refresh logic
- Configuration registers
- Power control block

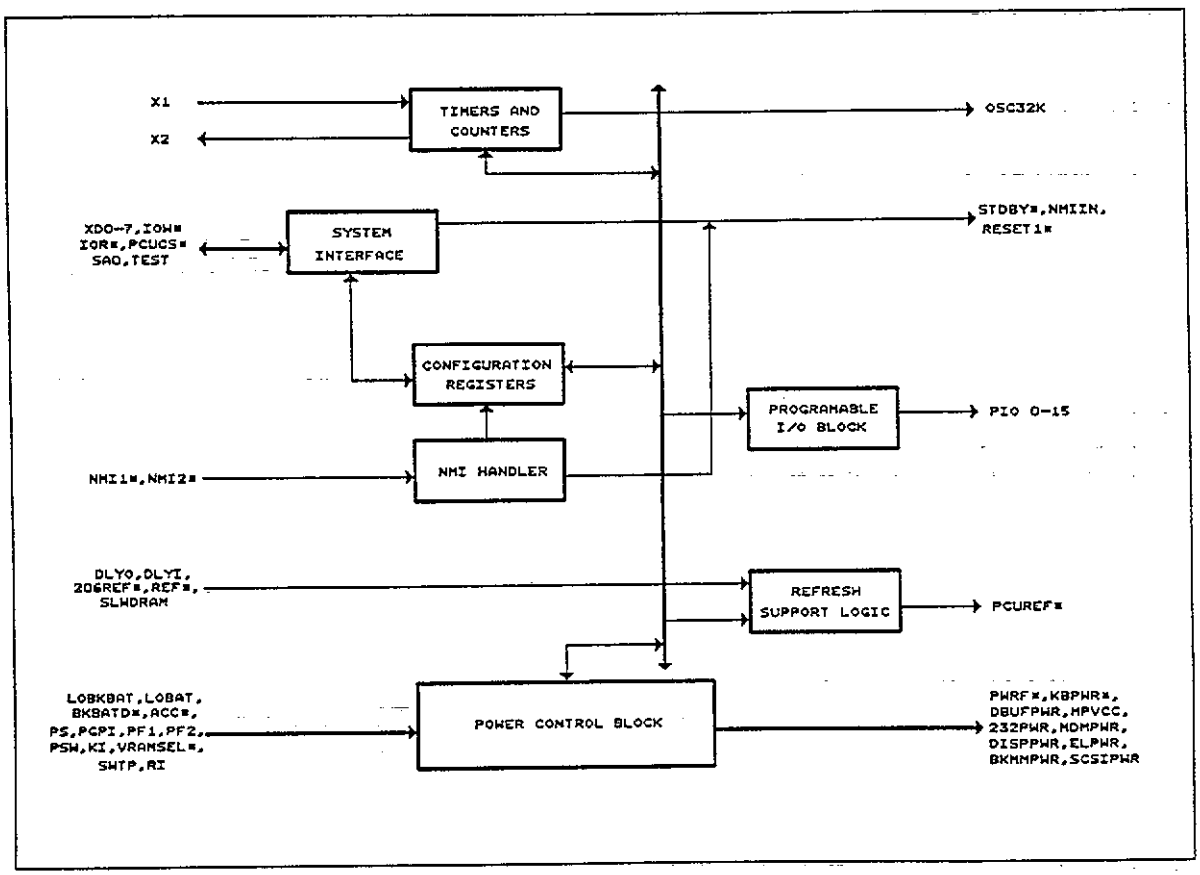


Figure 4.1. 82C636 Block Diagram

4.1.1 Timers and Counters

The timers and counters block generates all the necessary clocks and time bases needed by the 82C636. It receives a 32.768KHz input from a crystal oscillator to generate all the internal time bases and also an output of 32.768KHz at the OSC32K output pin, which is used by the 82C206. The various counters required for timed power control are also contained in this block.

4.1.2 System Interface

The system interface block contains all the necessary logic needed to interface with the system. To access the internal registers of the 82C636, the system port addresses 22H and 23H are decoded externally (in the 82C242) and input to the 82C636 as PCUCS*. The SA0 address line with this signal is used to distinguish the accesses to port 22H and 23H. The interface to the system data bus is through the XD bus on the XD0-XD7 bidirectional data lines. The system interface unit is also responsible for the generation of the STDBY* signal during stand-by mode, the system RESET1* and NMIIN.

4.1.3 Configuration Registers

The 82C636 contains a set of CHIPSet configuration registers. By programming these registers, the various configuration options and features of the 82C636 can be selected. These registers are accessed by an indexing scheme, whereby the index value of the register to be accessed is written to I/O port 22H, followed by the data transaction at I/O port 23H. Section 4.3 provides a detailed description of these registers.

4.1.4 NMI Handler

The 82C636 contains two inputs, NMI1* and NMI2* which can be connected to sources causing NMI to the CPU. These signals are sensed as active low and any time either of these pins are active, an NMI to the CPU is generated via the NMIIN output pin. The NMI caused due to the input pins can be selectively enabled or disabled by programming REG54H<3> and REG54H<2> respectively. The fact that NMI1* or NMI2* input caused an NMI is registered in REG59H<4> and REG59H<3> respectively. The 82C636 also generates an NMI to the CPU any time the power switch PSW* is activated and the 82C636 is not in stand-by mode. NMI due to the switch activity is registered in bit 2 of the same register. NMI due to switch is re-triggerable and used in the suspend/resume function (discussed later), and NMI due to the input pins is not re-triggerable.

4.1.5 Programmable I/O Block

The 82C636 contains a pair of byte wide programmable ports, PIO0-7 and PIO8-15, which can be configured as either input or output ports on a bit per bit basis. The CHIPSet registers, REG5AH<7:0> and REG5CH<7:0> are the direction control registers for PIO0-7 and PIO8-15 respectively and REG5BH<7:0> and REG5DH<7:0> are the status/command registers for PIO0-7 and PIO8-15 respectively. The default configuration of the pins PIO0-7 is input and that of PIO8-15 is output. During stand-by mode, these lines are all tri-stated and therefore all unused input pins should be pulled down to ground through a 10 KOhm resistor.

4.1.6 Refresh Support Logic

The 82C636 provides the DRAM refresh requests to the 82C241/82C841. During normal operations (when the system is not in stand-by mode), the 82C206 generates active low refresh requests to the 82C636 on the 206REF* line. The 82C636 passes this to the 82C241/82C841 as the DRAM refresh requests on the PCUREF* line to generate the necessary refresh cycles. During the stand-by mode, the 82C206 does not generate any refresh requests. Instead, the 82C636 generates these requests only if the BKMMPWR is active (implying that the power to the DRAMs is active and the DRAMs need to be refreshed). These refresh requests are active high pulses, whose width is controlled by a RC circuit connected across the DLYO and DLYI lines of the 82C636. The 82C241/82C841 uses these pulses directly to generate the RASs to the DRAMs. It is therefore crucial to meet the RAS pulse width requirements of the DRAMs during refresh.

The rate of refresh requests from the 82C636 can be varied to support slow refresh DRAMs. In power-on mode, the 82C206 can be programmed to generate the refresh requests at the rate of either 15us for normal DRAMs or at 120us for slow refresh DRAMs. During the stand-by mode, the 82C636 can do the same to support either of DRAMs. The input pin SLWDRAM along with REG54H<7> provides an option to generate the refresh requests at the slower rate. For normal refresh rate of 15us, this pin should be tied low and this automatically disables the programmability of the above bit for slow refresh rate. If slow refresh DRAMs are used, this pin must be tied high and REG54H<7> must be set to one to generate refresh requests at the rate of 120us. This allows the flexibility of disabling this feature on a system, in which memory is expanded using normal refresh DRAMs.

In a system which does not intend to implement the suspend/resume function, there is no need for refresh requests during stand-by mode as the BKMMPWR is turned off. In such cases the RC circuit on the DLYO and DLYI lines is not needed and DLYI must be tied to ground.

4.1.7 Power Control Block

The power control block is responsible for the monitoring and control of the various power supplies in the system. Section 4.2 describes in detail the functions supported by this block.

4.2 Features and Functions

The 82C636 provides all the necessary functions to perform power sequencing, and support the suspend and resume functions in a typical laptop environment. A power-on sequence is started anytime either the power switch line, PSW, is activated, the scheduled power-on is requested or a modem ring is detected. The power switch activity always generates a power-on sequence and the scheduled power-on and the power-on due to modem ring are optional programmable features.

The 82C636 allows the system software to select between two power-off modes. One is the total power down mode, in which the entire system power is turned off, including power to the memory subsystem. In this mode, the BKMMPWR signal is inactive and no refresh requests are generated. After entering this mode the contents of the DRAMs will not be valid on the next power-on. The second mode is the stand-by power mode, in which the entire system power is turned off except for the power to the memory subsystem. In this mode, the BKMMPWR signal is active and refresh requests are generated at the PCUREF pin in order to maintain the integrity of the data in the DRAMs until the next power-on.

4.2.1 Power-ON Sequence

Upon sensing the start of the power sequence, the 82C636 activates the power control signals, MPVCC and BKMMPWR, and tries to turn on the main power to the system. After about 8ms, it enables the sensing of the two power fail pins, the PF1 and PF2. If either of these are active, then the power-on sequence is aborted and stand-by mode is entered. In this stand-by mode, the MPVCC and BKMMPWR control signals are deactivated to turn the power supply off and the PWF* pin is asserted to indicate the power-fail status.

If neither PF1 nor PF2 is active, the 82C636 waits about two seconds for the power good signal, PG, to be active. When the PG pin is sensed active, the STDBY* signal is released followed by the RESET1* signal being pulsed to complete the power-on sequence. The system is now ready to start its normal operation. However, if the PG pin is sensed to be inactive after the two second wait, then the power-on sequence is aborted and the 82C636 enters the stand-by mode by deactivating the MPVCC control signal.

The PGPI (Power Good Polarity Indicator) input pin of the 82C636 controls the polarity of the active states of the status signals, PG, PF1, and PF2. If the PGPI input is tied high, then the PG input signal is interpreted as active high and the PF1 and PF2 signals are interpreted as active low. On the other hand, if PGPI is tied low, then the PG signal is interpreted as active low and the PF1 and PF2 signals are interpreted as active high. An application which does not use the stand-by mode could tie PGPI, PG, PF1, and PF2

either a high or low, leading to a definite power-on sequence at all times.

4.2.2 Power-OFF Sequence

The 82C636 performs a systematic power-off sequence, which provides the ability for the system to implement the Suspend/Resume function. Power-off can be initiated by either programming the power control register (REG55H<7:0>) or by some external hardware activity. Either the stand-by mode or the total power-off mode can be entered using the programmed method. Total power-off mode is entered by writing a zero to REG55H<7,2>, to control the MPVCC and BKMMPWR pins respectively. The panel backlight power, serial port power, modem power, display (VLCD) power, disk drive power and display buffer powers are also turned off by writing a zero to REG55H<7>. The BKMMPWR is the only signal that can be independently controlled. Stand-by mode is entered by writing a one to REG55H<2>, in which case the BKMMPWR will not be turned off.

Hardware initiated power-off can be due to activity on the power switch, PSW line, or by the PG pin going inactive or the PF1 or PF2 lines going active. In all cases, the 82C636 will perform the power-off sequence by generating an NMI. The cause of this NMI is registered in REG59H<2>. This NMI is routed to the CPU through the 82C241/82C841. If the CPU ignores this NMI, then the 82C636 will wait for two seconds and then enter the stand-by mode. On the other hand, the CPU can respond to this NMI and enter the suspend mode (discussed later). Also, by writing a one to REG59H<0>, a re-triggering of this NMI condition can be requested. Upon doing so, the NMI is posted again after a short time interval. The time interval between successive NMI postings can vary randomly between 4-8ms. This gives the CPU more time to complete the house keeping before entering the suspend state, as the two seconds timeout for the 82C636 to turn powers off starts only after the last NMI generated. After all the house keeping, the CPU can program the 82C636 to enter the stand-by mode as explained earlier. Exit from standby mode is only through the power-on sequence explained earlier.

4.2.3 Scheduled and Modem Ring Power ON

The 82C636 performs a power-on sequence, similar to the one mentioned earlier, at a pre-programmed time or in response to a modem ring. The CHIPSet register, indexes 50H-53H in the 82C636 can be programmed for a scheduled time at which the system power should be turned on. These registers can be written only if this feature is enabled, by writing a one into REG54H<6>. Typically, the scheduled time is programmed and the system is powered down into total power down or stand-by modes. After the elapsed interval of time, the 82C636 performs a power-on sequence. This cause of power-on is also registered into REG58H<2>.

The 82C636 can also perform a power-on sequence in response to a pre-programmed number of modem rings. This feature is enabled by setting REGH54H<5> and by programming the number of rings into REG56H<3:0>. A counter in the background counts up on every ring it detects. After the programmed number of rings, a power-on sequence is performed. If the ring stops before the count is reached, the power-on sequence is not performed and four seconds after the last ring is detected the counter is cleared. This cause of power-on is also registered into REG58H<3>.

4.2.4 Suspend/Resume Support

It may be desirable to temporarily turn the system power off and then back on into the same state as before the last power off, without having to re-boot the system. Before entering the stand-by mode, if the system has prepared itself such that it can come back to the existing state upon next power-on, then the system is referred to as being in the suspend mode. The process of such a preparation is referred to as suspend function. On power-on the process of getting back to the state before the last power-off is referred to as the resume function. In response to the NMI due to the activity on the PSW* line, the NMI service routine can use the re-trigger NMI feature in the 82C636 to buy time for all the house keeping activity needed for the suspend function. After the system enters the stand-by mode, the 82C636 supports the refresh of the

DRAMs in order to maintain the data in the DRAMs until the next power-on sequence. When the 82C636 turns the powers off after the two second timeout in response to the NMI, all the powers except the memory subsystem power (BKMMPWR) will be turned off. As a result DRAM refresh will still be performed and power consumed. The 82C636 should not be allowed to turn the system powers off after the time out if the suspend/resume function is not desired. Therefore it is wise to always use the programmed method to power off and enter either the total power-off mode or the stand-by mode.

4.2.5 Video Power Control

The 82C636 has an ability built into it to monitor and control the power to the video system such as the panel backlight power. By programming a counter located at REG57H<> to a non-zero value, video power control is enabled. When the counter counts down to zero, the control line to the backlight power source (ELPWR) goes inactive. This count down is at the rate of 32 seconds per count. Two more display related power sources can be controlled using the same counter and using the control lines DISPPWR and DBUFPWR. REG54H<0> and REG54H<1> are used to control the DISPPWR and DBUFPWR lines respectively. Writing a one into these bits enables this control. This activity is totally transparent to the operating system and application programs because the power is turned back on automatically anytime a keystroke is detected. Also, by setting REG54H<4> to a one, any access to the video buffer area will also turn on the power. Every time these powers are turned back on, the counter automatically gets reloaded to its initial value. This feature can be totally disabled by writing a value of zero into REG57H<>. The 82C636 uses the KI* input and the VRAMSEL* input to detect the keyboard activity and video buffer access respectively. Typically, the KI* input is connected to the keyboard interrupt line. The VRAMSEL* input to the 82C636 is connected to the VRAMSEL* output from the 82C241/82C841 which is active anytime the video buffer area between 0A0000H and 0BFFFFH is accessed.

4.2.6 Keyboard Power

The keyboard power can be supplied by a separate power source. This power can be turned on or off using the control signal KBPWR*. This line is not programmable, but is active any time the MPVCC line is active. It is also active all the time if the input status line ACC* is active, indicating that an AC source of power supply is used for the system. Thus, if an AC source is used, despite the main power being off (MPVCC inactive), the keyboard power will be on.

4.2.7 Significant Input Pins

Some of the input pins and their significance are discussed here.

- The PGPI input pin controls the interpretation of the active states of the PG, PF1, PF2, LOBAT, and LOBKBAT inputs. When it is tied low, the PG, LOBAT, and LOBKBAT pins are interpreted as active low and the PF1 and PF2 pins are interpreted as active high and when tied high, the PG, LOBATT, and LOBKBAT pins are interpreted as active high and the PF1 and PF2 pins are interpreted as active low.

- The PSW, PG, PF1, and PF2 cause the NMI output to go active.

- The SWTP input pin controls the interpretation of the PSW line activity. When an ON/OFF type switch is used, this line should be tied low and when a momentary toggle switch is used, it should be tied high.

- The ACC* input is used to indicate that an AC power source is used to power the system.

- The LOBAT and LOBKBAT are inputs which indicate the status of the batteries used.

- The BKBATD* line is an indication showing that the backup battery used to power the 82C636 is dead. A low to high transition on this line resets the 82C636 and all its internal circuitry.

4.3 82C636 Configuration Registers

The 82C636 contains a set of configuration/control registers. They are accessed by an indexing scheme, whereby the index value of the register to be accessed is written to I/O port 22H, followed by the data transaction at I/O port 23H.

Index: 50H **Scheduled Power ON - Seconds Register**

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
SEC HI3	SEC HI2	SEC HI1	SEC HI0	SEC LO3	SEC LO2	SEC LO1	SEC LO0

Bits	Access	Default	Function
7..4	R/W	0..0	High byte of seconds count in BCD (0-6)
3..0	R/W	0..0	Low byte of seconds count in BCD (0-9)

Index: 51H **Scheduled Power ON - Minutes Register**

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
MIN HI3	MIN HI2	MIN HI1	MIN HI0	MIN LO3	MIN LO2	MIN LO1	MIN LO0

Bits	Access	Default	Function
7..4	R/W	0..0	High byte of minutes count in BCD (0-6)
3..0	R/W	0..0	Low byte of minutes count in BCD (0-9)

Index: 52H **Scheduled Power ON - Hours Register**

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
HRS HI3	HRS HI2	HRS HI1	HRS HI0	HRS LO3	HRS LO2	HRS LO1	HRS LO0

Bits	Access	Default	Function
7..4	R/W	0..0	High byte of hours count in BCD (0-2)
3..0	R/W	0..0	Low byte of hours count in BCD (0-9)

Index: 53H **Scheduled Power ON - Days Register**

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
--	--	--	--	--	DAY2	DAY1	DAY0

Bits	Access	Default	Function
7..3	R/W	0..0	Reserved
2..0	R/W	0..0	Days count in BCD (0-7)

** Index 50H-53H are writable only when bit 6 of Index 54 is zero

Index: 54H **PCU Functions Enable Register**

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
SLOW REFSH	SCHED PWR ON	RING PWR ON	VFEL PWR ON	NMI1 EN	NMI2 EN	ELCNTR DBUFF PWR	ELCNTR DISP PWR

Bits	Access	Default	Function
7	R/W	1	Slow refresh rate for slow refresh DRAMS 0 = Disable 1 = Enable
6	R/W	0	Schedule Power on by PCU 0 = Disable 1 = Enable
5	R/W	0	Power ON due to modem ring 0 = Disable 1 = Enable
4	R/W	0	Power ON the panel backlight due to video buffer accesses 0 = Disable 1 = Enable
3	R/W	0	External NMI1 recognition 0 = Disable 1 = Enable
2	R/W	0	External NMI2 recognition 0 = Disable 1 = Enable
1	R/W	0	Display power control using EL counter timeout and DBUFPWR 0 = Disable 1 = Enable
0	R/W	0	Display power control using EL counter timeout and DISPPWR 0 = Disable 1 = Enable

Index: 55H **Power Control Register**

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
VCC PWR	EL PWR	RS232C PWR	MODEM PWR	DISP PWR	MEM PWR	SCSI PWR	DBUFF PWR

Bits	Access	Default	Function
7	R/W	0	Main Power VCC 0 = OFF 1 = ON
6	R/W	0	Panel backlight power using ELPWR 0 = OFF 1 = ON
5	R/W	0	RS232 Power 0 = OFF 1 = ON
4	R/W	0	Modem Power 0 = OFF 1 = ON
3	R/W	0	Display Power using DISPPWR 0 = OFF 1 = ON
2	R/W	1	Memory Power 0 = OFF 1 = ON
1	R/W	0	SCSI Power 0 = OFF 1 = ON
0	R/W	0	Display Power using DBUFPWR 0 = OFF 1 = ON

Index: 56H **Modem Ring Power ON count Register**

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
--	--	--	--	RING CNT3	RING CNT2	RING CNT1	RING CNT0

Bits	Access	Default	Function
7..4	R/W	0..0	Reserved
3..0	R/W	0..0	Number of ring counts before power up in hex (0H-FH)

Index: 57H **EL Power OFF count Register**

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
ELCNT7	ELCNT6	ELCNT5	ELCNT4	ELCNT3	ELCNT2	ELCNT1	ELCNT0

Bits	Access	Default	Function
7..0	R/W	0..0	Counter value to turn powers off controlled by ELPWR, DISPPWR and DBUFFPWR. The counter counts once every 32 seconds. 0 = disable power OFF function 1-255 = enable power OFF and use this count

Index: 58H **PCU Status Register**

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PWR FAIL	MAIN BAT	AC OPER	PWR SW ON	RING ON	ALARM ON	BKUP PWR GD	BKUP PWR ST

Bits	Access	Default	Function
7	R	0	Power failure indication 0 = did not occur 1 = did occur (maintained asserted till read by CPU)
6	R	X	Main Battery condition 0 = Weak 1 = Good
5	R	X	AC cube operation 0 = battery 1 = AC cube
4	R	X	Power ON due to power switch 0 = False 1 = True (maintained asserted till read by CPU)
3	R	X	Power ON due to modem ring 0 = False 1 = True (maintained asserted till read by CPU)
2	R	X	Power ON due to scheduled power ON option 0 = False 1 = True (maintained asserted till read by CPU)
1	R	X	Backup Battery Power status 0 = Dead 1 = Good (maintained asserted till read by CPU)
0	R	X	Backup Battery status 0 = Weak 1 = Good (maintained asserted till read by CPU)

Index: 59H

PCU NMI Status Register

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
--	--	--	NMI1	NMI2	PWR SW	PWR FL	RETRIG

Bits	Access	Default	Function
7..5	R	0	Reserved
4	R	0	Status of NMI1 Pin 0 = NMI did not occur 1 = NMI occurred (maintained asserted till read by CPU)
3	R	0	Status of NMI2 Pin 0 = NMI did not occur 1 = NMI occurred (maintained asserted till read by CPU)
2	R	0	NMI due to Power switch OFF 0 = NMI did not occur 1 = NMI occurred (maintained asserted till read by CPU)
1	R	0	NMI due to power fail 0 = NMI did not occur 1 = NMI occurred (maintained asserted till read by CPU)
0	R/W	0	Re-trigger NMI at a variable time interval. 0 = Disable 1 = Enable

Index: 5AH

PIO1 Direction Control Register

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
IO7	IO6	IO5	IO4	IO3	IO2	IO1	IO0

Bits	Access	Default	Function
7..0	R/W	1..1	Pin direction of PIO1 bits 7-0 pins. 1 = Input 0 = Output

Index: 5BH

PIO1 Data/Status Register

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
D7	D6	D5	D4	D3	D2	D1	D0

Bits	Access	Default	Function
7..0	R/W	X..X	Data/Status at PIO1 bits 7-0 pins.

Index: 5CH

PIO2 Direction Control Register

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
IO7	IO6	IO5	IO4	IO3	IO2	IO1	IO0

Bits	Access	Default	Function
7..0	R/W	0..0	Pin direction of PIO2 bits 7-0 pins. 1 = Input 0 = Output

Index: 5DH

PIO2 Data/Status Register

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
D7	D6	D5	D4	D3	D2	D1	D0

Bits	Access	Default	Function
7..0	R/W	X..X	Data/Status at PIO2 bits 7-0 pins.

4.4 82C636 Pin Assignments

Type	Symbol	Description
System Interface		
O	STDBY*	Stand-by - indicates that the system is in Stand-by Mode.
O	RESET1*	Reset for CHIPSet - used as Reset signal input to the 82C241.
I	PCUCS*	82C636 PCU Chip Select - used to select the internal registers of the chip via I/O addresses 22H and 23H.
I	206REF*	Refresh Request - input from 82C206 which indicates a refresh request for the DRAMs.
I	IOR*	I/O Read - used to enable I/O read from internal registers via I/O addresses 22H and 23H.
I	IOW*	I/O Write - used to enable I/O write to the internal registers via I/O addresses 22H and 23H enable.
I	SA0	Address A0 - used to access internal registers of the chip. 0 - Index Register at 22H is selected 1 - Data Register at 22H is selected
I/O	XD<7:0>	Data bus D7..D0 - bidirectional data bus signals used to access to internal registers.
O	NMIIN	NMI output - used to indicate power switch activity, or power failure due to PF1, PF2, or PG, lines activity. This signal is not generated in Stand-by mode.
I	X1	Crystal input for the 32.768KHz.
O	X2	Crystal output for the 32.768KHz.
O	OSC32K	32.768KHz oscillator output for 82C206's use.
I	TEST	Test pin - must be tied low for normal operation.
I	NMI1*	External NMI source 1 - used to generate NMI.
I	NMI2*	External NMI source 2 - used to generate NMI.
I	VCC	+5V power supply (tied to backup power).
I	GND	Ground.
Power On Control Signals:		
I	RI*	Ring on phone line - used to detect rings on the modem line and is connected to the ring detecting circuitry in the modem.
I	PSW*	Power Switch - connected to a power switch. If a toggle switch type is chosen, the signal is sensed active low. If an ON/OFF switch type is chosen, a high is sensed as ON and a low is sensed as OFF.

4.4 82C636 Pin Assignments(continued)

Type	Symbol	Description
I	KI*	Keyboard Interrupt - detects a keystroke and is used to activate ELPWR, DISPPWR, and DBUFPWR.
I	VRAMSEL*	Video RAM access signal - detects a video RAM access detect signal and is used to activate ELPWR, DISPPWR and DBUFPWR.
Power Unit Status Lines:		
I	PGPI	Power Good Polarity Indicator - used to interpret the active states of input status pins as follows: 0 : PG, LOBATT and LOBKBAT inputs are sensed as active low and PF1 and PF2 are sensed as active high. 1 : PG, LOBATT and LOBKBAT inputs are sensed as active high and PF1 and PF2 are sensed as active low.
I	PG	Power Good - sense the validity of system power. If detected inactive during system power on, MPVCC and BKMMPWR power control lines are deactivated and Stand-by Mode is entered.
I	PF1	Power Fail-1 - used to sense power source 1 failure.
I	PF2	Power Fail-2 - used to sense power source 2 failure.
I	ACC*	AC Cube operation - used to sense AC Cube in use as power source.
I	LOBAT	Low Battery - used to sense the status of the main battery source.
I	LOBKBAT	Low Backup Battery - used to sense the status of the backup battery source.
I	BKBATD*	Backup Battery Dead - used to sense status of the battery supplying power to the 82C636. A low to high transition on this line resets the 82C636 internally.
O	PWRF*	Power Failure - indicates power failure condition during power-on.
I	SWTP	Switch Type - used to interpret the type of the power switch being used. A low indicates a ON/OFF (SPDT) switch and a high indicates a toggle switch (SPST) is used.
Control Outputs for Powers		
O	MPVCC	Main Power V_{CC} - Signal to control the main power to the system.
O	232PWR	RS232C Power - Signal to control the RS232C buffers power.
O	MDMPWR	MODEM Power - Signal to control the MODEM power.
O	DISPPWR	Display Power - Signal to control a display module power (panel).
O	ELPWR	Electrical Luminance Power - Signal to control panel backlight power.
O	BKMMPWR	Backup Memory Power - Signal to control the power to the memory subsystem.

4.4 82C636 Pin Assignments(continued)

Type	Symbol	Description
O	SCSIPWR	SCSI Power - Signal to control the SCSI power (disk drives).
O	DBUFPWR	Display Buffer Power - Signal to control a display module power (VGA output circuitry).
O	KBPWR*	Keyboard power control - It is active all the time, if AC power is used and otherwise is active only if MPVCC is active.
Slow Refresh DRAM		
I	DLYI	Delay In - Delay line in to generate the appropriate refresh request pulse widths in stand-by mode.
O	DLYO	Delay out - Delay line in to generate the appropriate refresh request pulse widths in stand-by mode.
O	PCUREF*	PCU Refresh request - DRAM Refresh request for 82C241 (82C841). It is active low for normal mode and active high for stand-by mode.
I	REF*	System Refresh - Indicates the system memory controller is in the refresh cycle. PCU waits till refresh cycle is completed to enter Stand-by mode.
I	SLWDRAM	Slow refresh DRAM select pin - must be strapped as follows: 1 : Indicates slow refresh DRAM is used 0 : Indicates regular refresh DRAM is used
General I/O control		
I/O	PIO0-15	Programmable I/O control - Programmable input/output pins controlled by contents of index registers 5AH-5DH.

4.5 Pinout List

Pin	Name	Pin	Name	Pin	Name
1	PCUCS*	28	X1	55	232PWR
2	SA0	29	PIO15	56	PIO7
3	IOW*	30	PIO14	57	PIO6
4	IOR*	31	GND	58	PIO5
5	OSC32K	32	VCC	59	PSW*
6	RESET1*	33	VCC	60	RI*
7	XD7	34	SLWDRAM	61	KI*
8	XD6	35	PIO13	62	GND
9	XD5	36	PIO12	63	VRAMSEL*
10	XD4	37	PIO11	64	PGPI
11	VCC	38	PIO10	65	PG
12	GND	39	PIO9	66	PF1
13	GND	40	PIO8	67	PF2
14	REF*	41	KBPWR*	68	PIO4
15	XD3	42	PWRF*	69	PIO3
16	XD2	43	N.C	70	PIO2
17	XD1	44	MDMPWR	71	GND
18	XD0	45	DISPPWR	72	VCC
19	PCUREF	46	DBUFPWR	73	VCC
20	DLYO	47	SCSIPWR	74	PIO1
21	DLYI	48	BKMMPWR	75	PIO0
22	206REF*	49	VCC	76	SWTP
23	LOBKBAT	50	ELPWR	77	NMIIN
24	LOBAT	51	ACC*	78	NMI1*
25	BKBATD*	52	GND	79	NMI2*
26	TEST	53	N.C	80	STDBY*
27	X2	54	MPVCC		

Name	Pin	Name	Pin	Name	Pin
206REF*	22	NMI2*	79	REF*	14
232PWR	55	NMIIN	77	RESET1*	6
ACC*	51	OSC32K	5	RI*	60
BKBATD*	25	PCUCS*	1	SA0	2
BKMMPWR	48	PCUREF	19	SCSIPWR	47
DBUFPWR	46	PF1	66	SLWDRAM	34
DISPPWR	45	PF2	67	STDBY*	80
DLYI	21	PG	65	SWTP	76
DLYO	20	PGPI	64	TEST	26
ELPWR	50	PIO0	75	VCC	11
GND	12	PIO1	74	VCC	32
GND	13	PIO10	38	VCC	33
GND	31	PIO11	37	VCC	49
GND	52	PIO12	36	VCC	72
GND	62	PIO13	35	VCC	73
GND	71	PIO14	30	VRAMSEL*	63
IOR*	4	PIO15	29	X1	28
IOW*	3	PIO2	70	X2	27
KBPWR*	41	PIO3	69	XD0	18
KI*	61	PIO4	68	XD1	17
LOBAT	24	PIO5	58	XD2	16
LOBKBAT	23	PIO6	57	XD3	15
MDMPWR	44	PIO7	56	XD4	10
MPVCC	54	PIO8	40	XD5	9
N.C	43	PIO9	39	XD6	8
N.C	53	PSW*	59	XD7	7
NMI1*	78	PWRF*	42		

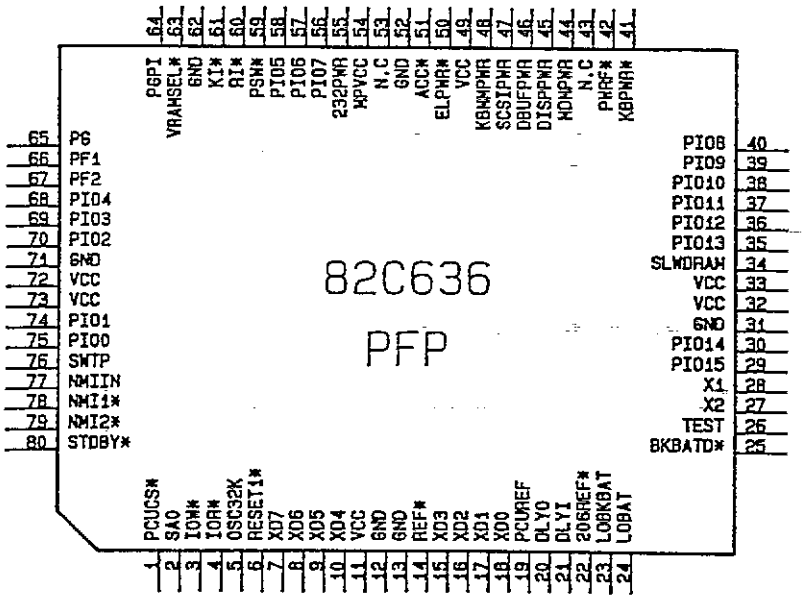
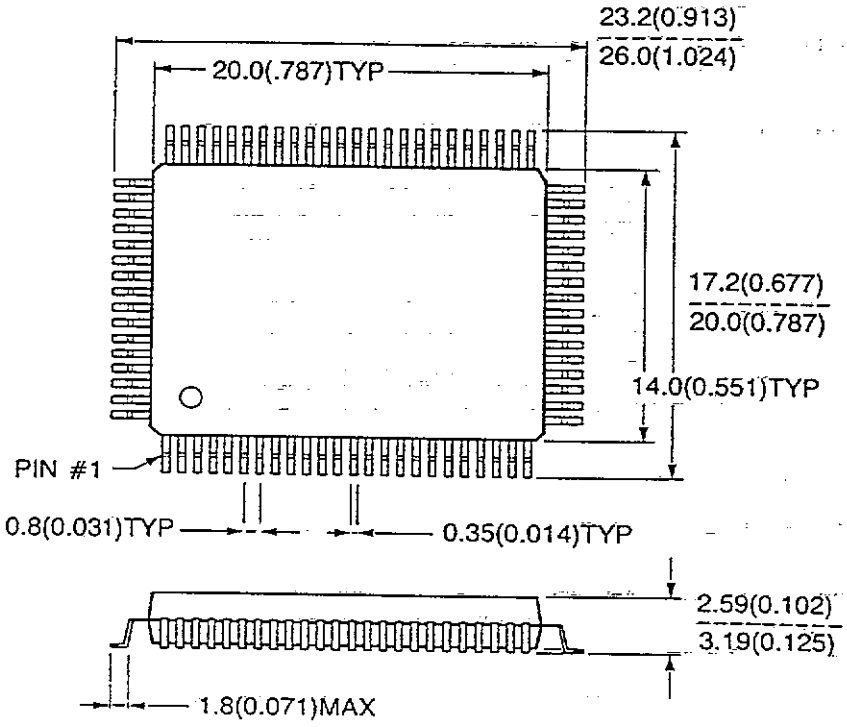


Figure 4.2. 82C636 Pin Diagram

4.6 Physical Dimensions

80-Pin Plastic Flat Package (Rectangular) Dimensions: mm(in)



4.7 82C636 Absolute Ratings

Parameter	Symbol	Min.	Max.	Units
Supply Voltage	V_{CC}	-	7.0	V
Input Voltage	V_I	-0.5	5.5	V
Output Voltage	V_O	-0.5	5.5	V
Operating Temperature	T_{OP}	-25°	85°	C
Storage Temperature	T_{STG}	-40°	125°	C

NOTE: Permanent device damage may occur if Absolute Maximum Ratings are exceeded. Functional operation should be restricted to the conditions described under Operating Conditions.

4.8 82C636 Operating Conditions

Parameter	Symbol	Min.	Max.	Units
Supply Voltage	V_{CC}	4.75	5.25	V
Ambient Temperature	T_A	0°	70°	C

4.9 82C636 DC Characteristics

Parameter	Symbol	Min.	Max.	Units
Input Low Voltage	V_{IL}	-	0.8	V
Input High Voltage	V_{IH}	2.0	-	V
Output Low Voltage	V_{OL}	-	0.2	V
Output High Voltage	V_{OH}	3.84	-	V
Input Low Current ($0 < V_{IN} < V_{CC}$)	I_{IL}	-	± 10	uA
Output High-Z Leakage Current ($0 < V_{IN} < V_{CC}$)	I_{OZI}	-	± 10	uA
Static Power Supply Current @5V	I_{CCSB}		1.5	mA

I_{OH} and I_{OL} - Output drive capability:

4mA: STDBY*, RESET1*, XD7-XD0, NMIIN, X2, OSC32K, PWRF*, MPVCC, 232PWR, MDMPWR, DISPPWR, ELPWR, BKMMPWR, SCSIPWR, DBUFPWR, KBPWR*, PIO15-PIO0, PCUREF*, DLYO.

Power Supply Current I_{cc}

Mode	12 MHz		16 MHz		20 MHz		Units
	Min	Max	Min	Max	Min	Max	
Normal	-	4.9	-	5.3	-	5.6	mA
Sleep mode	-	3.8	-	3.8	-	3.8	mA
Stand-by	-	170	-	170	-	170	uA

Note:
1. Power consumption measured using 2 MB of local DRAM and double ROMs.
2. Normal mode measurements made at DOS prompt.
3. Sleep mode measurements made at DOS prompt and using Chips and Technology BIOS for LeAPSet and the smart sleep feature.

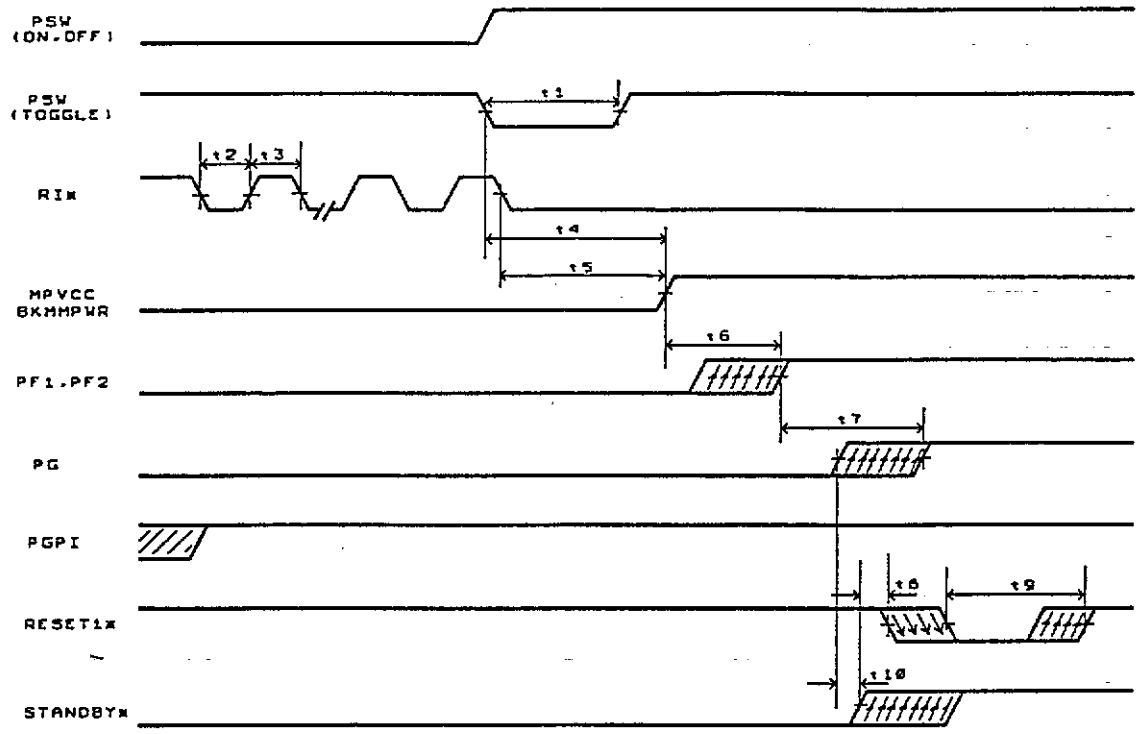
4.10 82C636 AC Characteristics

(T_A = 0°C to 70°C, V_{CC} = 5V ± 5%, C_L = 75pF, Speed = 12, 16 and 20MHz)

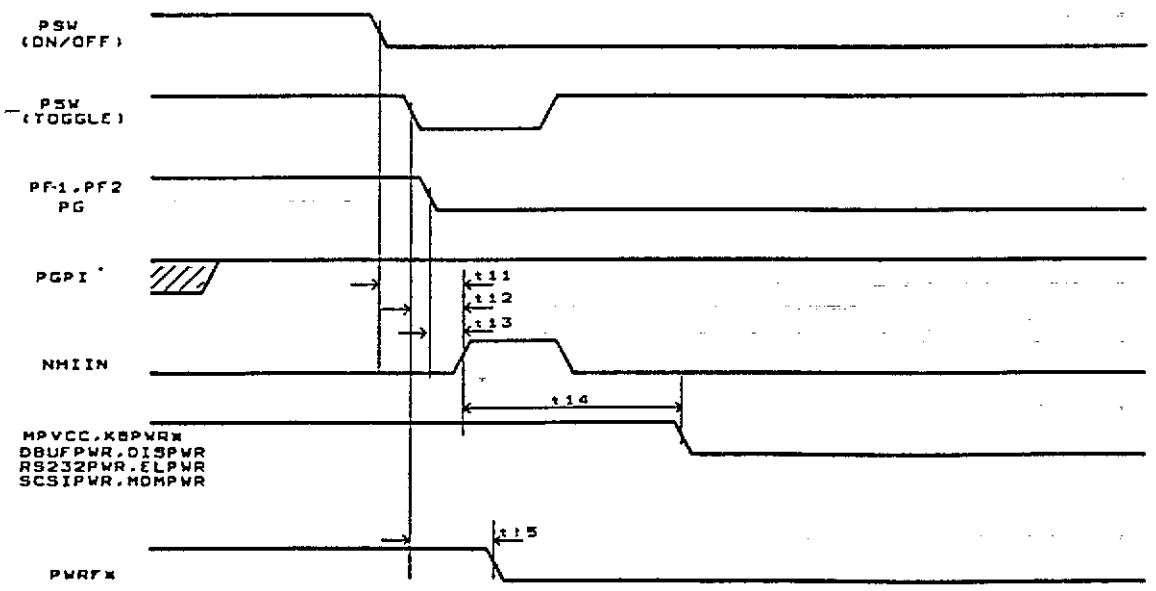
Sym	Description	Min.	Max.	Units
t1	PSW* pulse width	22		ms
t2	RI* low pulse width	320		ms
t3	RI* high pulse width	320		ms
t4	PSW* to $MPVCC_H$ delay		22	ms
t5	$RI*_L$ to $MPVCC_H$ delay		330	ms
t6	$MPVCC_H$ to PF1 PF2 active	8		ms
t7	PF1, PF2 to PG active		2	s
t8	$STDBY*_H$ to $RESET1_L$	15		us
t9	$RESET1_L$ pulse width	15		us
t10	PG_H to $STDBY*_L$	30		us
t11	PSW_L* to $NMIIN_H$ (ON/OFF switch)		20	ms
t12	PSW_L* to $NMIIN_H$ (toggle switch)		20	ms
t13	PF1, PF2, PG active to $NMIIN_H$		30	us
t14	$NMIIN_H$ to MPVCC, KBPWR, DBUFPWR, DISPWR, RS232PWR, ELPWR, SCSIPWR, MDMPWR inactive		2	s
t15	PF1, PF2 active to $PWRF*_L$		30	us
t16	PCUREF pulse width	500		ns
t17	PCUREF* repetition rate			
	- normal refresh DRAM	15		us
	- slow refresh DRAM	120		us
t18	KI* input pulse width	10		ns
t19	VRAMSEL* input pulse width	10		ns
t20	$KI*_L$, $VRAMSEL*_L$ to ELPWR, DISPWR, DBUFPWR active	60		us
t21	$IOW*_L$ to powers off		60	us
t22	DLYO time period			
	- normal refresh DRAM	30		us
	- slow refresh DRAM	240		us
t23	$X1_H$ to $OSC32K_H$		15	ns
t24	$X1_L$ to $OSC32K_L$		15	ns
t29	XD setup to $IOW*_H$	15		ns
t30	XD hold time from $IOW*_H$	10		ns
t31	XD vaild time from $IOR*_L$		40	ns
t32	XD invalid time from $IOR*_H$		10	ns
t33	PIO0-15 setup time to $IOR*_L$	60		ns
t34	PIO0-15 hold time from $IOR*_H$	10		ns

NOTES: - Signal names with a subscript of "L" refers to the low going edge and "H" refers to the high going edge.

4.11 82C636 AC Timing Diagrams



POWER ON SEQUENCE



POWER OFF SEQUENCE

4.11 82C636 AC Timing Diagrams (continued)