

WARRANTY INFORMATION

Qua Tech Inc. warrants the QS-1000 to be free of defects for one (1) year from the date of purchase. Qua Tech Inc. will repair or replace any board that fails to perform under normal operating conditions and in accordance with the procedures outlined in this document during the warranty period. Any damage that results from improper installation, operation, or general misuse voids all warranty rights.

Although every attempt has been made to guarantee the accuracy of this manual, Qua Tech Inc. assumes no liability for damages resulting from errors in this document. Qua Tech Inc. reserves the right to edit or append to this document at any time without notice.

Please complete the following information and retain for your records. Have this information available when requesting warranty service.

DATE OF PURCHASE:

MODEL NUMBER: QS-1000

PRODUCT DESCRIPTION: FOUR CHANNEL RS-232 ASYNCHRONOUS  
COMMUNICATIONS ADAPTER

SERIAL NUMBER:

IBM<sup>TM</sup>, PS/2<sup>TM</sup>, and Micro Channel<sup>TM</sup> are registered trademarks of International Business Machines.

## TABLE OF CONTENTS

WARRANTY INFORMATION . . . . .	i
LIST OF FIGURES . . . . .	iii
I. INTRODUCTION . . . . .	1
II. BOARD DESCRIPTION . . . . .	1
III. 16550 FUNCTIONAL DESCRIPTION . . . . .	3
INTERRUPT ENABLE REGISTER . . . . .	4
INTERRUPT IDENTIFICATION REGISTER . . . . .	5
FIFO CONTROL REGISTER . . . . .	7
LINE CONTROL REGISTER . . . . .	8
MODEM CONTROL REGISTER . . . . .	10
LINE STATUS REGISTER . . . . .	11
MODEM STATUS REGISTER . . . . .	13
SCRATCHPAD REGISTER . . . . .	14
FIFO INTERRUPT MODE OPERATION . . . . .	14
BAUD RATE SELECTION . . . . .	14
IV. ADDRESSING OPTIONS . . . . .	16
V. INTERRUPTS . . . . .	17
INTERRUPT STATUS REGISTER . . . . .	17
VI. PROGRAMMABLE OPTION SELECT . . . . .	18
VII. EXTERNAL CONNECTIONS . . . . .	22
VIII. HARDWARE INSTALLATION . . . . .	25
IX. CHANGING ADDRESSING MODES . . . . .	26
X. ADDITIONAL BLOCK MODE ADDRESSING . . . . .	27
XI. SPECIFICATIONS . . . . .	32

## LIST OF FIGURES

Figure 1.	QS-1000 board layout . . . . .	2
Figure 2.	16550 register map . . . . .	3
Figure 3.	Interrupt Identification Register . . . . .	6
Figure 4.	FIFO receiver trigger levels . . . . .	7
Figure 5.	Parity options . . . . .	9
Figure 6.	Word length and stop bit options . . . . .	9
Figure 7.	Input clock frequency options . . . . .	15
Figure 8.	Baud rate selections . . . . .	15
Figure 9.	Block mode address assignments . . . . .	16
Figure 10.	QS-1000 POS implementation . . . . .	19
Figure 11.	Discrete mode address selections . . . . .	20
Figure 12.	Interrupt selections . . . . .	20
Figure 13.	Output connector options . . . . .	22
Figure 14.	Output connector signal definitions . . . . .	23
Figure 15.	Handshake selection jumper . . . . .	24
Figure 16.	Handshake configurations . . . . .	24
Figure 17.	QTINSTAL.EXE opening menu . . . . .	28
Figure 18.	QTINSTAL.EXE address selection menu . . . . .	29
Figure 19.	QTINSTAL.EXE address input . . . . .	30
Figure 20.	QTINSTAL.EXE updated address menu . . . . .	31

## **I. INTRODUCTION**

The Qua Tech QS-1000 provides four independent asynchronous RS-232 serial communication channels for systems utilizing the MicroChannel architecture. Each port may be accessed individually from the predefined addresses of Serial 1 through Serial 8 or the four channels may be grouped together and located anywhere within the available I/O address range of the system. Two output options increase flexibility by allowing complete compatibility with a standard 25-pin connector or an abbreviated 6-wire phone jack style connector.

The QS-1000 serial interface is realized through four 16550 ACEs (Asynchronous Communication Elements). The 16550 is compatible with the 8250 and 16450 ACEs used in the PC/XT/AT models. In addition, the 16550 supports a FIFO mode to reduce CPU overhead at higher data rates.

The QS-1000 address and interrupt selections are accessed through the Programmable Option Select using the IBM installation utilities. In addition, jumpers are provided to select input clock frequency and on-board loopback of 'handshake' signals.

## **II. BOARD DESCRIPTION**

A component diagram of the QS-1000 showing the locations of the 16550 ACEs, clock frequency jumper J1, handshake selection jumpers, D-37 output connector, and phone jack connector is shown in figure 1. If the phone jack option has been selected, jumpers J2 - J5 have been installed to control the output of handshake signals. If the D-37 option has been selected, jumpers J2 - J5 have been replaced by additional drivers and receivers to provide all of the available handshake signals. A detailed description of output options is available in section VII: External Connections.

FUNCTIONAL DESCRIPTION

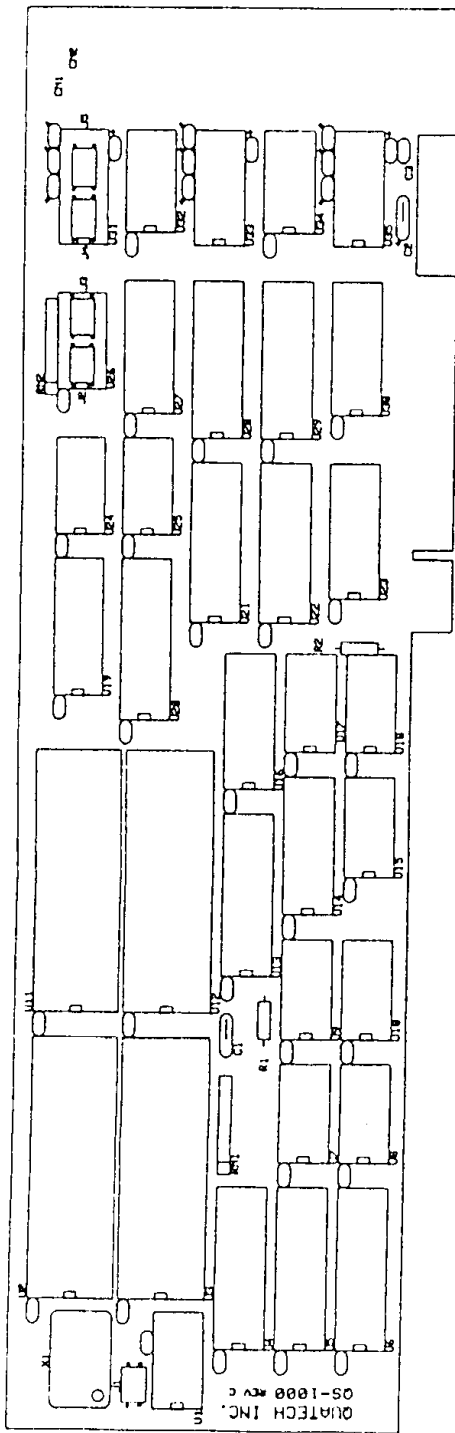


Figure 1. QS-1000 board layout.

**III. 16550 FUNCTIONAL DESCRIPTION**

The 16550 is an upgrade of the standard 16450 Asynchronous Communications Element (ACE). Designed to be compatible with the 16450, the 16550 enters the character mode on reset and in this mode will appear as a 16450 to user software. An additional mode, FIFO mode, can be selected to reduce CPU overhead at high data rates. The FIFO mode increases performance by providing two internal 16-byte FIFOs (one transmit and one receive) to buffer data and reduce the number of interrupts issued to the CPU.

Other features include:

- Programmable baud rate, character length, parity, and number of stop bits
- Automatic addition and removal of start, stop, and parity bits
- Independent and prioritized transmit, receive and status interrupts
- Transmitter clock output to drive receiver logic

The following pages provide a brief summary of the internal registers available within the 16550 ACE. The registers are addressed as shown in Figure 2 below.

DLAB	A2	A1	A0	REGISTER DESCRIPTION
0	0	0	0	Receive buffer (read only)
				Transmit holding register (write only)
0	0	0	1	Interrupt enable
x	0	1	0	Interrupt identification (read only)
				FIFO control (write only)
x	0	1	1	Line control
x	1	0	0	MODEM control
x	1	0	1	Line status
x	1	1	0	MODEM status
x	1	1	1	Scratch
1	0	0	0	Divisor latch (least significant byte)
1	0	0	1	Divisor latch (most significant byte)

Figure 2. Internal register map for 16550 ACE. DLAB is accessed through the Line Control Register.

FUNCTIONAL DESCRIPTION

**INTERRUPT ENABLE REGISTER**

D7	0	
D6	0	
D5	0	
D4	0	
D3	EDSSI	----- MODEM status
D2	ELSI	----- Receiver line status
D1	ETBEI	----- Transmitter holding register empty
D0	ERBFI	----- Received data available

**CAUTION:**

To maintain compatibility with earlier personal computer systems, the user defined output, OUT 2, is used as an external interrupt enable and must be set active for interrupts to be acknowledged. OUT 2 is accessed through the 16550's MODEM control register.

EDSSI - MODEM Status Interrupt:

When set (logic 1), enables interrupt on clear to send, data set ready, ring indicator, and data carrier detect.

ELSI - Receiver Line Status Interrupt:

When set (logic 1), enables interrupt on overrun, parity, and framing errors, and break indication.

ETBEI - Transmitter Holding Register Empty Interrupt:

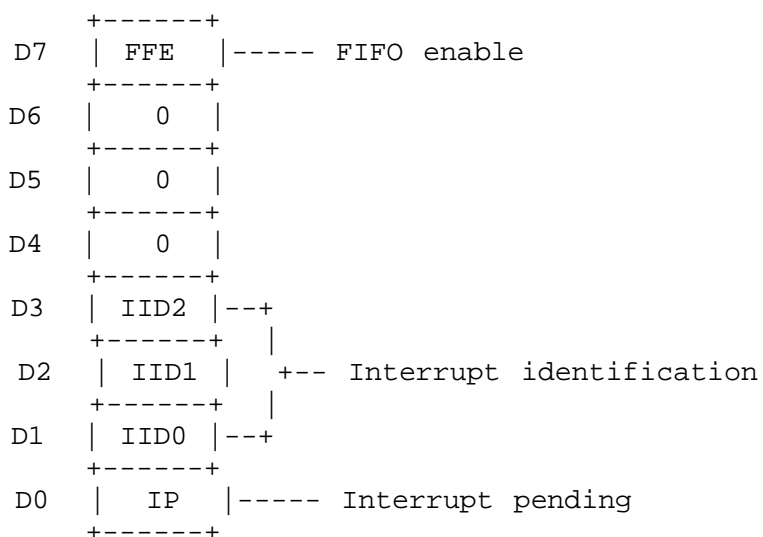
When set (logic 1), enables interrupt on transmitter register empty.

ERBFI - Received Data Available Interrupt:

When set (logic 1), enables interrupt on received data available or FIFO trigger level.

FUNCTIONAL DESCRIPTION

**INTERRUPT IDENTIFICATION REGISTER**



FFE - FIFO Enable:  
When logic 1, indicates FIFO mode enabled.

IIDx - Interrupt Identification:  
Indicates highest priority interrupt pending if any.  
See IP and Figure 3. NOTE: IID2 is always a logic 0  
in character mode.

IP - Interrupt Pending:  
When logic 0, indicates that an interrupt is pending  
and the contents of the interrupt identification  
register may be used to determine the interrupt  
source. See IIDx and Figure 3.



FUNCTIONAL DESCRIPTION

**INTERRUPT IDENTIFICATION REGISTER** (continued)

IID2	IID1	IID0	IP	Priority	Interrupt Type
x	x	x	1	N/A	None
0	1	1	0	Highest	Receiver Line Status
0	1	0	0	Second	Received Data Ready
1	1	0	0	Second	Character Timeout (FIFO only)
0	0	1	0	Third	Transmitter Holding Register Empty
0	0	0	0	Fourth	MODEM Status

Figure 3. Interrupt identification bit definitions.

Receiver Line Status:

Indicates overrun, parity, or framing errors or break interrupts. The interrupt is cleared by reading the line status register.

Received Data Ready:

Indicates receiver data available. The interrupt is cleared by reading the receiver buffer register

FIFO mode:

Indicates the receiver FIFO trigger level has been reached. The interrupt is reset when the FIFO drops below the the trigger level.

Character Timeout: (FIFO mode only)

Indicates no characters have been removed from or input to the receiver FIFO for the last four character times and there is at least one character in the FIFO during this time. The interrupt is cleared by reading the receiver FIFO.

Transmitter Holding Register Empty:

Indicates the transmitter holding register is empty. The interrupt is cleared by reading the interrupt identification register or writing to the transmitter holding register.

MODEM Status:

Indicates clear to send, data set ready, ring indicator, or data carrier detect have changed state. The interrupt is cleared by reading the MODEM status register.

**FIFO CONTROL REGISTER**

D7	RXT1	---+	
	+-----+		+-- Receiver trigger
D6	RXT0	---+	
	+-----+		
D5	x	---+	
	+-----+		+-- Reserved
D4	x	---+	
	+-----+		
D3	DMAM	-----	DMA mode select
	+-----+		
D2	XRST	-----	Transmit FIFO reset
	+-----+		
D1	RRST	-----	Receive FIFO reset
	+-----+		
D0	FE	-----	FIFO enable
	+-----+		

RXTx - Receiver FIFO Trigger Level:  
 Determines the trigger level for the FIFO interrupt as given in Figure 4 below.

RXT1 RXT0		RCVR FIFO Trigger level (bytes)
0	0	1
0	1	4
1	0	8
1	1	14

Figure 4. FIFO trigger levels.

DMAM - DMA Mode Select:  
 When set (logic 1), RxDY and TxDY change from mode 0 to mode 1. (DMA mode is not supported on the QS-1000.)

XRST - Transmit FIFO Reset:  
 When set (logic 1), all bytes in the transmitter FIFO are cleared and the counter is reset. The shift register is not cleared. XRST is self-clearing.

FUNCTIONAL DESCRIPTION

**FIFO CONTROL REGISTER** (continued)

- RRST - Receive FIFO Reset:  
When set (logic 1), all bytes in the receiver FIFO are cleared and the counter is reset. The shift register is not cleared. RRST is self-clearing.
- FE - FIFO Enable:  
When set (logic 1), enables transmitter and receiver FIFOs. When cleared (logic 0), all bytes in both FIFOs are cleared. This bit must be set when other bits in the FIFO control register are written to or the bits will be ignored.

**LINE CONTROL REGISTER**

D7	DLAB	-----	Divisor latch access bit
D6	BKN	-----	Break control
D5	STKP	-----	Stick parity
D4	EPS	-----	Even parity select
D3	PEN	-----	Parity enable
D2	STB	-----	Number of stop bits
D1	WLS1	--+	Word length select
D0	WLS0	--+	

- DLAB - Divisor Latch Access Bit:  
DLAB must be set to logic 1 to access the baud rate divisor latches. DLAB must be set to logic 0 to access the receiver buffer, transmitting holding register and interrupt enable register.
- BKN - Break Control:  
When set (logic 1), the serial output (SOUT) is forced to the spacing state (logic 0).
- STKP - Stick Parity:  
Forces parity to logic 1 or logic 0 if parity is enabled. See EPS, PEN, and Figure 5.

FUNCTIONAL DESCRIPTION

**LINE CONTROL REGISTER** (continued)

- EPS - Even Parity Select:  
Selects even or odd parity if parity is enabled.  
See STKP, PEN, and Figure 5.
- PEN - Parity Enable:  
Enables parity on transmission and verification on reception. See EPS, STKP, and Figure 5.

STKP	EPS	PEN	Parity
x	x	0	None
0	0	1	Odd
0	1	1	Even
1	0	1	Logic 1
1	1	1	Logic 0

Figure 5. 16550 parity selections.

- STB - Number of Stop Bits:  
Sets the number of stop bits transmitted. See WLSx and Figure 6.

- WLSx - Word Length Select:  
Determines the number of bits per transmitted word. See STB and Figure 6.

STB	WLS1	WLS0	Word length	Stop bits
0	0	0	5 bits	1
0	0	1	6 bits	1
0	1	0	7 bits	1
0	1	1	8 bits	1
1	0	0	5 bits	1½
1	0	1	6 bits	2
1	1	0	7 bits	2
1	1	1	8 bits	2

Figure 6. Word length and stop bit selections.

**MODEM CONTROL REGISTER**

D7	0	
D6	0	
D5	0	
D4	LOOP	----- Loopback enable
D3	OUT2	----- Output 2
D2	OUT1	----- Output 1
D1	RTS	----- Request to send
D0	DTR	----- Data terminal ready

**LOOP - Loopback Enable:**

When set (logic 1), the transmitter shift register is connected directly to the receiver shift register. The MODEM control inputs are internally connected to the MODEM control outputs and the outputs are forced to the inactive state.

Bits OUT2, OUT1, RTS, and DTR perform identical functions on their respective outputs. When these bits are set (logic 1) in the register, the associated output is forced to a logic 0. When cleared (logic 0), the output is forced to logic 1.

**OUT2 - Output 2:**

Controls the OUT2 output, pin 31, as described above. To maintain compatibility with earlier personal computer systems, OUT2 is used as an external interrupt enable and must be set active for interrupts to be acknowledged.

**OUT1 - Output 1:**

Controls the OUT1 output, pin 34, as described above. Unused on QS-1000.

**RTS - Request To Send:**

Controls the RTS output, pin 32, as described above.

**DTR - Data Terminal Ready:**

Controls the DTR output, pin 33, as described above.

FUNCTIONAL DESCRIPTION

**LINE STATUS REGISTER**

	+-----+	
D7	FFRX  -----	Error in FIFO RCVR (FIFO only)
	+-----+	
D6	TEMT  -----	Transmitter empty
	+-----+	
D5	THRE  -----	Transmitter holding register empty
	+-----+	
D4	BI  -----	Break interrupt
	+-----+	
D3	FE  -----	Framing error
	+-----+	
D2	PE  -----	Parity error
	+-----+	
D1	OE  -----	Overrun error
	+-----+	
D0	DR  -----	Data ready
	+-----+	

FFRX - FIFO Receiver Error:

Always logic 0 in character mode.

FIFO mode:

Indicates one or more parity errors, framing errors, or break indications in the receiver FIFO. FFRX is reset by reading the line status register.

TEMT - Transmitter Empty:

Indicates the transmitter holding register (or FIFO) and the transmitter shift register are empty and are ready to receive new data. TEMT is reset by writing a character to the transmitter holding register.

THRE - Transmitter Holding Register Empty:

Indicates the transmitter holding register (or FIFO) is empty and it is ready to accept new data. THRE is reset by writing data to the transmitter holding register (or FIFO).

**LINE STATUS REGISTER** (continued)

Bits BI, FE, PE, and OE are the sources of receiver line status interrupts. The bits are reset by reading the line status register. In FIFO mode, these bits are associated with a specific character in the FIFO and the exception is revealed only when that character reaches the top of the FIFO.

- BI - Break Interrupt:  
Indicates the receive data input has been in the spacing state (logic 0) for longer than one full word transmission time.
- FIFO mode:  
Only one zero character is loaded into the FIFO and transfers are disabled until SIN goes to the mark state (logic 1) and a valid start bit is received.
- FE - Framing Error:  
Indicates the received character had an invalid stop bit. The stop bit following the last data or parity bit was a 0 bit (spacing level).
- PE - Parity Error:  
Indicates that the received data does not have the correct parity.
- OE - Overrun Error:  
Indicates the receive buffer was not read before the next character was received and the character is destroyed.
- FIFO mode:  
Indicates the FIFO is full and another character has been shifted in. The character in the shift register is destroyed but is not transferred to the FIFO.
- DR - Data ready:  
Indicates data is present in the receive buffer or FIFO. DR is reset by reading the receive buffer register or receiver FIFO.

FUNCTIONAL DESCRIPTION

**MODEM STATUS REGISTER**

D7	DCD	-----	Data carrier detect
+-----+			
D6	RI	-----	Ring indicator
+-----+			
D5	DSR	-----	Data set ready
+-----+			
D4	CTS	-----	Clear to send
+-----+			
D3	DDCD	-----	Delta data carrier detect
+-----+			
D2	TERI	-----	Trailing edge ring indicator
+-----+			
D1	DDSR	-----	Delta data set ready
+-----+			
D0	DCTS	-----	Delta clear to send
+-----+			

DCD - Data Carrier Detect:  
Complement of the DCD input, pin 38.

RI - Ring Indicator:  
Complement of the RI input, pin 39.

DSR - Data Set Ready:  
Complement of the DSR input, pin 37.

CTS - Clear To Send:  
Complement of the CTS input, pin 36.

Bits DDCD, TERI, DDSR, and DCTS are the sources of MODEM status interrupts. These bits are reset when the MODEM status register is read.

DDCD - Delta Data Carrier Detect:  
Indicates the Data Carrier Detect input, pin 38, has changed state.

TERI - Trailing Edge Ring Indicator:  
Indicates the Ring Indicator input, pin 39, has changed from a low to a high state.

DDSR - Delta Data Set Ready:  
Indicates the Data Set Ready input, pin 37, has changed state.

DCTS - Delta Clear To Send:  
Indicates the Clear to Send input, pin 36, has changed state.



**SCRATCHPAD REGISTER**

This register is not used by the 16550. It may be used by the programmer for data storage.

**FIFO INTERRUPT MODE OPERATION**

1. The receive data interrupt is issued when the FIFO reaches the trigger level. The interrupt is cleared as soon as the FIFO falls below the trigger level.

**CAUTION:**

To maintain compatibility with earlier personal computer systems, the user defined output, OUT 2, is used as an external interrupt enable and must be set active for interrupts to be acknowledged. OUT 2 is accessed through the 16550's MODEM control register.

2. The interrupt identification register's receive data available indicator is set and cleared along with the receive data interrupt above.
3. The data ready indicator is set as soon as a character is transferred into the receiver FIFO and is cleared when the FIFO is empty.

**BAUD RATE SELECTION**

The 16550 ACE determines the baud rate of the serial output from a combination of the clock input frequency and the value written to the divisor latches. Standard PC, PC/XT, PC/AT, and PS/2 serial interfaces use an input clock of 1.8432 MHz. To increase versatility, the QS-1000 uses an 18.432 MHz clock and a frequency divider circuit to produce the standard clock frequency.

Jumper block J1 is used to set the input frequency to the 16550. It may be connected to divide the clock input by 1, 2, 5, or 10. To maintain compatibility with adapters using a 1.8432 MHz input, J1 should be configured to divide by 10 as shown in figure 7(d). A table of divisor latch values for various input frequencies is given in figure 8.

FUNCTIONAL DESCRIPTION

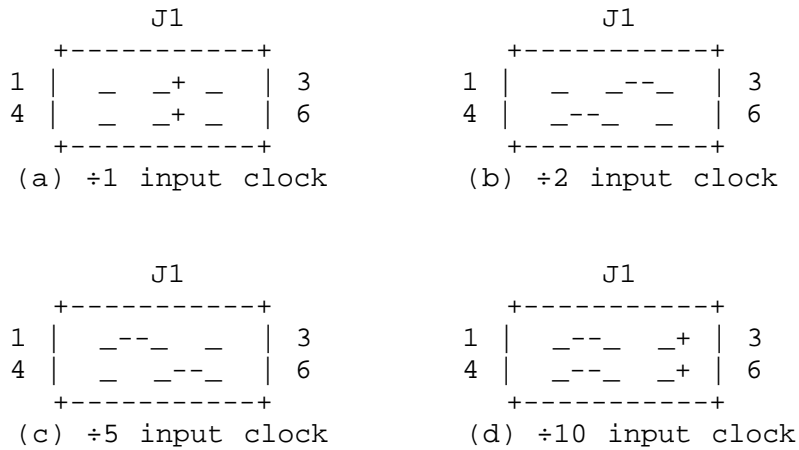


Figure 7. Input clock frequency options. For compatibility, the jumper should be set at ÷10 ( 18.432 MHz ÷ 10 = 1.8432 MHz ).

Baud Rate	Divisor latch value			
	÷10	÷5	÷2	÷1
110	1,047	2,094	5,236	10,473
300	384	768	1,920	3,840
600	192	384	960	1,920
1,200	96	192	480	960
2,400	48	96	240	480
3,600	32	64	160	320
4,800	24	48	120	240
9,600	12	24	60	120
19,200	6	12	30	60

Figure 8. Divisor latch settings for common baud rates using an 18.432 MHz input clock. For compatibility, connect jumper in the divide by 10 configuration (figure 7(d)).

**IV. ADDRESSING OPTIONS**

Each channel of the QS-1000 uses 8 consecutive I/O address locations beginning on an even 8 byte boundary (xxx0H - xxx7H) or (xxx8H - xxxFH). The 16550 uses these addresses as shown in figure 2.

Two addressing modes are available on the QS-1000: discrete addressing and block addressing. Each of these modes will be discussed separately.

Discrete Addressing Mode

In the discrete addressing mode, each port may choose an individual base address. This mode allows maximum compatibility with software supporting the pre-defined addresses for Serial 1 through Serial 8. Channels 1 and 2 may select from Serial 1 through Serial 7, Channels 3 and 4 may choose from Serial 2 through Serial 8. Each channel may be individually disabled.

Block Addressing Mode

In block addressing mode, the four serial channels are arranged to form a continuous 32-byte block of I/O addresses. This mode offers more compactness for custom software applications. The block may be placed anywhere in the available I/O address range on an even 32-byte boundary (e.g. 400H-41FH, 620-63FH, 980H-99FH) using the IBM installation utilities and the Qua Tech address installation utility QTINSTAL.EXE.

**WARNING:**

In block mode, each channel may be individually disabled, but the I/O space assigned to that channel is still considered in use and may not be used by another device.

Channel	Address range
1	Base+ 0 --> Base+ 7
2	Base+ 8 --> Base+15
3	Base+16 --> Base+23
4	Base+24 --> Base+31

Figure 9. Block mode address assignments.

## INTERRUPTS

### V. INTERRUPTS

The QS-1000 has support for three interrupt levels: IRQ 3, IRQ 4, and IRQ 9. During the installation process, one pair of interrupts must be selected, either IRQ 3 and IRQ 4, or IRQ 3 and IRQ 9. Each channel may then choose an interrupt from the active pair. If interrupts are being shared, the IP bit in the 16550's interrupt identification register or the interrupt pending bits in the interrupt status register should be used to test for the source of the interrupt.

#### **CAUTION:**

To maintain compatibility with earlier personal computer systems, the user defined output, OUT 2, is used as an external interrupt enable and must be set active for interrupts to be acknowledged. OUT 2 is accessed through the 16550's MODEM control register.

#### INTERRUPT STATUS REGISTER

```
+-----+
D7 | 0 |
+-----+
D6 | 0 |
+-----+
D5 | 0 |
+-----+
D4 | 0 |
+-----+
D3 | IP4 |----- Interrupt pending channel 4
+-----+
D2 | IP3 |----- Interrupt pending channel 3
+-----+
D1 | IP2 |----- Interrupt pending channel 2
+-----+
D0 | IP1 |----- Interrupt pending channel 1
+-----+
```

An interrupt status register has been implemented on the QS-1000 to ease software burden associated with the interrupt sharing process. An interrupt status bit will be set (logic 1) if there is an interrupt pending in the 16550 and the associated OUT 2 line (interrupt enable) is active.

## INTERRUPTS

When selected during the configuration process, the interrupt status register is accessed by reading any of the 16550 scratchpad registers. The interrupt status register is read only.

### **NOTE:**

When enabled, the interrupt status register will override the 16550's internal scratchpad register. Since the BIOS tests the scratchpad register during initialization, the channels may not appear in the system's equipment list. If the equipment list is updated through user software, the operating system should accept and use the channel.

## **VI. PROGRAMMABLE OPTION SELECT**

The IBM PS/2 family of computers using the Micro-Channel bus structure utilize on board registers referred to as the Programmable Option Select (POS) registers to hold the adapter's configuration information. The first two POS registers hold a unique adapter identification number that has been issued to Qua Tech for the QS-1000. This number is defined in hardware and can not be changed. These registers are read only.

The remaining POS registers are used for address and interrupt selections. Three additional POS registers are implemented on the QS-1000. These registers are programmed by the user through the IBM installation utility supplied with the PS/2 and the Qua Tech address installation software QTINSTALL.EXE. These registers are read/write but should not be written to by user software. The bit definitions of the registers are given in Figure 10.

PROGRAMMABLE OPTION SELECT

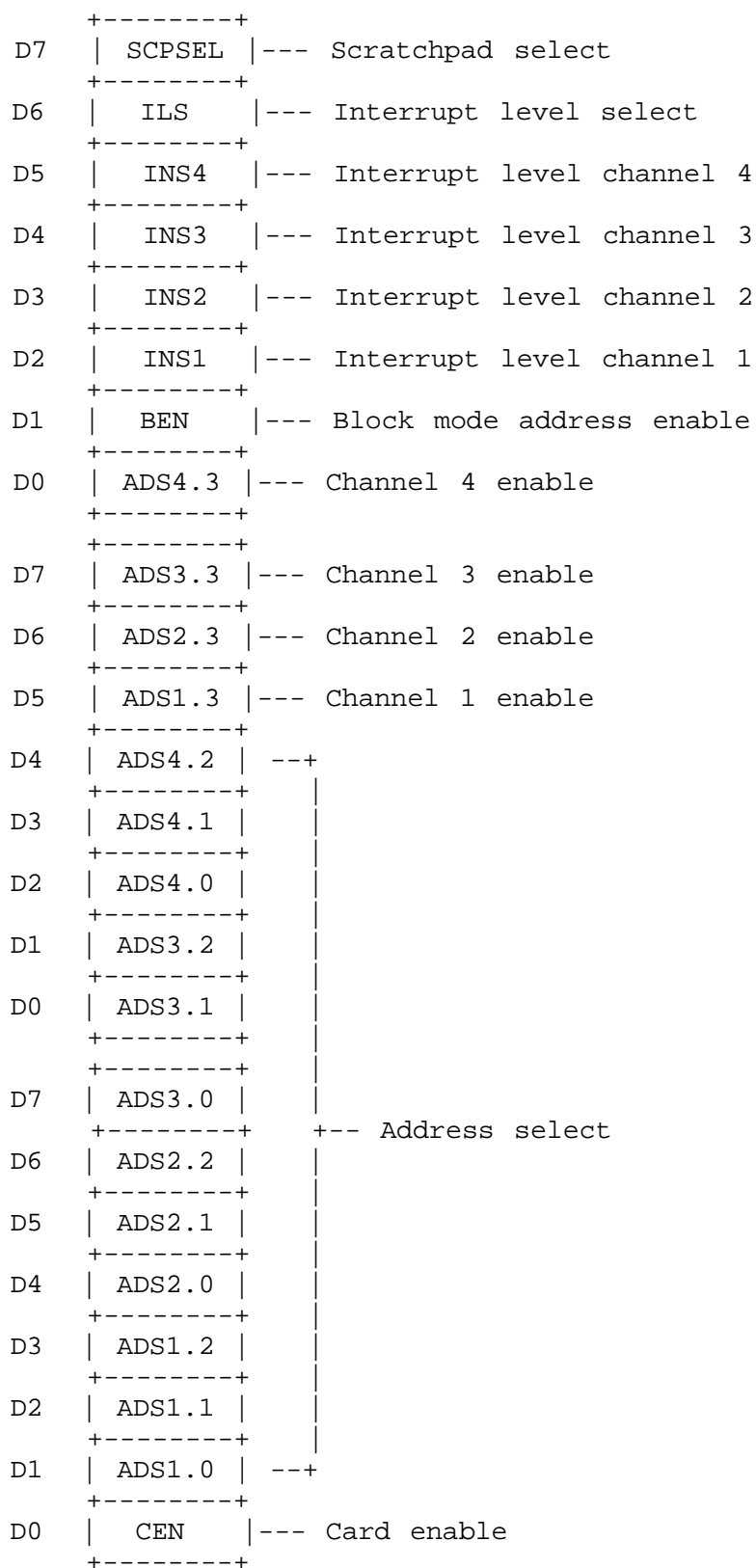


Figure 10. QS-1000 POS implementation.

PROGRAMMABLE OPTION SELECT

ADSx.3	ADSx.2	ADSx.1	ADSx.0	Base address
0	x	x	x	Disabled
1	0	0	0	03F8H (Serial 1)
1	0	0	1	02F8H (Serial 2)
1	0	1	0	3220H (Serial 3)
1	0	1	1	3228H (Serial 4)
1	1	0	0	4220H (Serial 5)
1	1	0	1	4228H (Serial 6)
1	1	1	0	5220H (Serial 7)
1	1	1	1	5228H (Serial 8)

Figure 11. QS-1000 discrete mode address options.

ILS	INSx	Interrupt
0	0	IRQ 3
0	1	IRQ 4
1	0	IRQ 3
1	1	IRQ 9

Figure 12. QS-1000 interrupt options.

The bits labeled ADSx.x in figure 10 contain the address decoding information for the QS-1000. In discrete addressing mode, these bits form a three bit code for each channel as defined in figure 11. In block addressing mode, bits ADS4.1 - ADS1.0 directly correspond to address lines A15 - A5. For example, if the QS-1000 is in block addressing mode with a base address of 5620H, the POS would appear as follows:

	5	6	2	0H	
	0101	0110	0010	0000B	
ADS4.2	-->	unused		ADS2.3	--> A10 = 1
ADS4.1	-->	A15 = 0		ADS2.2	--> A9 = 1
ADS4.0	-->	A14 = 1		ADS2.1	--> A8 = 0
ADS3.2	-->	A13 = 0		ADS2.0	--> A7 = 0
ADS3.1	-->	A12 = 1		ADS1.2	--> A6 = 0
ADS3.0	-->	A11 = 0		ADS1.1	--> A5 = 1

## PROGRAMMABLE OPTION SELECT

Once the addressing has been established, POS bits ADS1.3, ADS2.3, ADS3.3, and ADS4.3 are used to enable or disable channels 1 - 4 respectively. In discrete addressing mode, the addresses allocated for the disabled channel may be issued to another device. In block addressing mode, however, the addresses used by the disabled channel are still reserved for the QS-1000 and may not be allocated to another device.

A channel's interrupt level is determined by first selecting an interrupt pair for the QS-1000 using ILS and then selecting the channel interrupt using bits INS1 - INS4 for channels 1 - 4. The interrupt choices for each channel are shown in figure 12.

The final POS option is the Scratchpad/Interrupt status register selection. When SCPSEL is set to logic 0, the 16550 internal scratchpad registers are enabled for complete serial port compatibility. When set to logic 1, the scratchpad registers are overridden by the interrupt status register as described in section V.

### **NOTE:**

When enabled, the interrupt status register will override the 16550's internal scratchpad register. Since the BIOS tests the scratchpad register during initialization, the channels may not appear in the system's equipment list. If the equipment list is updated through user software, the operating system should accept and use the channel.



## CONNECTIONS

**VII. EXTERNAL CONNECTIONS**

The QS-1000 is available with two output configurations. The first option uses a female D-37 connector labeled CN1 on the circuit board. This configuration can provide all of the signals found on the standard 25-pin connector for each of the channels. The second option uses a quad 6-wire RJ-11 phone jack style connector labeled CN2 on the circuit board. This configuration provides only transmit and receive and one set of handshake signals (RTS/CTS or DTR/DSR). Both output configurations have optional adapter cables available to provide standard D-25 connectors for each channel. The various connectors and pinouts are given in the figures below.

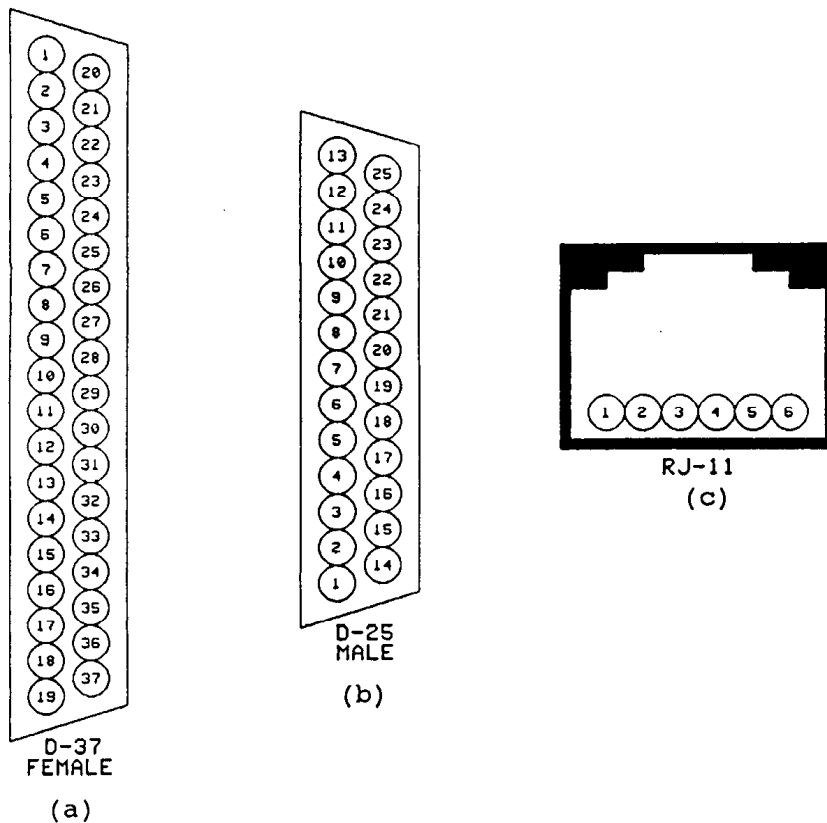


Figure 13. QS-1000 output connectors.

## EXTERNAL

## CONNECTIONS

SIGNAL	CHANNEL 1			CHANNEL 2		
	D-37	RJ-11	D-25	D-37	RJ-11	D-25
TxD	24	4	2	10	4	2
RxD	5	3	3	28	3	3
RTS	23	*	4	9	*	4
DTR	21	*	20	7	*	20
AUXOUT	--	6	--	--	6	--
CTS	4	**	5	27	**	5
DSR	22	**	6	8	**	6
AUXIN	--	2	--	--	2	--
DCD	2	--	8	25	--	8
RI	20	--	22	6	--	22
GND	3	1	7	26	1	7
SHIELD	##	5	##	##	5	##

SIGNAL	CHANNEL 3			CHANNEL 4		
	D-37	RJ-11	D-25	D-37	RJ-11	D-25
TxD	33	4	2	19	4	2
RxD	14	3	3	37	3	3
RTS	32	*	4	18	*	4
DTR	30	*	20	16	*	20
AUXOUT	--	6	--	--	6	--
CTS	13	**	5	36	**	5
DSR	31	**	6	17	**	6
AUXIN	--	2	--	--	2	--
DCD	11	-	8	34	-	8
RI	29	-	22	15	-	22
GND	12	1	7	35	1	7
SHIELD	##	5	##	##	5	##

\* When using RJ-11 connectors, only one output handshake (RTS or DTR) may be used. The selected signal is connected to AUXOUT using the handshake option jumpers.

\*\* When using RJ-11 connectors, only one input handshake (CTS or DSR) may be used. The selected signal is connected to AUXIN using the handshake option jumpers.

## D-37 and D-25 connectors have shielded housings.

Figure 14. Connector CN1 pin definitions. Pins not listed are not connected.

## CONNECTIONS

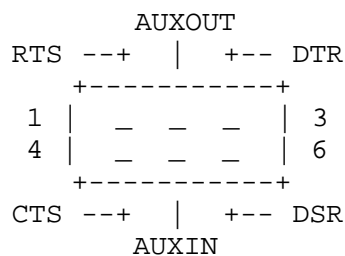


Figure 15. Handshake option jumper pinout.  
(RJ-11 output option only.)

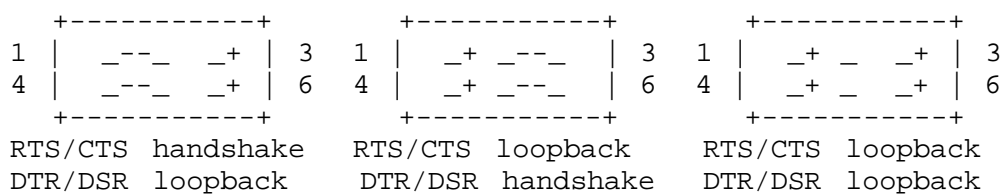


Figure 16. Handshake option configurations.  
(RJ-11 output option only.)

When using the RJ-11 style connectors, it may be necessary to loopback the unused handshake signals. Handshake signals RTS, CTS, DTR, and DSR are user configurable using jumpers J2 - J5 for channels 1 - 4 respectively. Loopback configurations are shown in figure 16.

The remaining handshake/status inputs, DCD and RI, are not connected in this output configuration and their values are therefore indeterminate.

## INSTALLATION

**VIII. HARDWARE INSTALLATION**

Make sure there is a copy of the original IBM PS/2 Model 50, 60, or 80 reference diskette available. This diskette must be modified to accept any option adapters.

1. Turn system on and allow to boot.
2. Insert the Qua Tech QS-1000 distribution disk into drive A and change the default drive to A.
3. Execute:  
    QS-1000 BLOCK           for block address mode  
    QS-1000 DISCRETE      for discrete address mode  
    See section IV for descriptions of addressing modes.
4. Turn unit off.
5. Remove system cover as instructed in the IBM Quick Reference Guide.
6. Insert adapter into any vacant slot following the guidelines for installing an optional adapter in the IBM Quick Reference Guide.
7. Replace system cover.
8. Turn unit on and insert a copy of the IBM PS/2 reference diskette into drive A.
9. Respond "N" at automatic configuration prompt.
10. Select "Copy an option diskette" and follow copying instructions.
11. Select "Set configuration"
12. Select "Change configuration" or "Run automatic configuration" and follow installation instructions.

NOTE: When installing the QS-1000 for block mode addressing, if the desired address is not available in the configuration routine, select any non-conflicting address and continue with Additional Block Mode Addressing (section X).

After the initial installation, the reference diskette will contain the configuration file for the QS-1000. Subsequent re-installation may omit step 10 and a "Y" response may be given during step 9 (automatically configure system) if desired.

## CHANGING

### ADDRESSING MODES

#### **IX. CHANGING ADDRESSING MODES**

Make sure there is a copy of the original IBM PS/2 Model 50, 60, or 80 reference diskette available. This diskette must be modified to accept any option adapters.

The QS-1000 may be addressed in discrete or block addressing modes as discussed in section IV. If the QS-1000 addressing mode is to be changed, the existing configuration must be purged from the configuration memory. The alternate addressing information may then be entered into configuration memory. The procedure is as follows:

1. Turn unit off.
2. Remove system cover as instructed in the IBM Quick Reference Guide.
3. Remove the QS-1000 from the system following the guidelines for removing an option adapter in the IBM Quick Reference Guide.
4. Turn unit on and insert a copy of the IBM PS/2 reference diskette into drive A.
5. Respond "Y" at automatic configuration prompt.
6. Exit the IBM installation procedure and restart the computer.

At this point the QS-1000 configuration has been purged from the configuration memory. The installation procedure (section VII of this document) may now be used to select the addressing mode and enter the new configuration information.

## PECIFICATIONS

### **X. ADDITIONAL BLOCK MODE ADDRESSES**

The QS-1000 block addressing mode supports the entire I/O address range of the PS/2 occupying 32 consecutive I/O locations. This produces 2K possible choices for base address location. Since it would not be feasible or practical to provide all of these choices in the configuration file, 25 addresses have been selected for inclusion in the file. An address installation utility (QTINSTALL.EXE) has been included on the distribution diskette to facilitate the address installation process. QTINSTALL should be used ONLY if the desired block mode base address cannot be found through the IBM installation utilities.

#### **WARNING:**

QTINSTALL must only be used when the QS-1000 has been installed and configured for BLOCK addressing mode. Executing QTINSTALL in discrete mode will cause unpredictable results and may destroy the contents of the adapter description file.

- . Insert the Qua Tech QS-1000 distribution disk in drive A.
  - . Execute QTINSTALL.
  - . Select the QS-1000 by using the cursor keys to highlight the selection and press <enter>. See Figure 17.
  - . At the prompt, insert the back-up copy of the IBM PS/2 reference in drive A.
  - . Select an address to change by using the cursor keys to highlight the address and press <enter>. (Addresses will appear in ascending order.) See Figure 18.
  - . Enter the desired address in hex, decimal, or binary. (hex is the default radix). See Figure 19.
  - . Repeat steps 5 and 6 as necessary.
  - . Press <esc> to exit the address menu.
  - . Press <enter> to save configuration changes. (A back-up copy of the configuration file will be generated.)
- OR -
- . Press <esc> to exit without saving changes.
  - . Press <esc> to exit the board selection menu.
  - . Press <esc> to return to DOS. The configuration file is modified but the system configuration is not updated.
- OR -
- . Press <enter> to enter the IBM installation utilities and update the system configuration.

PECIFICATIONS

**XI. SPECIFICATIONS**

Bus interface: IBM MicroChannel 16-bit bus  
 Controller: NS-16550-A  
 Interface: D-37 connector (female)  
           quad 6-wire RJ-11 (optional)  
 Transmit drivers: MAX234  
 Receive buffers: MC1489  
 I/O Address range  
   Discrete mode: Serial 1 - Serial 8  
   Block mode: 0000H - 0FFFFH  
 Interrupt levels: IRQ 3,4,9

Power requirements:

D-37 option		RJ-11 option		
IT	IMS	IT	IMS	Supply
1425mA	1618mA	1372mA	1566mA	+5 Volts
--	--	--	--	+12 Volts
--	--	--	--	-12 Volts

$I_T$  - Typical adapter current  
 $I_{MS}$  - Maximum statistical adapter current

PECIFICATIONS

```
=====+
                Qua Tech Address Installation Program
(C)1988 Qua Tech Incorporated                               Version 1.1
=====+
SLOT  ID #  TITLE                DESCRIPTION
-----+-----+-----+-----+
  1   5FE7  DS-2000             dual channel asynchronous RS-422 / 485 adapter
  3   5FE8  SP-1000            parallel printer port adapter
+-----+-----+-----+-----+
|  4   5FE0  QS-1000            four channel asynchronous RS-232 adapter
+-----+-----+-----+-----+
  5   5FE4  PXB-7200           72-bit parallel expansion adapter
  6   5FE1  MXI-1000           GPIB controller adapter

| Select      +- Edit selection      F1 help      Esc Exit
=====+
```

Figure 17. QTINSTAL.EXE opening menu. Outline indicates QS-1000 selected.



PECIFICATIONS

```
=====+
                Qua Tech Address Installation Program
Selection: QS-1000      four channel asynchronous RS-232 adapter
=====+

                CURRENTLY AVAILABLE BASE ADDRESSES

0100      02E0      0300      0320      0380
0420      0780      0800      0FC0      1000
1240      +-----+
           | 2680 |      3000      30A0      4040
           +-----+
0420      50E0      5540      6160      67A0
6F00      80C0      0A300     0C480     0E200

-- | Select      +- Edit selection      F1 help      Esc Exit
=====+
```

Figure 18. QTINSTAL.EXE address selection menu. Outline indicates address 2680H selected for change.

```

=====+
                Qua Tech Address Installation Program
Selection: QS-1000      four channel asynchronous RS-232 adapter
=====+

                CURRENTLY AVAILABLE BASE ADDRESSES

0100      02E0      0300      0320      0380
0420      0780
          +-----+
1240      | 2680 |      3000      30A0      4040
          +-----+
4220      50E0      5540      6160      67A0
6F00      80C0      0A300     0C480     0E200

Enter new base address: 500H

-- | Select      +- Edit selection      F1 help      Esc Exit
=====+

```

Figure 19. Address selection menu showing input prompt. Input indicates 500H being substituted for 2680H.

```
=====+
                Qua Tech Address Installation Program
Selection: QS-1000      four channel asynchronous RS-232 adapter
=====+

                CURRENTLY AVAILABLE BASE ADDRESSES

0100      02E0      0300      0320      0380
          +-----+
0420      | 0500 |      0780      0800      0FC0
          +-----+
1000      1240      3000      30A0      4040

4220      50E0      5540      6160      67A0

6F00      80C0      0A300     0C480     0E200

-- | Select      +- Edit selection      F1 help      Esc Exit
=====+
```

Figure 20. Address selection menu after modifications. Outline highlights the new selection.