Qua Tech Inc. warrants the **DS-1000** to be free of defects for **one (1) year** from the date of purchase. Qua Tech Inc. will repair or replace any board that fails to perform under normal operating conditions and in accordance with the procedures outlined in this document during the warranty period. Any damage that results from improper installation, operation, or general misuse voids all warranty rights.

Although every attempt has been made to guarantee the accuracy of this manual, Qua Tech Inc. assumes no liability for damages resulting from errors in this document. Qua Tech Inc. reserves the right to edit or append to this document at any time without notice.

Please complete the following information and retain for your records. Have this information available when requesting warranty service.

DATE OF PURCHASE:

MODEL NUMBER: **DS-1000**

PRODUCT DESCRIPTION: **DUAL CHANNEL RS-232 ASYNCHRONOUS COMMUNICATIONS BOARD**

SERIAL NUMBER:

FEDERAL COMMUNICATIONS COMMISSION STATEMENT

The Qua Tech DS-1000 is certified to comply with Class B limits, Part 15 of FCC Rules.

FCC ID: F4A4LUDS1000

This equipment generates and uses radio frequency energy and if not installed and used properly, that is, in strict accordance with the manufacturer's instructions, may cause interference to radio and television reception. It has been type tested and found to comply with the limits for a Class B computing device in accordance with the specifications in Subpart J of Part 15 of FCC Rules, which are designed to provide reasonable protection against such interference in a residential installation. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:

Reorient the receiving antenna.
Relocate the computer with respect to the receiver.
Move the computer away from the receiver.
Plug the computer into a different outlet so that the computer and receiver are on different branch circuits.

If necessary, the user should consult the dealer or an experienced radio / television technician for additional suggestions. The user may find the following booklet prepared by the Federal Communications Commission helpful:

"How to Identify and Resolve
Radio-TV Interference Problems"

This booklet is available from:

U.S. Government Printing Office
Washington, DC 20402
Stock No. 004-000-00345-4

TABLE OF CONTENTS

LIST OF FIGURES

I. INTRODUCTION

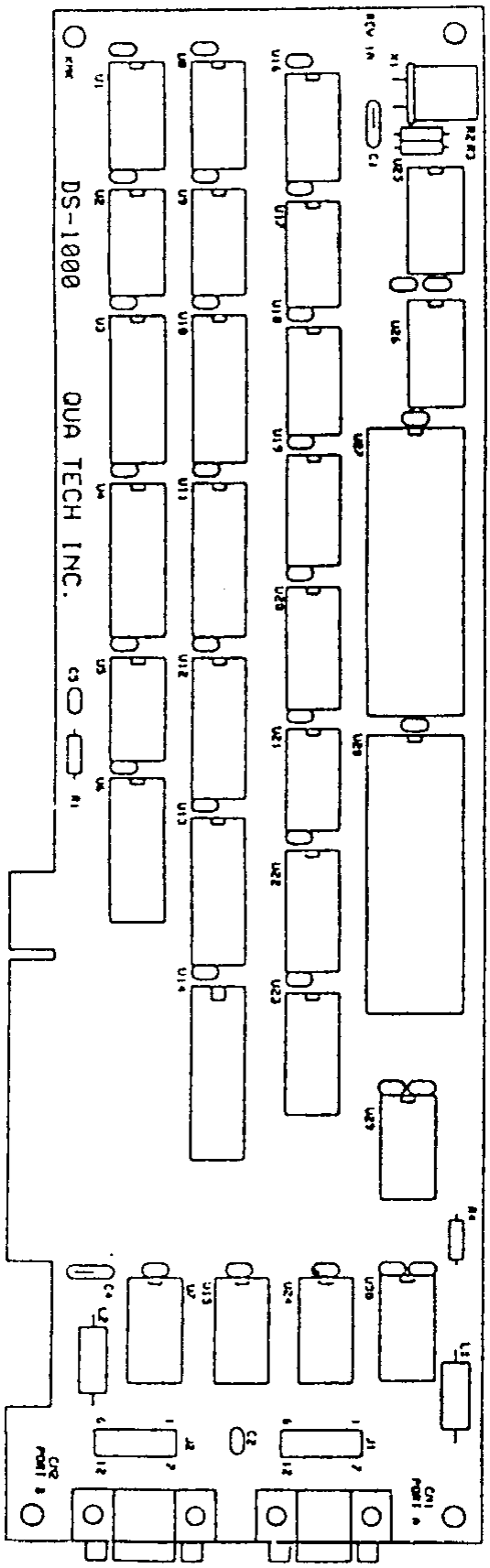
The DS-1000 is a dual channel RS-232C asynchronous serial communication adapter for the PS/2. The DS-1000 is designed to be used in the Serial 1 through Serial 8 address range as specified for the PS/2, although eight other addresses are available for applications requiring additional serial ports. The available interrupt selections (IRQ 3,4,7 and 9) can be used to reduce the number of interrupt sources on a single interrupt input. This feature can reduce software overhead in interrupt driven, high throughput applications.

The DS-1000 serial interface is accomplished through a pair of 16550 Asynchronous Communication Elements (ACEs). The 16550 is compatible with the 8250 and 16450 ACEs used in the IBM PC/XT/AT models. The 16550 also has an additional FIFO mode that reduces CPU overhead at higher data rates.

The DS-1000 address and interrupt selections are selected through the Programmable Option Select (POS) using the IBM installation utilities. In addition, jumpers are provided on the DS-1000 to configure the adapter as Data Terminal Equipment (DTE) or Data Communications Equipment (DCE). DTE/DCE selection can ease the cabling burden in local applications where MODEMS are not required.

II. BOARD DESCRIPTION

A component diagram of the DS-1000 showing the locations of the 16550 ACEs, DTE/DCE configuration jumpers, and D-9 connectors is shown in Figure 1. The first communication channel is controlled by the 16550 labeled U27, jumper J1, and is accessed through connector P1. The second channel uses the 16550 labeled U28, jumper J2, and is accessed through connector P2.


DS-1000
QUA TECH INC.

III. 16550 FUNCTIONAL DESCRIPTION

The 16550 is an upgrade of the standard 16450 Asynchronous Communications Element (ACE). Designed to be compatible with the 16450, the 16550 enters the character mode on reset and in this mode will appear as a 16450 to user software. An additional mode, FIFO mode, can be selected to reduce CPU overhead at high data rates. The FIFO mode increases performance by providing two internal 16-byte FIFOs (one transmit and one receive) to buffer data and reduce the number of interrupts issued to the CPU.

Other features include:

Programmable baud rate, character length, parity, and number of stop bits

Automatic addition and removal of start, stop, and parity bits

Independent and prioritized transmit, receive and status interrupts

Transmitter clock output to drive receiver logic

The following pages provide a brief summary of the internal registers available within the 16550 ACE. The registers are addressed as shown in Figure 2 below.

DLAB	A2	A1	A0	REGISTER DESCRIPTION
0	0	0	0	Receive buffer (read only)
				Transmit holding register (write only)
0	0	0	1	Interrupt enable
x	0	1	0	Interrupt identification (read only)
				FIFO control (write only)
x	0	1	1	Line control
x	1	0	0	MODEM control
x	1	0	1	Line status
x	1	1	0	MODEM status
x	1	1	1	Scratch
1	0	0	0	Divisor latch (least significant byte)
1	0	0	1	Divisor latch (most significant byte)

Figure 2. Internal register map for 16550 ACE. DLAB is accessed through the Line Control Register.

IIIA. INTERRUPT ENABLE REGISTER

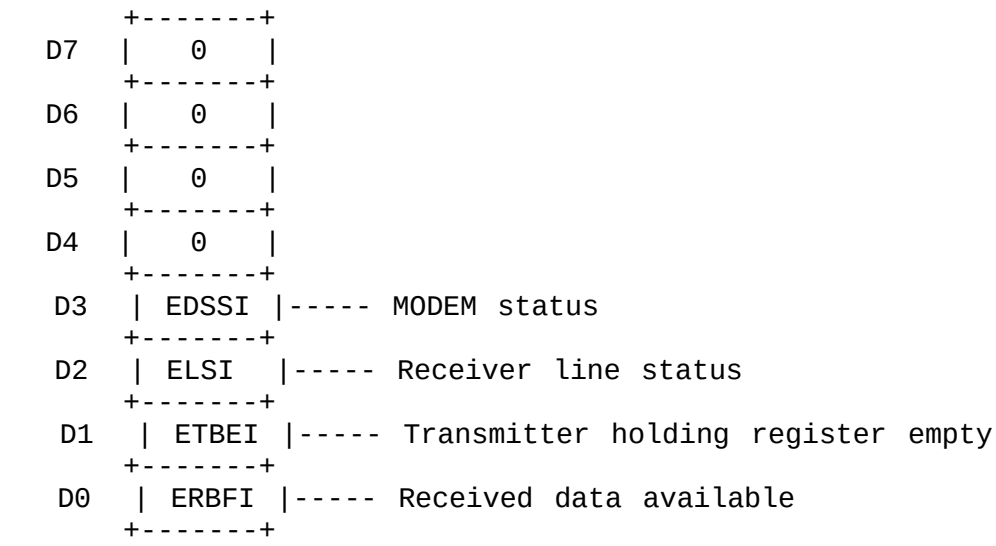


Figure 3. Interrupt enable register bit definitions.

EDSSI - MODEM Status Interrupt:
When set (logic 1), enables interrupt on clear to send, data set ready, ring indicator, and data carrier detect.

ELSI - Receiver Line Status Interrupt:
When set (logic 1), enables interrupt on overrun, parity, and framing errors, and break indication.

ETBEI - Transmitter Holding Register Empty Interrupt:
When set (logic 1), enables interrupt on transmitter register empty.

ERBFI - Received Data Available Interrupt:
When set (logic 1), enables interrupt on received data available or FIFO trigger level.

IIIB. INTERRUPT IDENTIFICATION REGISTER

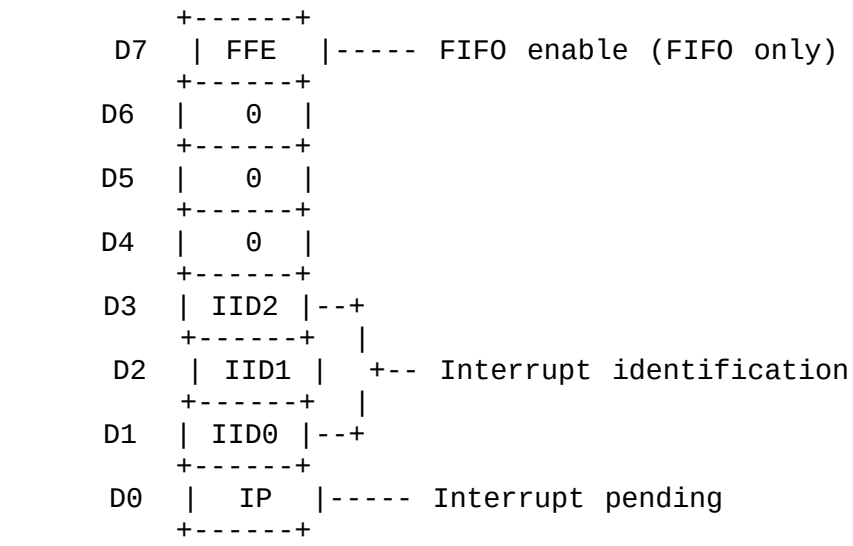


Figure 4. Interrupt identification register bit definitions.

FFE - FIFO Enable:
When logic 1, indicates FIFO mode enabled.

IIDx - Interrupt Identification:
Indicates highest priority interrupt pending if any. See IP and Figure 5. NOTE: IID2 is always a logic 0 in character mode.

IP - Interrupt Pending:
When logic 0, indicates that an interrupt is pending and the contents of the interrupt identification register may be used to determine the interrupt source. See IIDx and Figure 5.

IID2	IID1	IID0	IP	Priority	Interrupt Type
x	x	x	1	N/A	None
0	1	1	0	Highest	Receiver Line Status
0	1	0	0	Second	Received Data Ready
1	1	0	0	Second	Character Timeout (FIFO only)
0	0	1	0	Third	Transmitter Holding Register Empty
0	0	0	0	Fourth	MODEM Status

Figure 5. Interrupt identification bit definitions.

Receiver Line Status:
Indicates overrun, parity, or framing errors or break interrupts. The interrupt is cleared by reading the line status register.

Received Data Ready:
Indicates receiver data available. The interrupt is cleared by reading the receiver buffer register

FIFO mode:
Indicates the receiver FIFO trigger level has been reached. The interrupt is reset when the FIFO drops below the the trigger level.

Character Timeout: (FIFO mode only)
Indicates no characters have been removed from or input to the receiver FIFO for the last four character times and there is at least one character in the FIFO during this time. The interrupt is cleared by reading the receiver FIFO.

Transmitter Holding Register Empty:
Indicates the transmitter holding register is empty. The interrupt is cleared by reading the interrupt identification register or writing to the transmitter holding register.

MODEM Status:
Indicates clear to send, data set ready, ring indicator, or data carrier detect have changed state. The interrupt is cleared by reading the MODEM status register.

IIIC. FIFO CONTROL REGISTER

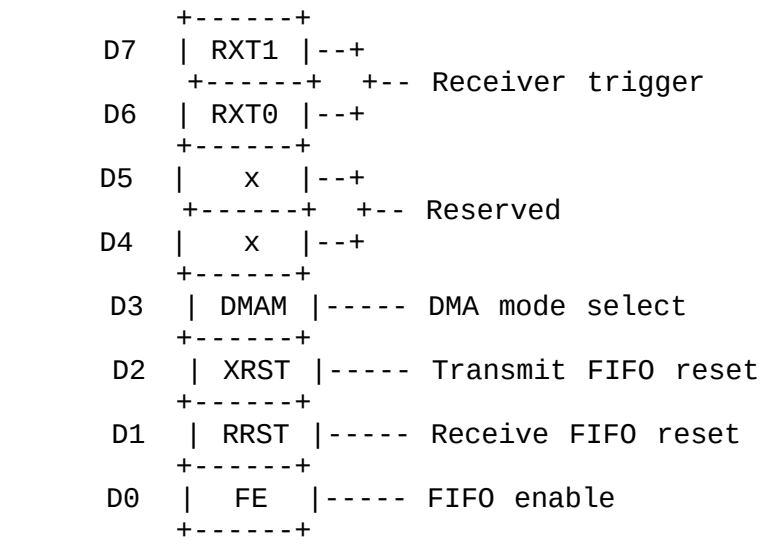


Figure 6. FIFO control register bit definitions.

RXTx - Receiver FIFO Trigger Level:
Determines the trigger level for the FIFO interrupt as given in Figure 7 below.

RXT1	RXT0	RCVR FIFO Trigger level (bytes)
0	0	1
0	1	4
1	0	8
1	1	14

Figure 7. FIFO trigger levels.

DMAM - DMA Mode Select:
When set (logic 1), RxRDY and TxRDY change from mode 0 to mode 1. (DMA mode not supported on DS-1000)

XRST - Transmit FIFO Reset:
When set (logic 1), all bytes in the transmitter FIFO are cleared and the counter is reset. The shift register is not cleared. XRST is self-clearing.

RRST - Receive FIFO Reset:
When set (logic 1), all bytes in the receiver FIFO are cleared and the counter is reset. The shift register is not cleared. RRST is self-clearing.

FE - FIFO Enable:
When set (logic 1), enables transmitter and receiver FIFOs. When cleared (logic 0), all bytes in both FIFOs are cleared. This bit must be set when other bits in the FIFO control register are written to or the bits will be ignored.

IIID. LINE CONTROL REGISTER

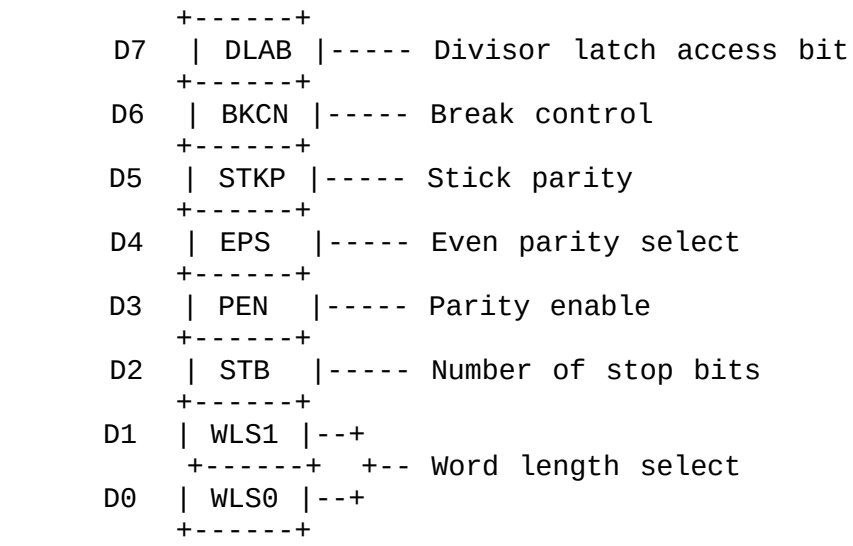


Figure 8. Line Control Register bit definitions.

DLAB - Divisor Latch Access Bit:
DLAB must be set to logic 1 to access the baud rate divisor latches. DLAB must be set to logic 0 to access the receiver buffer, transmitting holding register and interrupt enable register.

BKCN - Break Control:
When set (logic 1), the serial output (SOUT) is forced to the spacing state (logic 0).

STKP - Stick Parity:
Forces parity to logic 1 or logic 0 if parity is enabled. See EPS, PEN, and Figure 9.

EPS - Even Parity Select:
Selects even or odd parity if parity is enabled. See STKP, PEN, and Figure 9.

PEN - Parity Enable:
Enables parity on transmission and verification on reception. See EPS, STPK, and Figure 9.

STKP	EPS	PEN	Parity
x	x	0	None
0	0	1	Odd
0	1	1	Even
1	0	1	Logic 1
1	1	1	Logic 0

Figure 9. 16550 parity selections.

STB - Number of Stop Bits:
Sets the number of stop bits transmitted. See WLSx and Figure 10.

WLSx - Word Length Select:
Determines the number of bits per transmitted word. See STB and Figure 10.

STB	WLS1	WLS0	Word length	Stop bits
0	0	0	5 bits	1
0	0	1	6 bits	1
0	1	0	7 bits	1
0	1	1	8 bits	1
1	0	0	5 bits	1½
1	0	1	6 bits	2
1	1	0	7 bits	2
1	1	1	8 bits	2

Figure 10. Word length and stop bit selections.

IIIE. MODEM CONTROL REGISTER

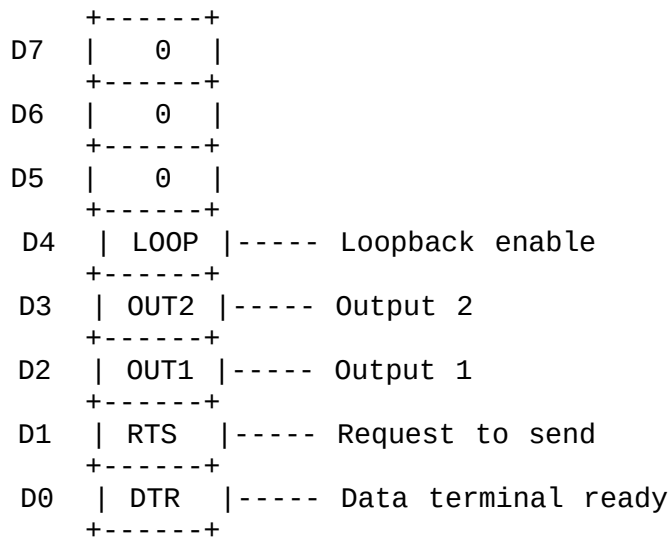


Figure 11. MODEM control register bit definitions.

LOOP - Loopback Enable:
When set (logic 1), the transmitter shift register is connected directly to the receiver shift register. The MODEM control inputs are internally connected to the MODEM control outputs and the outputs are forced to the inactive state. Therefore all characters transmitted are immediately received to verify transmit and receive data paths. Transmitter and receiver interrupts still operate normally. MODEM control interrupts are available but are now controlled through the MODEM control register.

Bits OUT2, OUT1, RTS, and DTR perform identical functions on their respective outputs. When these bits are set (logic 1) in the register, the associated output is forced to a logic 0. When cleared (logic 0), the output is forced to a logic 1.

OUT2 - Output 2:
Controls the OUT2 output, pin 31, as described above. Used for interrupt enable. See section VII.

OUT1 - Output 1:
Controls the OUT1 output, pin 34, as described above. Unused on DS-1000.

RTS - Request To Send:
Controls the RTS output, pin 32, as described above.

DTR - Data Terminal Ready:
Controls the DTR output, pin 33, as described above.

IIIF. LINE STATUS REGISTER

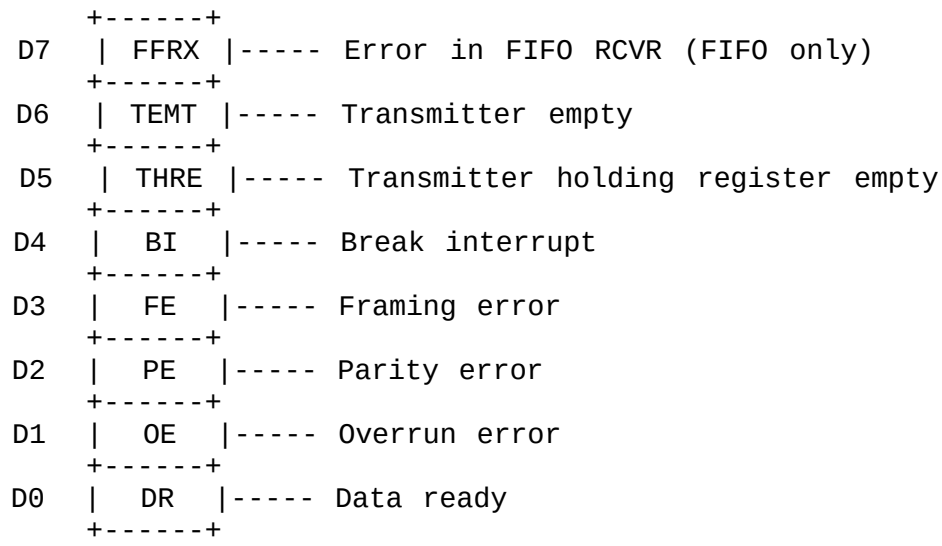


Figure 12. Line status register bit definitions.

FFRX - FIFO Receiver Error:
Always logic 0 in character mode.
FIFO mode:
Indicates one or more parity errors, framing errors, or break indications in the receiver FIFO. FFRX is reset by reading the line status register.

TEMT - Transmitter Empty:
Indicates the transmitter holding register (or FIFO) and the transmitter shift register are empty and are ready to receive new data. TEMT is reset by writing a character to the transmitter holding register.

THRE - Transmitter Holding Register Empty:
Indicates the transmitter holding register (or FIFO) is empty and it is ready to accept new data. THRE is reset by writing data to the transmitter holding register (or FIFO).

IIIF. LINE STATUS REGISTER (continued)

Bits BI, FE, PE, and OE are the sources of receiver line status interrupts. The bits are reset by reading the line status register. In FIFO mode, these bits are associated with a specific character in the FIFO and the exception is revealed only when that character reaches the top of the FIFO.

BI - Break Interrupt:
Indicates the receive data input has been in the spacing state (logic 0) for longer than one full word transmission time.

FIFO mode:
Only one zero character is loaded into the FIFO and transfers are disabled until SIN goes to the mark state (logic 1) and a valid start bit is received.

FE - Framing Error:
Indicates the received character had an invalid stop bit. The stop bit following the last data or parity bit was a 0 bit (spacing level).

PE - Parity Error:
Indicates that the received data does not have the correct parity.

OE - Overrun Error:
Indicates the receive buffer was not read before the next character was received and the character is destroyed.

FIFO mode:
Indicates the FIFO is full and another character has been shifted in. The character in the shift register is destroyed but is not transferred to the FIFO.

DR - Data ready:
Indicates data is present in the receive buffer or FIFO. DR is reset by reading the receive buffer register or receiver FIFO.

IIIG. MODEM STATUS REGISTER

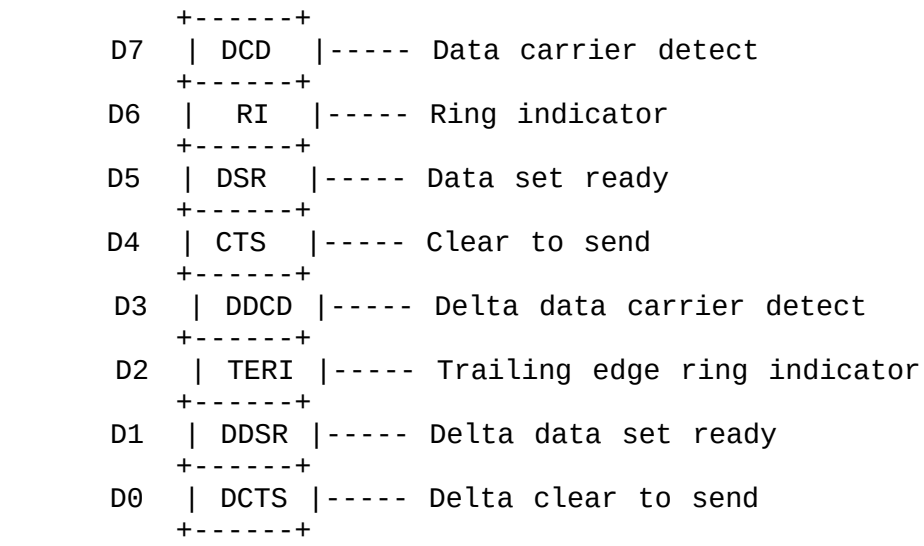


Figure 13. MODEM status register bit definitions.

DCD - Data Carrier Detect:
Complement of the DCD input, pin 38.

RI - Ring Indicator:
Complement of the RI input, pin 39.

DSR - Data Set Ready:
Complement of the DSR input, pin 37.

CTS - Clear To Send:
Complement of the CTS input, pin 36.

Bits DDCD, TERI, DDSR, and DCTS are the sources of MODEM status interrupts. These bits are reset when the MODEM status register is read.

DDCD - Delta Data Carrier Detect:
Indicates the Data Carrier Detect input, pin 38, has changed state.

TERI - Trailing Edge Ring Indicator:
Indicates the Ring Indicator input, pin 39, has changed from a low to a high state.

DDSR - Delta Data Set Ready:
Indicates the Data Set Ready input, pin 37, has changed state.

DCTS - Delta Clear To Send:
Indicates the Clear to Send input, pin 36, has changed state.

III H. SCRATCHPAD REGISTER

This register is not used by the 16550. It may be used by the programmer for data storage.

IV. FIFO INTERRUPT MODE OPERATION

1. The receive data interrupt is issued when the FIFO reaches the trigger level. The interrupt is cleared as soon as the FIFO falls below the trigger level.

2. The interrupt identification register's receive data available indicator is set and cleared along with the receive data interrupt above.

3. The data ready indicator is set as soon as a character is transferred into the receiver FIFO and is cleared when the FIFO is empty.

V. DIVISOR LATCH VALUES

Desired Baud Rate	Divisor Latch Value	Error Between Desired and Actual Value (%)
50	2304	-
75	1536	-
110	1047	0.026
150	768	-
300	384	-
600	192	-
1200	96	-
1800	64	-
2000	58	0.69
2400	48	-
3600	32	-
4800	24	-
7200	16	-
9600	12	-
19200	6	-
38400	3	-
56000	2	2.86

Figure 14. Divisor latch settings for common baud rates using a 1.8432 Mhz crystal.

VI. ADDRESSING

Each channel of the DS-1000 uses 8 consecutive I/O address locations. The base addresses are independent but must begin on an even 8-byte boundary (xxx0H - xxx7H or xxx8H - xxxFH). The numbers xxx are controlled by the Programmable Option Select (POS) and address decoders to provide complete 16-bit addressing for each channel. Sixteen choices of base address are provided for each channel and include the eight addresses defined as SERIAL 1 through SERIAL 8. The remaining eight addresses are a constant 8000H offset from these values. A complete table of available addresses is given in Figure 16. The 16550 utilizes its eight assigned addresses as shown in Figure 2.

VII. INTERRUPTS

The DS-1000 is capable of supporting four interrupt levels, IRQ 3,4,7 and 9. Each channel may select a separate interrupt or one may be shared by both channels. If interrupt sharing is used, the interrupt pending (IP) bit in the interrupt identification register should be used to test for the source of the interrupt.

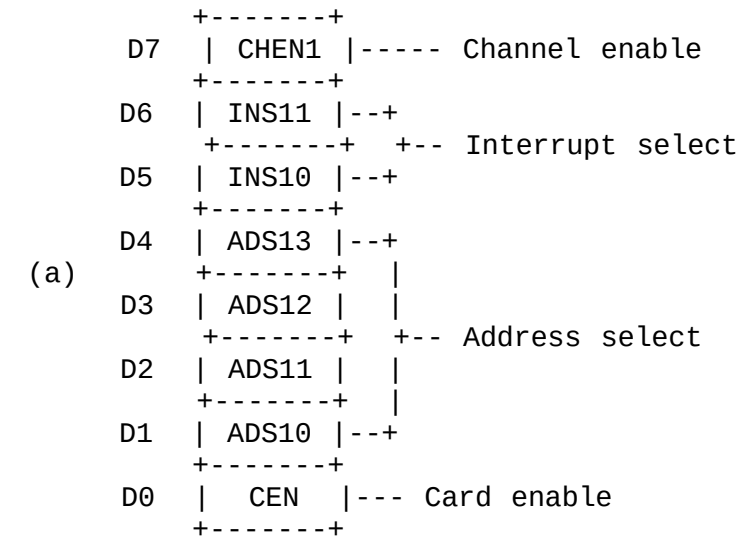
CAUTION:

To maintain compatibility with earlier personal computer systems, the user defined output, OUT 2, is used as an external interrupt enable and must be set active for interrupts to be acknowledged. OUT 2 is accessed through the 16550's MODEM control register.

VIII. PROGRAMMABLE OPTION SELECT

The IBM PS/2 family of computers using the MicroChannel bus structure utilize on board registers referred to as the Programmable Option Select (POS) registers to hold the adapter's configuration information. The first two POS registers hold a unique adapter identification number that has been issued to Qua Tech for the DS-1000. This number is defined in hardware and can not be changed. These registers are read only.

The remaining POS registers are used for address and interrupt selections. These registers are programmed by the user through the IBM installation utility supplied with the PS/2. These registers are read/write but should not be written to by user software. The bit definitions of these registers are given in Figures 15(a) and 15(b).



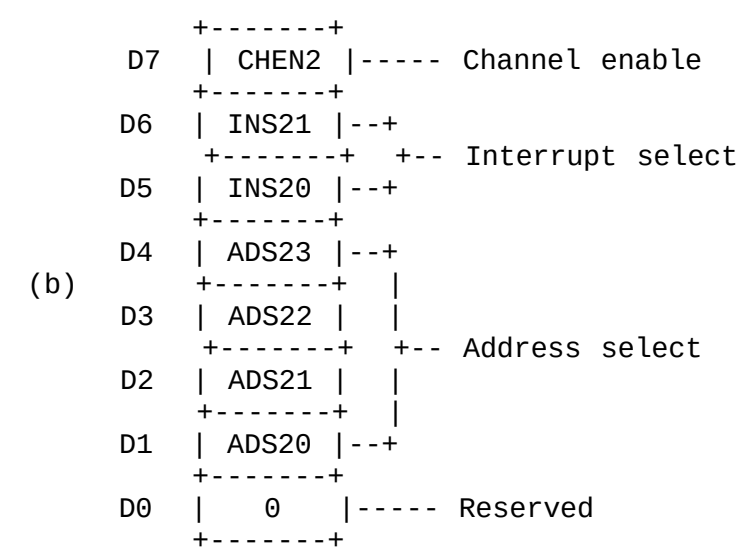


Figure 15. DS-1000 POS implementation.
(a) POS location 102H
(b) POS location 103H

ADSx3	ADSx2	ADSx1	ADSx0	Base address
0	0	0	0	3F8H (Serial 1)
0	0	0	1	2F8H (Serial 2)
0	0	1	0	3220H (Serial 3)
0	0	1	1	3228H (Serial 4)
0	1	0	0	4220H (Serial 5)
0	1	0	1	4228H (Serial 6)
0	1	1	0	5220H (Serial 7)
0	1	1	1	5228H (Serial 8)
1	0	0	0	83F8H
1	0	0	1	82F8H
1	0	1	0	B220H
1	0	1	1	B228H
1	1	0	0	C220H
1	1	0	1	C228H
1	1	1	0	D220H
1	1	1	1	D228H

Figure 16. Available base addresses.

INSx1	INSx0	IRQ
0	0	3
0	1	4
1	0	7
1	1	9

Figure 17. Available interrupt levels.

IX. OUTPUT CONFIGURATIONS

RS-232-C devices are classified by their function as either Data Terminal Equipment (DTE) or Data Communication Equipment (DCE). Generally, data terminal equipment is defined as the communication source while data communication equipment is defined as devices that provide a communication channel between two DTE type devices.

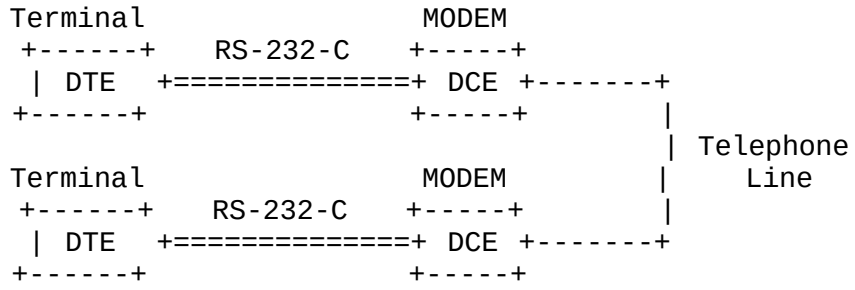


Figure 18. Use of Data Terminal Equipment (DTE) and Data Communication Equipment (DCE) to implement an RS-232-C communication link.

Data terminal equipment and data communication equipment have complementary pinouts to allow terminals and MODEMs to be connected directly using a one-to-one cable as shown in figure 21(a). In many applications, DCEs are unnecessary because of the short distances involved. In these cases, a custom cable called a null MODEM or MODEM eliminator is usually required to perform the direct connection of two DTEs. A typical null MODEM cable is shown in figure 21(b). To further simplify these connections, the DS-1000 is equipped with a DTE/DCE jumper configuration block for each channel. This allows the DS-1000 to communicate with DCE or DTE devices without any special cabling.

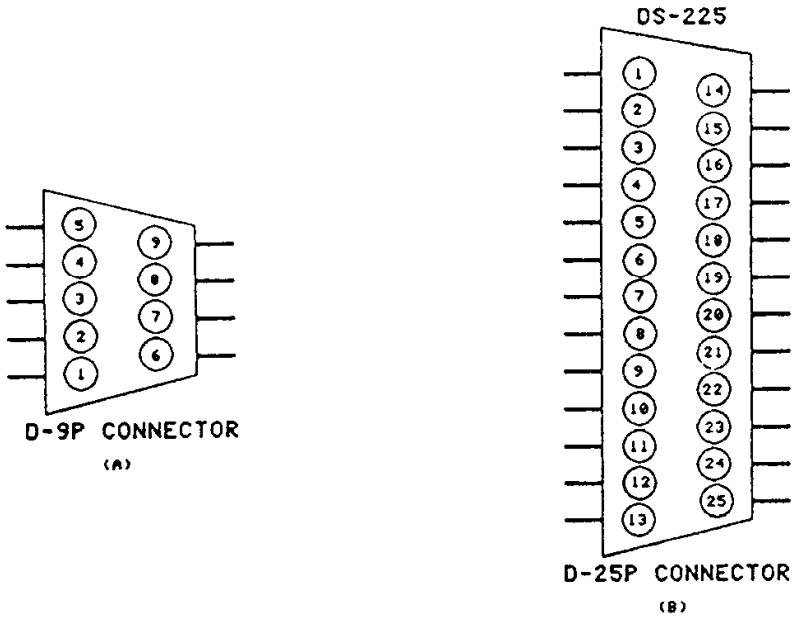
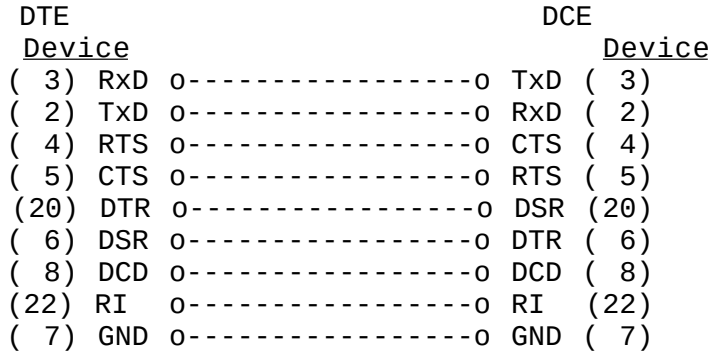


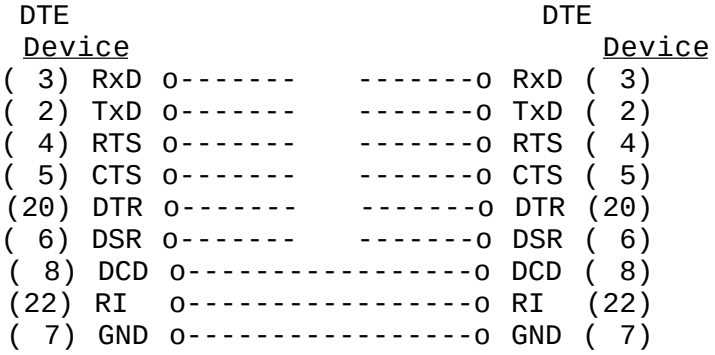
Figure 19. Output connectors.
(a) D-9 connector.
(b) D-25 connector. (adapter cable output)

RS-232-C Description	DTE Connection		DCE Connection	
	D-9	D-25	D-9	D-25
Data Carrier Detect (DCD)	1	8	1	8
Receive Data (RxD)	2	3	3	2
Transmit Data (TxD)	3	2	2	3
Data Terminal Ready (DTR)	4	20	6	6
Signal Ground	5	7	5	7
Data Set Ready (DSR)	6	6	4	20
Request To Send (RTS)	7	4	8	5
Clear To Send (CTS)	8	5	7	4
Ring Indicator (RI)	9	22	9	22

Figure 20. Connector definitions for RS-232-C.

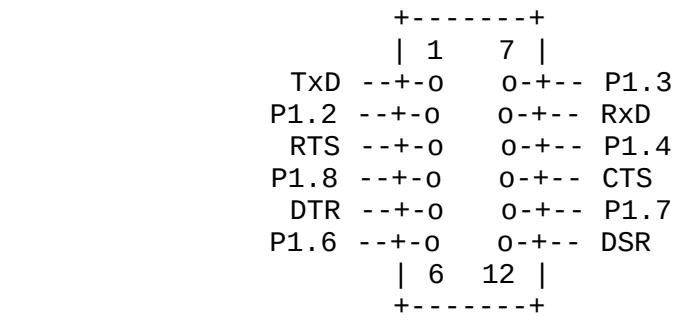


(a) Typical DTE to DCE cable.

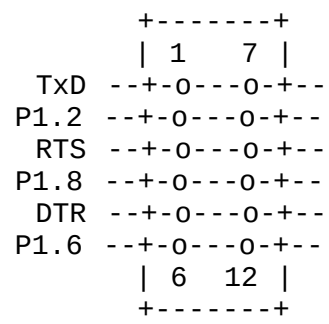


(b) Typical DTE to DTE (null MODEM) cable.

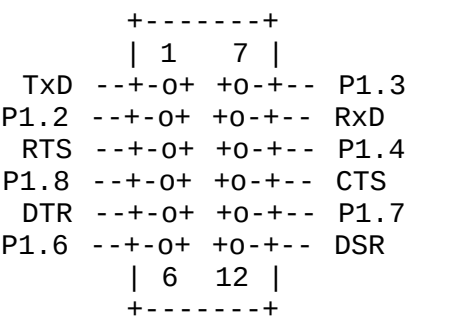
Figure 21. Cabling requirements for RS-232 devices.



(a) DTE/DCE configuration jumper.



(b) Jumper connections for DTE configuration.



(c) Jumper connections for DCE configuration.

Figure 22. DS-1000 output configuration jumpers. Shown are jumpers for port 1. NOTE: Connections are referenced by port and pin number. e.g. P1.3 _ port 1 pin 3, P1.6 _ port 1 pin 6.

X. INSTALLATION

Make sure there is a copy of the original reference diskette available. This diskette must be modified to accept any option adapters.

1. Turn unit off.
2. Remove system cover as instructed in the IBM Quick Reference Guide.
3. Insert adapter into any vacant slot following the guidelines for installing an optional adapter in the IBM Quick Reference Guide.
4. Replace system cover.
5. Turn unit on and insert copy of reference diskette into drive A.
6. Respond "N" to automatic configuration.
7. Select "Copy an option diskette" and follow copying instructions.
8. Select "Set configuration"
9. Select "Change configuration" or "Run automatic configuration" and follow installation instructions.

After the initial installation, the reference diskette will contain the configuration file for the DS-1000. Subsequent re-installation or address changes may omit step 7 and a "Y" response may be given in step 6 (automatically configure system) if desired.

XI. SPECIFICATIONS

Bus interface:	IBM MicroChannel 16-bit bus
Controllers:	2 - 16550 Asynchronous Communication Elements (ACEs)
RS-232 interface:	2 - D-9 connectors (male)
optional:	2 - D-25 connectors (male) available using adapter cables provided
Transmit drivers:	MC1488 or compatible
Receive buffers:	MC1489 or compatible
I/O Address range:	See Figure 16
Interrupt levels:	IRQ 3,4,7,9

Power requirements:

I_T	I_{MS}	Supply
500mA	575mA	+5 Volts
38mA	46mA	+12 Volts
36mA	43mA	-12 Volts

I_T - Typical adapter current

I_{MS} - Maximum statistical adapter current