EtherLink®/MC 32
Technical Reference Guide

A member of the EtherLink product family

For 3Com User Group Information
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Introduction

The EtherLink®/MC 32 adapter is a high performance, intelligent Ethernet adapter designed to operate in an IBM® Micro Channel® compatible computer. The adapter features:

- 16K bytes (on-board) static RAM
- 12.5 MHz Intel®/ 80186, 16-bit microprocessor
- Intel 82586 Local Area Network coprocessor
- High performance (on-board) DMA controller
- 32-bit Bus Master interface
- 32-bit/16-bit self-sensing interface
- Memory mapped mode of operation
- 3Com thin Ethernet transceiver circuit
- Two 27C128 EPROMs
- 15-pin AUI external connector

Architecture Overview

The Etherlink/MC 32 adapter fully complies with the Micro Channel Programmable Option Select (POS) protocol. Figure 1 illustrates the major sections of the adapter.

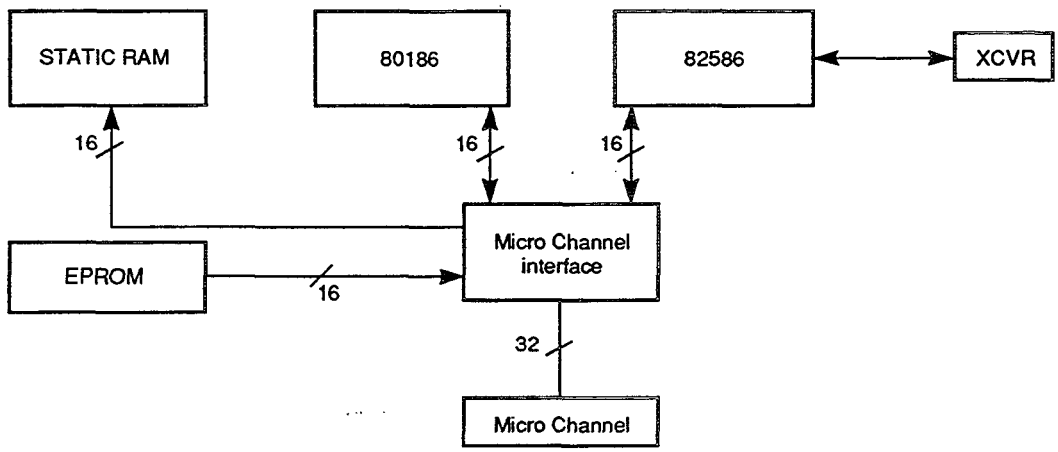

Figure 1. Etherlink/MC 32 Adapter Functional Diagram

Chapter 1
EtherLink/MC 32 Adapter Hardware Interface

The hardware interface of the EtherLink/MC 32 adapter is comprised of the programmable option select (POS) registers, the host I/O registers, the shared memory interface and the Micro Channel bus master interface. The POS registers provide the registers for the set-up utility of the Micro Channel architecture. The host I/O registers provide configuration and control information for the host software interface.

The shared memory interface allows the host to manipulate linked-list data structures on the adapter that are subsequently executed by the adapter's 80186 processor.

Finally, a high-performance bus-master interface is made available to the adapter's 80186 processor to accommodate the high volumes of data traffic between the host and the adapter. The Micro Channel does not have direct control of the DMA controller on the adapter which controls the bus master operation but the bus master may transfer data to and from memory anywhere in the 2G byte address range supported by the Micro Channel architecture.

POS Registers

This section describes the Programmable Option Select (POS) Register. The EtherLink/MC 32 adapter complies fully with the Micro Channel POS protocol. The adapter is configured by the host's power-on self test (POST) routine. Adapter features can be modified, enabled or disabled via the "Set Configuration Utility." When the adapter identification code is read (POS registers XXX0 and XXX1), the adapter will respond with 0041H. Refer to Figure 1-1.

Bit Map	Name	POS register
7 - 0	Adapter ID LSB	XXX0
7 - 0	Adapter ID MSB	XXX1
0	+CDEN	XXX2
3 - 1	+IOBASE (2:0)	XXX2
6 - 4	+MBASE (2:0)	XXX2
7	reserved	XXX2
3 - 0	+ARBLVL (3:0)	XXX3
4	+FAIR	XXX3
7 - 5	reserved	XXX3
0	+WDOEN	XXX4
1	+BNC	XXX4
5 - 2	reserved	XXX4
6	reserved	XXX4
7	reserved	XXX4
1 - 0	ABM	XXX5
3 - 2	+INT (1:0)	XXX5
5 - 3	+WDOSIZE (1:0)	XXX5
6	1	XXX5
7	1	XXX5
7 - 0	Subaddressing LSB	XXX6
7 - 0	Subaddressing MSB	XXX7

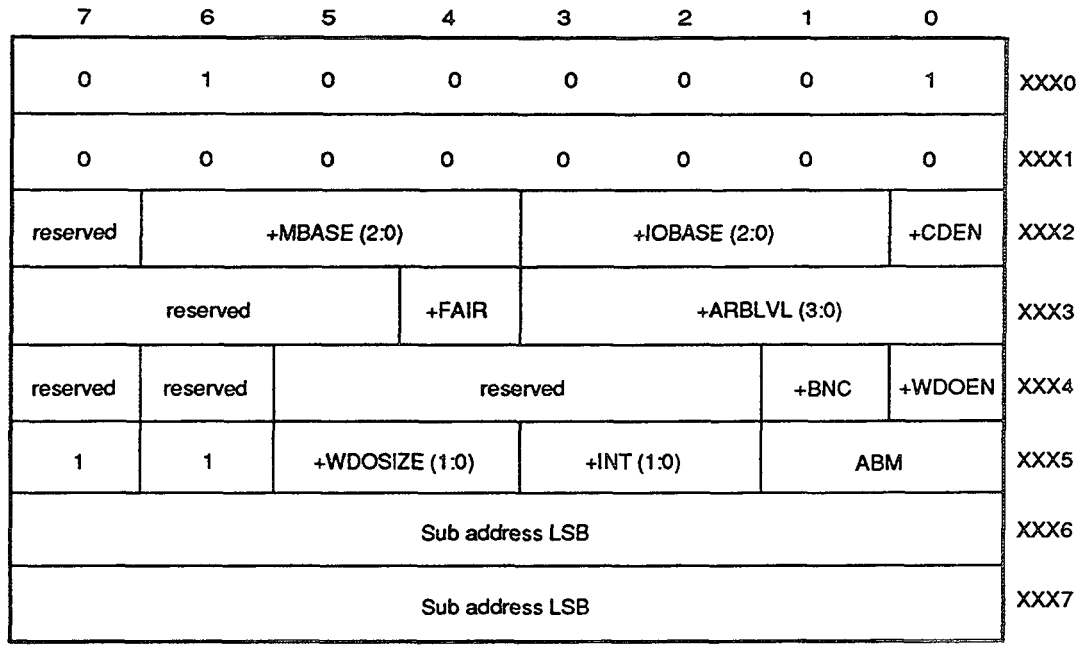

Figure 1-1. POS Register Bit Map Definition

Card Enable

POS register XXX2, bit 0 is used as a card enable bit. On power-up, this bit will be zero and the adapter will be disabled—responding only to the POS setup cycle.

+CDEN	Card Enable
0	Adapter disabled (power-up default)
1	Adapter enabled (POS default)

I/O Base Address

POS register XXX2, bits 1, 2 and 3 correspond to the Micro Channel address bits 4, 10 and 11. These POS register bits are designed so that on power-up the I/O base address default is 7280H. By using these three bits in the normal POS register bank, I/O base addresses 7280H, 7290H, 7680H, 7690H, 7A80H, 7A90H, 7E80H and 7E90H are possible.

The EtherLink/MC 32 adapter's Micro Channel I/O base address can be configured to any multiple of 16 bytes through the use of the POS Subaddressing feature. Address lines 5 through 9 and 12 through 14 are compared to bits 0 through 7 of POS subaddress register 100H respectively. Address line 15 is compared to bit 0 of POS subaddress register 101H.

Memory Base Address

POS register XXX2, bits 4, 5 and 6 are compared to the Micro Channel address bits 14, 15, and 16. By using these three bits in the POS register memory base locations 000C4000H, 000C8000H, 000CC000H, 000D0000H, 000D4000H, 000D8000H, 000C0000H, and 000DC000H are selectable.

The shared memory window may be configured to any memory base address that is a multiple of 16K through the POS subaddressing feature. Micro Channel address bits 17 through 24 are compared to bits 0 through 7 of the POS subaddress register 102H respectively. Micro Channel address bits 25 through 31 are compared to bits 0 through 7 of POS subaddress register 103H.

Memory Window Size

The memory window can be programmed to any one of three sizes:

+WDOSIZE(1:0)	Window Size
00	16K (power-up and POS default)
01	32K
10	64K
11	not supported

Memory Window Enable

+WDOEN	Window Status
0	disabled (power-up default)
1	enabled (POS default)

Interrupt Level

POS register XXX5, bits 4 and 5 contain the interrupt levels for the Micro Channel bus. The 80186 processor generates interrupts which are directed to the Micro Channel bus. There are four interrupt levels supported by the adapter, INT 9, 10, 11, and 12. Interrupt can be set to any one of four levels:

+INT(1:0)	Interrupt Level
00	9 (power-up and POS default)
01	10
10	11
11	12

Bus Master Arbitration Priority

POS register XXX3, bits, 0 1, 2, and 3 contain the Bus Master Arbitration Priority Level. The adapter's Micro Channel DMA request arbitration priority level can be set to any one of the 16 available levels. The POS arbitration level default is 10. The Adapter Description File (ADF) supplied with the EtherLink/MC 32 adapter allows selection of arbitration levels from eight through fourteen.

+ARBLVL(3:0)	Arbitration Level
1000	8
1001	9
1010	10 (power-up default)
1011	11
1100	12
1101	13
1110	14
1111	15**

**Arbitration Level 15 is reserved for the system processor.

Fairness

POS register XXX3, bit 4 will enable or disable Fairness. When Fairness is enabled, the adapter will wait until all lower priority bus masters have had a chance to use the bus before it will attempt to arbitrate for the Micro Channel again.

+FAIR	Fairness
0	Disabled (power-up default)
1	Enabled (POS default)

Transceiver Selection

POS register XXX4, bit 1 will select either the External Transceiver or the On-board Transceiver. An External Transceiver is attached at the AUI connector while the On-board Transceiver is networked at the BNC connector.

+BNC	Transceiver Selection
0	External transceiver selected (power-up)
1	On-board transceiver selected

Address Burst Management

POS register XXX5, bits 0 and 1 contain the byte boundary for address burst management. The address burst management (ABM) feature can be either disabled or set to 16, 32, or 64 bytes. When acting as a bus master, the adapter can be programmed to give up the bus when crossing a particular address boundary. In most systems this will have minimal performance impact, but systems that have cache sizes corresponding to 16, 32 or 64 bytes may have improved bus operations when configured at the appropriate ABM setting.

+ABM(1:0)	Address Burst Management Mode
00	Disabled (power-up and POS default)
01	16-byte boundary
10	32-byte boundary
11	64-byte boundary

Subaddressing

POS registers 6 and 7 are used to write 16-bit addresses to the adapter so that extended POS information can be accessed. When both register 6 and 7 are set to zero, POS register 3 functions normally (as defined above). Whenever the register is non-zero POS register 3 becomes an access port to a 64K-byte field of general purpose POS registers. POS register 6 provides the least significant 8 bits of the 16-bit address while register 7 provides the most significant 8 bits of the 16-bit address.

Locations 0001H through 0104H are used in this adapter. Product specific data (including the adapter's unique 48-bit network address) is contained within a special 256-byte bipolar network management PROM that is installed on the adapter. The network management PROM resides in the subaddress space from 0001H to 00FFH.

Locations 0100H through 0104H are used for additional address decode comparison bits that allow the I/O base address to be mapped to any 16-byte boundary and the shared memory window base address mapped to any 16K boundary.

Host I/O Registers

The Micro Channel host and the EtherLink/MC 32 adapter may communicate through the I/O mapped Command register. In addition to this register, each side of the Micro Channel and adapter interface has a control register and a status register which are used for data transfer, handshaking and interface configuration. The Host I/O registers provide configuration and control information for the host software interface and the Command and Status registers pass commands to the 80186 processor. See Figure 2-2 Host I/O Register Map.

The base address of these registers is configured during power-up by the power-on self test (POST) routine. Refer to the POS Register descriptions for a detailed discussion of the adapter's configuration options.

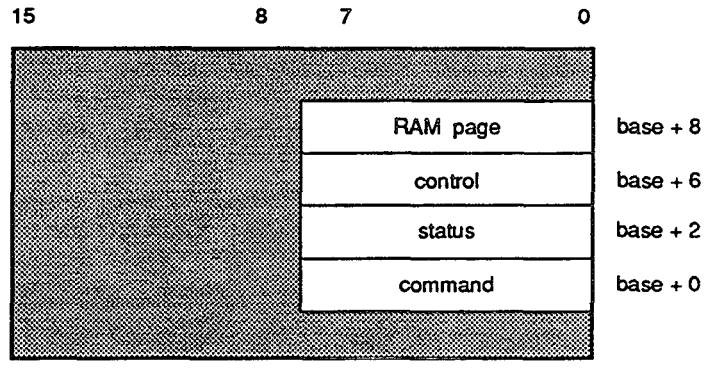

Figure 1-2. Host I/O Register Map

Host Command Register (I/O base + 0, R/W)

The command register is a full duplex, byte-wide register used to transfer commands and small amounts of data between the Micro Channel and the adapter. The host and the adapter can simultaneously exchange bytes of data. Data written to the command register (from the host) can be read only by the adapter's 80186 processor. Data read from the command register (by the host) is written to the command register by the adapter.

The command register can be polled using the command register ready (+CRR) and command word received (+CWR) bits in the host status register. Alternately, the command register can be used in an interrupt driven mode. In this mode, an interrupt to the Micro Channel bus will be generated when a byte is written into the command register from the adapter's 80186 processor.

The command register data field is free form but the software interface has defined the bit assignments. Reference the software Interface section for further explanation of the command register field definitions.

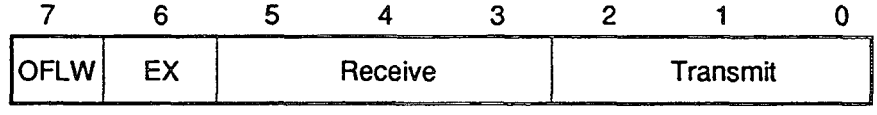

Figure 1-3. Host Command Register

Host Status Register (I/O base + 2, R/W)

The host status register is an 8-bit register used by the Micro Channel host to determine interrupt source and check status of the command registers. This register also provides the path to synchronize the host to the adapter's 80186 processor.

+CRR(RO) **Command register ready.** The +CRR flag handshakes data transfers through the command register from the host to the adapter. When the host writes to the command register, +CRR is cleared indicating that the register is not empty. When the adapter's 80186 processor has read the command register, +CRR is set, indicating that the command register is now empty.

+CWR(RO) **Command word received.** The +CWR flag handshakes data transfers through the command register from the adapter to the Micro Channel host. When the adapter's 80186 processor writes a data byte to its command register, +CWR is set, indicating that the register is full. When the host reads the command register, +CWR is cleared, indicating that the register is now empty.

* Reserved. Host software should not modify these bit locations.

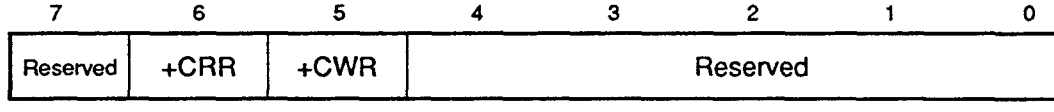

Figure 1-4. Host Status Register

Host Control Register (I/O base + 6, R/W)

The host control register is an 8-bit register used by the Micro Channel host to cause hard or soft resets on the EtherLink/MC 32 adapter and control interrupts The contents of this register can be read back by the host at any time. All bits in this register are cleared on a Micro Channel reset.

+ATTN — **Attention.** When the host sets +ATTN, a non-maskable interrupt (NMI) is generated to the EtherLink/MC 32 adapter's 80186 processor. The NMI function is used to cause a soft restart of the adapter. The host control and status registers on the adapter are not affected.

+RESET — **Adapter reset.** When the host simultaneously sets both +ATTN and +RESET, the adapter hardware decodes it as a "hard reset." The adapter status and control registers, the host status register, and the adapter DMA registers are reset. A RESET signal is propagated throughout the adapter, returning the adapter to a known power-up state. The adapter remains in this reset condition as long as both +ATTN and +RESET are set.

+CMD INTE — **Command register interrupt enable.** The +CMD INTE control bit allows the host to be interrupted when the adapter has written a data byte to the command register. Testing the +CWR bit will verify the command register as being the source of an interrupt.

* Reserved. Host software should not modify these bit locations.

7	6	5	4	3	2	1	0
+ATTN	Reset	Reserved			+CMD INTE	Reserved	

Figure 1-5. Host Control Register

RAM Page Register (I/O base + 8, R/W)

The base address of the memory access window may be set within the adapter's memory space on any boundary that is a multiple of 4K. This is accomplished by programming the appropriate value into the RAM page register (I/O base + 8). The value required for this register is computed by shifting the desired base address of the window (relative to the adapter's RAM memory map) to the correct 12-bit positions. The resulting value is programmed into the least significant 8 bits of the 8-bit RAM page register.

For example, to access a page of adapter memory starting at location 38000H (relative to the base of the adapter's memory space), write 38H to the RAM page register. The memory access page now starts at location 38000H of the adapter's memory space.

NOTE: In normal operation, the use of the RAM Page Register is not required and the value should remain at zero.

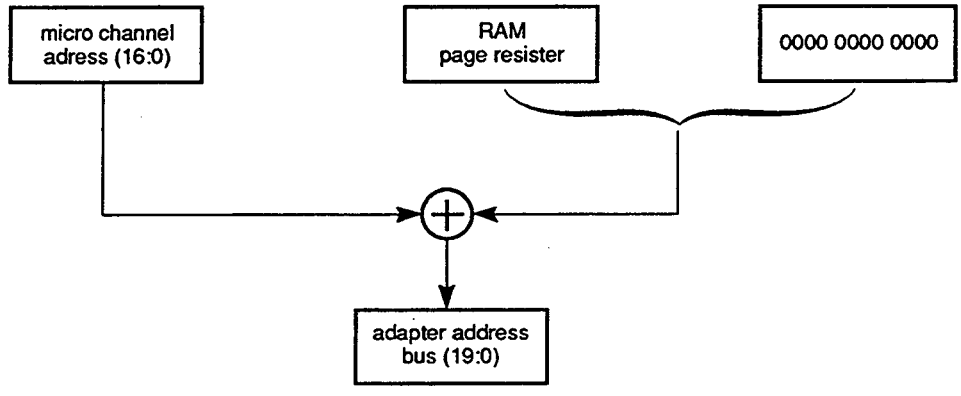

Figure 1-6. Host Address Mapping Mechanism

Shared Memory Interface

The adapter's 16K RAM is available to the Micro Channel as 16K of shared memory. The shared memory window is used to pass control/configuration information between the 80186 processor and the Micro Channel host and is not normally used to transfer data. Data transfer is accomplished through bus mastering which utilizes the bus more efficiently.

The configurations displayed in the ADF for the EtherLink/MC 32 adapter show the eight possible base addresses for the 16K window. It is possible to map the base address of the shared memory window to any 16K boundary in the 4G byte range supported by the Micro Channel architecture through the subaddressing feature in the POS registers. The base addresses and the subaddressing features are described in more detail in the POS Register section.

In general, shared memory operations should be minimized in code written for the EtherLink/MC 32 adapter because the shared memory interface is implemented as an asynchronous +CD CHRDY cycle which slows host CPU processing.

Bus Master Interface

The 80186 controls the Micro Channel Bus Master interface operations. The Bus Master interface accommodates the high volume of data transfer between the operating system and the Intel 80186 processor—transferring data to and from memory within the 2G byte address range.

Bus Master transfers operate in bursts of 200 ns which is the maximum rate that the Micro Channel will allow without data streaming controllers. It can be programmed to transfer numbers of bytes up to $(2^{20} - 1)$ from either a 32-bit Micro Channel starting address or a 20-bit adapter bus starting address.

The adapter's First-in First-out (FIFO) is designed to accommodate a burst of 32-bit words of 200 ns per cycle. When the adapter is installed in a 32-bit slot and destination of the data is a 32-bit device, the adapter will perform 32-bit transfers for every transfer except possibly the first and last transfer. The Bus Master Controller will always transfer the maximum number of bytes per cycle that is physically possible, depending upon the byte alignment of the data. However, the adapter will automatically use 16 bits as the maximum width cycle when it is installed in a 16-bit slot.

The Bus Master Controller will preempt the Micro Channel and arbitrate for control of the Bus Master interface when the FIFO becomes full or empty. Once granted the bus, the adapter will drive all Micro Channel control signals—bursting data across the interface until the FIFO is either full or empty or until one of the following events should occur: the programmed Micro Channel address boundary crossing occurs; the programmed transfer count decrements to zero, which is normal completion; or a 3.8µs elapse from another device preempting the Micro Channel.

The Micro Channel specification stipulates that the Bus Master must relinquish the bus within 7.8µs of receiving a preempt from another device or the system itself. The adapter will release the bus within 7.8µs of a preempt as long as the memory slave device deasserts (+CD CHRDY) is no longer than 3.5µs.

Micro Channel Interrupts

POS register XXX5, bits 4 and 5 contain the interrupt levels for the Micro Channel bus. The 80186 processor generates interrupts which are directed to the Micro Channel bus. Interrupts can be detected by testing the state of the +CWR bit in the host's status register. If true, then the 80186 has written a byte to the adapters command register. Interrupts from the adapter's processor can be disabled by clearing the +CMDINTE in the host's control register. There are four interrupt levels supported by the adapter, INT 9, 10, 11, and 12.

+INT(1:0)	Interrupt Level
00	9 (power-up and POS default)
01	10
10	11
11	12

For a discussion on interrupt sharing and other related issues, refer to appropriate IBM Micro Channel technical reference guide.

Network Management ROM Access

The 256 byte bipolar Network Management PROM contains the 48-bit network address value as well as other pertinent adapter information. Only the Micro Channel's host processor has access to read the PROM which is accomplished through the POS mechanism of subaddressing—a technique that entails writing 16-bit address values to POS registers 6 and 7. When the address values are non-zero, then the Network Management PROM data is visible to the host through the POS register bit 3.

POS subaddress locations 01H through FFH are used to access the 256 x 8 bipolar Network Management PROM which is programmed with an ASCII string that describe several aspects of the adapter:

Type	Content	Comments
ascii	"NMR"	Network Management PROM
dw	length of NMR	
dw	check code (crc)	
ascii	"*NA"	Network Address
db	5	length of field
db	"02608C******"	
ascii	"*RL"	
db	4	length of field
ascii	current firmware rev. level	"0012"
ascii	"*DS"	Description String
db	13	length of field
ascii	"EtherLink/MC 32 3C527"	Product Info
ascii	"*PN"	Part Number
db	7	length of field
ascii	"0008209000"	3COM assembly number
ascii	"*EC"	
db	5	length of field
ascii	"00000A"	3COM revision letter
ascii	"*DD"	
db	3	length of field
ascii	"01"	
ascii	"*DG"	
db	3	length of field
ascii	"01"	
ascii	"*FN"	
db	6	length of field
ascii	"00000000"	
ascii	"*SN"	Serial number
db	6	length of field
ascii	"00000000"	option is not supported at present
ascii	"*MF"	Manufacturers Number
db	5	length of field
ascii	"000001"	
ascii	"*DT"	Date code
db	5	length of field
ascii	"******"	yr-mo-day (i.e. 910408)
ascii	"*CR"	copyright field
db	12	length of field
ascii	"Copyright 3COM Corp."	

***** = Varies depending on the adapter being used.

Chapter 2
EtherLink/MC 32 Adapter Software Interface

This chapter presents the EtherLink/MC 32 adapter software interface definition. The definition explains the data structure and data flow. A full complement of diagnostic, configuration and statistics collection capabilities are also provided by the adapter's software interface.

Overview

The adapter's software interface consists of the following components:

- A full-duplex command register
- Three shared memory based command mailboxes
- Two shared memory based list structures

The host provides the adapter with simplistic low-level commands through the adapter's Command register. The adapter reads these low-level commands and determines which command mailbox to interpret. The adapter, in turn, notifies the host of completion of specific commands as well as other asynchronous activities via the Command register.

Two circularly linked list structures (transmit and receive) are maintained within the adapter's RAM—describing the host's receive and transmit buffer addresses to the adapter.

These list structures are composed of structures called buffer descriptors. By manipulating the contents of the buffer descriptors, the host and the adapter are able to control the reception and transmission of packets. This is shown in Figure 2-1.

The adapter has temporary staging buffers that are used to buffer (queue-up) transmit and receive data. These staging buffers are transparent to the host.

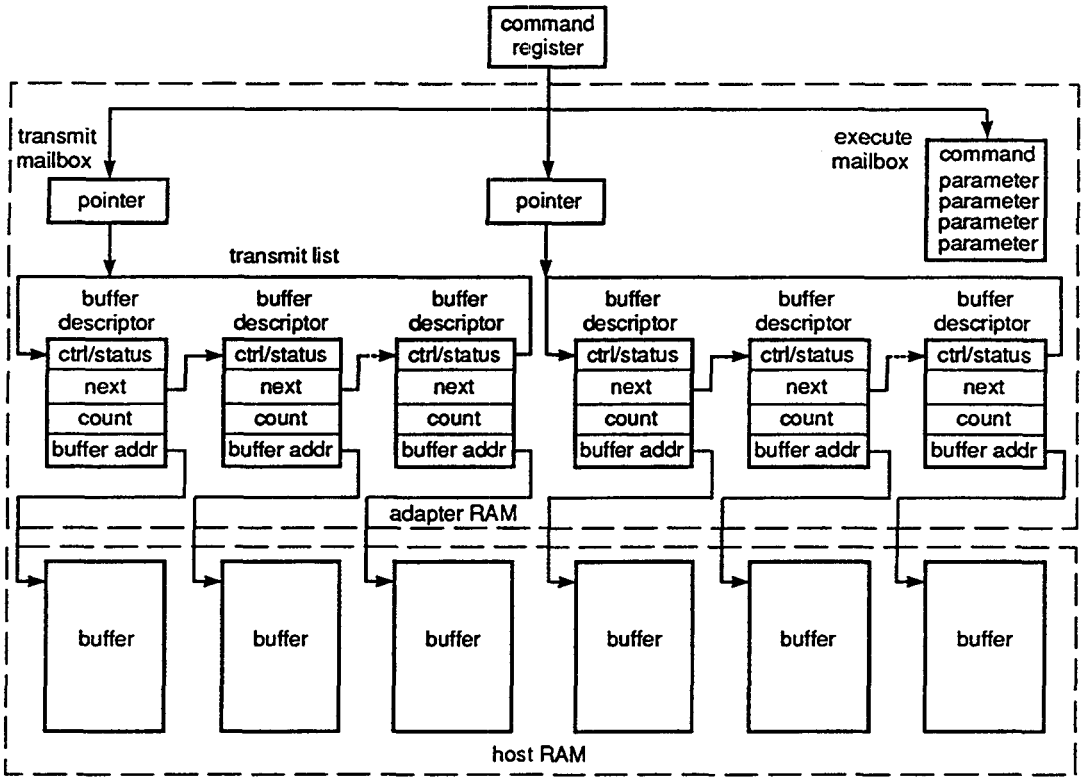

Figure 2-1. Adapter Data Structure as Viewed by the Host

Transmit/Receive Buffer Descriptor Data Structures

The transmit and receive data structures consist of buffer descriptors linked in a circular list. There are two separate lists: one for receive and one for transmit.

The buffer descriptor is used to describe individual transmit or receive packets. Any particular transmit packet can be made of one or more buffer descriptors. Each buffer descriptor is used to describe an arbitrary number of contiguous bytes within the host's memory. The buffer descriptors themselves reside within the adapter's RAM and are readable/writable by the host and adapter processors.

The buffer descriptor consists of a 16-bit control/status word, a 16-bit pointer to the next buffer descriptor, a 16-bit count field that indicates the actual number of bytes in the buffer, and a 32-bit physical address of the actual data buffer in the host's memory. The structure for both the transmit and receive packet and buffer descriptors are identical in format. However, there are some status and flag bits that do not apply in both the transmit and receive cases.

NOTE: It is assumed that each buffer descriptor in the receive list defines a receive buffer in the host's memory that is large enough to hold a maximum sized Ethernet packet (1514 bytes). This maximum size can be changed by using the set maximum upload command.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	offset
EOP	EL	*	*	*	*	*	*	C	OK	B	*	error code				0
link to next package buffer																2
2nd byte (MSB)								1st byte (LSB)								4
2nd byte						buffer address						1st byte (LSB)				6
4th byte (MSB)								3rd byte								8

Figure 2-2. Buffer Descriptor

Control/Status Word

The control/status word contains the bits that indicate the condition of the data in the packet as well as instructions for the adapter from the host. The status portion of the word (bits 0-7) contains 8 status bits. These bits generally have different definitions depending on whether the descriptor is associated with a transmit or a receive packet. In both cases, this byte is written by the adapter. The following paragraphs define each of the bits for both the transmit and receive cases.

+C — **Transmit/receive: Complete.** This bit is set by the adapter when the corresponding transmit or receive command has been completed. This bit does not indicate that the command was completed successfully. This bit is reset by the host.

+B — **Transmit/receive: Busy.** This bit is set by the adapter when the packet buffer is in use. This bit is reset by the host.

+OK — **Transmit/receive: Okay.** This bit is set by the adapter when no errors have been detected in the transmission or reception of the packet. This bit is reset by the host.

Error Code — **Transmit/receive:** This field contains the error code when an error has occurred during the transmission or reception of a packet. The error codes are as follows:

0001h	Transmit: Maximum collisions Receive: CRC error
0002h	Transmit: FIFO underrun Receive: FIFO overrun
0003h	Transmit: Carrier sense lost Receive: Alignment error
0004h	Transmit: Clear to send lost Receive: No resources
0005h	Transmit: Transmit timeout Receive: Packet too short

NOTE: These error codes should be considered "soft" error conditions with the adapter remaining fully functional.

The control portion (bits 8-15) of the control/status word contains option bits that are set by the host prior to the use of the buffer descriptor by the adapter. These bits are defined as follows:

+EOP **Transmit/receive: End of Packet.** This bit is set by the host (transmit only) if this buffer contains the end of the packet. Alternately, this bit is set by the adapter (receive) if this buffer contains the end of the packet.

+EL **Transmit/receive: End of List.** This flag indicates to the adapter that this buffer descriptor is the last one in the list available to the adapter. This bit is set by the host.

NOTE: Although the control/status word can be logically thought of as a 16-bit entity, both the adapter and host are actively manipulating the buffer descriptors. Consequently, the control/status word must be updated by both sides as separate and distinct 8-bit entities. In other words, if the host wishes to update one of the bits in the control portion (bits 8-15) of a buffer descriptor, it must only perform an 8-bit operation not a 16-bit operation. Failure to observe this constraint could lead to race conditions.

Link to Next Buffer Descriptor

This 16-bit value points to the first location of the next buffer descriptor. This field is initially set by the adapter at power-on/reset and should not be written by either the host or adapter processors during actual operation.

Byte Count

The byte count value stored here reflects the actual number of valid data bytes stored within the buffer. The adapter sets this value during receives while the host writes this value for transmits.

Buffer Address

This value is the 32-bit physical address of the host memory location at the start of the buffer. The least significant word is written to location 6 of the buffer descriptor.

The Command Register

The command register is a full duplex 8-bit I/O mapped register which is structured so that transmit, receive and general purpose commands can be issued or acknowledged in a single transfer through the register. After the adapter is either powered-up or reset, the adapter's status will be returned to the host via the command register.

Immediately after reset, the adapter will write FFH* to the command register. This indicates to the host, that the adapter has been reset and that the self-tests are in progress.

If the self-tests are successful, the adapter will write 00H** to the command register—indicating successful completion of the self-tests. The adapter will not wait for the host to read the FF from the command register before writing the self-test result.

A non-zero code indicates a hard error condition and the adapter is considered non-functional.

* If the command register remains at FFH for more than one second, then the adapter was unable to perform the tests and is considered non-functional.

** If the host reads 00H from the adapter's command register, the host will then read additional bytes (used by the host) to build the 32-bit physical adapter memory address for the location of the execute mailbox. The least significant byte of the 32-bit address is presented first.

As part of the self-test routine, automatic execution of the report adapter "Configuration" command will occur. The results of this command will be posted (in RAM) in the execute mailbox location as specified by the 32-bit address that was supplied through the command register.

NOTE: The reading of the command register, from the host, will cause an implicit clearing of any/all active command register bits in the adapter's command register image, but the bits in the command register itself remains unchanged until the adapter posts a new/updated image to the command register.

This section provides the command register field definitions and explains the functions of the register:

Transmit — **Transmit Command field.** This 3-bit field (bits 0, 1, and 2) is used by the host to issue transmit commands to the adapter and in turn used by the adapter to issue transmit status to the host.

Receive — **Receive Command field.** This 3-bit field (bits 3, 4, and 5) is used by the host to issue receive commands to the adapter and in turn used by the adapter to issue receive status to the host.

Ex — **Ex Command field.** This 1-bit field (bit 6) is used by the host to issue an execute command to the adapter and in turn used by the adapter to notify the host that an execute command has been completed.

OFLW — **OFLW Status field.** This 1-bit field (bit 7) is set by the adapter to inform the host that the most significant word of one of the statistics counters has reached the value of 0FFFFh and is approaching an overflow condition. Whenever the host sees this bit set, it will read all of the statistics counters and then reset to zero.

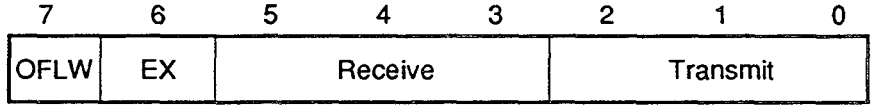

Figure 2-3. Command Register Format

Transmit Operation

This section describes transmit commands/acknowledges passed through the transmit field of the command register as well as the packet transmit operation.

Transmit Commands/Acknowledges

The following bit combinations for command register bits 2, 1, and 0 are defined by the adapter as the transmit command field.

TXCMD	Command/Acknowledge Definition
000	NOP/NOP
001	Reserved
010	Single packet transmitted/Not Applicable
011	Suspend transmission/transmission suspended
100	Abort transmission/transmission aborted
101	Restart transmission/Not Applicable
110	Transmission error/Not Applicable
111	Reserved

NOTE: Before issuing a transmit command through the command register, the host must clear the status word in the transmit mailbox.

NOP (000)

The NOP, no operation command, has no effect on the current state of the transmit state machine. The adapter will return a 000 status either in response to a NOP command or if either the receive or execute state machines issues an acknowledgement when there is no relevant activity from the transmit state machine to report.

Single Packet Transmitted (010)

Upon posting of the C and OK bits in the buffer descriptor of a packet just transmitted, the adapter will output an acknowledgement code of 010 to the command register (if indications are enabled) to interrupt the host to indicate that an individual packet has been transmitted.

Suspend Transmission (011)

This command will cause the transmit state machine to suspend further transmissions immediately after the packet that is currently being transmitted has completed its transmission. If no packet is currently being transmitted, then the adapter is simply inhibited from initiating a transmission. This command merely places a hold on transmissions. No queued-up data is lost. Transmissions may be restarted beginning with the next packet in the transmit list by issuing the restart transmission (code 101) command.

As soon as the transmit state machine has been successfully halted, the adapter will output a transmit suspended acknowledgement code (011) to the command register to acknowledge that this has occurred.

Abort Transmission (100)

This command will immediately shut down the adapter's transmitter regardless of its current condition. All pending transmissions are cancelled and all transmit packet buffers are recovered for future use. There is no recovery from an abort command. To begin transmitting again, the host will have to move the EL bit in the transmit list.

The adapter will output a transmit aborted acknowledgement code (100) to the command register as soon as the transmitter has been halted and the transmit buffers have been recovered.

Restart Transmission (101)

If the transmissions have been suspended, this command will cause them to resume with the next packet in the transmit list. This command is ignored if the transmit state machine is not currently suspended.

There is no response from the adapter regarding the restart transmission command. Single packet transmitted (010H), or transmission error (110H) acknowledgement codes will be output to the command register (if indications are enabled) once the transmissions resume.

Transmission Error (110)

The transmission error acknowledgement code (110) will be written to the command register by the transmit state machine if any transmission errors occurred (maximum collisions, FIFO underrun, carrier sense lost, clear to send lost, and transmit timeout).

Packet Transmission Operation

This section describes the operations, from the adapter and the host sides, which take place in order to transmit a packet. After the adapter is powered-up/reset, the transmit list will be set up as follows:

- All buffer descriptors, in the transmit list, will have been linked into a circularly-linked list. The adapter will set the EL bit, in the first buffer descriptor in the transmit buffer descriptor ring, and place the value of the first transmit buffer descriptor in the transmit mailbox.
- The transmit list EL pointer, in the transmit mailbox, will point to the first buffer descriptor in the transmit list.
- The first buffer descriptor, in the transmit list, will have the following bits set in the Control/Status word: EL, EOP, C, and B.

When the adapter detects that the EL bit has been moved, then the adapter will start at the transmit list EL pointer, and follow the chain of transmit buffer descriptors until finding a buffer descriptor with the EL bit set. The adapter will then update the value in the transmit mailbox with the new transmit list EL pointer.

NOTE: After power-on/reset, it is the host's responsibility to ensure that a valid transmit list EL pointer exists at all times.

The host will follow this procedure in order to transmit a packet:

- Obtain the pointer, to the current transmit EL, from the transmit mailbox.
- Obtain the pointer, to the next buffer descriptor, and use that pointer as the first buffer descriptor to be filled in.

Fill in the buffer descriptor fields as follows:

- Place the 32-bit physical address of the buffer, which contains the data to be transmitted into the host's memory.
- Place the length (in bytes) of the data to be transmitted.
- Clear the status portion (bits 0-7) of the control/status word.
- The control portion (bits 8-15) of the control/status word should be set with the appropriate bits. If the buffer descriptor is the last one defining a packet, then the EOP bit should be set. Additionally, if the buffer descriptor is for the last packet to be transmitted, then the EL bit should also be set.
- When all buffer descriptors have been prepared, then the host must clear the EL bit in the buffer descriptor currently pointed to by the transmit EL pointer in the transmit mailbox.

If a packet to be transmitted exists in the host's memory as non-contiguous pieces, then more than one buffer descriptor will be used to inform the adapter of where, in the host's memory, the pieces are located. The packets to be transmitted may be defined using one or more buffer descriptors. The adapter will then perform the gather operation.

When the adapter detects that the EL bit in the buffer descriptor, currently pointed to by the transmit EL pointer in the transmit mailbox, has been cleared, the adapter will perform the following:

- When the host wishes to transmit a packet, the host must set the EL bit in the buffer descriptor, which is currently pointed to by the transmit EL pointer, and then clear the EL bit in the buffer descriptor currently pointed to in the transmit EL pointer.
- The last buffer descriptor, defining a packet to be transmitted, must have the EOP bit in the control/status word of the buffer descriptor set.
- The last buffer descriptor, describing the last packet to be transmitted, must have the EL bit in the control/status word set.
- Starting at the buffer descriptor pointed to by the transmit EL pointer, the adapter will follow the buffer descriptor chain until it finds a buffer descriptor with it's EL bit set. As it follows the chain, it will add all packets to be transmitted to the internal list of packets to be transmitted.

When the adapter has found the buffer descriptor with the EL bit set, it will update the transmit EL pointer in the transmit mailbox. When a packet transmission is complete, the adapter will set the status bits of the control/status word of the buffer descriptor containing the EOP bit of the packet just transmitted.

The adapter will set the C and OK bits, if the packet was transmitted successfully. The OK bit will not be set if there was an error during transmission. Instead, the adapter will increment the appropriate transmit statistic counter and set the error code field of the buffer descriptor's control/status word with one of the following values:

001H	Maximum collisions
002H	FIFO underrun
003H	Carrier sense lost
004H	Clear to send lost
005H	Transmit timeout

The adapter will then update the image of the command register with one of the appropriate acknowledgement codes: single packet transmitted (010H), or transmission error (110H).

The adapter's next descriptor decides whether or not to interrupt the host. The adapter will see if interrupts to the host have been suspended via the indication enable/disable command. If the posting of interrupts to the host have not been suspended, then the adapter will output the command register image to the command register.

NOTE: The adapter itself will perform no retries over or above those performed by the 82586 except in the case of a transmit timeout error. If a transmit timeout error is reported, then the adapter has already exhausted the number of retry attempts to get the packet transmitted.

Once the adapter has started a packet transmission, the adapter will see if there is another packet in the transmit list to be transmitted. If so, then it will overlap the transfer of data from the host to the adapter while the transmit is in progress.

Receive Operation

The following bit combinations for command register bits 5, 4, and 3 are defined by the adapter.

RXCMD	Command/Acknowledge Definition
000	NOP/NOP
001	Start packet reception/Not Applicable
010	Packet received/Not Applicable
011	Suspend reception/reception suspended
100	Abort reception/reception aborted
101	Restart reception/Not Applicable
110	Out-of-receive resources/Not Applicable
111	Reserved

NOTE: Before issuing a receive command through the command register, the host must clear the status word in the receive mailbox.

The following sections expand upon the preceding definitions.

NOP (000)

The NOP command has no effect on the current state of the adapter's receive mechanism. The adapter will return a NOP acknowledge either in response to a NOP command being completed or if either the transmit or execute state machines returns a status while the receive state machine has nothing significant to report.

Start Packet Reception (001)

When the receive state machine receives this command code it will read the contents of the receive mailbox and use the address pointer value stored there by the host to find the start of the receive list.

NOTE: Prior to issuing the start packet reception command, the host should have accomplished the following tasks:

- Prepared the buffer descriptors comprising the receive list as follows:
  - Cleared the bits in the control/status word. The only exception to this is that the last buffer descriptor in the receive list must have the EL bit in the control/status word set.
  - Placed the 32-bit physical address of a buffer in host memory large enough to accommodate a maximum-sized Ethernet packet (1514 bytes) in the buffer address field of the buffer descriptor.
- Placed the offset of the first buffer descriptor in the receive list in the receive list pointer field of the receive mailbox and cleared the status field of the receive mailbox.
- Optionally issued the set receive filter command.
- Optionally issued the set pattern match filter command.
- Optionally issued the set multicast command.

Packet Received (010)

When the adapter is notified by the 82586 processor of the arrival of a received packet, it will look to see if the packet is in error or not. If it is in error, the adapter will take the following actions:

- Increment the appropriate receive statistic counter.
- Examine the SAV BP bit in the configuration information to determine if the host wants bad packets transferred. If so, it will set the appropriate error code in the error code field. If the SAV BP bit is zero, then the adapter will discard the packet.

If the packet is to be transferred to the host, the adapter will set the C bit in the status portion of the receive buffer descriptor's control/status word and update it's command register with the packet received acknowledgement code (010). If the posting of interrupts have not been disabled via the disable indications command, then the updated command register image will be output to the command register.

Suspend Reception (011)

This command will cause the receive state machine to suspend further reception of packets following the completion of the reception of the current packet. If there is no packet currently being received, the adapter's receiver is shut off immediately. A restart reception command may be issued to cause the adapter to resume receiving packets where it left off in the buffer pool.

The receive state machine will output a receive suspended acknowledgement code (011) to the command register to indicate to the host that the adapter's receiver has been shut down. If there had been a packet in the process of being received, its reception indication (assuming that it was a well-formed packet) would have preceded the suspend reception acknowledgement.

Abort Reception (100)

The abort command will cause the immediate shut-down of the adapter's receiver. Any packet in the process of being received will not be made available to the host. There is no recovery from an abort command. A new start reception command must be issued to begin reception again.

The receive state machine will return a reception aborted acknowledgement code (100) to the command register as soon as the adapter's receiver has been satisfactorily shut down.

Restart Reception Command (101)

The restart reception command is issued to begin packet reception again on the adapter following the earlier suspension of reception. The command will begin at the next receive buffer descriptor following the last buffer descriptor which the host was notified to have successfully completed. If the end of list bit and the complete bit are encountered in the buffer descriptor to be used to start with by the adapter, the adapter will issue an out of resource notification to the host and will fail to restart the adapter.

Out-of-Receive Resources (110)

This status indication is made available to the host so that the host may take some form of corrective action to restructure or expand the receive buffer area so that no further packets are dropped.

NOTE: When the adapter issues this acknowledgement, the adapter discards all subsequent packets received from the network. The host must issue a start packet reception command in order to receive more packets.

Execute Command/Acknowledges

The execute commands are characterized by their infrequency of use. A variety of configuration, diagnostic and statistical functions are made available to the host through this mechanism.

The execute command bodies are set up in the execute command mailbox within adapter memory. These variable length command blocks are then interpreted by the adapter and carried out as defined. The following sections define the various execute commands.

NOTE: Before issuing a execute command through the command register, the host must clear the status word in the execute mailbox.

EXCMD	Command/Acknowledge Definition
0	NOP/NOP
1	Execute command/command executed

Mailboxes

Three mailboxes are used to expand upon the primitive command indications given to the adapter by the host. These mailboxes are located at fixed adapter RAM locations and provide either pointers to descriptors or provide the actual commands and parameters. The values in the mailboxes are set up by the host prior to writing a corresponding command to the command register. The generic format for the first word in each of the mailboxes is:

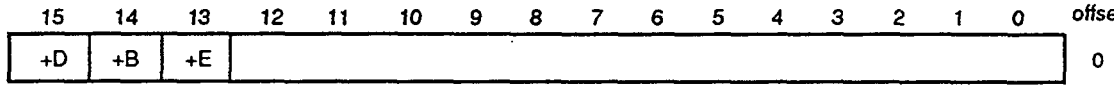

Figure 2-4. Mailbox Format

The three status bits are defined as:

+D **Done.** This bit indicates that the adapter has processed the command. This bit does not indicate the success or failure of the adapter to complete the desired operation.

+B **Busy.** The busy bit is set by the adapter while it is processing the command. It is reset by the adapter after either successful or unsuccessful completion.

+E **Error.** This bit indicates that an error occurred during the processing of the command. Further indications of the source of the error may be provided within the parameter region.

Transmit Mailbox

The transmit mailbox consists of two 16-bit words. The first word is a status word that indicates the completion status of transmit commands issued through the command register. The second word is a pointer to the transmit buffer descriptor which currently has it's EL bit set. The physical location of the transmit mailbox is reported by the report configuration command.

The transmit mailbox's status word contains the value that indicates the completion status of a transmit command issued through the command register.

The second word in the transmit mailbox, the transmit list EL pointer, contains the pointer value associated with the buffer descriptor in the transmit list which currently has it's EL bit set. This pointer is maintained by the adapter (READ/WRITE) and is read-only for the host. When the host wishes to transmit a packet, the host must set the EL bit in a buffer descriptor succeeding the buffer descriptor which is currently pointed to by the transmit EL pointer. The host then clears the EL bit in the buffer descriptor currently pointed to by the transmit EL pointer. When the adapter detects that the EL bit has been moved, it will start at the transmit list EL pointer and follow the chain of transmit buffer descriptors until it finds a buffer descriptor with it's EL bit set. The adapter will then update the value in the transmit mailbox with the new transmit list EL pointer. After a power-on/reset, the adapter will set the EL bit in the first buffer descriptor in the transmit buffer descriptor ring, and place the value of the first transmit buffer descriptor in the transmit mailbox.

NOTES:

1. *After power-on/reset, it is the host's responsibility to ensure that a valid transmit list EL pointer exists at all times.*
2. *Before issuing a transmit command through the command register, the host must clear the status word in the transmit mailbox.*

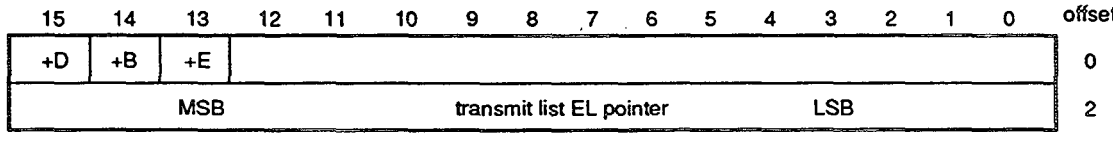

Figure 2-5. Transmit Mailbox

Receive Mailbox

The receive mailbox is very similar to the transmit mailbox in that there is a status word followed by a pointer value. Like the transmit mailbox, the status word indicates the completion status of a receive command issued through the command register.

The second word in the receive mailbox, the receive list pointer, is only used when the start packet reception command is issued. This pointer is maintained by the host and contains the offset of the buffer descriptor which is the first buffer descriptor in the receive list (i.e., the buffer descriptor which will be filled in by the adapter upon when a packet is received).

NOTE: Before issuing a receive command through the command register, the host must clear the status word in the receive mailbox.

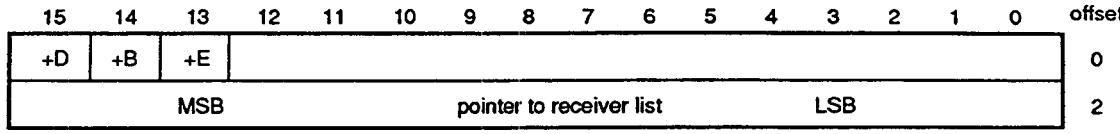

Figure 2-6. Receive Mailbox

Execute Command Mailbox

The execute command mailbox is different from both the transmit and receive mailboxes. The execute command mailbox consists of a 16-bit command word followed by optional parameter words. The completion of the desired execute command is indicated by the adapter setting the +EXCMD bit in the command register.

NOTE: Before issuing a execute command through the command register, the host MUST clear the status word in the execute mailbox.

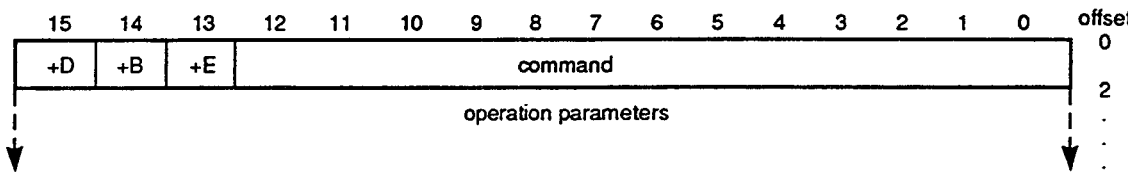

Figure 2-7. Execute Mailbox

Execute Mailbox Commands

Set Receive Filter (0000H)

The set receive filter command is used to qualify which destination addresses the 82586 will accept. When this command is issued, the adapter will automatically suspend the 82586's receive processing until after it has issued the new parameters to the 82586. When the 82586 has completed the command, the adapter will restore the previous 82586 receive processing state. This allows the host to issue this command "on-the-fly."

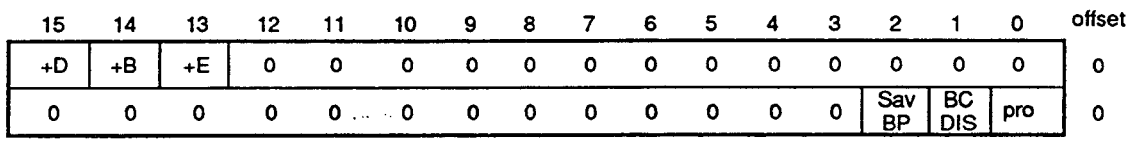

Figure 2-8. Set Receive Filter Command

Pro — **Promiscuous mode.** When this bit is set to a 1, the adapter is enabled to receive every packet on the network regardless of its destination address. Default value = 0.

Sav BP — If this bit is zero (0), bad received frames are not forwarded to the host. Default value = 0.

BC Dis — Setting this bit to one (1) disables the reception of broadcast packets. Default value = 1.

NOTE: Following a power-up/reset, the 82586 is configured to receive ONLY the address programmed via the set network address command.

Set Network Address (0001H)

The adapter's unique network address value is established by this command. Default network address = 000000H. Setting this bit to 1 disables the reception of broadcast packets following a power-up/reset. The 82586 is configured to receive only the address programmed via the "Set Network Address" command.

NOTE: The first byte (MSB) of the network address is the byte which appears first on the wire when the bytes are grouped in left-to-right order with byte 1 being the left-most byte and byte 6 being the right-most byte.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	offset
+D	+B	+E	0	0	0	0	0	0	0	0	0	0	0	0	1	0
2nd byte								1st byte (MSB)								2
4th byte								3rd byte								4
6th byte (LSB)								5th byte								6

Figure 2-9. Set Network Address Command

Set Multicast Addresses (0002H)

A set of multicast addresses may be programmed into the adapter through this command. The multicast table entry count field contains the number of 48-bit address entries in the execute command parameter field. DEFAULT = NO multicast addresses.

NOTE: The maximum number of multicast addresses which can be set with this command is 10. The first byte (MSB) of the network address is the byte which appears first on the wire when the bytes are grouped in left-to-right order with byte 1 being the left-most byte and byte 6 being the right-most byte.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	offset
+D	+B	+E	0	0	0	0	0	0	0	0	0	0	0	1	0	0
multicast table entry count																2
2nd byte								1st byte (MSB)								4
4th byte							multicast I.D.			3rd byte						6
6th byte (LSB)								5th byte								8

Figure 2-10. Multicast Setup Command

Set Receive Pattern Match Filter (0003H)

The set receive pattern match filter command allows the host to specify a list of values which can be used to further qualify received packets. This list will be used by the adapter in deciding whether or not to discard a received packet. If a received packet is good and it has met the prerequisite filtering (broadcast, multicast, or station), then the pattern match list will be scanned to see if the packet's data matches any of the values in the list. If no match occurs, the packet will be discarded; otherwise, the packet will be forwarded to the host.

Each time the command is issued it supersedes any prior issued command. Therefore, to add or delete a list entry requires that the entire modified list must be specified. If the command is issued with a count of zero, then no pattern match filtering will be performed by the adapter. After a power-on/reset, the adapter will perform no pattern match filtering.

Displacement This field specifies the byte-offset from the beginning (byte 0) of the packet where the pattern matching should start.

Count This field specifies the number of entries in the pattern match list. Default = 0.

Length This field specifies the size (in bytes) of each entry in the pattern match list. All pattern match entries must be the same size (i.e., if Length = 1, then all pattern match list entries must be 1-byte values).

NOTES:

1. *The total size of the pattern match list (COUNT * LENGTH) must not exceed 64 bytes.*
2. *If LENGTH = 2, then each entry in the pattern match list must be in the format shown in Figure 2-11.*

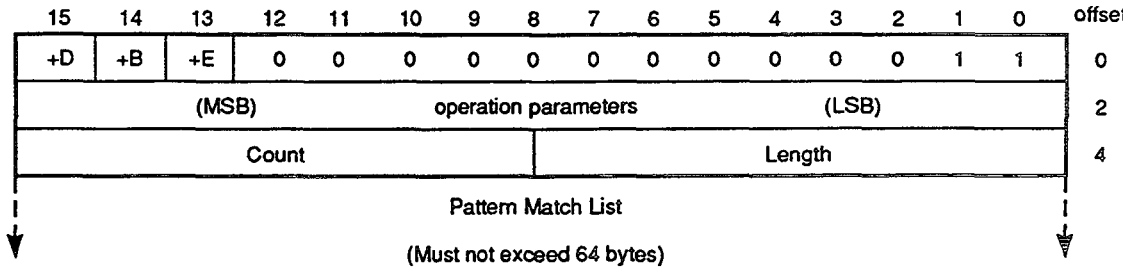

Figure 2-11. Set Receive Pattern Match Filter Command

Indication Enable/Disable (0004H)

This command is issued to enable and disable the generation of interrupts (the writing of byte to the command register) by the adapter. The adapter continues to execute any pending transmit commands and remains enabled for packet reception regardless of the setting of this status bit. Setting bit 0 of word 2 enables the interrupts, resetting this bit disables the adapter's command register interrupts. This action is distinguished from clearing the +CMD INTE bit in the host control register of the adapter in that the adapter's 80186 will have an indication of the execute command but not of the +CMD INTE bit. DEFAULT=DISABLED (bit 0=0).

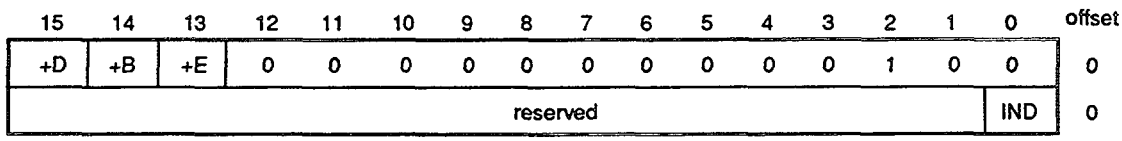

Figure 2-12. Indication Enable/Disable Command

Diagnose (0005H)

The diagnose command causes the following series of tests to be performed by the adapter:

- ROM checksum
- Non-destructive RAM test
- Internal loopback test of the 82586

The completion code values are:

0000H	Completed successfully
0001H	ROM checksum failure
0002H	RAM test failure
0004H	82586 internal loopback failure

NOTES:

1. *A non-zero completion code denotes a hard error condition and indicates that the adapter is currently non-functional.*
2. *This command should be viewed as a diagnostic command and as such should not be issued under normal operation. Upon completion of this command, the adapter should be reset.*

The following sections describe the tests.

ROM Checksum Test. This test verifies that the contents of ROM are valid.

Nondestructive RAM Test. Skipping the RAM used for interrupt vectors and stack space, this test performs a read/write logical complement/compare/write original operation on each RAM location until the last location in RAM is reached.

82586 Internal Loopback Test. This test issues a configure command to the 82586 to place it in the internal loopback mode. It then transmits a canned (predetermined) test packet and compares the received packet against the test packet to determine if the 82586's internal loopback is functioning correctly. If the test completes successfully, the adapter will return the 82586 back to normal network operation.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	offset
+D	+B	+E	0	0	0	0	0	0	0	0	0	0	1	0	1	0
reserved for response												completion code				2
reserved for response																4
reserved for response																6
reserved for response																8

Figure 2-13. Set Diagnose Command

Report Configuration (0006H)

The current configuration of the adapter is reported into that block of parameter RAM that follows the execute mailbox. This command is automatically executed by the adapter after a reset. Therefore, this information will be available to the host immediately after the completion of the adapter's initialization process.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
+D	+B	+E	0	0	0	0	0	0	0	0	0	0	1	1	0	0
MSB						main offset (LSW)						LSB				2
main offset (MSW)																4
receive mailbox offset																6
transmit mailbox offset																8
execute mailbox offset																A
statistics counters offset																C
memory size, in KBytes																E
buffer descriptor region size																10
transmit list start offset																12
transmit list count																14
receive list start offset																16
receive list count																18
firmware version																1A
reserved																1C
82586 SCB statistics offset																1E

Figure 2-14. Report Configuration Command

Main offset

This 32-bit value should be added to the various 16-bit offset values supplied to determine the actual physical adapter address of the structures reported by this command.

Receive mailbox offset

This 16-bit value, when added to the main offset, provides the physical location of the receive mailbox within the adapter's memory.

Transmit mailbox offset

This 16-bit value, when added to the main offset, provides the physical location of the transmit mailbox within the adapter's memory.

Execute mailbox offset

This 16-bit value, when added to the main offset, provides the physical location of the execute mailbox within the adapter's memory.

Statistics counters offset

This 16-bit value, when added to the main offset, provides the physical location of the statistics counters within the adapter's memory.

End of RAM offset	This 16-bit value contains the offset of the last byte in RAM.
Buffer descriptor region size	This 16-bit value contains the amount of RAM (in bytes) available for the transmit and receive buffer descriptor lists.
Transmit list start offset	This 16-bit value, when added to the main offset, provides the physical location of the start of the transmit list within the adapter's memory.
Transmit list count	This 16-bit value informs the host how many buffer descriptors have been allocated in the transmit list.
Receive list start offset	This 16-bit value, when added to the main offset, provides the physical location of the start of the receive list within the adapter's memory.
Receive list count	This 16-bit value informs the host how many buffer descriptors have been allocated for the receive list.
Firmware revision	This hexadecimal value provides the revision level of the firmware installed in the adapter. It is incremented by 1 for each firmware revision.
82586 SCB statistics offset	This 16-bit value, when added to the main offset, provides the physical location of the 82586 SCB statistics block within the adapter's memory.

Command Register "Wrap" (0007H)

This command allows the host to verify the correct operation of the duplex path of the command register operation. After this command is issued, the adapter will echo any data it receives from the command register back through the command register to the host. This will allow the host to check for correct adapter operation as well as check for shorts or opens in the duplex path.

If the +CMD INTE bit in the host control register is set, then the host can also test the interrupt logic.

The only way the host can terminate this command is to force an adapter reset by simultaneously setting the +ATTN and +RESET bits in the host control register.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	offset
0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	0

Figure 2-15. Command Register "Wrap"

Configure Lists (0008H)

This command allows the host to change the number of buffer descriptors in the receive and transmit lists. After a power-on/reset, the adapter sets both of the lists to contain equal numbers of buffer descriptors.

For tuning and/or optimization purposes, the host may wish to change the default configuration. The adapter will report an error if the host tries to configure the lists with illegal/invalid combinations of buffer descriptor counts (e.g., the total counts are larger than the total area allocated for the buffer descriptors, or one of the counts is less than six).

NOTE: The minimum count is four.

If the command successfully completes, the new counts and list starting offsets can be obtained/verified by the execution of the report configuration command.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	offset
+D	+B	+E	0	0	0	0	0	0	0	0	0	1	0	0	0	0
(MSB)			transmit list count									(LSB)				2
(MSB)			receive list count									(LSB)				4

Figure 2-16. Configure Lists Command

Set Loopback (0009H)

This command allows the internal/external loopback bits in the 82586's configuration to be set/cleared.

Int Lbk — **Internal Loopback Enable.** When enabled (=1), the adapter's 82586 logically disconnects itself from the transceiver circuitry and loops the transmit data back into the receive inputs. DEFAULT = DISABLED (0).

Ext Lbk — **External Loopback Enable.** When enabled (=1), this mode allows the 82586 to transmit and receive simultaneously. For Ext Lbk to work correctly, the 82586's receiver must be placed in promiscuous mode (via the set receive filter command), and a loopback plug must be attached to the active Ethernet connector (AUI or BNC). DEFAULT = DISABLED (0).

NOTE: Internal loopback will override external loopback if both bits are set. This command should be viewed as a "diagnostic" command and as such should not be issued under normal operation. Upon completion of this command, the adapter should be reset.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	offset
+D	+B	+E	0	0	0	0	0	0	0	0	0	1	0	0	1	0
Ext Lbk	Int Lbk	0	0	0	0	0	0	0	0	0	0	0	0	0	0	2

Figure 2-17. Set Loopback Command

Set Maximum Upload Size (000CH)

This command allows the host to specify the maximum packet size uploadable for the adapter to the host. Received frames exceeding this size will be discarded by the adapter. The range of possible values is from 60 bytes to 1514 bytes. The default size will be 1514 bytes which is the maximum allowed by the IEEE 802.3 specification. This command is issued through the execute mailbox.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	offset
+D	+B	+E	0	0	0	0	0	1	1	0	0	1	1	0	0	0
Maximum Size of Uploadable Frame																2

Figure 2-18. Set Maximum Upload Size

586AL-LocOff (000DH)

The LocOff command changes the 82586 AL-Loc bit configuration from the default value of one, which is on, to the value of zero, which is off. The effects of this change are transparent to the driver, however the adapter characteristics change slightly. This command allows the driver the option of controlling the setting of the AL-Loc bit to handle an 82586 errata whereby the 82586 is unable to handle back-to-back receive frames with the minimum interframe spacing (9.6 uSec) when AL-Loc = 1. The 82586 experiences DMA overrun conditions requiring higher level protocols to retransmit the discarded frame thereby degrading the system performance. Clearing the AL-Loc bit slightly degrades adapter performance although it may in fact improve overall system performance. It is recommended that adapters being placed in busy networks invoke this command. This command should be invoked early in the initialization process. To change the AL-Loc bit from a zero to a one, the adapter must be reset.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	offset
+D	+B	+E	0	0	0	0	0	0	0	0	0	1	0	0	1	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	2

Figure 2-19 586AL-LocOff Command

Interrupts Generated by the Adapter

The sole source of interrupts to the host by the adapter is the command register. The cause of the interrupt (once it is verified that the adapter is the source of the interrupt by checking the +CWR bit in the status register) can be determined by the value read from the command register. A branch table can be used to quickly respond to the various possible combinations of status indications.

The generation of interrupts to the host can be suspended via the indication disable command. If the host has suspended indications from the adapter, the adapter will continue to process the transmit list and to receive packets. It will update it's command register image, but will not output the updated image to the command register until after indications have been enabled.

The recommended procedure for a host's interrupt handler is to scan both the receive and transmit lists and process any completed buffer descriptors. The host should not exit it's interrupt handler until it has ascertained that there are no completed buffer descriptors. Only when it is ready to exit the interrupt handler should indications be enabled and the adapter allowed to interrupt the host.

The host's interrupt handler must be able to handle the case where an interrupt will be generated, but there may be no buffer descriptors with the C bit set. This would occur when the host had suspended indications, but the adapter had completed the reception or transmission of additional packets during the time when indications are suspended.

Statistics Counters

The adapter will maintain a number of counters pertinent to the reception and transmission of packets. All the counters are 32 bits and are contiguous in the adapter's physical memory except where noted as 16-bit counters. When the most significant word of any of the counters reaches the value of 0FFFFH, the adapter will generate a counter overflow interrupt. This should provide sufficient threshold to the host to allow the host to read and clear the counters before any of the counters roll over. The counters are available in memory in the order listed below. The counters the adapter will maintain are as follows:

Offset	Host Access Rights	Receive Related Counters
0	R/W	CRC errors
4	R/W	Alignment errors
8	R/W	Overrun errors
C	R/W	Too short packets
10	R/W	Too large packets
14	R/W	Out of resource errors
18	R/W	No. packets discarded (via pattern match filter)

Offset	Host Access Rights	Transmit Related Counters
1C	R/W	Maximum collisions
20	R/W	Carrier lost
24	R/W	Underrun errors
28	R/W	Clear to send lost
2C	R/W	Transmit timeouts

Offset	Host Access Rights	Function
30	R/W	32-bit count of times EL bit seen in receive list
34	R/W	32-bit count of number of No Receive Resources interrupt from 82586
38	R/W	32-bit count of number of good packets received
3C	R/W	32-bit count of number of received packets uploaded into host memory
40	R/W	32-bit count of number of times the "Start Packet Reception" command has been issued
44	R/W	32-bit count of the number of bus master transfer timeouts
48	RO	16-bit misc. variable - RESERVED FOR 3COM USE

(continued)

Offset	Host Access Rights	Function
4A	RO	16-bit misc. variable - RESERVED FOR 3COM USE
4C	RO	16-bit misc. variable - RESERVED FOR 3COM USE
4E	RO	16-bit state variable, bit mapped, reflects various PRIMARY firmware conditions/states
50	RO	16-bit state variable, bit mapped, reflects various SECONDARY firmware conditions/states
52	R/W	Reserved
56	R/W	Number of Packets Downloaded
5A	R/W	Reserved
5E	R/W	Number of Transmit Errors
62	R/W	Reserved
66	R/W	Reserved
6A	R/W	Reserved
6E	R/W	Number of Transmit Retries
72	R/W	Number of Transmits That Failed
76	R/W	Reserved
7A	R/W	Number of Packets that saw one collision
7E	R/W	Number of Packets that saw 2 - 15 collisions
82	R/W	Number of RBD's Discarded
84	R/W	32-bit misc. variable - RESERVED FOR 3COM USE

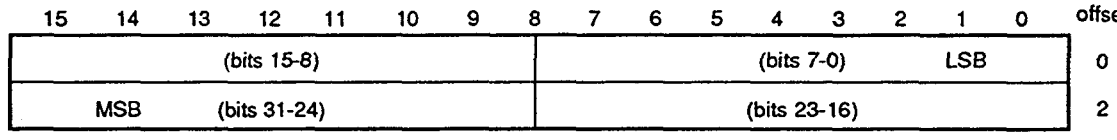

Figure 2-20. Counter Format

Power-on/Reset Tests

These are the tests that the adapter will perform at power-on/reset:

- Processor Instruction Test
- Processor Data Bus Test
- Adapter Data Bus Test
- ROM Checksum Test
- Base RAM Test
- Extended RAM Test
- 82586 Initialization/Configuration/Verification
- 82586 Internal Loopback Test

After the tests have been completed, the adapter will post the results in the command register as well as posting information in RAM, just as though a report configuration command had been issued. The successful completion of the tests may take up to 500 msec. The RAM initialization portion of the power-on/reset tests will not be complete until 300 msec after reset deasserted. If the power-on/reset test fails, the adapter will output a non-zero value to the command register. The following list details the error codes and their meanings:

Error Code	Meaning
01H	Processor instruction test failure
02H	Processor data bus test failure
03H	Processor data bus test failure
04H	Processor data bus test failure
05H	Adapter data bus test failure
06H	ROM checksum test failure
07H	Base RAM test failure
08H	Extended RAM test failure
09H	82586 internal loopback test failure
0AH	82586 initialization/configuration failure
0BH	Adapter list configuration error

The objective of each test is described below.

Processor Instruction Test. Verifies the correct operation of the processor's flags, registers, and conditional jumps.

Processor Data Bus Test. Ensures that the internal data bus of the 80186 is working correctly.

Adapter Data Bus Test. Ensures that none of the data bus lines are shorted or opened.

ROM Checksum Test. Verifies that the code residing in the ROM is valid.

Base RAM Test. Verifies that the memory used for interrupt vectors and the stack space is working correctly.

Extended RAM Test. Verifies that the remaining adapter RAM is functional by performing a series of bit pattern reads and writes.

82856 Initialization/Configuration/Verification. Performs a "hard" reset of the 82586, a default configuration of the 82586 and then issues a "dump" command to the 82586 to verify that the 82586 was configured correctly.

82856 Internal Loopback Test. This test sets up the 82586 to transmit and receive a "canned" test packet. If the 82586 receives the packet without error, the contents of the received packet are compared against the contents of the transmitted "canned" packet.

Adapter List Configuration Error. The adapter was unable to properly setup the transmit and receive queues.

Differences Between 3Com's EtherLink/MC 32 and the IBM High Performance Ethernet LAN Adapter* February 13, 1991

1. The IBM POS adapter I.D. number is 8EF5, and the EtherLink/MC 32 is 0041.

2. The IBM adapter supports exception condition handling such as parity checking/generation, and the EtherLink/MC 32 does not.

3. The two products will have slightly different pc board fabs.

4. The IBM adapter has a Vital Product Data ROM containing the network address and revision information. The 3Com adapter has a similar ROM called a Network Management ROM that has the same fields but with different field content.

* also known as "Etherboy"

2/4/91
dlb

The network management ROM is a hybrid of the Csay ROM. IT is identical except the first ascii field has "NMR" instead of "VPD" and two fields have been added, date (*DT) and a copyright (*CR). The fields have been filled with zeroes as place holders for IBM proprietary data.

Network Management ROM Format

type	field	bytes	comments
db	blank	1	00 address cannot be used
ascii	NMR	3	(IBM has VPD)
dw	length of NMR	2	(in words)
dw	check code (crc)	2	
ascii	*NA	3	pointer to Network Address (IBM)
db	5	1	network address length (IBM)
db	02608Cxxxxxx	6	network address (IBM)
ascii	*RL	3	same as IBM, ROS level
db	4	1	ROS length field
ascii	current ROS level	4	(ex. 0012)
ascii	*DS	3	Data string
db	13	1	character string length - 1
ascii	"EtherLink/MC 32 3C527"	22	pruduct info.
ascii	*PN	3	Part number
db	7	1	part number length field
ascii	008209000	10	assembly number
ascii	*EC	3	EC level
db	5	1	EC length field
ascii	000000	6	3Com is all zeroes
ascii	*DD	3	device driver
db	3	1	DD length field
ascii	0 !	2	3Com is all zeroes
ascii	*DG	3	diagnostic level
db	3	1	DG length field
ascii	0 !	2	3Com is all zeroes
ascii	*FN	3	FRU number
db	6	1	FRU length field
ascii	00000000	8	3Com is all zeroes
ascii	*SN	3	Serial number
db	6	1	SN length field
ascii	********	8	8 alpha-numeric character for 3com serial number.
ascii	*MF	3	Manufacturer's number
db	5	1	MF length field
ascii	000001	6	assembly location 00=PCAO 01=Solectron
ascii	*DT	3	Date code
db	5	1	Date code lenght
ascii	xxxxxx	6	yr-mo-day (ie 910131)

```
ascii           *CR                     3       copyright
db               12                     1       copyright length
ascii   "Copyright 3Com Corp." 20

                                       ----
total                                  156
```