IDT WinChip C6+: The Next Generation

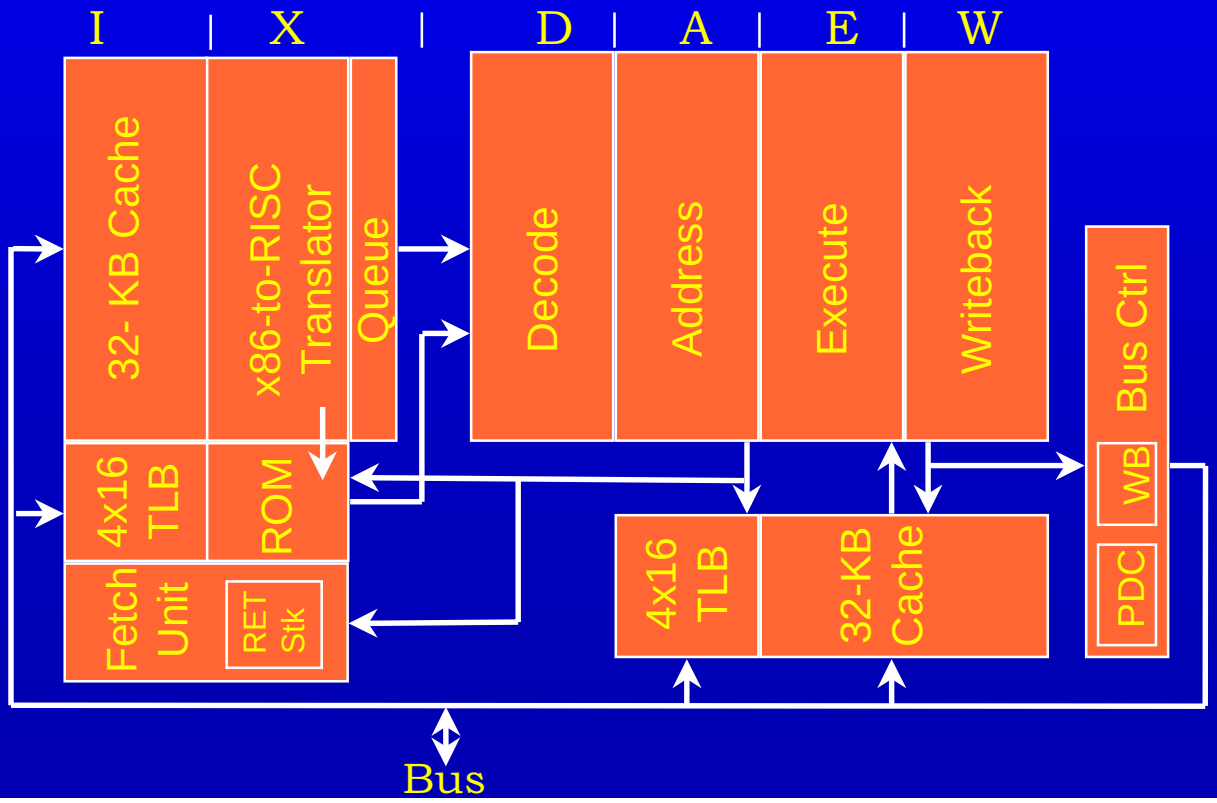
WinChip Background

- Started 4/95 (4 in my kitchen, home PC, etc)
- Designed IDT-C6 Processor (Ann'd 5/97)
  - P55-compatible (Includes MMX™)
  - Optimized for business applications
  - Smallest 0.35µ die (88 mm^2) ➔ lowest cost
  - 8.9 W max power at 200 MHz (3.3V)
- Started Production Shipments In Sept
  - Windows certified, XXCAL Platinum certified
  - 4 BIOSes available, 10's qualified boards
  - Targeting tier 3 sub-$1000 PCs
  - Primarily via distribution (HHT, Wyle)
- 180 ($90) & 200 MHz ($135) Shipping Now
  - 225 & 240 Sample In November

MMX is a trademark of Intel Corporation

IDT C6 Architecture

- Simple RISC Pipeline
  - Highly tuned for high MHz & small size
  - Large caches (64 KB), large TLBs, etc.
  - Many non-obvious tricks for x86 (50 patents filed)



Next Generation Goals (C6+™)

- "2x" MMX & FP CPI Improvement
  - For those who care (not everyone)
  - Primary FP focus is 3D graphics
- Some Winstone CPI Improvement
  - Already very competitive
- Same Small Die Size (at same 0.35µ)
  - Exploit our small-size design & methodology
- Support New Technologies
  - 2.5V transistor & 0.25µ shrink
  - Faster MHz, lower cost, less power
- Ship 6 Months After C6
  - Exploit our fast development cycle

IDT C6+ MMX Improvements

- Full MMX Pairing (Superscalar)
  - Dual MMX units ala P55 (1 multiplier, 1 shifter)
  - 2 Instructions decoded, issued & executed per clock
  - Same pairing rules as P55
- Faster MMX Instruction Timing Than P55
  - 1 cycle multiply latency (vs 3) !
  - 1 cycle multiply-add latency (vs 3) !
  - 1 cycle store (vs 2)
- No MMX-Integer Pairing
  - But, larger caches, larger TLBs, etc.
- Result: Better MMX Performance Than P55
  - *Even on biased Intel Media Benchmark!*

IDT C6+ FP Improvements

- Fully Pipelined (Complete Redesign → Same Size)
- Some Instructions Slower Than P55
  - FMUL → 4/2 or 3/1 (SP) (vs 3/1)
  - FXCHG → 1 (vs 1/0)
  - 1 clock penalty on register-memory forms
- Some Instructions Faster Than P55
  - FST → 1 (vs 2-3), FIST, FSTSWAX-SAHF, etc.
- Results: 80-100% P55 FP Performance
  - 80% on biased Intel Media Benchmark (FP)
  - Typically same/faster P55 on real FP applications
- We Intentionally Stopped Here!
  - Silicon better spent on 3D assists/Winstone/etc.

3D Graphics Improvements

- 53 New x86 Instructions (12 x86 opcodes)
  - Designed to speed coord transforms/lighting
  - Addresses 20-50% CPU time in heavy-duty 3D
- 22 Additional FP Registers
- Minimal Die Size Impact (< $1mm^2$)
  - Primarily reuse of existing dataflow
  - New instruction decodes, a few muxes, etc.
- Intended For Distribution In Future MS D3D
  - Working with Microsoft to add our code
  - Automatically selected machine-specific code
  - Transparent to applications & users

3D Graphics Improvements

- Base Instruction Functions (Hdw)
  - 22 additional FP registers (30 total)
  - 1-clock multiply-accumulate
  - 1-clock load of 2 single-precision (SP) values
  - 1-clock compare & set bit flags
  - Fast SP inverse square root, square root, divide
  - 1-clock convert to/from integer
  - Fast & flexible moves to/from integer registers
  - Individual instruction control of precision
- Microcode Instructions For Future Speedups
  - Multiple clocks initially → single clock in future
  - 2x & 4x multiply-accumulates
  - Store 2 single-precision values at once

3D Graphics Improvements

Results (SP data)

	Best P55 [1]	*C6+* [2]
[x y z] Transform (12 values)	34	14 clks
$1/\sqrt{x^2+y^2+z^2}$	125 (hw) ≈80 (sw)	29
[x y z] Edge Detect (6)	37	8
Total	196	51

- etc.

Notes

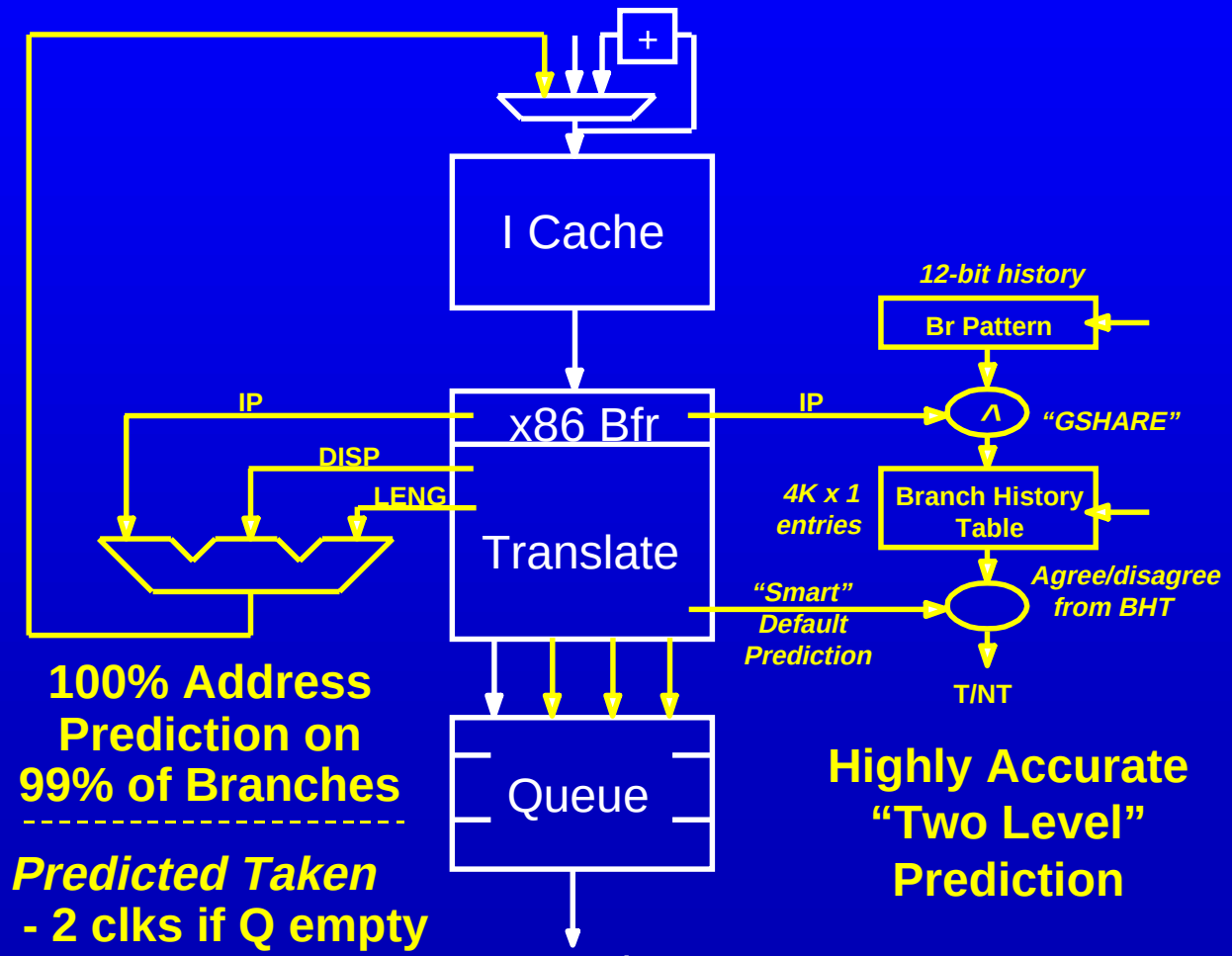
1. Highly optimized low-level assembler code for P55. Much better than any real code that we have found in programs/benchmarks.

2. Highly optimized low-level assembler code for IDT C6+.

IDT C6+ Integer Improvements

- Many Misc Improvements
  - Multiply → 6 (vs 10 for P55)
  - Load-ALU-Store → 2 (vs 3 for P55)
  - No penalty for 0F prefixes
  - Reduced AGIs, no penalty on base+index, etc.
- Limited Instruction Pairing
  - PUSH-PUSH, POP-POP
  - Pairs executed in same clock
- Generate Up to 4 Micro Instructions per Clock
  - Helps fill queue faster → key to branch prediction
- Great Branch Prediction
  - Better performance & much smaller than P55

IDT C6+ Branch Prediction



100% Address Prediction on 99% of Branches

Predicted Taken
- **2 clks if Q empty**
- **else 1 clk (85%)**

Predicted Not Taken
- **1 clock**

Highly Accurate "Two Level" Prediction

IDT C6+ Branch Prediction

	P55	*C6*
BTB/BHT Bits	34 Kb	4 Kb
Correctly Predicted Branch	1	1-2 clks (1.1 avg)
Mispredict Time	5-6	4 clks
Predict Rates		
- Norton SI32	77%	89%
- Winstone Business	82%	93%
Avg Branch Clocks		
- Norton SI32	2.03	1.41
- Winstone Business	1.81	1.30

System Perf Improvements

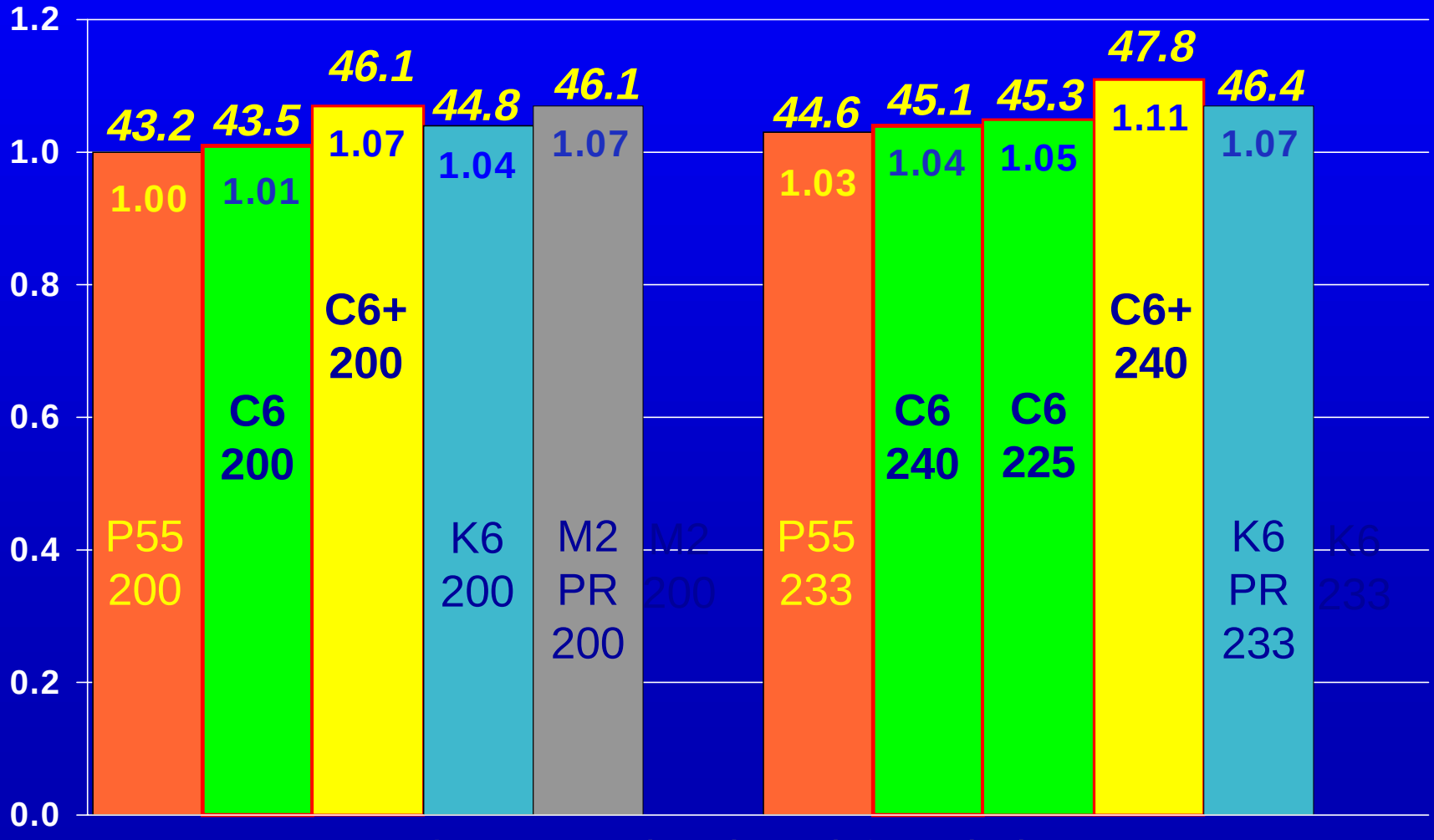
- 4-way D-Cache (vs. current 2-way)
- Write Allocate (optional)
- Weak Read Ordering (optional)
- Plus Branch Prediction, etc.

Results

- 6% Faster Winstone 97 Business (Win95)
  - As fast as anyone at same MHz (P55, K6, M2)

Business Performance

Low-end commodity desktop (TX, 512 KB, 32-MB EDO, S3 Virge)



Winstone97 (Business) for Windows 95

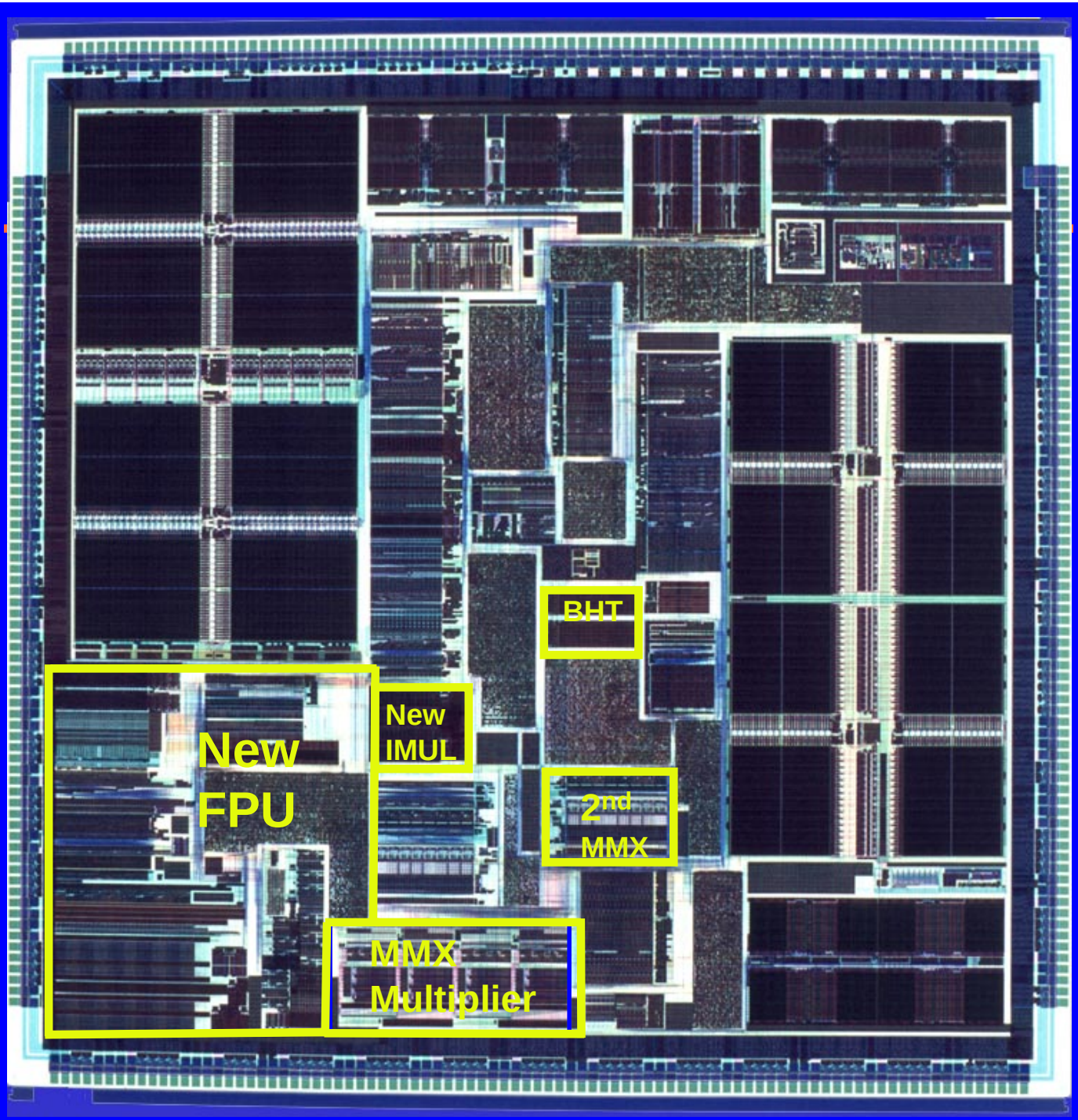
IDT C6+ Summary

- 2x C6 MMX CPI Performance
  - Better Than P55 MMX (on its own benchmark)!
- 2x C6 FP CPI Performance
  - Worst-case 80% of P55 (biased Intel Media BM)
- 2-4x P55 CPI on Specific 3D Graphics Kernels
  - Will be transparently available via MS D3D
- 6% Winstone CPI Improvement
  - As good as any other socket 7 at same MHz
- Support For New Technology (Split Voltage)
- 91 mm^2 vs. 88 for Current C6 (both 0.35μ)

IDT C6+ Summary

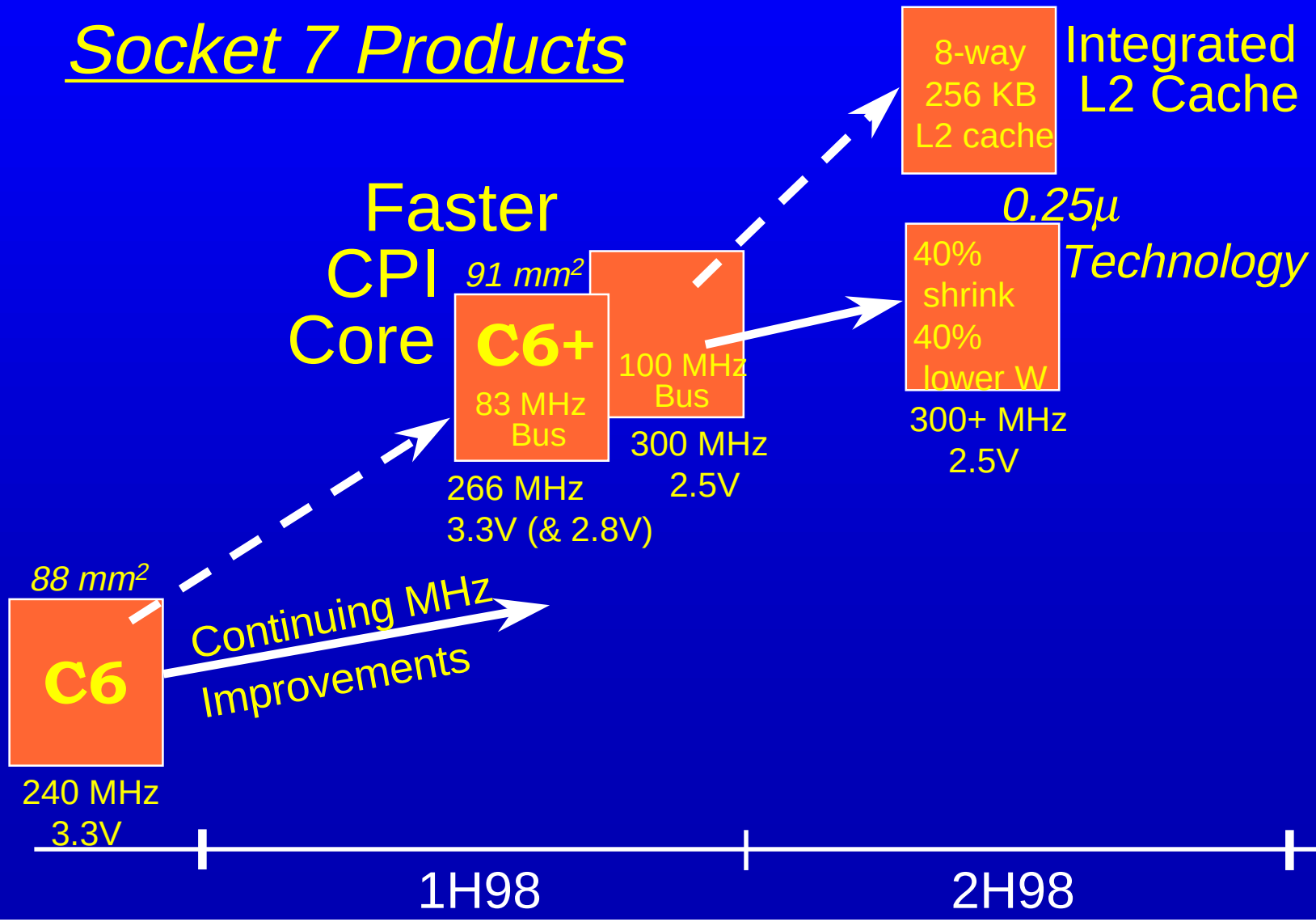
- Production Tapeout 11/15
- Target Shipments 2Q98
  - Samples 1Q98
- Two Technology Options
  - 3.3V core
    - Up to 266 MHz
    - Split V core allows reduced power & MHz
  - 2.5V core
    - 300 MHz at first ship
    - 40% lower power (at same MHz)
    - 3 months after 3.3V version

C6+ Die



WinChip '98 Roadmap

Socket 7 Products



.25μ
C6