Introduction to the IBM 6x86L Microprocessor

Application Note

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Revision Summary: This is the initial release of this Application Note.

Introduction

This application note is addressed to system and system board designers as well as to Field Application Engineers (FAEs) and any one responsible for using an IBM 6x86L microprocessor[1] in their system designs. This note is intended to provide technical details about the IBM 6x86L CPU and the differences between the IBM 6x86 processor and the IBM 6x86L processor.

Split-rail Power Supply Design

The IBM 6x86L CPU takes advantage of split-rail technology. The CPU's voltage inputs are separated into two categories:

1) The CPU core voltage and
2) The CPU I/O voltage.

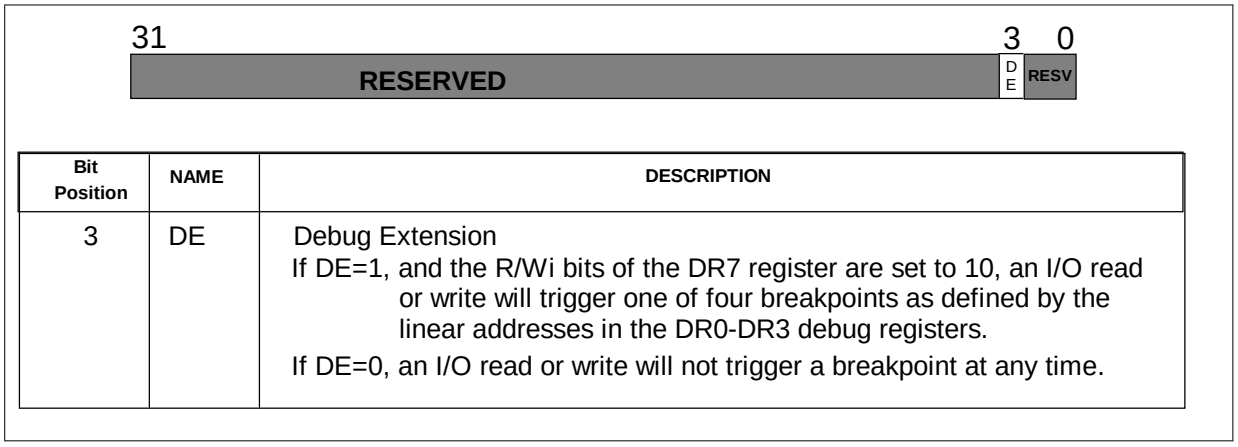
The core voltage is 2.8V +/- 170mV and the corresponding module pins are labeled $V_{CC}2$. The core voltage refers to the power to the main (core) logic on the CPU. The I/O voltage is 3.3V +/-150mV and the corresponding module pins are labeled $V_{CC}3$. The I/O voltage refers to the power only to the Input/Output transceivers for the CPU module I/O pins.

This split-rail design allows for an overall reduced power consumption for the CPU and provides for an easier system thermal solution.

6x86L Architecture - The CR4 Register

The IBM 6x86L processor architecture originates from the architecture of the IBM 6x86 CPU. Therefore, the architectural features of the IBM 6x86 processor, as well as the usage of these features, are also found in the IBM 6x86L processor.

There is one new register that was added in the IBM 6x86L CPU which is not in the IBM 6x86 microprocessor. This is the CR4 register and is used for debug purposes only. The register bit settings and descriptions are outlined below:



Bit Position	NAME	DESCRIPTION
3	DE	Debug Extension If DE=1, and the R/Wi bits of the DR7 register are set to 10, an I/O read or write will trigger one of four breakpoints as defined by the linear addresses in the DR0-DR3 debug registers. If DE=0, an I/O read or write will not trigger a breakpoint at any time.

Figure 1. Register C4 Bit Setting and Description

[1] The IBM 6x86 and IBM 6x86L processors are designed by Cyrix, Corp. and manufactured by IBM Microelectronics

Instruction Set - The CMPXCHG8B Instruction

The IBM 6x86L CPU's instruction set, like that of the IBM 6x86 CPU, is fully compatible with the 486 processor instruction set. One additional instruction has been added to the microcode for the IBM 6x86L microprocessor. This is the Compare and Exchange 8 Bytes instruction (the mnemonic is CMPXCHG8B).

This instruction will compare the 64-bit value which is in the EDX:EAX register pair with the r/m quad-word (a 64-bit memory Destination) within 13 clock counts. If the values are equal, the ZF (bit 6 in the EFLAGS register) will be set to a logic '1' and the ECX:EBX register pair will be loaded into the r/m quad-word memory destination. If the register pair value and the 64-bit memory destination value are not equal, then the ZF will be cleared to a logic '0' and the 64-bit memory destination value will be loaded into the EDX:EAX register pair.

The CMPXCHG8B instruction op-code is: 0F C7 [mod 001 r/m]

CPU Identification

As with the IBM 6x86 processor, device identification for the IBM 6x86L processor is performed by indexing the DIR0 and DIR1 registers. The following table illustrates the values which will be found in these registers for both processors:

DEVICE	DIR0	DIR1*
IBM 6x86	31h	0xh or 1xh
IBM 6x86L		2xh

*x represents any hex number

Table 1. Device Identification

Signal Pins - The VCC2DET Pin

The following list of IBM 6x86 processor signals are NOT supported by the IBM 6x86L CPU and have been removed from the PGA pinout diagrams:

- DHOLD (pin S35)
- BHOLD (pin R34)
- LBA# (pin S5)
- QDUMP# (pin AL7)

This will not affect standard systems operation since these signals were not used on standard PC platforms

For motherboard designers who wish to add circuitry to auto-detect that a split-rail (or dual-voltage) microprocessor has been installed, the V_{CC}2DET output pin (pin AL1) has been added. This pin is internally tied to a V_{SS} (or ground) pin to indicated that a dual voltage power supply is needed for operation.

The following table lists the physical SIGNAL pinout DIFFERENCES Between an IBM 6x86 processor, an IBM 6x86L processor, an Intel** P54C** processor, and an Intel Pentium** processor with MMX Technology CPU:

Pin Number	IBM 6x86	IBM 6x86L	Intel P54C	Intel Pentium Processor with MMX Technology
A37	NC	NC	RESV	RESV
H34	NC	NC	PICCLK	PICCLK
J33	RESV	NC	PICD0	PICD0
L35	NC	NC	PICD1	PICD1
P4	NC	NC	IERR#	IERR#
Q3	RESV	RESV	PM0BP0	PM0BP0
Q35	NC	NC	CPUTYP	CPUTYP
R4	RESV	RESV	PM1BP1	PM1BP1
R34	BHOLD	NC	RESV	RESV
S3	RESV	RESV	BP2	BP2
S5	LBA#	NC	BP3	BP3
S35	DHOLD	RESV	RESV	RESV
V34	SUSP#	SUSP#	STPCLK#	STPCLK#
W33	SUSPA#	SUSPA#	RESV	RESV
X34	RESV	RESV	BF1	BF1
Y33	CLKMUL	CLKMUL	BF0	BF0
Y35	RESV	RESV	FRCMC#	RESV
Z34	NC	NC	PEN#	PEN#
AA3	RESV	NC	PHIT#	PHIT#
AA33	WM_RST	WM_RST	INIT	INIT
AC3	RESV	NC	PHITM#	PHITM#
AC5	NC	NC	PRDY	PRDY
AC35	NC	NC	R/S#	R/S#
AD4	NC	NC	PBGNT#	PBGNT#
AE3	NC	NC	PBREQ#	PBREQ#
AL1	NC	Vcc2DET	NC	Vcc2DET
AL7	QDUMP#	NC	BUSCHK#	BUSCHK#
AL19	RESV	NC	RESV	RESV

NOTE: NC means internally the pin is Not Connected to the chip die (Intel uses term INC) and
RESV means the pin is Reserved and should not be connected to any circuitry (Intel uses term NC)

Table 2. Signal Pinout Differences

Vcc2 Pins (2.8V)

A7	A9	A11	A13	A15	A17	G1	J1	L1	N1	Q1	S1	U1
W1	Y1	AA1	AC1	AE1	AG1	AN9	AN11	AN13	AN15	AN17	AN19	

Vcc3 Pins (3.3V)

A19	A21	A23	A25	A27	A29	E37	G37	J37	L33	L37	N37	Q37	S37
T34	U33	U37	W37	Y37	AA37	AC37	AE37	AG37	AN21	AN23	AN25	AN27	AN29

Clock Multiplier

The definitions of pins X34 and Y33 differ among the Intel parts and the IBM parts. The following table defines these clock multiplier pins and their corresponding internal CPU clock multiplication:

Pin X34	Pin Y33	IBM 6x86 processor	IBM 6x86L processor	Intel P54C processor	Intel Pentium processor w/ MMX Technology
0	0	2x	2x	2.5x	2.5x
0	1	3x	3x	3x	3x
1	0	2x	2x	2x	2x
1	1	3x	3x	1.5x	Reserved

Table 3. Comparisons of Clock Multiplier Pins

References

1. The IBM 6x86L Microprocessor Databook Addendum
2. The IBM 6x86 Microprocessor Databook
3. Intel Pentium Processor with MMX Technology, Intel Corp., 1997
4. Intel Pentium Processor Family Developer's Manual, Intel Corp., 1995
