Proper Decoupling Solutions for the IBM 6x86 and 6x86L Microprocessors

IBM®

Application Note

Revision Summary: This is the initial release of this Application Note.

Introduction

The IBM 6x86 and 6x86L microprocessors deliver more performance than comparable microprocessors, but as a result, often draw more current and dissipates more power in active mode as well. As a result, some precautions need to be taken to ensure proper operation of the IBM 6x86 and 6x86L microprocessor. In particular, there is a need for using proper decoupling techniques with the power source. There are two types of decoupling techniques which are used in maintaining the best system performance.

Low Frequency Decoupling Techniques

The first technique is Low Frequency decoupling which is commonly referred to as Bulk Decoupling. The purpose of this technique is provide energy storage capacity for the processor during prolonged transients which the power source is unable to meet due to it's transient response time. Power sources vary widely in their response to transients from the processor. Typically the response time of most power sources range from 1 to 100µs.

Power plane and power trace inductance to the processor must be minimized. This inductance impedes the response time if the power source, resulting in more intense voltage spikes during processor switching transients. By placing the decoupling capacitors as close to the processor or load as possible, the inherent inductance in the supply leads is compensated for, resulting in a smoother power supply voltage.

Another very important parameter to be concerned with in choosing capacitors for bulk decoupling is Effective Series Resistance (ESR). High ESR capacitors will drop too much voltage across the capacitor at high currents, adding to the voltage transients. Precautions should be taken to select bulk decoupling capacitors which have low ESR values.

The formula for calculating the required bulk capacitance including ESR is as follows:

$$C = \left({}^{I \times \delta t} / _{\delta V - I \times E} \right)$$

I =	Worst case change in current for the supply
δt =	Response time of the power source to the change in current
δV =	Maximum allowable change in voltage for the load
E =	ESR of all capacitors used in decoupling the power source

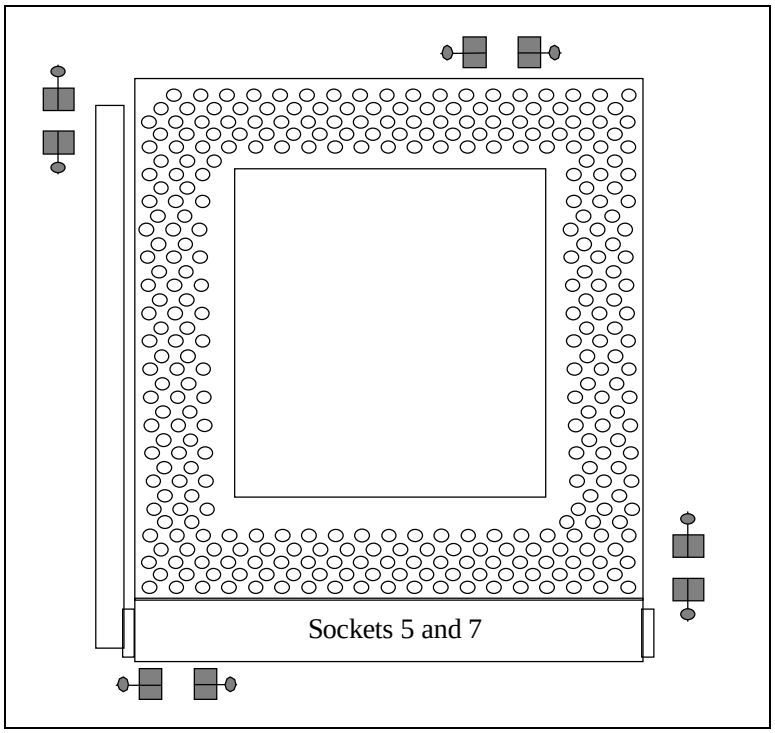

Figure 1. Placement suggestions for bulk decoupling capacitors.

High Frequency Decoupling Techniques

The high frequency technique for decoupling is required to handle transients that are faster than can be handled by the bulk decoupling capacitors. Typically, the high frequency decoupling capacitors are ceramic type devices which have a much lower inductance. These decoupling devices need to be placed as close to the power pins of the processor as is physically possible. It is also critical that the traces from the capacitors go directly to the power and ground planes with leads as short as possible. This will prevent any board inductances from voiding the decoupling effectiveness.

It is recommended that the system board designers use a minimum if 30 high frequency decoupling capacitors. It would be desirable that they be surface mount capacitors and be evenly distributed close to the processor. Suggested values would be 15 0.1µf capacitors and 15 0.01 µf capacitors. This is an additon to the low frequency decoupling capacitors.

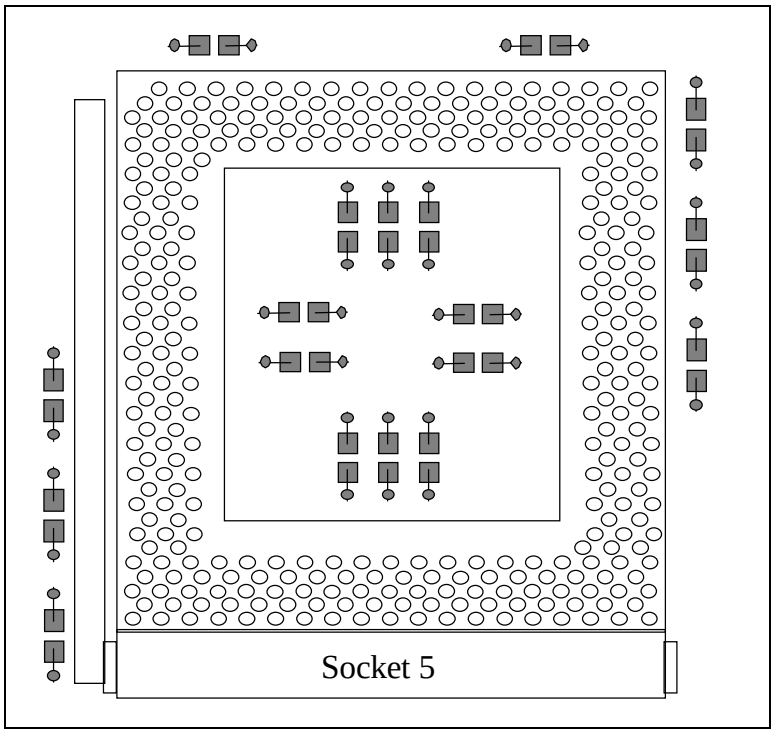

Figure 2. Placement suggestions for high frequency decoupling capacitors for Socket 5.

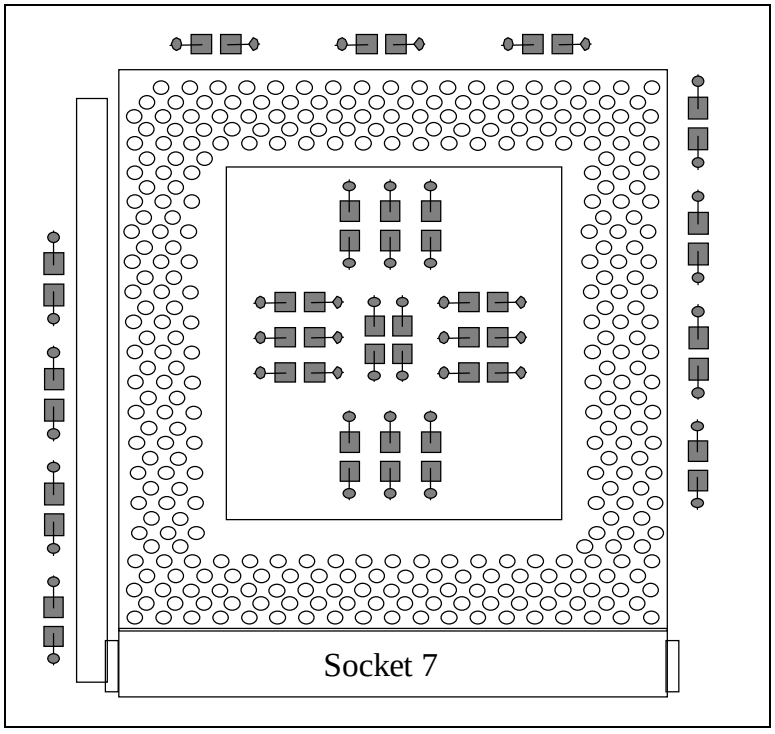

Figure 3. Placement suggestions for high frequency decoupling capacitors for Socket 7.

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