Guide for Adapting lntel Pentium Processor Design for the IBM 6x86 Microprocessor

Application Note

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Revision Summary: This update includes updated information on the Intel** Pentium** clock mode.

Introduction

The IBM 6x86** microprocessor is plug compatible with Intel** Pentium** Socket5 or Socket7 motherboards. This application note describes the differences between single-rail 6x86 and single-rail Pentium processors with respect to pin-outs and pin functions. By "single-rail", the author means processors which use a single power supply (usually 3.3v or 3.5v). "Pentium" refers to Intel processors based upon "P54C" architecture. This application note outlines the steps necessary for the IBM 6x86 processor to "plug and run" in these motherboards. In some cases and for best performance, the IBM 6x86 microprocessor requires changes to BIOS.

The first step in resolving this problem is to understand the areas of similarity between the IBM 6x86 processor and the Intel Pentium processor. Both processors are available in a 296 pin PGA package.[1] The majority of the pins are identical, but approximately 30 pins differ functionally. The principle difference that must be taken into account, when adapting a board designed around the Pentium processor for use with the IBM 6x86 processor, is in the area of processor clocking. The 6x86 processor supports 2X or 3X clock while Intel Pentium supports 2X or 3/2X. Pentium processors rated at 150MHz or higher support 2X, 3/2X, 5/2X and 3X clocking.

Internally the processors are very similar. The physical bus structure, paging operation, and architectural registers are all compatible. The instruction set is compatible with the exception of a few instructions that are described later in this document. However, there are enhanced features on the IBM 6x86 processor that either are not present on the Intel Pentium or are in a different form. These differences account for both the pin-out and pin function differences. The rest of this application note details these differences and then gives a description of how to Plug and Run using the PGA package in a system designed for the Intel Pentium processor.

[1] All data pertaining to the Intel Pentium processors is taken from *Pentium Family User's Manual: Volumes 1 and 3*

Pin and System Function Differences

The differences in the pins between the IBM 6x86 and the Intel Pentium processors can be divided into eight areas: clock mode select, microprocessor support, scatter-gather function, processor initialization, breakpoints and performance monitoring, power management, debug and test pins, and error detection. These individual areas are described in the following sections.

Additionally two software areas are of concern. The first is processor identification which describes the codes found in the IBM 6x86 processor on reset. These codes are, by necessity, different from those of other manufacturers (company id, revision number). The second area is that of optimum performance of the IBM 6x86 processor. These topics are covered in *The IBM 6x86 Microprocessor BIOS Writer's Guide* that is also available as an application note.

Pinout Differences: IBM 6x86 Microprocessor and Intel Pentium processor			
Pin #	**IBM 6x86 Microprocessor**	**Intel Pentium Microprocessor**	**Description (I/O)**
H34	NC	PICCLK	Programmable interrupt controller clock (I)
J33	R	PICD0/DPEN#	6x86 microprocessor: Reserved Pentium processor: Programmable interrupt controller data bit 0 (I/O) or second socket occupied (I/O)
L35	NC	PICD1/APICEN	Programmable interrupt controller data bit 1 (I/O) or APIC enable (I)
P4	NC	IERR#	Internal error (O)
Q3	R	PM0/BP0	6x86 microprocessor: Performance monitor data bit 1 (O) Pentium processor: Performance monitor data bit 0 or breakpoint match 0 (O)
Q35	NC	CPUTYP	Identifies CPU as primary or dual (I)
R4	R	PM1/BP1	6x86 microprocessor: Performance monitor data bit 1 (O) Pentium processor: Performance monitor data bit 1 or breakpoint match 1 (O)
R34	BHOLD	NC	Byte enable hold (I)
S3	R	BP2	6x86 microprocessor: Performance monitor clock (O) Pentium processor: Breakpoint match 2 (O)
S5	LBA#	BP3	6x86 microprocessor: Local bus access (O) Pentium processor: Breakpoint match 3 (O)
S33	R	NC	6x86 microprocessor: Reserved
S35	DHOLD	NC	Data & parity hold (I)
V34	SUSP#	STPCLK#	6x86 microprocessor: Suspend request (I) Pentium processor: Stop internal clock (I)
W33	SUSPA#	NC	Suspend acknowledge (O)

Pinout Differences: IBM 6x86 Microprocessor and Intel Pentium processor			
Pin #	**IBM 6x86 Microprocessor**	**Intel Pentium Microprocessor**	**Description (I/O)**
W35	R	NC	6x86 microprocessor: Reserved
X34	R	NC/BF1	6x86 microprocessor: Reserved
Y33	CLKMUL	BF/BF0	Core/Bus frequency ratio (I)
Y35	R	FRCMC#	6x86 microprocessor: Reserved Pentium processor: Functional redundancy checking master/checker (I)
Z34	NC	PEN#	Parity enable (I)
AA3	R	PHIT#	6x86 microprocessor: Reserved Pentium processor: Private hit (I/O)
AA33	WM_RST	INIT	Warm reset (I)
AC3	R	PHITM#	6x86 microprocessor: Reserved Pentium processor: Private modified hit (I/O)
AC5	NC	PRDY	Probe ready (O)
AC35	NC	R/S#	Run/stop (I)
AD4	NC	PBGNT#	Private bus grant (I/O)
AE3	NC	PBREQ#	Private bus request (I/O)
AE35	NC	D/P#	Dual/primary indicator (O)
AL7	QDUMP#	BUSCHK#	6x86 microprocessor: Q buffer dump (I) Pentium processor: Bus check (I)
AL19	R	NC	6x86 microprocessor: Reserved
AN35	R	NC	6x86 microprocessor: Reserved

(R=RESERVED, NC=NO CONNECT)

Table 1. List of pinout differences between the two products.

The following sections detail these differences grouped together as functions. The first function we will examine is that of clock mode selection.

Clock Mode Select

IBM 6x86 processor and all Pentium processors sample the clock multiplier pin(s) at RESET. These pin(s) control the frequency of the internal (core) clock with respect to the system clock (CLK), so it is known as the core-to-bus frequency ratio or simply "clock mode". Table 2 summarizes the clock modes supported by the IBM 6x86 and Pentium processors.

Notice that the IBM 6x86 and lower MHZ versions of Intel Pentium use one pin (Y33) to control the clock mode. Also note that the default values are different for these two processors. This is because the 6x86 has an internal pull-down resistor on this pin while Pentium has an internal pull-up resistor. If pin Y33 is driven low, both 6x86 and lower MHz Pentium processors enter

2X clock mode. If Y33 is driven high, the 6x86 enters 3X mode while Pentium enters 3/2X mode.

Pin X34	Pin Y33	Clock Mode		
		IBM 6x86 processor Pin X34: Reserved Pin Y33: CLKMUL	**Pentium (133MHz and lower) Pin X34: NC Pin Y33: BF**	**Pentium (150MHz and higher) Pin X34: BF1 Pin Y33: BF0**
0	0	2X (default)	2X	5/2X
0	1	3X	3/2X (default)	3X
1	0	2X (default)	2X	2X
1	1	3X	3/2X (default)	3/2X (default)

Table 2. Clock mode summaries for the IBM 6x86 and Intel Pentium processors

Higher MHz Pentium processors control the clock mode through two pins (X34 and Y33). The table lists the four possible clock modes for these Pentium processors. The only selection which has the same effect on 6x86 and Pentium is X34=1, Y33=0. This puts the processor in 2X mode.

The common socket or motherboard must provide jumpers on pins X34 and Y33 to allow the user to select the desired clock mode.

Multiprocessor Support Pins

The Pentium processor supports multi-processor implementations within a system design. However, the IBM 6x86 processor does not support this. For this reason an IBM 6x86 processor will not plug and run in a multi-processor system designed under the Intel multi-processor strategy.

Scatter/Gather Interface Pins

The IBM 6x86 microprocessor has a unique bus interface that allows the separate gathering of data that is scattered across multiple memory locations. The Intel Pentium processor does not have this interface. Therefore, installing the IBM 6x86 microprocessor into a board designed for a Pentium processor does not require any action on these pins.

Pin #	IBM 6x86 Processor	Pentium Processor
R34	BHOLD	NC
S5	LBA#	BP3
S35	DHOLD	NC
AL7	QDUMP#	BUSCHK#

Table 3. Scater/Gather Interface Pins

Processor Initialization

The IBM 6x86 microprocessor and Intel Pentium processor are initialized in similar ways. RESET is an active high signal for full initialization, and WM_RST (6x86) or INIT (Pentium) are active high signals for partial initialization.

The RESET sequence is described below. At system power-up, RESET must remain asserted at least 1ms after Vcc and CLK reach their specified AC/DC limits. After power-up, RESET must be asserted 15 CLK cycles to be recognized. Asserting RESET suspends all operations in progress, invalidates internal caches, and clears the write buffers, configuration registers and architected registers. Modified cache lines are not written back. Output signals are driven to their reset value within two CLKs of the rising edge of RESET. The IBM 6x86 microprocessor and the Pentium processor are similar in that outputs and bi-directional signals common to both chips have the same reset state.

Signal Name	Pin	Operation	Processor
FLUSH#	AN7	If 0, tri-state test mode. All outputs except TDO and bidis float until the next RESET.	IBM 6x86 micro-processor and Pentium processor
WM_RST or INIT	AA33	If 1, BIST performed prior to program execution. Takes 2^{19} CLK cycles. Register EAX=0 if all tests pass. If an internal parity error is detected during BIST on Pentium processor, the CPU will assert IERR# (pin P4) and attempt to shutdown.	IBM 6x86 micro-processor and Pentium processor
FRCMC#	Y35	If 0, checker mode. All outputs except IERR# and TDO tri-state. The processor samples the output pins that would normally be driven in master mode. If the sampled value differs from the value computed internally, the processor asserts IERR# to indicate an error. IERR# is not asserted until two CLKs after the ADS# of the first bus cycle.	Pentium processor only
QDUMP#	AL7	If 0, scatter/gather interface enabled.	6x86 microproces-sor only

Table 4. Signals that are sampled when falling edge of RESET determines the mode of operation.

Signal FRCMC# on a Pentium processor is sampled when RESET is active and at the falling edge of RESET to determine whether the processor is configured as a master or checker. The final master/checker configuration is determined at the falling edge of RESET. After the falling edge of RESET, the processor issues the first ADS# to address FFFFFFF0h (150-250 CLK cycles after falling edge of RESET, if built-in self-test (BIST) is not requested, 2^{19} CLKs if, BIST is requested).

Signal FRCMC# is supported by Pentium processors only. The IBM 6x86 microprocessor uses pin Y35 for dual processing, a function that is disabled by the common socket. The common socket keeps the Y35 pin of the CPU connected to the planar, but redundancy checking will only occur when the CPU is a Pentium processor.

Signal QDUMP# is supported by the IBM 6x86 microprocessor only. The Pentium processor uses pin AL7 to signal unsuccessful completion of a bus cycle. The common socket has a jumper to connect pin AL7 to the planar when the CPU is a Pentium processor and disconnect when the CPU is 6x86 microprocessor.

Output signal IERR# is supported by Pentium processors only. Pin P4 is a no-connect on the IBM 6x86 microprocessor. When the CPU is a Pentium processor, the common socket has a jumper that is disconnected; when the CPU is an IBM 6x86 processor, the common socket is connected to Vcc to force IERR# inactive.

WM_RST(IBM 6x86 microprocessor) and INIT(Pentium processor) perform a partial CPU reset. These signals differ from RESET in that the contents of the on-chip cache, write buffers, configuration registers and floating point registers remain unchanged. WM_RST and INIT are located at the same pin and are fully compatible.

Breakpoints and Performance Monitors

Breakpoints

Both the IBM 6x86 microprocessor and Intel Pentium processor allow breakpoints to be programmed through debug registers, but only the Pentium processor has output pins (BP0-BP3) to identify when a breakpoint match occurs. The processors use these pins for different functions, so the common socket must disconnect them from the planar when an IBM 6x86 microprocessor replaces a Pentium processor in a system.

Performance Monitors

The Intel Pentium processor has output pins for monitoring performance, however the IBM 6x86 microprocessor does not support this. Therefore, the common socket must disconnect these pins from the planar.

Power Management

System Management Mode

Both the IBM 6x86 microprocessor and Intel Pentium processors support System Management Mode. Both use the same hardware protocol. The SMI# pin is a falling edge-sensitive input sampled on the rising edge of the processor clock (CLK). When the system asserts SMI#, the processor responds by asserting SMIACT# and enters SMM mode. SMIACT# remains asserted as long as the processor remains in SMM mode. Both processors exit SMM mode via the RSM instruction. The differences are described below, and they are resolved in software by changing the BIOS and SMM subroutine whenever a 6x86 microprocessor replaces a Pentium processor.

The IBM 6x86 microprocessor offers a software interrupt instruction (SMINT) for entering SMM as an alternative to the hardware interrupt but this is not supported by the Pentium processor. The

IBM 6x86 microprocessor controls SMM through configuration registers; the Pentium processor does this by writing to the SMM header. The SMM pins on 6x86 microprocessors must be enabled before use, whereas the Pentium processor always recognizes these pins.

The IBM 6x86 microprocessor processes NMI events during SMM only if the appropriate configuration bit is set; otherwise, it latches one event and processes it after SMM is exited. Pentium processors process NMI events during SMM only if the SMM handler has previously invoked a service routine that issues the IRET instruction. For Pentium processors, if IRET has not been issued during SMM prior to the NMI event, the processor will latch up to one event and service it after exiting SMM.

The IBM 6x86 microprocessor ignores the A20M# pin (no A20 masking) during SMM accesses, write-back cycles and cache inquiry cycles. A Pentium processor recognizes this pin during these conditions, so boards designed for the Pentium processor require external logic to prevent A20 masking under these conditions. This is not a problem for plug and run. A 6x86 microprocessor on a Pentium processor board will have redundant gating of the A20M# pin, both internal and external.

BIOS changes for SMM:
The IBM 6x86 microprocessor configuration bits for SMM are described below. The configuration registers are initialized by BIOS software. They are accessed by writing an 8-bit register index to I/O port 22h followed by an I/O read or write to port 23h. The index numbers are C1h(CCR1), C3h(CCR3) and D2h(ARR3).

CCR1(1)=1	If set, enables SMI# and SMIACT# pins.
CCR1(2)	If set, accesses SMM memory instead of normal memory when not in SMM mode. SMI# input is ignored while this bit is set. Useful for initializing SMM memory.
CCR1(3)	If set, accesses normal memory instead of SMM memory during SMM mode.
CCR1(7)=1	If set, designates Address Region Register 3 for SMM address space.
CCR3(0)=1	If set, prevents modification of CCR1(1:3,7), CCR3(1) and ARR3 except during SMM. Once set, this bit can only be cleared by RESET.
CCR3(1)	If set, NMI is recognized and processed during SMM. This bit should only be set during SMM. If reset, NMI is not processed during SMM. It latches up to one event and processes it after exiting SMM. The Pentium processor uses the IRET instruction to control whether or n ot NMI events are processed during SMM. If IRET is executed during SMM, then NMI events are recognized and processed during SMM. Otherwise, up to one event is latched and processed after SMM is exited.
CCR3(7:4)=Fh	If equals Fh, all configuration registers are accessible. Otherwise, only registers
ARR3(31:0)	Defines SMM address space if CCR1(7)=1.

Table 5. IBM 6x86 microprocessor configuration bits for SMM

The Pentium processor uses bits in the SMM header to change the location of the SMM routine, cause automatic restart of trapped I/O instructions, and control whether SMM interrupts during HALT return to HALT or to the next instruction.

In contrast, the 6x86 microprocessor changes the location of the SMM header and service routine by writing to the ARR3 register. No mechanism exists on 6x86 microprocessors to automatically restart I/O instructions. If an I/O event is trapped, the header contains information on the event, but the SMM routine must contain code that uses the information in the header to force the I/O instruction to restart. On 6x86 microprocessors, there is no way to control whether an SMM exit returns to HALT or the instruction following HALT.

Information stored in SMM header

The 6x86 microprocessor stores the following architected registers in the header upon entering SMM: CS, EIP, next EIP, EFLAGS, CR0, DR7. In addition, the header contains information on I/O instructions.

The Pentium processor saves the following registers in the header: general registers (EAX, EBX, ECX, EDX, ESI, EDI, EBP, ESP), segment registers (CS, SS, DS, ES, FS, GS), EIP, EFLAGS, CR0, CR3, GDT base, IDT base, system segment registers (TR, LDTR), DR6, DR7. In addition, the Pentium processor saves information on I/O instruction restart, return to halt state, SMM revision ID and SMM base address relocation.

Initial register settings upon entering SMM:
The IBM 6x86 microprocessor processor initializes the following registers upon entry into SMM. All other registers have unpredictable values.

CS=SMM base address	EFLAGS=00000002h	DR7=00000400h
EIP=00000000h	CR0=60000010h	

The Pentium processor initializes the following registers upon entry into SMM. All other registers have unpredictable values.

CS=3000h	FS=0000h	CR0 bits 0,2,3,31 cleared;
SS=0000h	GS=0000h	*others unmodified*
DS=0000h	EIP=00008000h	
ES=0000h	EFLAGS=00000002h	DR7=00000400h

Changes to SMM subroutine

Any assumptions made by the SMM routine about the CPU state must be reviewed. Registers not stored in the header must be backed up before modification by the SMM routine, and they must be restored before exiting SMM. Since the IBM 6x86 processor saves a smaller portion of the CPU state to the header and the initial values differ, it is likely that SMM routines written for the Pentium processor will need to be modified slightly to work on the IBM 6x86 processor.

Clock control

Both processors have the ability to stop the internal clock. This is accomplished by asserting the SUSP# pin on the IBM 6x86 microprocessor or the STPCLK# pin on the Pentium processor. These pins are interrupts that cause the processor to stop execution at the next instruction boundary and then stop the internal clock. When using an IBM 6x86 processor in place of a Pentium processor, the BIOS must set CCR2(7) to enable the SUSP# pin.

Debug Control

Both processors have I/O pins for controlling debug. The IBM 6x86 microprocessor uses SUSP# (pin V34) and SUSPA# (pin W33), and the Pentium processor uses R/S# (pin AC35) and PRDY (pin AC5). On the IBM 6x86 processor, SUSP# is an active low input that interrupts the processor, halts execution and then asserts the SUSPA# output. Similarly, on the Pentium processor, R/S# is an active low input that stops execution and causes the PRDY output to go active. The main difference is that SUSPA# is active low and PRDY is active high, so the common socket requires an inverter and jumper to be used when an IBM 6x86 processor replaces a Pentium processor. Also, since the pin numbers are different and the IBM 6x86 processor uses these pins for two purposes (clocking and debug), the common socket must contain logic to gate the control signals into and out of the appropriate processor pins

Error Detection

Signal Name	Pin	Operation	Processor
BUSCHK#	AL7	If 0, system signals to CPU an unsuccessful completion of a bus cycle.	Pentium processor only
PEN#	Z34	If 0, system allows CPU to take a machine check exception if a read data parity error occurs. Sampled with BRDY#.	Pentium processor only
APCHK#	AE5	If 0, CPU detected bad parity on A31-A5 during a cache inquiry cycle. Driven two cycles after ADS# is asserted.	6x86 microprocessor and Pentium processor
PCHK#	AF4	If 0, CPU detected bad parity on D63-D0 during a data read. Driven two cycles after BRDY# is asserted.	6x86 microprocessor and Pentium processor
FERR#	Q5	If 0, CPU detected an unmasked floating point error. Driven every cycle.	6x86 microprocessor and Pentium processor
IGNNE#	AA35	If IGNNE#=0 and NE bit in CR0 is 0, system tells CPU to ignore any pending unmasked floating point errors and continue executing floating point instructions as long as this pin is asserted. Sampled every cycle.	6x86 microprocessor and Pentium processor

Table 6. Signals for Error Detection

Signal BUSCHK# (pin AL7) was discussed in the processor initialization section, and the common socket implementation was described.
Signal PEN# (pin Z34) is supported by Pentium processor only. This pin is a no-connect on the 6x86 microprocessor. The common socket keeps pin Z34 connected to the planar for both processors. It will only have an effect if the CPU is a Pentium processor.

Signal APCHK# works identically for both processors.

Signal PCHK# on 6x86 microprocessors detects read data parity errors, but has no effect on processor execution. Pentium processors handle this differently. On a Pentium processor, if PEN# is active when PCHK# is asserted, the cycle address and type is latched into the MCA and MCT registers and a machine check occurs if the MCE bit in CR4 is set. If PEN# is inactive when PCHK# occurs, the Pentium processor operates just like the 6x86 microprocessor.

Signal FERR# works the same way for both processors.

Signal IGNNE# works the same way for both processors as long as the system asserts it for at least two CLK cycles.

Processor Identification

The CPU is identified in software, usually in BIOS. An Intel Pentium processor is uniquely identified using the CPUID instruction. Under standard conditions, the IBM 6x86 microprocessor does not support the CPUID instruction so it requires a different method for identification.

The following describes how to identify a Pentium processor in a system. Before executing CPUID, the software must ensure that it can set and reset EFLAGS bit 21. The ability to set and reset this bit indicates that the CPUID instruction is supported by the processor. EAX is set to 00000000h and CPUID is executed. If EAX=756E6547h, ECX=6C65746Eh and EDX=49656E69h then the processor is an Intel Pentium processor. Next, EAX is set to 00000001h and the CPUID instruction is executed. After doing this, the value of EAX(3:0) is the stepping ID and EAX(7:4) is the model number.

An IBM 6x86 microprocessor is identified by first detecting the processor vendor as IBM, then reading internal registers DIR0 and DIR1 to determine the processor type as a 6x86 microprocessor. To determine the processor vendor as IBM, check the value of undefined flag bits following the execution of the divide instruction with operands 5 and 2 (5 divided by 2). It is sufficient to clear the EFLAGS register, execute the divide instruction and then check the low byte of the flags register (EFLAGS bits 7:0). If it equals 02h, an IBM processor is detected since the flags are unchanged (note that bit 1 of EFLAGS is hardwired to 1). Otherwise, a non-IBM processor is detected. Once an IBM CPU is detected, the values of DIR0 and DIR1 should be read to determine whether the processor is a 6x86 microprocessor or some other type. These registers are accessed by writing an eight bit register index (FEh for DIR0, FFh for DIR1) to I/O port 22h followed by an I/O read from port 23h. When reading DIR0, the eight bits returned is the device ID. When reading DIR1, the high nibble (bits 7:4) is the stepping ID and the low nibble (bits 3:0) is the revision ID.

Other Differences

Bus State Machine

There is one difference between the bus state machines for IBM 6x86 microprocessors and Pentium processors. For any two consecutive non-pipelined (NA# negated) bus cycles, the Pentium processor inserts an idle cycle between the last data transfer of the first cycle and the ADS# for the second cycle. Referring to the state diagram for the Pentium processor, the processor moves from state T2 to state Ti and then to state T1. In the same situation, a 6x86 microprocessor does not insert an idle cycle. The IBM microprocessor moves from state T2 directly to state T1 for all cycles except a cache inquiry hit on modified data (HITM# asserted). The net effect, under the conditions described above, is that the IBM 6x86 microprocessor and the Pentium processor initiate bus cycles at different rates, so the system (chipset) must be able to operate under different rates of bus cycle initiation.

Misaligned Accesses

The IBM 6x86 microprocessor and the Pentium processor handle misaligned accesses differently. A misaligned access is a non-cacheable memory or I/O cycle that crosses a 32-bit boundary. In this situation, a Pentium processor always issues two bus cycles, with the high address issued first. In this same situation, an IBM 6x86 processor issues only a single bus cycle (with the appropriate byte enables active) if the access is contained within a 64-bit boundary. This difference results in lower bus activity for the IBM 6x86 processor.

If the access crosses a 64-bit boundary, the IBM 6x86 microprocessor issues two bus cycles (same as Pentium processor) **.**

RDMSR and WRMSR Instructions

RDMSR and WRMSR are instructions used by the Pentium processor to access its internal configuration registers. RDMSR and WRMSR are not supported by IBM 6x86 microprocessor. Configuration registers in 6x86 microprocessor are accessed through I/O ports 22h and 23h. Attempts to execute RDMSR or WRMSR on 6x86 microprocessor result in an invalid opcode exception.

INVD Instruction

When IBM 6x86 processor executes INVD, it writes all modified cache data to external memory prior to invalidating the cache, thereby preventing data incoherency. In other words, the INVD and WBINVD instructions perform the same function on the IBM 6x86 processor.

Universal Socket Diagram

Figure 1 on the following page shows a possible board layout that would allow an IBM 6x86 microprocessor and an Intel Pentium processor to be used interchangeably. The jumper settings listed below apply to that diagram.

Jumper Settings

Jumper	IBM 6x86 Processor	Pentium processor
J1	open	1-2
J2	1-2 or 2-3	don't care
J3	1-2	2-3
J4	open	1-2
J5	1-2	2-3
J6	1-2	2-3
J7	1-2	2-3
J8	1-2	2-3
J9	1-2	2-3
J10	1-2	2-3
J11	1-2 or 2-3	don't care
J12	1-2	2-3

Jumper J2 (sets core/bus frequency ratio for 6x86 microprocessor CPU)

J2	Clock Mode
1-2	2x
2-3	3x

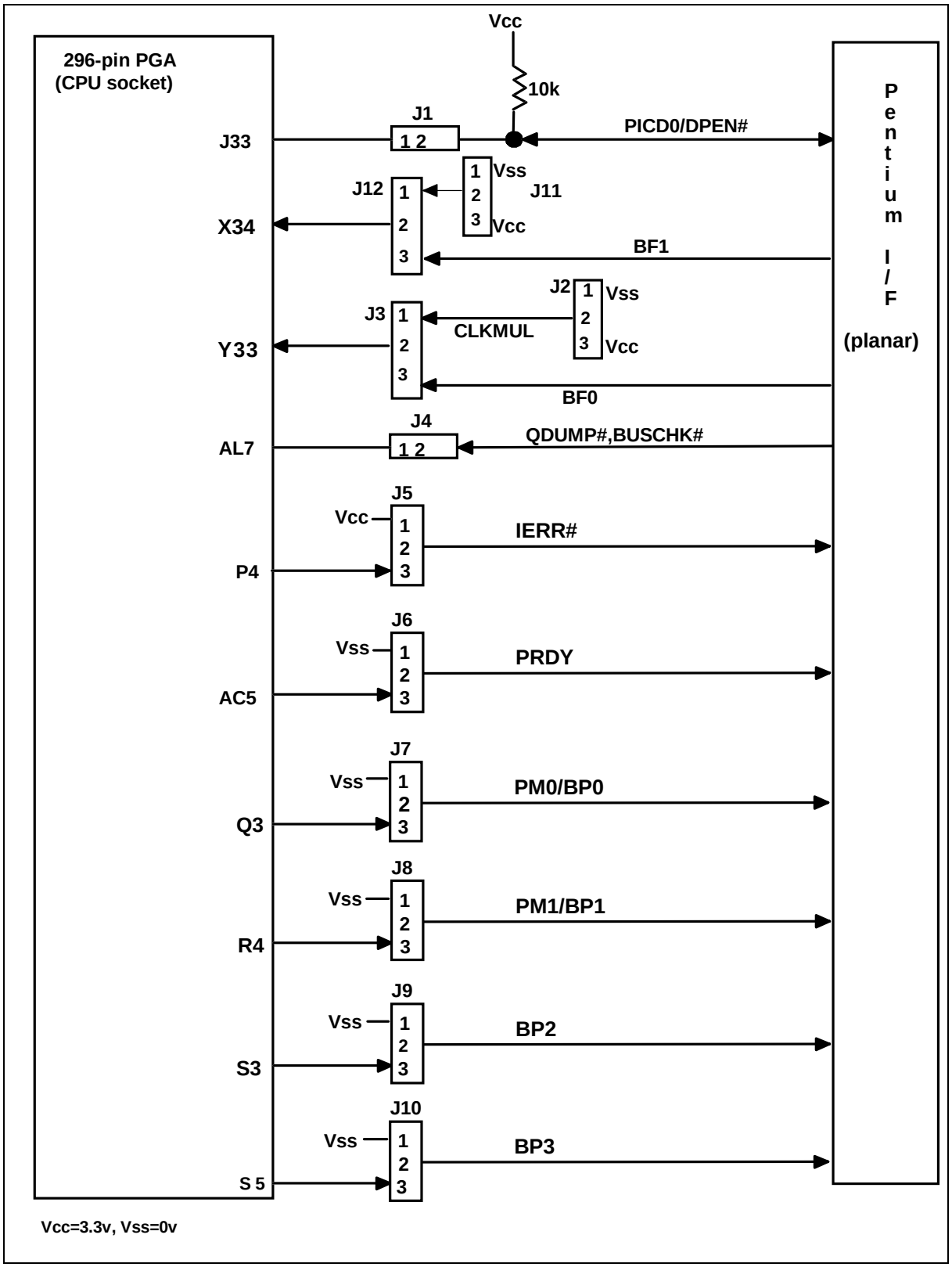

Figure 1. IBM 6x86 Microprocessor/Pentium Processor Common Socket Specification

References

1. *IBM 6x86 Microprocessor Databook*, IBM Microelectronics, 1996.

2. *Pentium Processor Family User's Manual*: Volumes 1 and 3, Intel Corporation, 1994.