IBM 486 DX4 MICROPROCESSORS
486DX4 Style CPUs with 8K Write-Back Cache, On-Chip FPU, and Advanced Power Management

IBM Microelectronics

Addendum to BL486 DX/DX2 Data Book

- **HIGH SPEED OPERATION**
  - 100 MHz with 33 MHz external bus
  - 75 MHz with 25 MHz external bus
  - Pin selectable core/bus clock ratio
  - 8 KByte write-back cache
  - Burst write capability
- **SMALL FOOTPRINT**
  168-pin PGA, 208-pin QFP packages
- **BUILT-IN POWER MANAGEMENT**
  - IBM system management mode with programmable SMM pin interface
  - Low-power suspend mode
  - 3 Volt process technology
  - 5 Volt tolerant I/O

1. Overview

This addendum to the BL486 DX/DX2 Data Book documents product improvements for the IBM 486 DX4 series of IBM CPUs. Specifications in this addendum are valid for the IBM 486 DX4 devices only except where noted.

2. Pin and Configuration Control Register Differences

2.1 Pin Description

The IBM 486 DX4 pin operation and locations are the same except for the pins listed in Tables 2-1 and 2-2. The pin assignments for the PGA and QFP are presented in Section 5 of this addendum.

The IBM 486 DX4 has two new pins, CLKMUL and VOLDET which were not included in the IBM 486DX/DX2. CLKMUL is connected to an internal 20Kohm pull-up resistor.

2.1.1 CLKMUL Pin

Clock Multiplier (CLKMUL) is an input that allows selection of clock doubled (2x) mode or clock tripled (3x) mode. If CLKMUL = 0, 2x mode is selected. If CLKMUL = 1 or not connected (NC), 3x mode is selected.

2.1.2 VOLDET Pin

Voltage Detect (VOLDET) is an output that is permanently driven low by the IBM 486 DX4 to indicate to the system that the CPU requires a 3 V power supply.

Table 2-1. Pinout Differences for 168-Pin PGA Package

Pin Number	IBM 486 DX2-V	IBM 486 DX4
A10	SUSPA#	INVAL
A12	SMI#	HITM#
A13	RPLSET1	SUSPA#
B10	NC	SMI#
B12	NC	RPLSET1
B13	WM_RST	RPLVAL#
B14	NC	RPLSET0
C10	SMADS#	WM_RST
C12	RPLSET0	SMADS#
C13	RPLVAL#	NC
R17	HITM#	CLKMUL
S4	INVAL	VOLDET

Table 2-2. Pinout Differences for 208-Pin QFP Package

Pin Number	IBM 486 DX2-V	IBM 486 DX4
11	NC	CLKMUL

2.2 Configuration Control Register Differences

2.2.1 No_Lock Bit

Note: The following information concerning the No_Lock bit applies to all IBM 486 DX/DX2 devices with stepping identification of 33h or higher, as well as IBM 486 DX4 devices. The Device Identification Register 1 (DIR1) contains the stepping identification value.

If No_Lock (bit 4 in CCR1) is set, locked cycles are inhibited for instructions that are considered as locked instructions by the CPU. These instructions include interrupt acknowledge cycles, descriptor loads, and updates and accesses to the interrupt descriptor table. However, locked cycles are not inhibited by No_Lock bit for TLB table look ups, XCHG instructions to memory, and any instruction that includes a lock prefix.

If No_Lock = 0, locked cycles occur for instructions that are considered as locked instructions by the CPU.

2.2.2 DIR0 Register

The contents of the Device Identification Register 0 (DIR0) are set to values determined by the CLKMUL pin and the device type as shown in Table 2-3. Data in the DIR0 is read only.

Table 2-3. DIR0 Register Contents

DEVICE TYPE	CLKMUL INPUT PIN	DIRO CONTENTS
IBM 486 DX	-	1Ah
IBM 486 DX2	-	1Bh
IBM 486 DX4	0	1Bh
	1	1Fh

3. Electrical Specifications

The electrical specifications listed in this addendum are in addition to the electrical specifications presented in the IBM 486 DX/DX2 Data Book and reference the same notes and drawings.

3.1 Absolute Maximum Ratings

The following table lists absolute maximum ratings for the IBM 486 DX4 microprocessors. Stresses beyond the limits listed in Table 3-1 may cause permanent damage to the device. These are stress ratings only and do not imply that operation under any conditions other than those listed under Table 3-2,"Recommended Operating Conditions" is possible. Exposure to conditions beyond Table 3-1 may (1) reduce device reliability and (2) result in premature failure even when there is no immediately apparent sign of failure.

Table 3-1. IBM 486 DX4 Absolute Maximum Ratings

Case Temperature	-65	+110	˚C	Power Applied
Storage Temperature	-65	+150	˚C	No Bias
Supply Voltage, V_{CC}	-0.5	4.5	V	
Voltage On Any Pin	-0.5	6.0	V	
Input Clamp Current, I_{1K}		10	mA	Power Applied
Output Clamp Current, I_{OK}		25	mA	Power Applied

Note: All voltage values specified in this document are relative to Vss unless otherwise noted.

3.2 Recommended Operating Conditions

Table 3-2 presents the recommended operating conditions for the IBM 486 DX4 device.

Table 3-2. IBM 486 DX4 Recommended Operating Conditions

PARAMETER	PGA		QFP		UNITS	NOTES
	MIN	MAX	MIN	MAX		
T_C Case Temperature	0	+85	0	+90	˚C	Power Applied
V_{CC} Supply Voltage						
75 MHz	3.3	3.6	3.3	3.6	V	With Respect to V_{SS}
100 MHz	3.3	3.6	-	-	V	With Respect to V_{SS}
V_{IH} High Level Input Voltage	2.0	5.5	2.0	5.5	V	
V_{IL} Low Level Input Voltage	-0.3	0.6	-0.3	0.6	V	
I_{OH} Output Current (High)		-1.0		-1.0	mA	$V_{OH}=V_{OH(MIN)}$
I_{OL} Output Current (Low)		3.0		3.0	mA	$V_{OL}=V_{OL(MAX\}}$

3.3 DC Characteristics

Table 3-3. IBM 486 DX4 DC Characteristics (at Recommended Operating Conditions)

PARAMETER	PGA (-GP)		QFP (-QP)		UNITS	NOTES
	MIN	MAX	MIN	MAX		
V_{OL} Output Low Voltage I_{OL} = 3 mA		0.45		0.45	V	
V_{OH} Output High Voltage I_{OH} = -1 mA	2.4		2.4		V	
I_{IL} Input Leakage Current For all pins except those listed in Table 4-1.		15		15	µA	$0 < V_{IN} < V_{CC}$
I_{IH} Input Leakage Current For all pins with internal pull-downs.		200		200	µA	V_{IH} = 2.4 V See Table 4-1.
I_{IL} Input Leakage Current For all pins with internal pull-ups.		-400		-400	µA	V_{IL} = 0.45 V See Table 4-1.
I_{CC} Active I_{CC} 75 MHz 100 MHz	Typical: 600 750	755 920	Typical: 600 -	755 -	mA	Note 1
I_{CCSM} Suspend Mode I_{CC} 75 MHz (3.45V) 100 MHz (3.45V)	Typical: 16 18	20 24	Typical: 16 -	20 -	mA	Note 1, 3
I_{CCSS} Standby I_{CC} 0 MHz (Suspended/CLK Stopped)	Typical: 6	12	Typical: 6	12	mA	Note 4
C_{IN} Input Capacitance		20		20	pF	f = 1 MHz (Note 2)
C_{OUT} Output or I/O Capacitance		20		20	pF	f = 1 MHz (Note 2)
C_{CLK} CLK Capacitance		20		20	pF	f = 1 MHz (Note 2)

Notes:
1. MHz ratings refer to internal clock frequency.
2. Not 100% tested.
3. All inputs at 0.4 or V_{CC} - 0.4 (CMOS levels). All inputs held static except clock and all outputs unloaded (static I_{OUT} = 0 mA) Specification also valid for UP# = 0.
4. All inputs at 0.4 or V_{CC} - 0.4 (CMOS levels). All inputs held static and all outputs unloaded (static I_{OUT} = 0 mA).

3.4 AC Characteristics

Tables 3-5 and 3-6 list the AC characteristics including output delays, input setup requirements, input hold requirements, and output float delays. These measurements are based on the measurement points identified in Figure 4-1 (Page 4-6) and Figure 4-2 (Page 4-6) of the BL486 DX/DX2 Data Book. The reference level for rising clock edge V_{REF} and other reference levels are shown in Table 3-4 below for the IBM 486 DX4. Input or output signals must cross these levels during testing.

Table 3-4. Drive Level and Measurement Points for Switching Characteristics

SYMBOL	IBM 486 DX4	UNITS
V_{REF}	1.5	V
V_{IHD}	2.3	V
V_{ILD}	0	V

Note: Refer to Figure 4-1 of the BL486 DX/DX2 Data Book

Table 3-5. AC Characteristics for IBM 486 DX475
T_{CASE} = 0˚ to 85˚ C, C_L = 50pF
External CLK = 25 MHz (Max.)

SYMBOL	PARAMETERS	MIN (ns)	MAX (ns)	FIGURE	NOTES
T1	CLK Period	40		4-2	
T2	CLK High Time	14		4-2	At 2 V
T3	CLK Low Time	14		4-2	$V_{IL(MAX)}$
T4	CLK Fall Time		4	4-2	2 V to $V_{IL(MAX)}$
T5	CLK Rise Time		4	4-2	$V_{IL(MAX)}$ to 2 V
T6	A31-A2, ADS#, BE3#-BE0#, BREQ, D/C#, HLDA, FERR#, LOCK#, M/IO#, PCD, PWT, W/R# Valid Delay	2	19	4-6	
T6a	SMADS#, SMI# Valid Delay	2	19	4-6	
T7	A31-A2, ADS#, BE3#-BE0#, BREQ, D/C#, HLDA, LOCK#, M/IO#, PCD, PWT, W/R# Float Delay		28	4-7	Note 1
T7a	SMADS#, SMI# Float Delay		28	4-7	Note 1
T8	PCHK# Valid Delay	3	24	4-5	
T8a	BLAST#, PLOCK# Valid Delay	2	24	4-6	
T8b	HITM#, RPLSET(1-0), RPLVAL#, SUSPA# Valid Delay	2	24	4-6	
T9	BLAST#, PLOCK# Float Delay		28	4-7	Note 1
T9a	RPLSET(1-0), RPLVAL# Float Delay		28	4-7	Note 1
T10	D31-D0, DP3-DP0 Write Data Valid Delay	2	20	4-6	
T11	D31-D0, DP3-DP0 Write Data Float Delay		28	4-7	Note 1
T12	EADS# Setup Time	8		4-3	
T12a	INVAL Setup Time	8		4-3	
T13	EADS# Hold Time	3		4-3	
T13a	INVAL Hold Time	3		4-3	
T14	BS16#, BS8#, KEN# Setup Time	8		4-3	
T15	BS16#, BS8#, KEN# Hold Time	3		4-3	
T16	BRDY#, RDY# Setup Time	8		4-4	
T17	BRDY#, RDY# Hold Time	3		4-4	
T18	AHOLD, HOLD Setup Time	10		4-3	
T18a	BOFF# Setup Time	10		4-3	
T19	AHOLD, BOFF#, HOLD Hold Time	3		4-3	
T20	A20M#, FLUSH#, IGNNE#, INTR, NMI, RESET Setup Time	10		4-3	
T20a	SMI#, SUSP#, WM_RST Setup Time	10		4-3	
T21	A20M#, FLUSH#, INTR, IGNNE#, NMI, RESET Hold Time	3		4-3	
T21a	SMI#, SUSP#, WM_RST Hold Time	3		4-3	
T22	A31-A4, D31-D0, DP3-DP0 Read Setup Time	6		4-3, 4-4	
T23	A31-A4, D31-D0, DP3-DP0 Read Hold Time	3		4-3, 4-4	

Note 1: Not 100% tested.

Table 3-6. AC Characteristics for IBM 486 DX4100
T_{CASE} = 0˚ to 85˚ C, C_L = 50pF
External CLK = 33 MHz (Max.)

SYMBOL	PARAMETERS	MIN (ns)	MAX (ns)	FIGURE	NOTES
T1	CLK Period	30		4-2	
T2	CLK High Time	11		4-2	At 2 V
T3	CLK Low Time	11		4-2	$V_{IL(MAX)}$
T4	CLK Fall Time		3	4-2	2 V to $V_{IL(MAX)}$
T5	CLK Rise Time		3	4-2	$V_{IL(MAX)}$ to 2 V
T6	A31-A2, ADS#, BE3#-BE0#, BREQ, D/C#, FERR#, HLDA, LOCK#, M/IO#, PCD, PWT, W/R# Valid Delay	2	16	4-6	
T6a	SMADS#, SMI# Valid Delay	2	16	4-6	
T7	A31-A2, ADS#, BE3#-BE0#, BREQ, D/C#, HLDA, LOCK#, M/IO#, PCD, PWT, W/R# Float Delay		20	4-7	Note 1
T7a	SMADS#, SMI# Float Delay		20	4-7	Note 1
T8	PCHK# Valid Delay	3	22	4-5	
T8a	BLAST#, PLOCK# Valid Delay	2	20	4-6	
T8b	HITM#, RPLSET(1-0), RPLVAL#, SUSPA# Valid Delay	2	20	4-6	
T9	BLAST#, PLOCK# Float Delay		20	4-7	Note 1
T9a	RPLSET(1-0), RPLVAL# Float Delay		20	4-7	Note 1
T10	D31-D0, DP3-DP0 Write Data Valid Delay	2	18	4-6	
T11	D31-D0, DP3-DP0 Write Data Float Delay		20	4-7	Note 1
T12	EADS# Setup Time	6		4-3	
T12a	INVAL Setup Time	6		4-3	
T13	EADS# Hold Time	3		4-3	
T13a	INVAL Hold Time	3		4-3	
T14	BS16#, BS8#, KEN# Setup Time	6		4-3	
T15	BS16#, BS8#, KEN# Hold Time	3		4-3	
T16	BRDY#, RDY# Setup Time	6		4-4	
T17	BRDY#, RDY# Hold Time	3		4-4	
T18	AHOLD, HOLD Setup Time	6		4-3	
T18a	BOFF# Setup Time	9		4-3	
T19	AHOLD, BOFF#, HOLD Hold Time	3		4-3	
T20	A20M#, FLUSH#, IGNNE#, INTR, NMI, RESET Setup Time	6		4-3	
T20a	SMI#, SUSP#, WM_RST Setup Time	6		4-3	
T21	A20M#, FLUSH#, IGNNE#, INTR, NMI, RESET Hold Time	3		4-3	
T21a	SMI#, SUSP#, WM_RST Hold Time	3		4-3	
T22	A31-A4, D31-D0, DP3-DP0 Read Setup Time	6		4-3, 4-4	
T23	A31-A4, D31-D0, DP3-DP0 Read Hold Time	3		4-3, 4-4	

Note 1: Not 100% tested.

4. Programmable SMM Pin Interface

Following power-up or RESET, the IBM 486 DX4 SMM interface pins are disabled. Once enabled, these two pins can either function as defined in the IBM 486 DX/DX2 data book (SMI# and SMADS#) or can be programmed to function with a signalling protocol compatible with the 486 SL-enhanced CPUs (SMI#, SMIACT#). This section describes the operation of the SMM interface pins when operating in the SL-compatible mode.

4.1 SMM Mode Control Bit

Configuration register CCR3 bit 3 (SMM_Mode) controls the SMM interface mode. 0=IBM mode, 1=SL-compatible mode, and the default state is 0. If the SMI_Lock bit=0, SMM_Mode may be modified. If the SMI_Lock bit is set, the SMM_Mode bit can no longer be modified. Once the SMI_Lock bit is set, the CPU must be reset (RESET pin) in order to modify SMI_Lock and SMM_Mode.

4.2 Pin Definitions and Timing

The two pins that change function in SL-compatible mode are SMI# and SMADS#. Table 4-1 lists the pin definitions for these two pins. Figure 4-1 illustrates the required timing for the SMI# and SMIACT# signals.

Table 4-1. SMM Pin Definitions

IBM MODE	SL-COMPATIBLE MODE
SMI#: Bidirectional System Management Interrupt pin. Asserted by the system logic to request an SMI interrupt. Sampled by the CPU on each rising clock edge. Causes I/O trap to occur if sampled and found asserted at least two clocks prior to ready sampled asserted for an I/O cycle. Asserted by the CPU during execution of an SMI service routine or in response to SMINT if SMAC is set.	SMI#: System Management Interrupt input pin. Asserted by the system logic to request an SMI interrupt. Sampled by the CPU on each rising clock edge. SMI# is falling edge sensitive and causes an I/O trap to occur if sampled and found asserted at least three clocks prior to RDY#/BRDY# sampled asserted for any I/O cycle.
SMADS#: SMI Address Strobe output used to indicate that the current bus cycle is an SMM memory access.	SMIACT#: SMI Active output asserted by the CPU during execution of an SMI service routine.

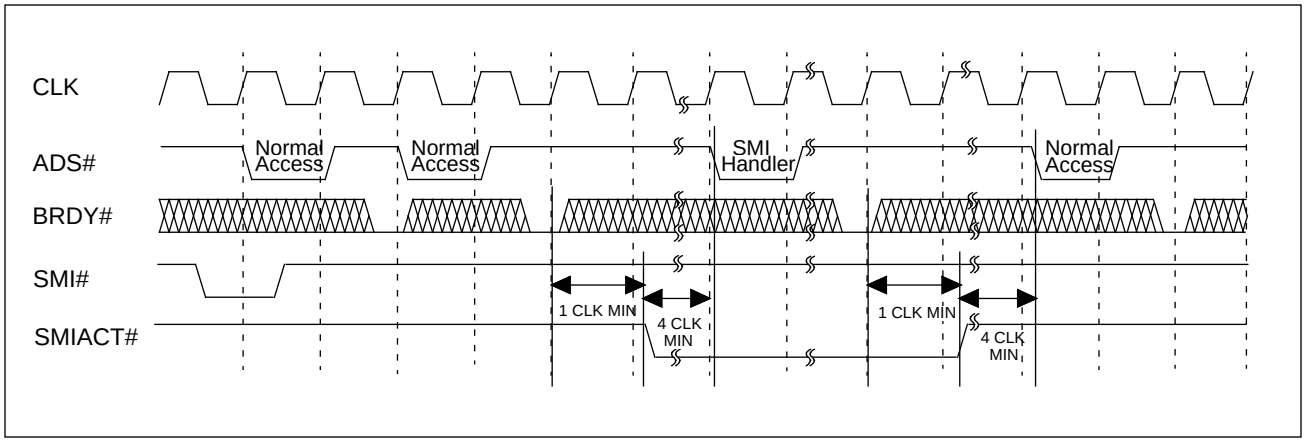


Figure 4-1. SMIACT# Timing

Note 1. SMIACT# is asserted a minimum of one clock after completion of the last normal access.
SMIACT# is asserted a minimum of four clocks prior to asserting ADS# to start the SMM state save.
Note 2. SMIACT# is negated a minimum of one clock after completion of the last SMM access of the state restore.
SMIACT# is negated a minimum of four clocks prior to asserting ADS# for the first normal access following the SMM state restore.

4.3 Nested SMI

In IBM compatible SMM mode, nested SMI's cannot occur due to the fact that the SMI# pin becomes an output during SMI servicing. In SL-compatible mode, if an SMI occurs during an SMI service routine, one and only one SMI# is latched. The latched SMI# is then serviced *immediately* following execution of a RSM instruction (used to exit the original SMI service routine).

4.4 IBM SMM Features Not Used with SL-Compatible Interface

The SMAC and MMAC functions are disabled when in SL-compatible mode. Additionally, SMIACT# remains asserted while executing an SMI service routine regardless of the address being accessed. In other words, if the SMI service routine accesses memory outside the defined SMM memory space, SMIACT# remains asserted. Also, the SMINT instruction should not be used in SL-compatible mode.

4.5 Write-Back Caching and SMM

486 SL-enhanced CPUs allow caching of SMM memory accesses. The SMM memory caching may cause coherency problems in systems where SMM memory space and normal memory space overlap. Therefore, Intel recommends one of following options: (1) flush the cache when entering and exiting an SMI service routine, or (2) flush the cache when entering an SMI service routine and then make all SMM accesses non-cacheable using the KEN# pin.

In either case, Intel recommends asserting the FLUSH# input pin when the SMIACT# pin is asserted[1]. Asserting FLUSH# in this manner is acceptable for a CPU with a write-through cache as the flush invalidates the cache in a single clock.

However, on CPUs with write-back cache, asserting FLUSH# requires the writing of all dirty data to external memory prior to invalidating the cache contents. Bus cycles that address normal memory addresses that overlap with SMM memory space should not be issued while SMIACT# is asserted.

Therefore, while in SL-compatible mode, the IBM CPU automatically writes all dirty data to memory and then invalidates the cache prior to asserting SMIACT#. This guarantees that no dirty data exists in the CPU at the time that SMIACT# is asserted.

SMM accesses are always non-cacheable on IBM CPUs, and the cache is flushed before entering the SMI service routine. For these reasons, a bus snoop that occurs while SMIACT# is asserted cannot hit on a dirty line that is in SMM space or the overlapped normal memory space. Therefore, bus snoops that occur, while SMIACT# is asserted, do not result in memory incoherences.

1. This statement is taken directly from the "Cx486DX4™ -V MICROPROCESSORS Addendum to the Cx486DX/DX2 Data Book" published by Cyrix Corporation.

5. MECHANICAL SPECIFICATIONS

5.1 168-Pin PGA Package (Intel DX4-like Pinout)

The pin assignments for the IBM 486 DX4 168-pin Pin Grid Array (PGA) package (Intel-like pinout) are shown in Figures 5-1. The pins are listed by signal name and pin number in Tables 5-1 and 5-2.

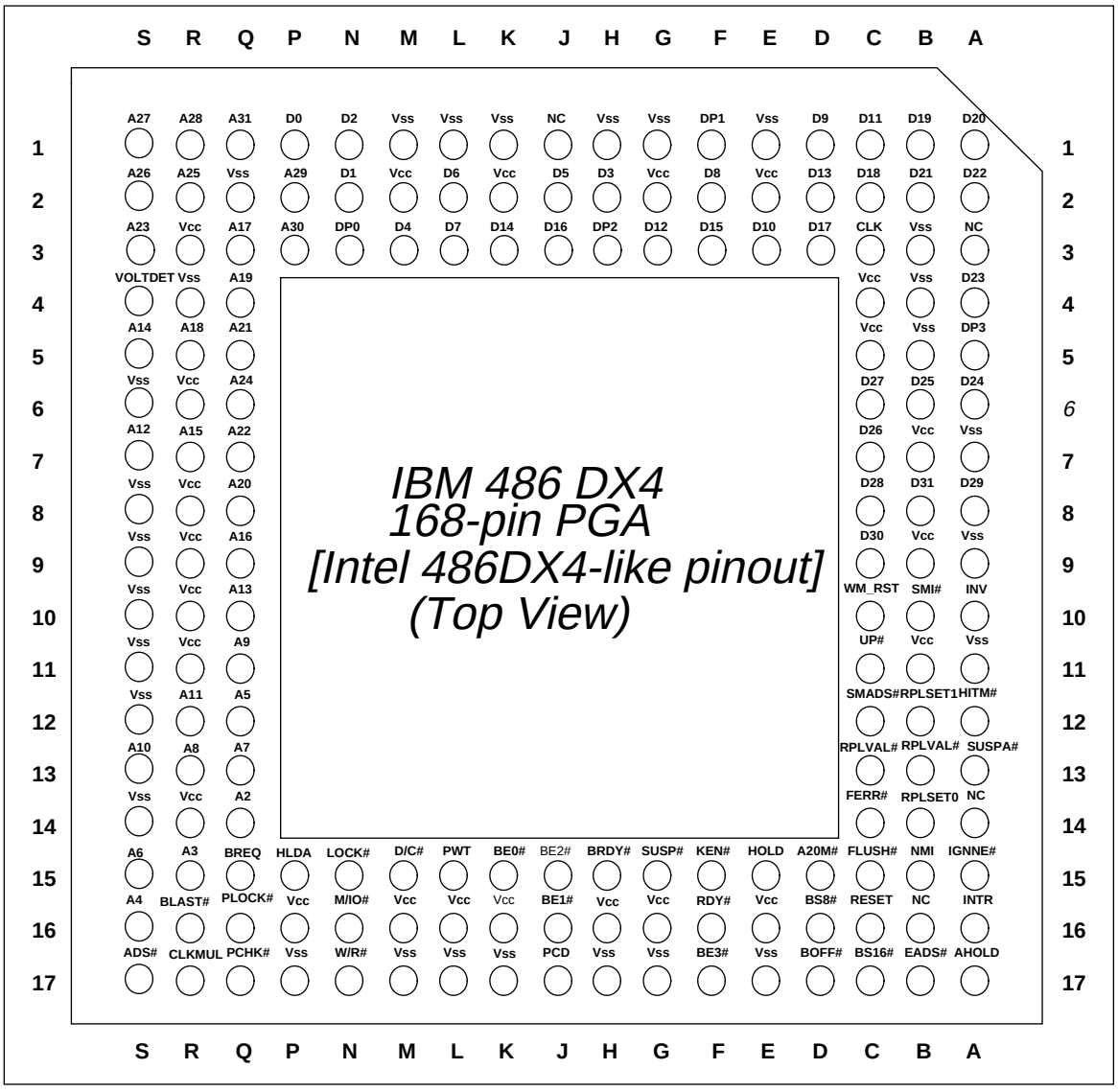


Figure 5-1. 168-Pin PGA Package Pin Assignments [Intel DX4-like Pinout] (Top View)

Table 5-1. 168-Pin PGA Package (Intel DX4-like Pinout) Pin Numbers Sorted by Signal Name

Signal	Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal	Pin
A2	Q14	A29	P2	D10	E3	FLUSH#	C15	SUSPA#	A13	VSS	A11
A3	R15	A30	P3	D11	C1	HITM#	A12	UP#	C11	VSS	B3
A4	S16	A31	Q1	D12	G3	HLDA	P15	VCC	B7	VSS	B4
A5	Q12	ADS#	S17	D13	D2	HOLD	E15	VCC	B9	VSS	B5
A6	S15	AHOLD	A17	D14	K3	IGNNE#	A15	VCC	B11	VSS	E1
A7	Q13	BE0#	K15	D15	F3	INTR	A16	VCC	C4	VSS	E17
A8	R13	BE1#	J16	D16	J3	INVAL	A10	VCC	C5	VSS	G1
A9	Q11	BE2#	J15	D17	D3	KEN#	F15	VCC	E2	VSS	G17
A10	S13	BE3#	F17	D18	C2	LOCK#	N15	VCC	E16	VSS	H1
A11	R12	BLAST#	R16	D19	B1	M/IO#	N16	VCC	G2	VSS	H17
A12	S7	BOFF#	D17	D20	A1	NC	A3	VCC	G16	VSS	K1
A13	Q10	BRDY#	H15	D21	B2	NC	A14	VCC	H16	VSS	K17
A14	S5	BREQ	Q15	D22	A2	NC	B16	VCC	K2	VSS	L1
A15	R7	BS8#	D16	D23	A4	NC	C13	VCC	K16	VSS	L17
A16	Q9	BS16#	C17	D24	A6	NC	J4	VCC	L16	VSS	M1
A17	Q3	CLK	C3	D25	B6	NMI	B15	VCC	M2	VSS	M17
A18	R5	CLKMUL	R17	D26	C7	PCD	J17	VCC	M16	VSS	P17
A19	Q4	D/C#	M15	D27	C6	PCHK#	Q17	VCC	P16	VSS	Q2
A20	Q8	D0	P1	D28	C8	PLOCK#	Q16	VCC	R3	VSS	R4
A20M#	D15	D1	N2	D29	A8	PWT	L15	VCC	R6	VSS	S6
A21	Q5	D2	N1	D30	C9	RDY#	F16	VCC	R8	VSS	S8
A22	Q7	D3	H2	D31	B8	RESET	C16	VCC	R9	VSS	S9
A23	S3	D4	M3	DP0	N3	RPLSET0	B14	VCC	R10	VSS	S10
A24	Q6	D5	J2	DP1	F1	RPLSET1	B12	VCC	R11	VSS	S11
A25	R2	D6	L2	DP2	H3	RPLVAL#	B13	VCC	R14	VSS	S12
A26	S2	D7	L3	DP3	A5	SMADS#	C12	VOLDET	S4	VSS	S14
A27	S1	D8	F2	EADS#	B17	SMI#	B10	VSS	A7	W/R#	N17
A28	R1	D9	D1	FERR#	C14	SUSP#	G15	VSS	A9	WM_RST	C10

Table 5-2. 168-Pin PGA Package (Intel DX4-like pinout) Signal Names Sorted by Pin Number

Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal
A1	D20	B12	RPLSET1	D17	BOFF#	J15	BE2#	P2	A29	R7	A15
A2	D22	B13	RPLVAL#	E1	VSS	J16	BE1#	P3	A30	R8	VCC
A3	NC	B14	RPLSET0	E2	VCC	J17	PCD	P15	HLDA	R9	VCC
A4	D23	B15	NMI	E3	D10	K1	VSS	P16	VCC	R10	VCC
A5	DP3	B16	NC	E15	HOLD	K2	VCC	P17	VSS	R11	VCC
A6	D24	B17	EADS#	E16	VCC	K3	D14	Q1	A31	R12	A11
A7	VSS	C1	D11	E17	VSS	K15	BE0#	Q2	VSS	R13	A8
A8	D29	C2	D18	F1	DP1	K16	VCC	Q3	A17	R14	VCC
A9	VSS	C3	CLK	F2	D8	K17	VSS	Q4	A19	R15	A3
A10	INVAL	C4	VCC	F3	D15	L1	VSS	Q5	A21	R16	BLAST#
A11	VSS	C5	VCC	F15	KEN#	L2	D6	Q6	A24	R17	CLKMUL
A12	HITM#	C6	D27	F16	RDY#	L3	D7	Q7	A22	S1	A27
A13	SUSPA#	C7	D26	F17	BE3#	L15	PWT	Q8	A20	S2	A26
A14	NC	C8	D28	G1	VSS	L16	VCC	Q9	A16	S3	A23
A15	IGNNE#	C9	D30	G2	VCC	L17	VSS	Q10	A13	S4	VOLDET
A16	INTR	C10	WM_RST	G3	D12	M1	VSS	Q11	A9	S5	A14
A17	AHOLD	C11	UP#	G15	SUSP#	M2	VCC	Q12	A5	S6	VSS
B1	D19	C12	SMADS#	G16	VCC	M3	D4	Q13	A7	S7	A12
B2	D21	C13	NC	G17	VSS	M15	D/C#	Q14	A2	S8	VSS
B3	VSS	C14	FERR#	H1	VSS	M16	VCC	Q15	BREQ	S9	VSS
B4	VSS	C15	FLUSH#	H2	D3	M17	VSS	Q16	PLOCK#	S10	VSS
B5	VSS	C16	RESET	H3	DP2	N1	D2	Q17	PCHK#	S11	VSS
B6	D25	C17	BS16#	H15	BRDY#	N2	D1	R1	A28	S12	VSS
B7	VCC	D1	D9	H16	VCC	N3	DP0	R2	A25	S13	A10
B8	D31	D2	D13	H17	VSS	N15	LOCK#	R3	VCC	S14	VSS
B9	VCC	D3	D17	J1	NC	N16	M/IO#	R4	VSS	S15	A6
B10	SMI#	D15	A20M#	J2	D5	N17	W/R#	R5	A18	S16	A4
B11	VCC	D16	BS8#	J3	D16	P1	D0	R6	VCC	S17	ADS#

5.2 168-Pin PGA Package (IBM 486 DX2 Pinout)

The pin assignments for the IBM 486 DX4 168-pin Pin Grid Array (PGA) package (IBM 486 DX2 pinout) are shown in Figure 5-2. The pins are listed by signal name and pin number in Tables 5-3 and 5-4.

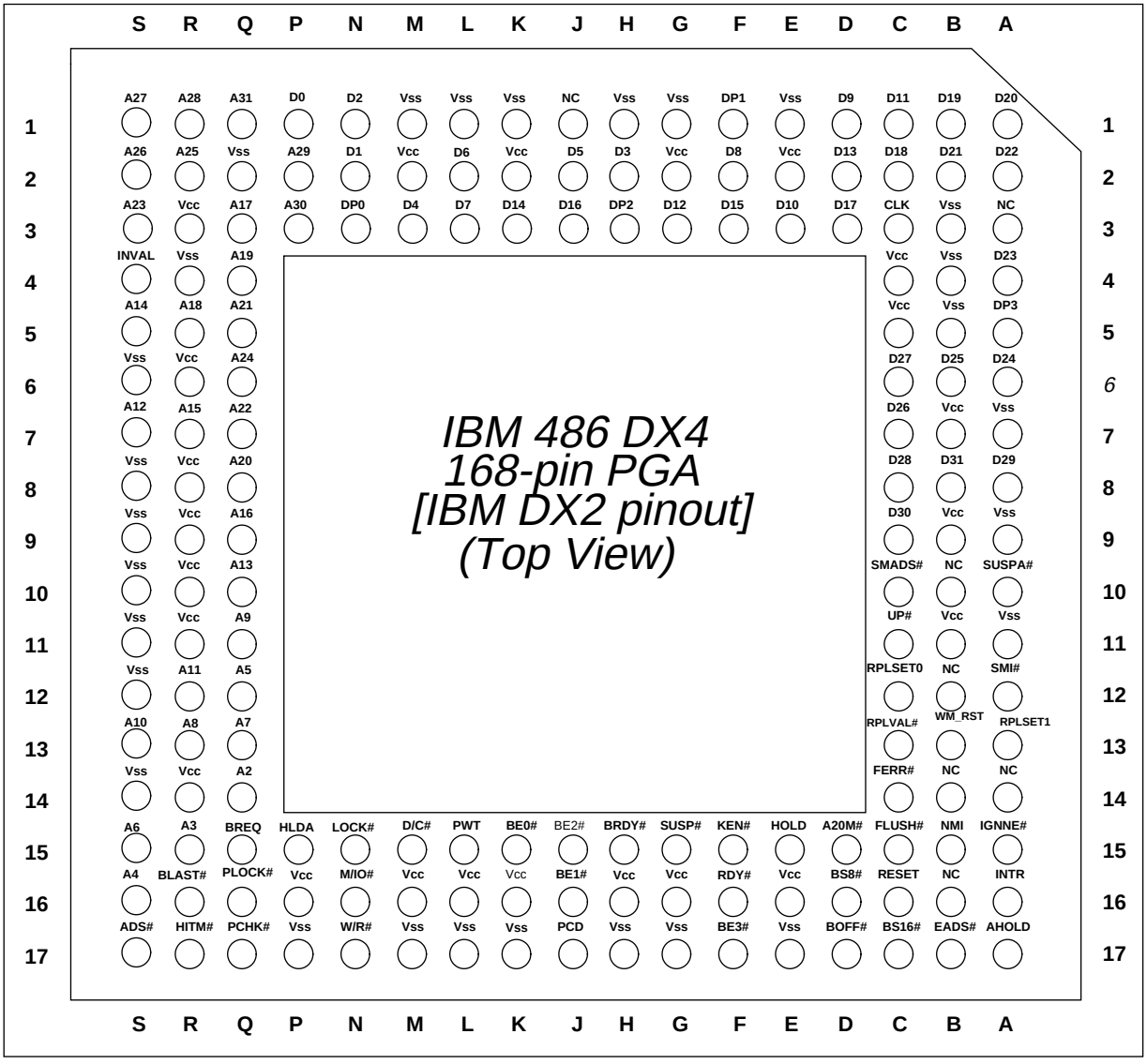


Figure 5.2 168-Pin PGA Package Pin Assignments [IBM 486 DX2 Pinout] (Top View)

Table 5-3. 168-Pin PGA Package (IBM DX2 pinout) Pin Numbers Sorted by Signal Name

Signal Name	Pin No.	Signal Name	Pin No.	Signal Name	Pin No.	Signal Name	Pin No.	Signal Name	Pin No.	Signal Name	Pin No.
A2	Q14	A29	P2	D11	C1	HITM#	R17	SUSP#	G15	VSS	A11
A3	R15	A30	P3	D12	G3	HLDA	P15	SUSPA#	A10	VSS	B3
A4	S16	A31	Q1	D13	D2	HOLD	E15	UP#	C11	VSS	B4
A5	Q12	ADS#	S17	D14	K3	IGNNE#	A15	VCC	B7	VSS	B5
A6	S15	AHOLD	A17	D15	F3	INTR	A16	VCC	B9	VSS	E1
A7	Q13	BE0#	K15	D16	J3	INVAL	S4	VCC	B11	VSS	E17
A8	R13	BE1#	J16	D17	D3	KEN#	F15	VCC	C4	VSS	G1
A9	Q11	BE2#	J15	D18	C2	LOCK#	N15	VCC	C5	VSS	G17
A10	S13	BE3#	F17	D19	B1	M/IO#	N16	VCC	E2	VSS	H1
A11	R12	BLAST#	R16	D20	A1	NC	A3	VCC	E16	VSS	H17
A12	S7	BOFF#	D17	D21	B2	NC	A14	VCC	G2	VSS	K1
A13	Q10	BRDY#	H15	D22	A2	NC	B10	VCC	G16	VSS	K17
A14	S5	BREQ	Q15	D23	A4	NC	B12	VCC	H16	VSS	L1
A15	R7	BS8#	D16	D24	A6	NC	B14	VCC	K2	VSS	L17
A16	Q9	BS16#	C17	D25	B6	NC	B16	VCC	K16	VSS	M1
A17	Q3	CLK	C3	D26	C7	NC	J1	VCC	L16	VSS	M17
A18	R5	D/C#	M15	D27	C6	NMI	B15	VCC	M2	VSS	P17
A19	Q4	D0	P1	D28	C8	PCD	J17	VCC	M16	VSS	Q2
A20	Q8	D1	N2	D29	A8	PCHK#	Q17	VCC	P16	VSS	R4
A20M#	D15	D2	N1	D30	C9	PLOCK#	Q16	VCC	R3	VSS	S6
A21	Q5	D3	H2	D31	B8	PWT	L15	VCC	R6	VSS	S8
A22	Q7	D4	M3	DP0	N3	RDY#	F16	VCC	R8	VSS	S9
A23	S3	D5	J2	DP1	F1	RESET	C16	VCC	R9	VSS	S10
A24	Q6	D6	L2	DP2	H3	RPLSET0	C12	VCC	R10	VSS	S11
A25	R2	D7	L3	DP3	A5	RPLSET1	A13	VCC	R11	VSS	S12
A26	S2	D8	F2	EADS#	B17	RPLVAL#	C13	VCC	R14	VSS	S14
A27	S1	D9	D1	FERR#	C14	SMADS#	C10	VSS	A7	W/R#	N17
A28	R1	D10	E3	FLUSH#	C15	SMI#	A12	VSS	A9	WM_RST	B13

Table 5-4. 168-Pin PGA Package (IBM DX2 Pinout) Signal Numbers Sorted by Pin Number

Pin No.	Signal Name	Pin No.	Signal Name	Pin No.	Signal Name	Pin No.	Signal Name	Pin No.	Signal Name	Pin No.	Signal Name
A1	D20	B12	NC	D17	BOFF#	J15	BE#2	P2	A29	R7	A15
A2	D22	B13	WM_RST	E1	VSS	J16	BE#1	P3	A30	R8	VCC
A3	NC	B14	NC	E2	VCC	J17	PCD	P15	HLDA	R9	VCC
A4	D23	B15	NMI	E3	D10	K1	VSS	P16	VCC	R10	VCC
A5	DP3	B16	NC	E15	HOLD	K2	VCC	P17	VSS	R11	VCC
A6	D24	B17	EADS#	E16	VCC	K3	D14	Q1	A31	R12	A11
A7	VSS	C1	D11	E17	VSS	K15	BE0#	Q2	VSS	R13	A8
A8	D29	C2	D18	F1	DP1	K16	VCC	Q3	A17	R14	VCC
A9	VSS	C3	CLK	F2	D8	K17	VSS	Q4	A19	R15	A3
A10	SUSPA#	C4	VCC	F3	D15	L1	VSS	Q5	A21	R16	BLAST#
A11	VSS	C5	VCC	F15	KEN#	L2	D6	Q6	A24	R17	HITM#
A12	SMI#	C6	D27	F16	RDY#	L3	D7	Q7	A22	S1	A27
A13	RPLSET1	C7	D26	F17	BE3#	L15	PWT	Q8	A20	S2	A26
A14	NC	C8	D28	G1	VSS	L16	VCC	Q9	A16	S3	A23
A15	IGNNE#	C9	D30	G2	VCC	L17	VSS	Q10	A13	S4	INVAL
A16	INTR	C10	SMADS#	G3	D12	M1	VSS	Q11	A9	S5	A14
A17	AHOLD	C11	UP#	G15	SUSP#	M2	VCC	Q12	A5	S6	VSS
B1	D19	C12	RPLSET0	G16	VCC	M3	D4	Q13	A7	S7	A12
B2	D21	C13	RPLVAL#	G17	VSS	M15	D/C#	Q14	A2	S8	VSS
B3	VSS	C14	FERR#	H1	VSS	M16	VCC	Q15	BREQ	S9	VSS
B4	VSS	C15	FLUSH#	H2	D3	M17	VSS	Q16	PLOCK#	S10	VSS
B5	VSS	C16	RESET	H3	DP2	N1	D2	Q17	PCHK#	S11	VSS
B6	D25	C17	BS16#	H15	BRDY#	N2	D1	R1	A28	S12	VSS
B7	VCC	D1	D9	H16	VCC	N3	DP0	R2	A25	S13	A10
B8	D31	D2	D13	H17	VSS	N15	LOCK#	R3	VCC	S14	VSS
B9	VCC	D3	D17	J1	NC	N16	M/IO#	R4	VSS	S15	A6
B10	NC	D15	A20M#	J2	D5	N17	W/R#	R5	A18	S16	A4
B11	VCC	D16	BS8#	J3	D16	P1	D0	R6	VCC	S17	ADS#

5.3 208-Lead QFP Package

Pin Assignments

The pin assignments for the IBM 486 DX4 208-lead QFP (Quad Flat Pack) package are shown in Figure 5-3. The signal names are shown in Table 5-5 sorted by signal name and in Table 5-6 sorted by pin numbers.

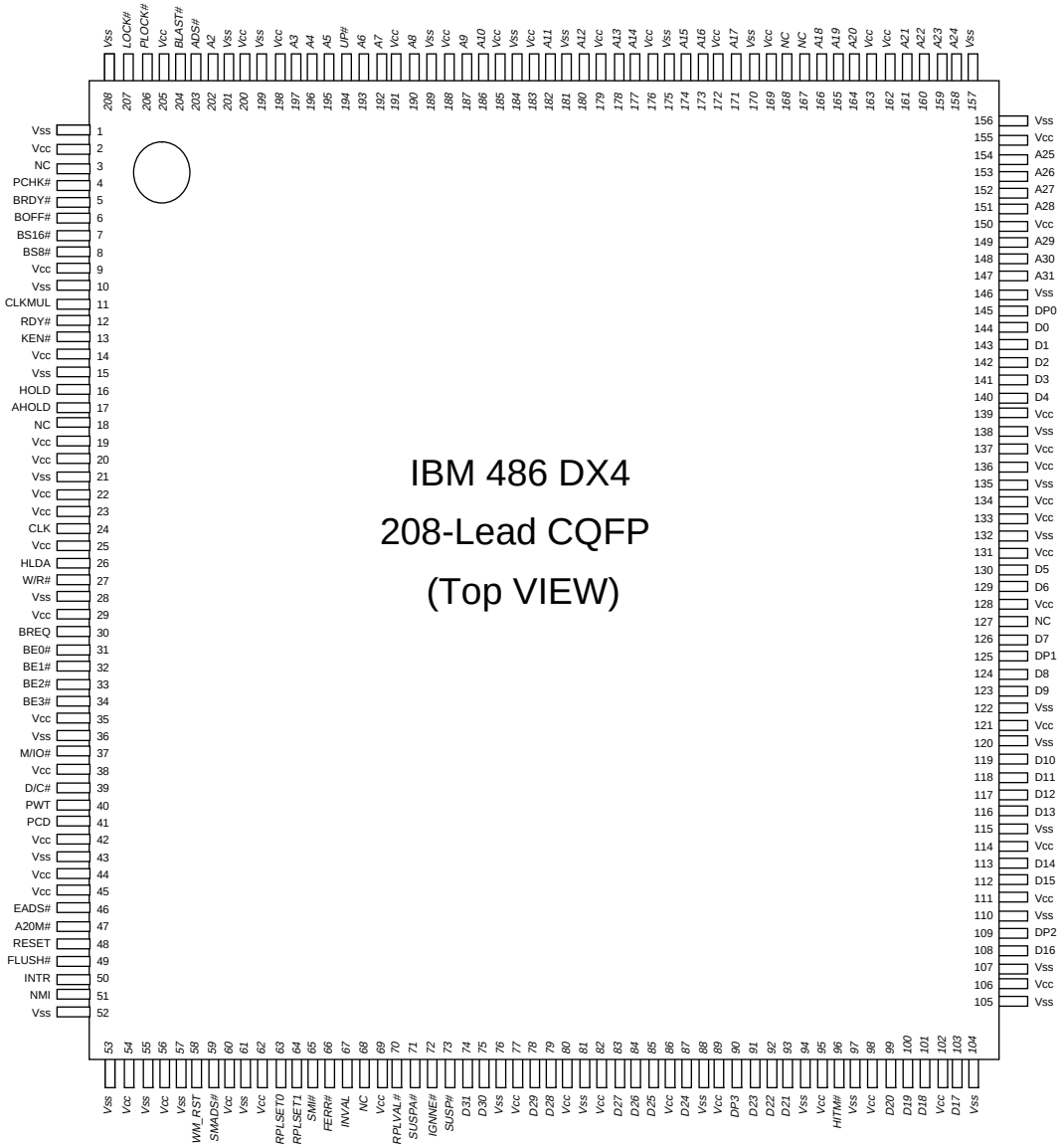


Figure 5-3. 208-Lead QFP Package Pin Assignments (Top View)

Table 5-5. 208-Lead QFP Package Pins Sorted by Signal Name

Signal	Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal	Pin
A2	202	BE2#	33	D25	85	RDY#	12	Vcc	98	Vss	52
A3	197	BE3#	34	D26	84	RESET	48	Vcc	102	Vss	53
A4	196	BLAST#	204	D27	83	RPLSET0	63	Vcc	106	Vss	55
A5	195	BOFF#	6	D28	79	RPLSET1	64	Vcc	111	Vss	57
A6	193	BRDY#	5	D29	78	RPLVAL #	70	Vcc	114	Vss	61
A7	192	BREQ	30	D30	75	SMADS#	59	Vcc	121	Vss	76
A8	190	BS16#	7	D31	74	SMI#	65	Vcc	128	Vss	81
A9	187	BS8#	8	D/C#	39	SUSP#	73	Vcc	131	Vss	88
A10	186	CLK	24	DP0	145	SUSPA#	71	Vcc	133	Vss	94
A11	182	CLKMUL	11	DP1	125	UP#	194	Vcc	134	Vss	97
A12	180	D0	144	DP2	109	Vcc	2	Vcc	136	Vss	104
A13	178	D1	143	DP3	90	Vcc	9	Vcc	137	Vss	105
A14	177	D2	142	EADS#	46	Vcc	14	Vcc	139	Vss	107
A15	174	D3	141	FERR#	66	Vcc	19	Vcc	150	Vss	110
A16	173	D4	140	FLUSH#	49	Vcc	20	Vcc	155	Vss	115
A17	171	D5	130	HITM#	96	Vcc	22	Vcc	162	Vss	120
A18	166	D6	129	HLDA	26	Vcc	23	Vcc	163	Vss	122
A19	165	D7	126	HOLD	16	Vcc	25	Vcc	169	Vss	132
A20	164	D8	124	IGNNE#	72	Vcc	29	Vcc	172	Vss	135
A20M#	47	D9	123	INTR	50	Vcc	35	Vcc	176	Vss	138
A21	161	D10	119	INVAL	67	Vcc	38	Vcc	179	Vss	146
A22	160	D11	118	KEN#	13	Vcc	42	Vcc	183	Vss	156
A23	159	D12	117	LOCK#	207	Vcc	44	Vcc	185	Vss	157
A24	158	D13	116	M/IO#	37	Vcc	45	Vcc	188	Vss	170
A25	154	D14	113	NC	3	Vcc	54	Vcc	191	Vss	175
A26	153	D15	112	NC	18	Vcc	56	Vcc	198	Vss	181
A27	152	D16	108	NC	68	Vcc	60	Vcc	200	Vss	184
A28	151	D17	103	NC	127	Vcc	62	Vcc	205	Vss	189
A29	149	D18	101	NC	167	Vcc	69	Vss	1	Vss	199
A30	148	D19	100	NC	168	Vcc	77	Vss	10	Vss	201
A31	147	D20	99	NMI	51	Vcc	80	Vss	15	Vss	208
ADS#	203	D21	93	PCD	41	Vcc	82	Vss	21	WM_RST	58
AHOLD	17	D22	92	PCHK	4	Vcc	86	Vss	28	W/R#	27
BE0#	31	D23	91	PLOCK#	206	Vcc	89	Vss	36		
BE1#	32	D24	87	PWT	40	Vcc	95	Vss	43		

Table 5-6. 208-Lead QFP Package Singals Sorted by Pin Number

Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal
1	Vss	36	Vss	71	SUSPA#	106	Vcc	141	D3	176	Vcc
2	Vcc	37	M/IO#	72	IGNNE#	107	Vss	142	D2	177	A14
3	NC	38	Vcc	73	SUSP#	108	D16	143	D1	178	A13
4	PCHK#	39	D/C#	74	D31	109	DP2	144	D0	179	Vcc
5	BRDY#	40	PWT	75	D30	110	Vss	145	DP0	180	A12
6	BOFF#	41	PCD	76	Vss	111	Vcc	146	Vss	181	Vss
7	BS16#	42	Vcc	77	Vcc	112	D15	147	A31	182	A11
8	BS8#	43	Vss	78	D29	113	D14	148	A30	183	Vcc
9	Vcc	44	Vcc	79	D28	114	Vcc	149	A29	184	Vss
10	Vss	45	Vcc	80	Vcc	115	Vss	150	Vcc	185	Vcc
11	CLKMUL	46	EADS#	81	Vss	116	D13	151	A28	186	A10
12	RDY#	47	A20M#	82	Vcc	117	D12	152	A27	187	A9
13	KEN#	48	RESET	83	D27	118	D11	153	A26	188	Vcc
14	Vcc	49	FLUSH#	84	D26	119	D10	154	A25	189	Vss
15	Vss	50	INTR	85	D25	120	Vss	155	Vcc	190	A8
16	HOLD	51	NMI	86	Vcc	121	Vcc	156	Vss	191	Vcc
17	AHOLD	52	Vss	87	D24	122	Vss	157	Vss	192	A7
18	NC	53	Vss	88	Vss	123	D9	158	A24	193	A6
19	Vcc	54	Vcc	89	Vcc	124	D8	159	A23	194	UP#
20	Vcc	55	Vss	90	DP3	125	DP1	160	A22	195	A5
21	Vss	56	Vcc	91	D23	126	D7	161	A21	196	A4
22	Vcc	57	Vss	92	D22	127	NC	162	Vcc	197	A3
23	Vcc	58	WM_RST	93	D21	128	Vcc	163	Vcc	198	Vcc
24	CLK	59	SMADS#	94	Vss	129	D6	164	A20	199	Vss
25	Vcc	60	Vcc	95	Vcc	130	D5	165	A19	200	Vcc
26	HLDA	61	Vss	96	HITM#	131	Vcc	166	A18	201	Vss
27	W/R#	62	Vcc	97	Vss	132	Vss	167	NC	202	A2
28	Vss	63	RPLSET0	98	Vcc	133	Vcc	168	NC	203	ADS#
29	Vcc	64	RPLSET1	99	D20	134	Vcc	169	Vcc	204	BLAST#
30	BREQ	65	SMI#	100	D19	135	Vss	170	Vss	205	Vcc
31	BE0#	66	FERR#	101	D18	136	Vcc	171	A17	206	PLOCK#
32	BE1#	67	INVAL	102	Vcc	137	Vcc	172	Vcc	207	LOCK#
33	BE2#	68	NC	103	D17	138	Vss	173	A16	208	Vss
34	BE3#	69	Vcc	104	Vss	139	Vcc	174	A15		
35	Vcc	70	RPLVAL#	105	Vss	140	D4	175	Vss		

6.0 Thermal Characteristics

PGA Package

Table 6-1 lists the maximum ambient temperatures permitted for various clock frequencies and airflows for the PGA Package for Vcc equal to 3.45 volts.

Table 6-1. PGA Package Maximum Ambient Temperature (T_A) with V_{cc} = 3.45 Volts

CPU Internal Clock Frequency	Heatsink	Supply Current	AIRFLOW				
			0 (ft/min)	50 (ft/min)	100 (ft/min)	200 (ft/min)	400 (ft/min)
75 MHz	NO	.755 A	47 ^{o}C	48 ^{o}C	50 ^{o}C	52 ^{o}C	61 ^{o}C
100 MHz	NO	.920 A	39 ^{o}C	40 ^{o}C	42 ^{o}C	45 ^{o}C	55 ^{o}C

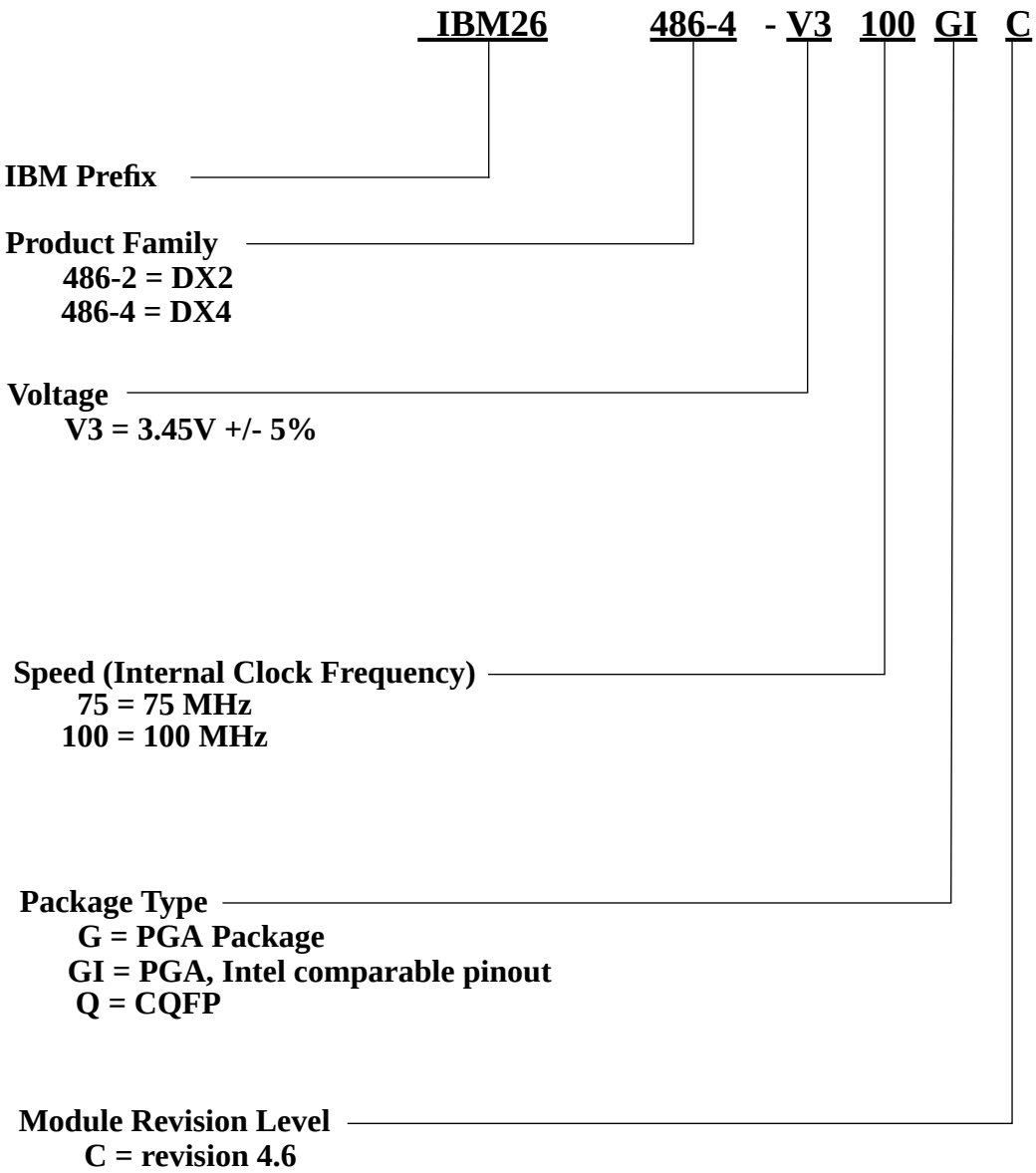
CQFP Package

Table 6-2 lists the maximum ambient temperatures permitted for various clock frequencies and airflows for the CQFP Package for Vcc equal to 3.45 volts.

Table 6-2. CQFP Package Maximum Ambient Temperature (T_A) with V_{cc} = 3.45 Volts

CPU Internal Clock Frequency	Heatsink	Supply Current	AIRFLOW				
			0 (ft/min)	50 (ft/min)	100 (ft/min)	200 (ft/min)	400 (ft/min)
75 MHz	NO	.755 A	15 ^{o}C	24 ^{o}C	32 ^{o}C	40 ^{o}C	47 ^{o}C

Ordering Information for Rev Levels 4.6 and above



The IBM 486 DX4 part numbers for revisions 4.6 and above are as follows:

Table B-1. IBM 486 DX4 Part Numbers for Revs 4.6 and above

Part Number	V_{cc} (V)	Frequency (MHz)		Package			AC Specification
		Bus	Internal	CQFP	PGA (Intel) (Pinout)	PGA (DX2) (Pinout)	
IBM26486-4V375GC	3.45	25	75			X	Table 3-5 (addendum)
IBM26486-4V375GIC	3.45	25	75		X		Table 3-5 (addendum)
IBM26486-4V375QIC	3.45	25	75	X			Table 3-5 (addendum)
IBM26486-4V3100GIC	3.45	33	100		X		Table 3-6 (addendum)
IBM26486-4V3100GC	3.45	33	100			X	Table 3-6 (addendum)

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