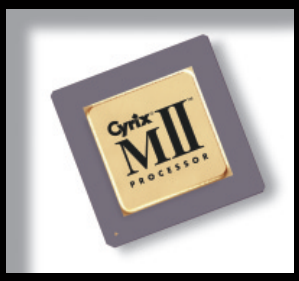
Technical Brief

Cyrix® M II™ Processor



The Cyrix® M II™ processor delivers optimum performance while running Windows® 98, Windows 95 and other operating systems.

Architectural Overview

The Cyrix® M II™ processor operates at higher frequencies than the previous 6x86MX™ processor. Based on the proven Cyrix 6x86™ processor core and compatible with MMX™ technology, the M II™ CPU is superscalar in that it contains two separate pipelines that allow multiple instructions to be processed at the same time. It features a 64-KByte internal cache, a two-level TLB and a 512-entry BTB. The M II™ processor also contains a scratchpad RAM feature, supports performance monitoring and allows caching of both SMI code and SMI data. It delivers optimum 16-bit and 32-bit performance while running Windows 98, Windows 95, Windows NT, OS/2,® DOS, UNIX® and other operating systems.

The M II™ processor features a super-pipelined architecture that increases the number of pipeline stages to reduce timing constraints and increase frequency scalability. Advanced architectural techniques include register renaming, out-of-order completion, data dependency removal, branch prediction and speculative execution. These design innovations eliminate many data dependencies and resource conflicts to achieve higher performance when executing both 16-bit and 32-bit software.

Architectural Features	Cyrix M II™ Processor	Pentium® II Processor	Pentium Processor with MMX Technology
MMX Instruction Set	X	X	X
Superscalar	X	X	X
Superpipelined	X	X	
Register Renaming	X	X	
Data Dependency Removal	X	X	
Multi-Branch Prediction	X	X	
Speculative Execution	X	X	
Out-of-Order Completion	X	X	
80-Bit Floating Point Unit	X	X	X
Primary Cache (Data+Instruction)	64K (unified)	16K+16K	16K+16K

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Cyrix® MII™ PROCESSOR

U.S. Product Information

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Channel Sales and Technical Support
Cyrix Direct Connect (U.S. Channel Program)
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800 340 0953 Technical Support
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International Offices

Contact one of these National Semiconductor offices for information on Cyrix products:

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Hong Kong	852 2737 1800
India	91 80 559 9467 91 80 509 5075
Japan	81 3 5639 7340
Korea	82 2 3771 6900
Malaysia	60 4 644 9061
Mexico	5 488 0134
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South and Central America	55 11 3043 7450
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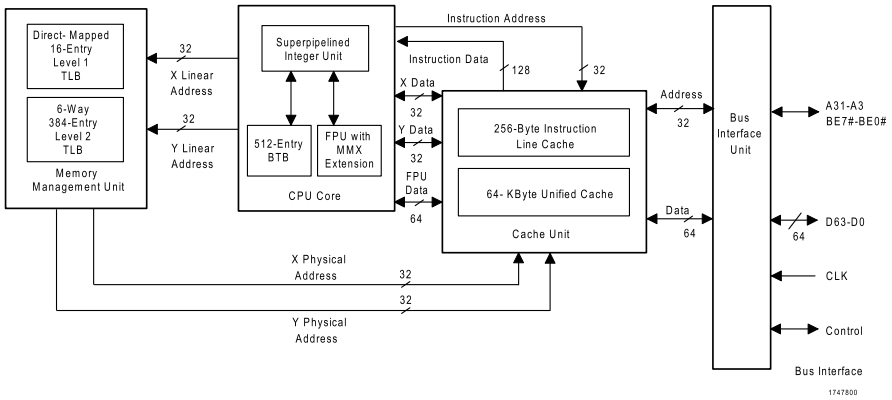

Technical Specifications

Clocking	**2x, 2.5x, 3x, 3.5x flexible core/bus clock ratios**
L1 Cache	**64-KByte; write-back; 4-way associative; unified instruction and data; dual port address**
Bus	**64-bit external data bus; 32-bit pipelined address bus**
Pin/Socket	**Socket 7 pinout compatible (P55C)**
Compatibility	**Compatible with MMX™ technology and x86 operating systems including Windows® 98, Windows 95, Windows NT, Windows, OS/2,® DOS, Solaris, UNIX® and others**
Floating Point Unit	**80-bit with 64-bit interface; parallel execution; uses x87 instruction set; IEEE-754 compatible**
Voltage	**2.9V core with 3.3V I/O**
Power Management System	**Management Mode (SMM); hardware suspend; FPU auto-idle**
Burst Order	**1-plus-4 or linear burst**

For a full technical report, visit the Cyrix Web site at www.cyrix.com.