CYRIX 6x86MX™ PROCESSOR technical brief

The 6x86MX™ processor is an MMX™ enhanced CPU offering the highest level of Windows® 95 performance available for mainstream desktop systems. The 6x86MX™ processor is compatible with MMX technology to run the latest MMX games and multimedia software.

With its enhanced memory management unit, a 64-KByte internal cache, and other advanced architectural features, the 6x86MX™ processor achieves higher performance and offers better value than competitive processors.

extreme
processing
for the
multimedia
rush™

Cyrix® 6x86MX™ PROCESSOR

Architectural Overview

The 6x86MX™ processor offers significant enhancements over the 6x86™ processor. These enhancements enable the 6x86MX™ processor to achieve higher performance at any given clock speed.

The 6x86MX™ design quadruples the internal cache size to 64-KBytes, triples the TLB size, and increases the frequency scalability to 200 MHz and beyond, relative to the 6x86™ processor. Additionally, it features 57 new MMX instructions that speed up the processing of certain computing-intensive loops found in multimedia and communication applications. The 6x86MX™ processor also contains a scratchpad RAM feature, supports performance monitoring and allows caching of both SMI code and SMI data. It delivers optimum 16-bit and 32-bit performance while running Windows® 95, Windows NT, OS/2,® DOS, UNIX® and other operating systems.

The 6x86MX™ processor features a superpipelined architecture that increases the number of pipeline stages to reduce timing constraints and increase frequency scalability. Advanced architectural techniques include register renaming, out-of-order completion, data dependency removal, branch prediction and speculative execution. These design innovations eliminate many data dependencies and resource conflicts to achieve higher performance when executing both 16-bit and 32-bit software.

Feature	Cyrix 6x86MX™ Processor	Cyrix 6x86™ Processor
Pinout	P55C (socket 7)	P54C (socket 7)
Supply Voltage	2.8V Core; 3.3V I/O	6x86: 3.3V or 3.52V; 6x86L: 2.8V core; 3.3V I/O
CPU Primary Cache	64-KByte	16-KByte
TLB	L1: 16 entry; L2: 384 entry	L1: 128 entry; Victim TLB: 8 entry
Branch Prediction	512 entry branch target cache; 1024 entry branch history table	256 entry branch target cache; 512 entry branch history table
MMX Instructions	Yes	No
Performance Monitor including Time Stamp Counter and Model Specific Registers	Yes	No
Scratchpad RAM in Primary Cache	Yes	No
Cacheable SMI Code/Data	Yes	No

Architectural Features	Cyrix 6x86MX™ Processor	Cyrix 6x86™ Processor	Pentium® Processor with MMX™ Technology	Pentium II Processor
MMX Instruction Set	X		X	X
Superscalar	X	X	X	X
Superpipelined	X	X		X
Register Renaming	X	X		X
Data Dependency Removal	X	X		X
Multi-Branch Prediction	X	X		X
Speculative Execution	X	X		X
Out-of-Order Completion	X	X		X
80-Bit Floating Point Unit	X	X	X	X
Primary Cache (Data+Instruction)	64K (unified)	16K (unified)	16K + 16K	16K + 16K

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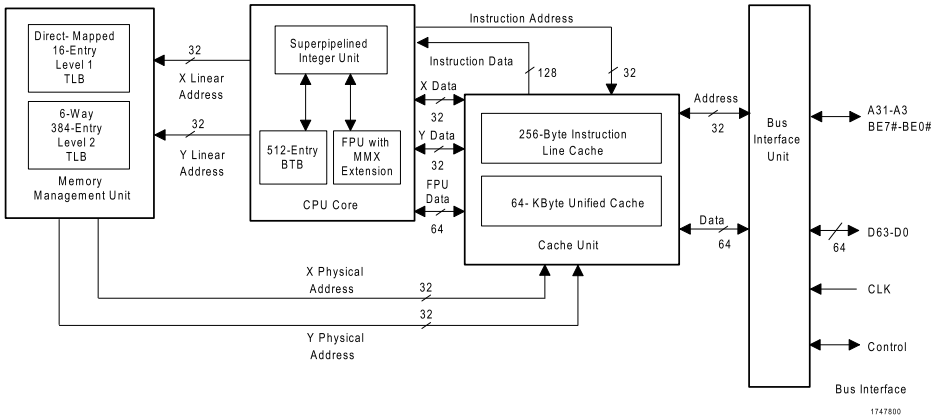

TECHNICAL SPECIFICATIONS

Clocking	2x, 2.5x, 3x, 3.5x flexible core/bus clock ratios
L1 Cache	64-KByte; write-back; 4-way associative; unified instruction and data; dual port address
Bus	64-bit external data bus; 32-bit pipelined address bus
Pin/Socket	Socket 7 pinout compatible (P55C)
Compatibility	Compatible with MMX™ technology and x86 operating systems including Windows® 95, Windows NT, Windows, OS/2,® DOS, Solaris, UNIX® and others
Floating Point Unit	80-bit with 64-bit interface; parallel execution; uses x87 instruction set; IEEE-754 compatible
Voltage	2.8-volt core with 3.3-volt I/O
Power Management	System Management Mode (SMM); hardware suspend; FPU auto-idle
Burst Order	1-plus-4 or linear burst

PERFORMANCE RATINGS

Processor Part No.	Performance Rating	Bus/Clock Speed
6x86MX-PR166GP	PR166	60/150
6x86MX-PR200GP	PR200	66/166
6x86MX-PR233GP	PR233	75/188

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