Application Note 102
Pin and Bus Cycle Differences

for the 6x86, 6x86L , 6x86MX and MII

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APPLICATION NOTE 102

Pin and Bus Cycle Differences

1. Introduction

This application note describes the bus and pin differences between the Cyrix 6x86, 6x86L, 6x86MX, MII, the Intel P54C and P55C.

2. 296-Pin Socket Pin Definitions

The Cyrix 6x86, 6x86L, 6x86MX and the MII family of processors physically fit into the 296-pin Staggered Pin Grid Array (SPGA) also known as the “Socket 7.” This is the same pin arrangement used by Intel for their P54C and P55C processors.

Certain pins have different definitions to accommodate processors with different types of power supplies, clock to bus ratios and features.

2.1. Pin Differences

The table below lists the pin differences for 296-Pin Socket processors manufactured by Intel and Cyrix.

SOCKET 7 PIN DIFFERENCES FOR INTEL AND CYRIX PROCESSORS

PIN NO.	P54C 296 PGA	P55C 296 PGA (SOCKET 7)	6X86 296-PIN PGA	6X86L 296-PIN PGA	6x86MX/MII 296-PIN PGA	COMMON SOCKET IMPLEMENTATION
H34	PICCLK	PICCLK	NC	NC	NC	No interference from 6x86 parts.
J33	PICD0 [DPEN#]	PICD0 [DPEN#]	Reserved	NC	NC	10K Ohm pull-up.
L35	PICD1 [APICEN]	PICD1 [APICEN]	NC	NC	NC	10K Ohm pull-down.
P4	IERR#	IERR#	NC	NC	NC	No interference from 6x86 parts.
Q3	PM0/BP0	PM0/BP0	Reserved	Reserved	Reserved	No signal.
Q35	CPUTYP	CPUTYP	NC	NC	NC	No interference from 6x86 parts.
R4	PM1/BP1	PM1/BP1	Reserved	Reserved	Reserved	No signal.
R34	NC	NC	BHOLD	NC	NC	No signal.
S3	BP2	BP2	Reserved	Reserved	NC	No signal. Note 6.
S5	BP3	BP3	LBA#	NC	NC	No signal.
S33	NC	NC	Reserved	Reserved	Reserved	No signal.
S35	NC	NC	DHOLD	Reserved	Reserved	No signal.
V34	STPCLK#	STPCLK#	SUSP#	SUSP#	SUSP#	SUSP#/STPCLK# Note 1.
W33	NC	NC	SUSPA#	SUSPA#	SUSPA#	SUSPA# Note 1.
W35	NC	NC	Reserved	Reserved	Reserved	No signal.
X34	[BF1]	[BF1]	Reserved	Reserved	CLKMUL1	Note 3.
Y33	[BF0]	[BF0]	CLKMUL	CLKMUL	CLKMUL0	Note 3.
Y35	FRCMC#	FRCMC#	Reserved	Reserved	Reserved	10K Ohm pull-up.
Z34	PEN#	PEN#	NC	NC	NC	Note 4.
AA3	PHIT#	PHIT#	Reserved	NC	NC	No signal.
AA33	INIT	INIT	WM_RST	WM_RST	WM_RST	WM_RST/INIT
AC3	PHITM#	PHITM#	Reserved	Reserved	NC	No signal.
AC5	PRDY	PRDY	NC	Reserved	NC	No signal.
AC33	NMI/LINT1	NMI/LINT1	NMI	NMI	NMI	NMI
AC35	R/S#	R/S#	NC	NC	NC	No interference from 6x86 parts.
AD4	PBGNT#	PBGNT#	NC	NC	NC	No interference from 6x86 parts.
AD34	INTR/LINT0	INTR/LINT0	INTR	INTR	INTR	INTR
AE3	PBREQ#	PBREQ#	NC	NC	NC	No interference from 6x86 parts.
AE35	D/P#	D/P#	NC	NC	NC	No interference from 6x86 parts.
AH32	Note 2.	UPVRM#	Note 2.	Note 2.	Note 2.	No interference from 6x86 parts.
AL1	NC	VCC2DET	NC	VCC2DET	VCC2DET	VCC2DET
AL7	BUSCHK#	BUSCHK#	QDUMP#	NC	NC	Note 5.
AL19	NC	NC	Reserved	NC	NC	No signal.
AN01	NC	VCC5	NC	NC	NC	No interference from 6x86 parts.
AN03	NC	VCC5	NC	NC	NC	No interference from 6x86 parts.
AN35	NC	NC	Reserved	Reserved	Reserved	No signal.

Note 1: The SUSP# input may be driven by the chipset provided the chipset supports the Cyrix Suspend Mode. In this case, SUSPA# may then be monitored by the chipset. If Suspend Mode is not used, these pins should not be enabled.

Note 2: The indicated package pin does not exist on these devices.

Note 3: CLKMUL0 and CLKMUL1 signals control the 6x86MX and MII core/bus clock ratio as defined in the table below. The socket implementation should allow for jumpers to drive a "1" or "0" on either of these pins. These pins have internal pull-ups and pull-downs resistors and default to a 2:1 core/bus clock ratio.

CLKMUL1	CLKMUL0	CORE TO BUS CLOCK RATIO
0	0	2.5
0	1	3.0
1	0	2.0 (Default)
1	1	3.5

Note 4: The Pentium PEN# (Parity Enable) may not be used in all systems. If parity is not used, PEN# should be pulled high through a 10K Ohm pull-up. If parity is used, PEN# should be driven low, only if a Pentium is installed.

Note 5: The QDUMP# pin must be pulled high during the RESET high-to-low transition to disable the scatter/gather interface pins on the 6x86.

Note 6: LBA# is driven to a logic high during the RESET high-to-low transition and can be used to identify the presence of an 6x86.

2.2. Common Socket Implementation

The table on the previous page, contains information to help the designer ensure that a socket design works with all the CPUs listed in the table. For a common socket implementation, the listed pins should not be connected to any signal and should be either pulled high, pulled low or left unconnected as shown in the table.

It may be possible to implement a variation of the common socket that supports a specific feature, such as a socket supporting 6x86 suspend (SUSP#, SUSPA#). Care must be taken when implementing common socket variations to eliminate pinout conflicts and ensure proper system operation.

2.3. NC and Reserved Pins

NC Pins

Pins labeled “NC” are not internally connected.

Reserved Pins

Pins labeled “Reserved” are reserved for testing during manufacture or are reserved for signals to be defined in the future. Do *not* connect any traces to a reserved pin.

2.4. Single-Rail Devices

The P54C and 6x86 devices connect to a single power supply of 3.3 volts (refer to respective data books for exact voltage ranges).

2.5. Split-Rail Devices

The P55C, 6x86L, 6x86MX and MII connect to two power supply voltages. The core of these devices is powered by a 2.8 volt (VCC2) supply. The I/O circuit of these devices is powered by a 3.3 volt (VCC3) supply. The voltages listed here are approximate, and one should refer to the device’s data book for exact voltage ranges.

These split-rail devices drive pin AL1 (VCC2DET) low (Vss). Board circuitry can be used to detect this voltage and automatically switch VCC2 power from 3.3 to 2.8 volts using a circuit similar to the “Recommended Power Supply Block Diagram” shown on page 7.

2.5.1 Cyrix Split-Rail Power Supply Pins

The VCC2 pins for the Cyrix 6x86L 6x86MX and the MII CPUs are listed in the table below.

VCC2 PINS (6X86L, 6X86MX, MII)

A7	A9	A11	A13	A15
A17	G1	J1	L1	N1
Q1	S1	U1	W1	Y1
AA1	AC1	AE1	AG1	AN9
AN11	AN13	AN15	AN17	AN19

The VCC3 pins for the 6x86L 6x86MX and the MII are listed in the table below.

VCC3 PINS (6X86L, 6X86MX, MII)

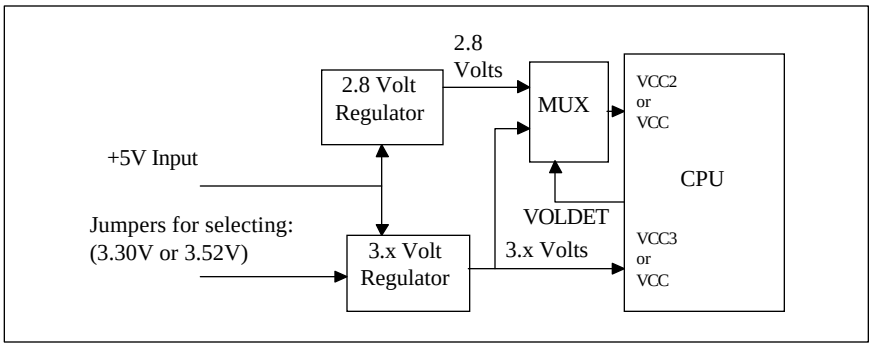
A19	A21	A23	A25	A27
A29	E37	G37	J37	L33
L37	N37	Q37	S37	T34
U33	U37	W37	Y37	AA37
AC37	AE37	AG37	AN21	AN23
AN25	AN27	AN29		

2.5.2 Circuit Used with Split-Rail Regulators

When using a split-rail device such as a 6x86L, 6x86MX and MII, it is important not to connect the device to the wrong voltage.

It is recommended that a voltage multiplexer circuit be used to avoid this problem such as the one shown below. This circuit detects the VOLDET signal on the VCCDET pin and correctly applies either 2.8 or 3.3 volts to the CPU core.

RECOMMENDED POWER SUPPLY BLOCK DIAGRAM



If a 2.8 / 3.3 volt jumper is used instead, an incorrect jumper setting could cause damage to a split-rail device. An external pull-up resistor should be connected to VOLDET so that single-rail devices are detected.

2.5.3 Regulator Current Requirements

The regulator current requirements for the 6x86, 6x86L, 6x86MX, and MII devices are listed in the table below. Note that the currents ICC2T and ICC3T include current not going to the CPU. Refer to respective Cyrix databooks for more information.

RECOMMENDED REGULATOR CURRENT FOR 6X86, 6X86L, 6X86MX, MII

SUGGESTED REGULATOR				PROCESSOR SPECIFICATIONS			
VOLTAGE (V)		TOTAL CURRENT (A) NOTE 1		CYRIX DEVICE	BUS/CORE (MHZ)	MAX CPU I_{CC} (A)	
3.3 or 3.52		7.5		6x86-P120+	50/100	5.4	
				6x86-P133+	55/110	5.8	
				6x86-P150+	60/120	6.1	
				6x86-P166+	66/133	6.6	
		8.0		6x86-P200+	75/150	7.0	
ICC3T	*ICC2T*	*ICC3T*	*ICC2T*			*ICC3*	*ICC2*
3.3	2.8	2.0	7.0	6x86L-P120+	50/100	0.70	4.7
				6x86L-P133+	55/110	0.78	5.0
				6x86L-P150+	60/120	0.82	5.3
				6x86L-P166+	66/133	0.88	5.6
				6x86L-P200+	75/150	0.96	6.0
ICC3T	*ICC2T*	*ICC3T*	*ICC2T*			*ICC3*	*ICC2*
3.3	2.8	2.5	10	6x86MX Note 2	66/166	1.10	7.4
				6x86MX Note 2	60/180	1.15	7.8
				6x86MX Note 2	66/200	1.25	8.4
				6x86MX Note 2	75/225	1.40	9.1
ICC3T	*ICC2T*	*ICC3T*	*ICC2T*			*ICC3*	*ICC2*
3.3	2.8	2.5	10	MII Note 2	66/166	1.10	7.4
				MII Note 2	60/180	1.15	7.8
				MII Note 2	66/200	1.25	8.4
				MII Note 2	75/225	1.40	9.1

Note 1: ICC3T includes an estimated maximum 600 mA 3.3/3.52 V current for L2 cache (512K Bytes) and an estimated 300 mA for other components (chipset, buffers, etc.) in addition to the ICC3 current drawn by the CPU. It is assumed that ICC2T = ICC2 and only the CPU is driven by this voltage.

Note 2: Max CPU I_{CC} for the 6x86MX and MII are estimated. Other CPU values subject to change. Consult the 6x86MX and MII Data Books, and the Cyrix web site at www.cyrix.com for updated information.

2.6. Phase Lock Loop Power Pin

The AN19 pin on the 6x86MX and MII, in the future, may be used to power the phase-lock-loop clock oscillator on the CPU chip. For this reason, the VCC2 power applied to pin AN19 should be decoupled for highest reliability.

2.7. Unique Pentium Pins

The pins in the table below list the unique Pentium pins that are not supported by the 6x86, 6x86MX or the MII CPU.

PENTIUM PINS NOT SUPPORTED BY 6X86, 6X86MX, MII

PIN NAME	PIN FUNCTION
[BF]	Bus Frequency Select
BP(3:2), BP/PM(1:0)	Breakpoint, Performance Monitor Outputs
CPUTYP	CPU Type Indicator
D/P#	Dual/Primary Processor Indicator
FRCMC#, IERR#, PEN#, BUSCHK#	Data Integrity, Error Checking
LINT1 (NMI)*, LINT0 (INTR)*	Local Interrupt (0:1)
PHIT#, PHITM#, PBGNT#, PBREQ#	Interprocessor signals for dual processor implementation
PICCLK, PICD0 [DPEN#], PICD1 [APICEN]	APIC Interface Signals and Dual Processor Enable
PRDY	Probe Ready
R/S#	Run/Stop Control
STPCLK#	Stop Clock Request

*Note: The NMI and INTR functions of these pins are supported on the 6x86 product line.

2.8. Unique 6x86 Pins

The 6x86 supports the scatter/gather interface which requires the signals and pins listed in the table below. The same pins on the 6x86L and 6x86MX are listed for reference.

6x86 Unique Pins

Pin #	6x86	6x86L	6x86MX	MII
R34	BHOLD	NC	NC	NC
S5	LBA#	NC	NC	NC
S35	DHOLD	Reserved	Reserved	Reserved
AL7	QDUMP#	NC	NC	NC

2.9. Unique 6x86, 6x86MX and MII Pins

The table below lists the pins that are unique to the 6x86 and/or 6x86MX and are not supported on the Pentium CPU.

Unique 6x86, 6x86MX and MII Pins

Pin Name	Pin Function
BHOLD, DHOLD, LBA#, QDUMP#	Scatter/Gather Interface Pins
PMON0, PMON1, PMC	Performance Monitor Outputs
SUSP#, SUSPA#	Suspend Mode Control
CLKMUL	Core/Bus Clock Frequency Ratio Control
TEST	Test Control Input
Reserved	Reserved for future use.

2.10. Core-to-Bus Clock Ratio Selection

While the 6x86 and 6x86L support one input pin to select the core-to-bus clock ratio, the 6x86MX and MII has two inputs. On the 6x86 and 6x86L, CLKMUL (Y33) is sampled at RESET to select the clock ratio. The 6x86MX and MII use two pins CLKMUL0 (Y33) and CLKMUL1 (X34) to select the clock ratio as described in the table below. If the two CLKMUL pins are left floating, internal pull-up and pull-down resistors will force the pins to the default mode as described in the table.

CORE-TO-BUS CLOCK RATIO SELECTION

CPU	6x86 AND 6x86L	6x86MX/MII	P54CS	P55C
PIN	CLKMUL (Pin Y33)	CLKMUL0 (Pin Y33) CLKMUL1 (Pin X34)	BF0 (Pin X34) BF1 (Pin Y33)	BF0 (Pin X34) BF1 (Pin Y33)
SELECTION	0 = 2.0 (default) 1 = 3.0	00 = 2.5 01 = 3.0 10 = 2.0 (default) 11 = 3.5	00 = 2.5 01 = 3.0 10 = 2.0 11 = 1.5 (default)	00 = 2.5 01 = 3.0 10 = 2.0 (default) 11 = Reserved

Note: The “default” setting indicates the clock mode of the device when the indicated pins are floated.

3. Bus Cycle Differences

3.1. Misaligned Accesses

The Pentium processor defines a misaligned access for any non-cacheable cycle as any 16, 32, or 64-bit access that crosses a 32-bit boundary. The Pentium processor always issues two bus cycles for non-cacheable memory reads/writes or I/O cycles that cross a 32-bit boundary. Pentium drives/reads the bytes corresponding with the highest address first (indicated by address and byte enables).

In contrast, the 6x86 processor behaves as follows:

1) For transfers within a 64-bit boundary, the 6x86 processor issues only a single cycle, with the appropriate byte enables valid, for all accesses requiring data within a 64-bit quadword. This difference results in lower bus utilization for the 6x86.

2) For transfers that cross the 64-bit boundary, the 6x86 processor issues the cycle for the lower address first, followed by the cycle for the higher address.

3.2. Cycles Resulting from INVD Instruction

The Pentium processor invalidates the contents of its internal caches as the result of executing an INVD instruction. This invalidation occurs even if modified data exists in the data cache. This could potentially result in a data incoherency. In contrast, the 6x86 processor always writes all modified data to external memory prior to invalidating the internal cache contents.

3.3. WM_RST Function

Assertion of the WM_RST signal causes the 6x86 to complete the current instruction and then places the 6x86 in a known state. WM_RST differs from RESET in that the contents of the on-chip cache, the write buffers, the configuration registers, and the floating-point registers remain unchanged. This functionality is similar to the Pentium INIT pin. The only difference is that the INIT signal does not reset the

Pentium 'model specific registers' whereas the WM_RST does not reset the 6x86 configuration registers. The Pentium 'model specific registers' are not supported on the 6x86. The 6x86 configuration registers are not supported on the Pentium.

3.4. Pins Sampled at RESET

If FLUSH# or WM_RST is sampled asserted at the RESET falling edge, the 6x86 enters tri-state test mode or enters built-in self-test, respectively. This functionality is consistent with the Pentium functionality. The 6x86 also samples the QDUMP# pin at the RESET falling edge. If QDUMP# is sampled asserted (logic low), the 6x86 enables the scatter/gather interface pins. If this 6x86 unique feature is not supported, the QDUMP# input pin should be driven inactive at RESET.

Additionally, the Pentium samples APICEN (PICD1), DPEN# (PICD0), FRCMC#, BRDYC#, BUSCHK#, CPUTYP and BE(0:3) at the falling edge of RESET to enable various functions. The 6x86 does not support these functions.

3.5. System Management Mode

If System Management Mode (SMM) is enabled on the 6x86 (USESMI bit in CCR1 is set), SMIACT# is asserted as the result of servicing a System Management Interrupt (SMI# pin). This functionality is consistent with the Pentium functionality. Additionally, the 6x86 asserts SMIACT# as the result of executing the SMINT instruction or when the SMAC bit (6x86 CCR1 register) is set.

The SMINT instruction provides a mechanism for software to initiate an SMI. The SMAC bit allows software to access SMM space without servicing an SMI. The SMAC bit may be used to initialize system management memory. The Pentium does not support the SMINT instruction or the SMAC bit functionality.

After servicing an SMI, both the 6x86 and Pentium negate the SMIACT# signal as the result of executing the RSM (Resume) instruction.

3.6. Burst Cycle Address Sequence

When performing burst cycles, the Pentium processor only issues the first address for the burst cycle. The remaining three addresses of the burst are not issued by the processor but are assumed to follow the sequences shown in the table below.

PENTIUM BURST SEQUENCES

BURST CYCLE FIRST ADDRESS	ASSUMED BURST CYCLE ADDRESS SEQUENCE
0	0-8-10-18
8	8-0-18-10
10	10-18-0-8
18	18-10-8-0

The 6x86 does not strictly follow the burst cycle address sequence shown in Table 3-1 but provides two different burst modes. The 6x86 burst cycle address sequence modes are referred to as “1+4” and “linear”. After reset, the 6x86 default burst mode is “1+4”. The burst sequences for the “1+4” mode are shown in the table below.

6X86 “1+4” BURST ADDRESS SEQUENCES

BURST CYCLE FIRST ADDRESS	SINGLE READ CYCLE PRIOR TO BURST	ASSUMED BURST CYCLE ADDRESS SEQUENCE
0	None.	0-8-10-18
8	Address 8.	0-8-10-18
10	None.	10-18-0-8
18	Address 18.	10-18-0-8

In “1+4” mode, the 6x86 performs a single read cycle, prior to the burst cycle, if the desired address is (...xx8) or (...xx18). Performing this single read cycles allows the 6x86 to read the critical data. In addition, the 6x86 samples the state of KEN# during this cycle. If KEN# is active, the 6x86 then performs the burst cycle with the address sequence shown in Table 3-2. The 6x86 CACHE# output is not asserted during the single read cycle prior to the burst. Therefore, CACHE# must not be used to qualify the KEN# input to the processor. If the 6x86 CACHE# output is not used to qualify the KEN# input, this burst mode is compatible with chipsets designed for the Pentium. In addition, if KEN# is returned active for the “1” read cycle in the “1+4”, all bytes supplied to the CPU must be valid.

The address sequences for the 6x86's linear burst mode are shown in the table below. Operating the 6x86 in linear burst mode is recommended since it minimizes processor bus activity translating to higher processor-system performance. Linear burst mode can be enabled through the 6x86 configuration registers.

6x86 Linear Burst Address Sequences

BURST CYCLE FIRST ADDRESS	ASSUMED BURST CYCLE ADDRESS SEQUENCE
0	0-8-10-18
8	8-10-18-0
10	10-18-0-8
18	18-0-8-10

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