AMD-K6™E Processor Family CompactPCI CPU Board Schematics

AMD-K6E CompactPCI (M1541/43) REFERENCE SCHEMATICS

*** NOTICE ***

These are schematics of a design example

developed by ACER LABS (a5schv22). It has been

modified by Stellcom Technologies, Inc. for AMD.

Revision notes are referenced to the Aladdin V Reference

schematics version 2.2.

1. CIRCUIT HISTORY LIST:

REVISION	TOTAL PAGES	MODIFIED PAGES	ERRATA NO.	DATE
1.0	29	Aladdin V Reference Schematic, Version 2.2	----	05/13/98
1.1	30	1-2	----	08/07/98

			----	

2. CPU SUBSYSTEM CHANGES FROM REV B:

PAGE 2: UPDATE REVISION NOTES
PAGE 3: UPDATE PAGE NOTES
PAGE 9: REMOVE 1 DIMM MODULE
PAGE 13: REMOVE USB, IDE TERMINATIONS
PAGE 14: REMOVE SD[7:0] PU
PAGE 16: REMOVE IDE PAGE
PAGE 20: REMOVE PWG, SPEAKER, PWR BUTTON CIRCUIT
PAGE 21: REMOVED 2ND SER PORT, CHANGE RS-232 DRIVER
PAGE 22: REMOVE USB
PAGE 24: REMOVE AT POWER SUPPLY, CHANGE SWITCHING SUPPLY SOURCE FROM 12V TO 5V
PAGE 25: REMOVE AT POWER SUPPLY

|LINK
|2.SCH
|3.SCH
|4.SCH
|5.SCH
|6.SCH
|7.SCH
|8.SCH
|9.SCH
|10.SCH
|11.SCH
|12.SCH
|13.SCH
|14.SCH
|15.SCH
|16.SCH
|17.SCH
|18.SCH
|19.SCH
|20.SCH
|21.SCH
|22.SCH
|23.SCH
|24.SCH
|25.SCH
|26.SCH
|27.SCH
|28.SCH
|29.SCH
|30.SCH
|31.SCH
|32.SCH

AMD

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LAYOUT NOTES:

MANUAL ROUTE THE FOLLOWING SUBSYSTEMS IN ORDER

MATCH CPU, L2 CACHE, DRAM, AND PCI CLOCKS TO WITHIN 3mils. (LAYERS 6, 7).
MATCH CPCI CLOCKS TO WITHIN 10mils (LAYERS 6, 7).
M1541 TO SDRAM INTERFACE, MATCH SIGNALS TO WITHIN 1.5" (LAYERS 4,3,9,10).
CPU TO L2 CACHE AND M1541, ROUTE FROM CPU TO L2 CACHE TO 1541. MAX 2" BETWEEN CPU AND L2 CACHE. MAX 4" BETWEEN L2 CACHE AND 1541. (LAYERS 4,3,9,10).
M1541 TO TAG SRAM, MAX 2.5" TRACE LENGTH (LAYERS 4,3,9,10).
ROUTE THE FOLLOWING CPU SIGNALS WITH 12 MIL CLEARANCE:
HADSJ, HADSCJ, HWRJ, BOFFJ, HBRDYJ, EADSJ, CPUINIT, INTR, NMI, CPURST, SMIJ, STPCLKJ
21150 INTERFACE TO CPCI CONNECTOR (LAYERS 4,3,9,10).
M1541 PCI INTERFACE TO ALL PCI DEVICES (LAYERS 4,3,9,10).
ROUTE THE FOLLOWING PCI SIGNALS WITH 12 MIL CLEARANCE:
PCI_FRAMEn, PCI_IRDYn, PCI_TRDYn, PCI_DEVSELn, PCI_STOPn, PCI_LOCKn, PCI_PERRn, PCI_SERRn, PCI_PAR
ROUTE CPU FAN POWER/GND WITH FAT TRACES.
ROUTE CPCI VCCIO WITH FAT TRACES.
CONNECT CPCI IDSELs TO CORRESPONDING ADDRESS LINES WITH MINIMUM TRACE LENGTH.
CPCI SIGNAL LENGTHS NEED TO BE 1.5" OR LESS BETWEEN IC PIN AND CPCI CONNECTOR.
FLASH TARGET INTERFACE (ANY LAYER).
M1543 IO (ANY LAYER).
ROUTE THE FOLLOWING SIGNALS WITH 12 MIL CLEARANCE:
SYS_RSTn, SW_RESET, FL_RSTn, SPCI_PRSTn, SPCI_FALn
MS_CLK, KB_CLK, SMBCLK, AO_CLK, AO_RSTn, AO_PTATNn, AO_DXFER
RTCAS, RTCRW, RTCDS

ASSEMBLY NOTES:

1. DO NOT STUFF THE FOLLOWING COMPONENTS:
   C28, C30
   R14, R25, R26, R42, R58, R79, R111, R155, R156, R164, R140, R143
   U13
   JP2, JP3, P2

2. INSTALL PGA321 SOCKET AT U16
   INSTALL 32 PIN PLCC SOCKET AT U6.
   INSTALL DIMM168 SOCKET AT DIMM1.
   ARROW (NOT DOT) IS PIN 1 INDICATOR ON AM29F032-75FC PARTS

3. WIND 7 TURNS OF 20AWG MAGNET WIRE AROUND T30-26 BEFORE INSTALLING AT L13.

4. INSTALL R10 FROM R10p2 TO R10p3 (RIGHT PADS)
   INSTALL R38 FROM R38p2 TO R38p3 (RIGHT PADS)
   INSTALL R12 FROM R12p2 TO R12p3 (RIGHT PADS)
   INSTALL R36 FROM R36p2 TO R36p3 (RIGHT PADS)

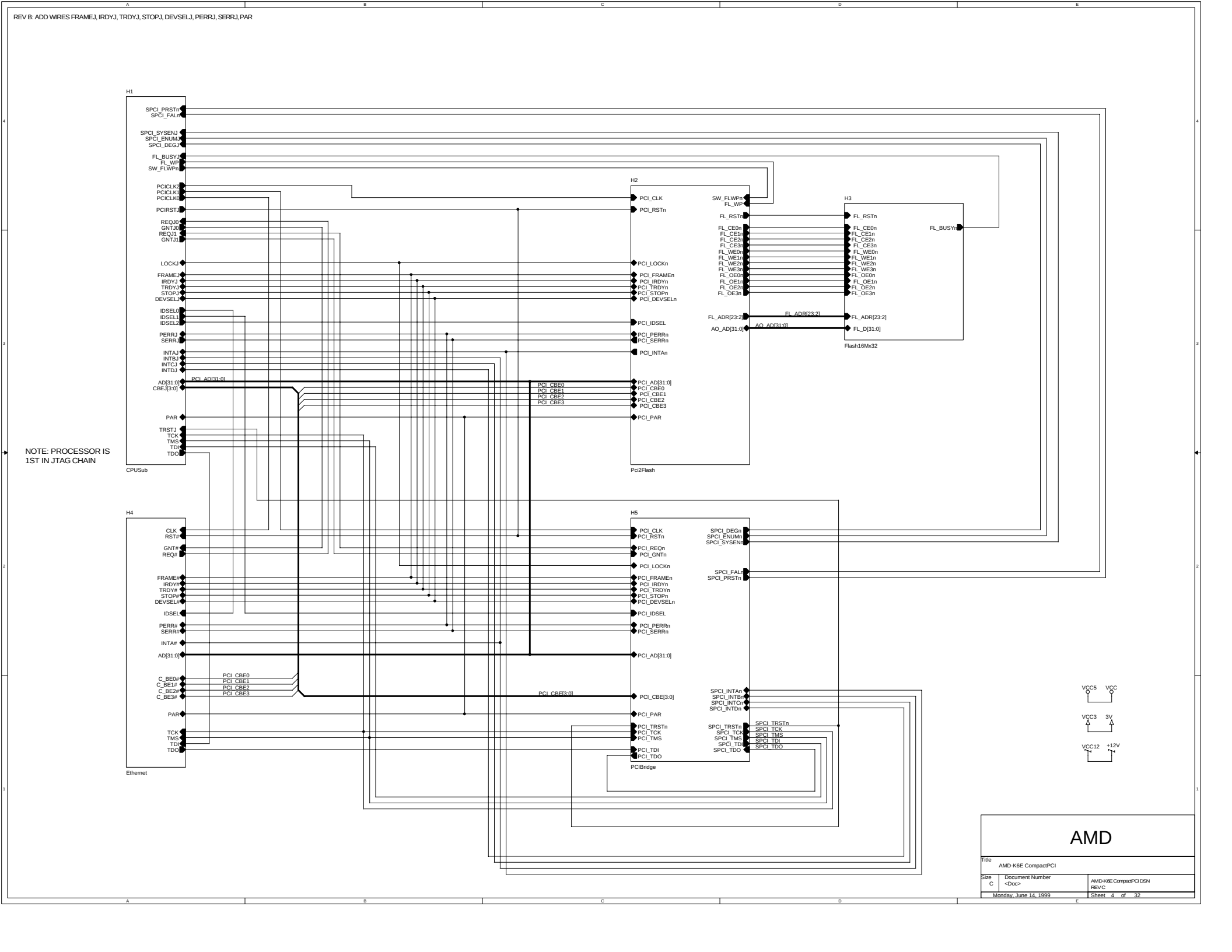
5. INSTALL WIRE FROM JP2p4 TO JP2p5
   INSTALL WIRE FROM JP3p1 TO JP3p2

6. INSTALL 2 PIN JUMPER JP1p1 TO JP1p2 (TOP PINS).
   INSTALL 2 PIN JUMPER JP2p4 TO JP2p5 (BOTTOM PINS).
   INSTALL 2 PIN JUMPER JP3p1 TO JP3p2.
   INSTALL 2 PIN JUMPER JP4p2 TO JP4p3 (LEFT PINS).
   INSTALL 2 PIN JUMPER JP6p3 TO JP6p4 (MIDDLE PINS).
   INSTALL 2 PIN JUMPER JP7p3 TO JP7p4 (MIDDLE PINS).
   INSTALL 2 PIN JUMPER JP10p3 TO JP10p4 (2ND FROM TOP).

7. INSTALL HEATSINK ON CPU, JUMPER WIRE SHOULD BE ON JP5p1 (RED WIRE) TO JP5p2 (BLACK WIRE)

8. WIRE U8pK18 TO R98p1 (RIGHT PAD), CIRCUIT SIDE.

REV B: ADD WIRES FRAMEJ, IRDYJ, TRDYJ, STOPJ, DEVSELJ, PERRJ, SERRJ, PAR



NOTE: PROCESSOR IS
1ST IN JTAG CHAIN

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REV B: GND U20pA3

U12

AMD-K6-2/300AFR

CORE/BUS RATIO

BF2	BF1	BF0	CPU FREQ
1	1	0	2.0X
1	0	0	2.5X
1	0	1	3.0X
1	1	1	3.5X
0	1	0	4.0X
0	0	0	4.5X
0	0	1	5.0X
0	1	1	5.5X

05/13/98 UPDATED

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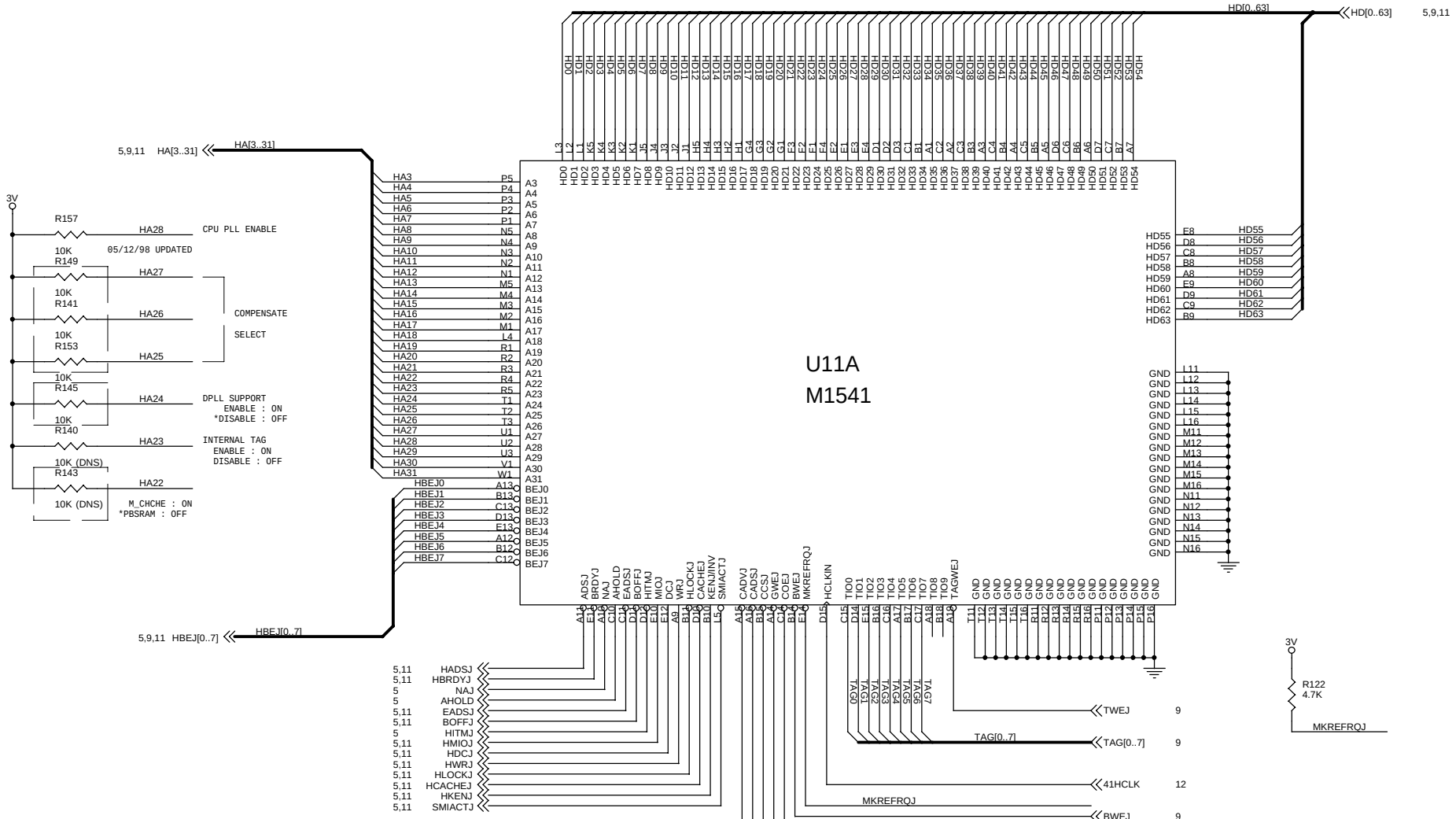
NOTE: HAND ROUTE 1541 TO CPU INTERFACE.



NOTE:

YOU MAY USE HA20/21 & HA29/30/31 TO INDICATE THE L2 SIZE & HOST FREQ.,
THEN BIOS CAN DIRECT GET INFORMATION FROM M1541 (PLEASE REFER SECTION5
IN M1541 DATA SHEET), AND SAVE MORE CODE SPACE FOR SIZING.

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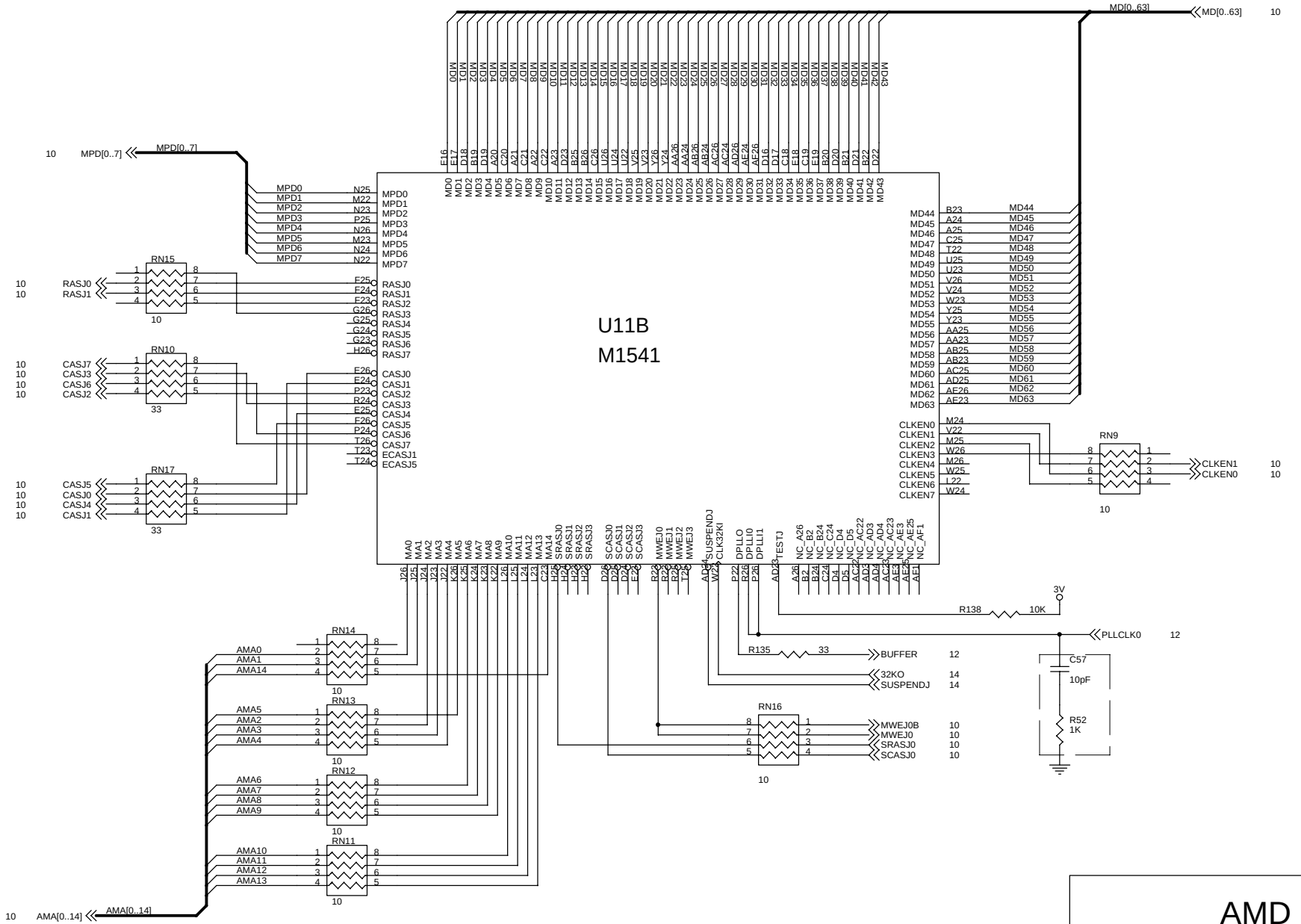
NOTE: HAND ROUTE 1541 TO SDRAM INTERFACE.



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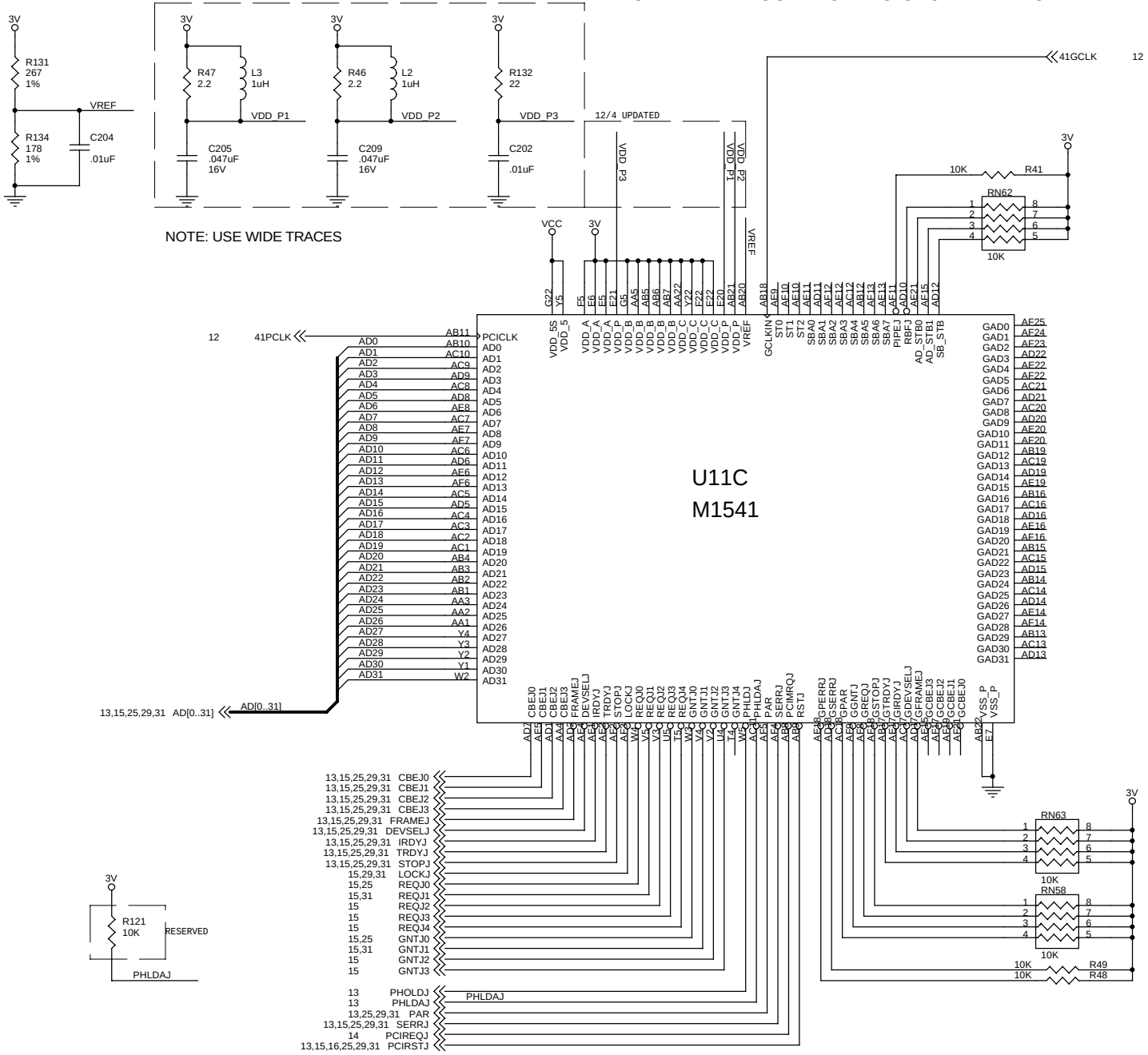
NOTE: HAND ROUTE 1541 TO CPU INTERFACE.



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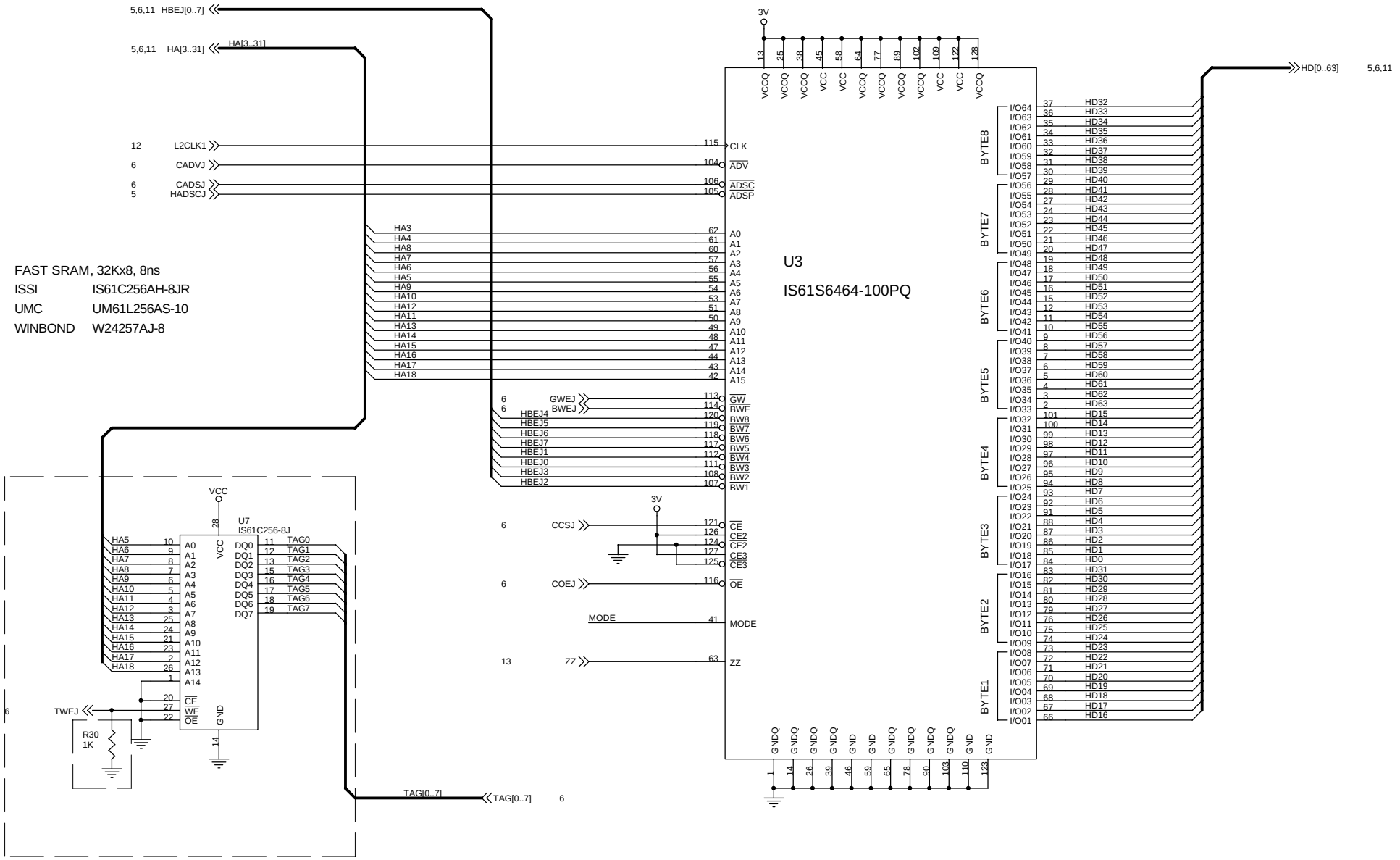
NOTE: HAND ROUTE CACHE TO CPU INTERFACE.



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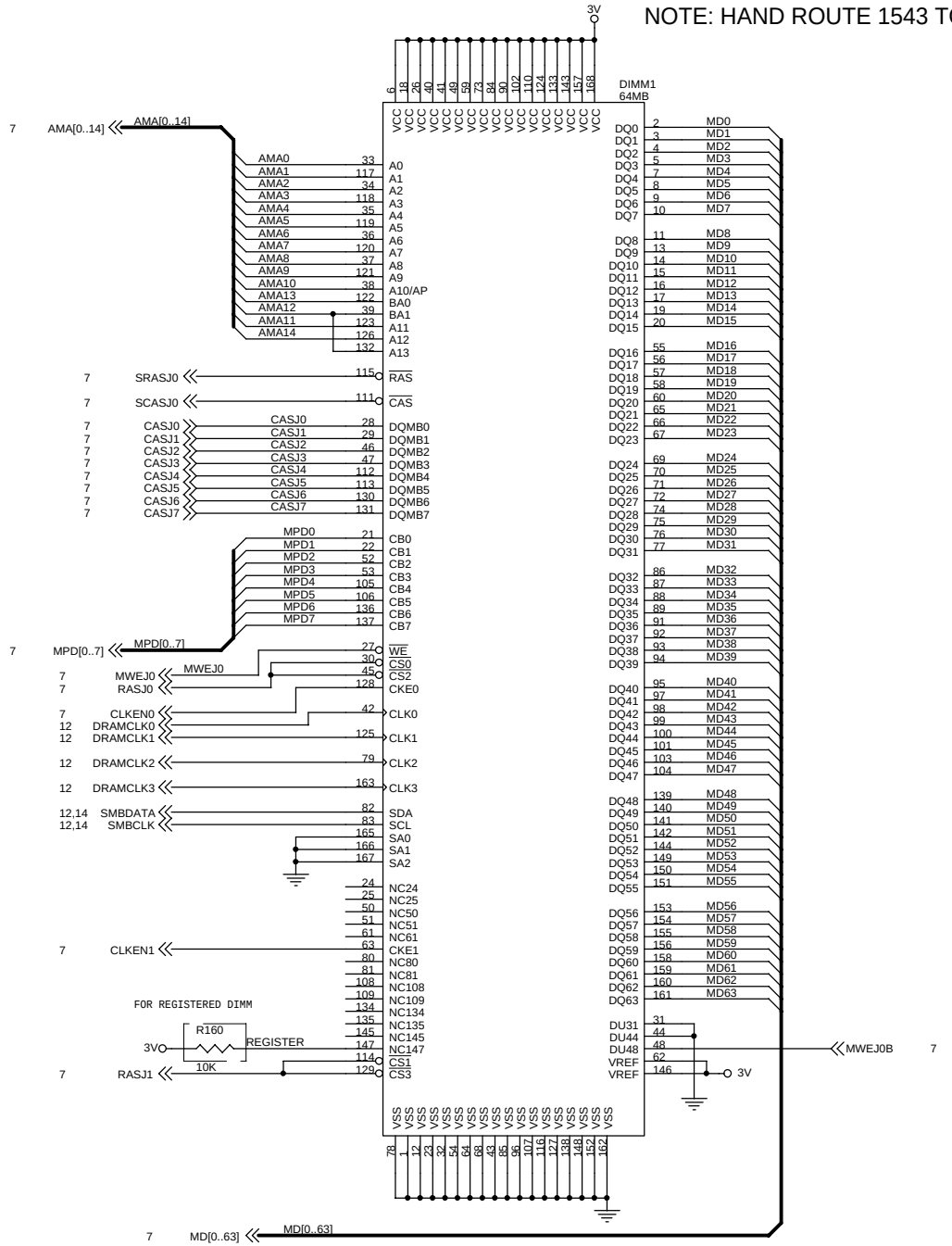
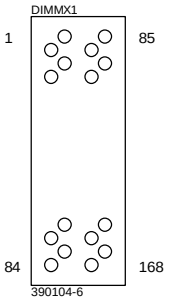
NOTE: HAND ROUTE 1543 TO SDRAM INTERFACE.





DAISY CHAIN RASJX, CASJX, MWEJX

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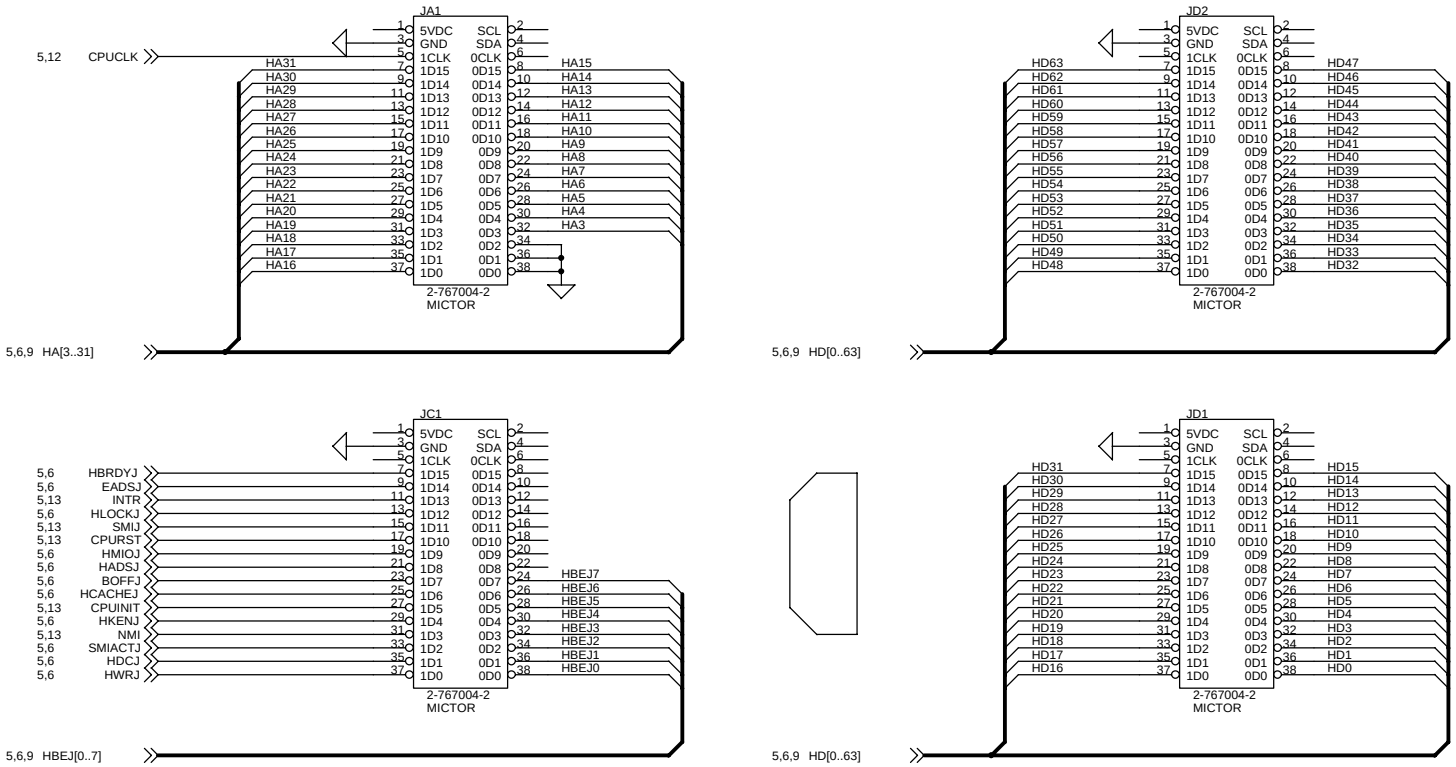
PLACE TEST HEADERS NEAR CPU (PAGE4)



NOTE: GND MICTOR MOUNTING HOLES

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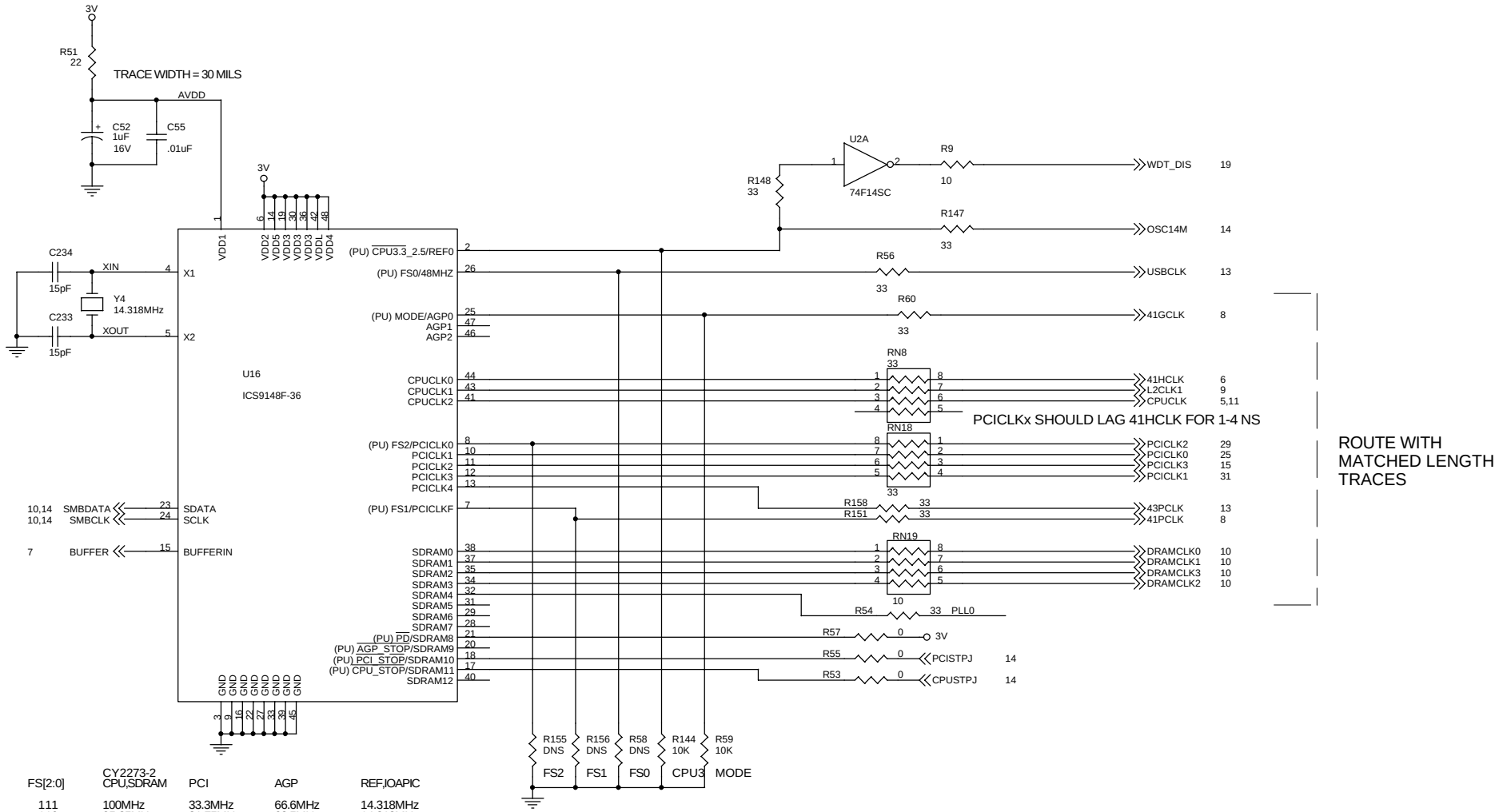
REV B: REMOVED SERIES RESISTORS FOR DRAMCLK[7:0], TSTCLK[1:0]

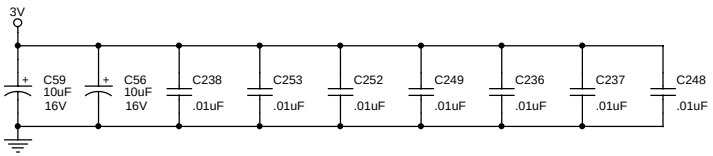


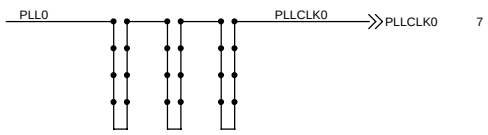
CY2273-2

FS[2:0]	CPU,SDRAM	PCI	AGP	REF,IOAPIC
111	100MHz	33.3MHz	66.6MHz	14.318MHz
110	95.25MHz	31.75MHz	63.5MHz	14.318MHz
101	83.3MHz	33.3MHz	66.6MHz	14.318MHz
100	75MHz	30MHz	60MHz	14.318MHz
011	75MHz	37.5MHz	75MHz	14.318MHz
010	68.5MHz	34.25MHz	68.5MHz	14.318MHz
001	66.8MHz	33.4MHz	66.8MHz	14.318MHz
000	60MHz	30MHz	60MHz	14.318MHz

THE TOTAL LENGTH = LENGTH OF DRAM CLK + 10INCH

PLEASE REFER "LAYOUT GUIDE".





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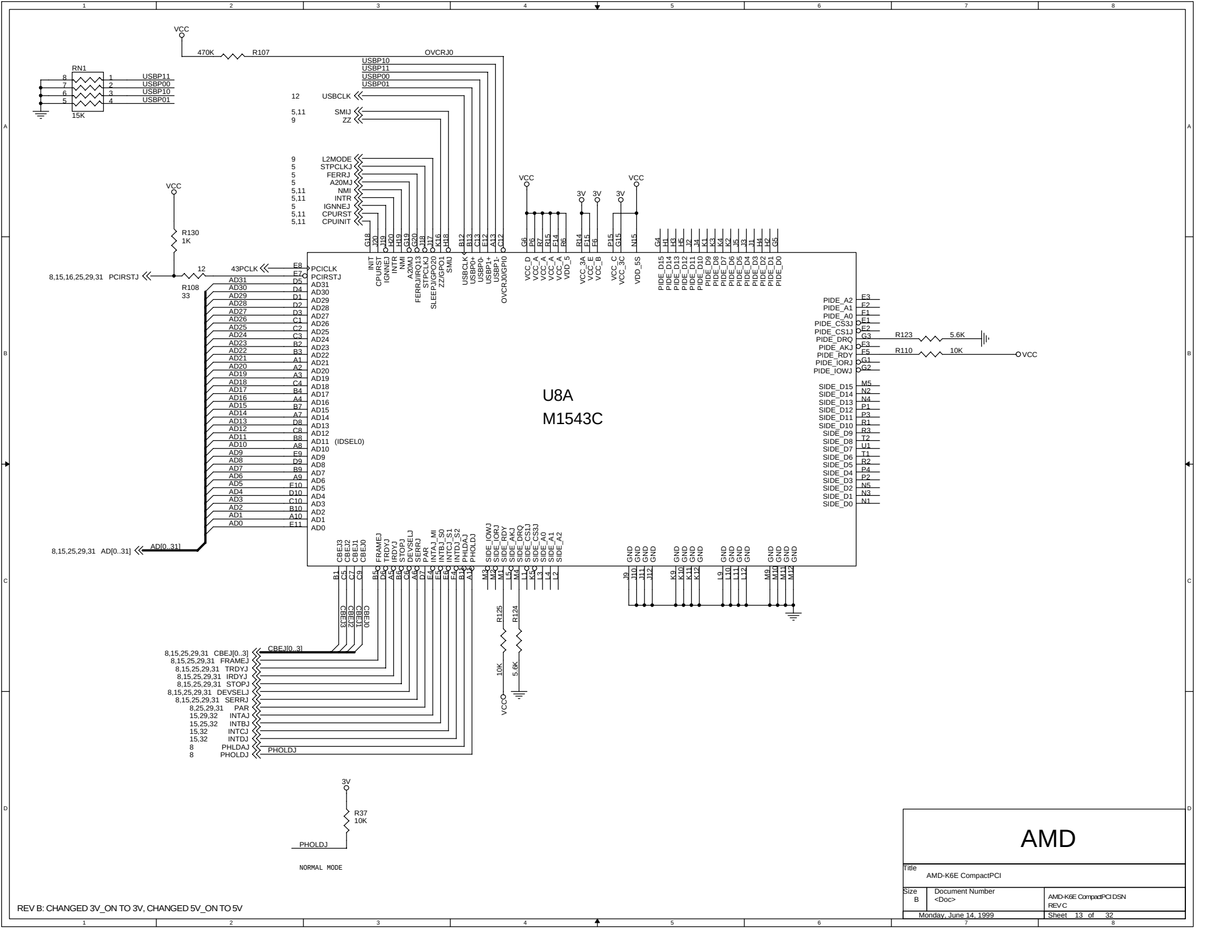
VCC
470K
R107
OVCRJ0
RN1
15K
USBP11
USBP00
USBP10
USBP01
USBP10
USBP11
USBP00
USBP01
12 USBCLK
5,11 SMIJ
9 ZZ
9 L2MODE
5 STPCLKJ
5 FERRJ
5 A20MJ
5,11 NMI
5,11 INTR
5 IGNNEJ
5,11 CPURST
5,11 CPUINIT
R130
1K
8,15,16,25,29,31 PCIRSTJ
12
R108
33
43PCLK
PCICLK
PCIRSTJ
AD31
AD30
AD29
AD28
AD27
AD26
AD25
AD24
AD23
AD22
AD21
AD20
AD19
AD18
AD17
AD16
AD15
AD14
AD13
AD12
AD11 (IDSEL0)
AD10
AD9
AD8
AD7
AD6
AD5
AD4
AD3
AD2
AD1
AD0
8,15,25,29,31 AD[0..31]
AD[0..31]
U8A
M1543C
PIDE_A2
PIDE_A1
PIDE_A0
PIDE_CS3J
PIDE_CS1J
PIDE_DRQ
PIDE_AKJ
PIDE_RDY
PIDE_IORJ
PIDE_IOWJ
R123
5.6K
R110
10K
VCC
SIDE_D15
SIDE_D14
SIDE_D13
SIDE_D12
SIDE_D11
SIDE_D10
SIDE_D9
SIDE_D8
SIDE_D7
SIDE_D6
SIDE_D5
SIDE_D4
SIDE_D3
SIDE_D2
SIDE_D1
SIDE_D0
CBEJ3
CBEJ2
CBEJ1
CBEJ0
FRAMEJ
TRDYJ
IRDYJ
STOPJ
DEVSELJ
SERRJ
PAR
INTAJ_MI
INTBJ_S0
INTCJ_S1
INTDJ_S2
PHLDAJ
PHOLDJ
SIDE_IOWJ
SIDE_IORJ
SIDE_RDY
SIDE_AKJ
SIDE_DRQ
SIDE_CS1J
SIDE_CS3J
SIDE_A0
SIDE_A1
SIDE_A2
GND
R125
10K
R124
5.6K
VCC
8,15,25,29,31 CBEJ[0..3]
CBEJ[0..3]
8,15,25,29,31 FRAMEJ
8,15,25,29,31 TRDYJ
8,15,25,29,31 IRDYJ
8,15,25,29,31 STOPJ
8,15,25,29,31 DEVSELJ
8,15,25,29,31 SERRJ
8,25,29,31 PAR
15,29,32 INTAJ
15,25,32 INTBJ
15,32 INTCJ
15,32 INTDJ
8 PHLDAJ
8 PHOLDJ
PHOLDJ
3V
R37
10K
PHOLDJ
NORMAL MODE
REV B: CHANGED 3V_ON TO 3V, CHANGED 5V_ON TO 5V
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REV B: REMOVED RSM CIRCUIT, WIRE SYS_RSTn TO K18

REV C: ADDED SW_FLWPn

U8B
M1543C

FOR M1543C

Function selection by "TC", refer right-bottom corner.

M1543: PULL HIGH ONLY
M1543C- HIGH : HOTKEY DISABLE
LOW : HOTKEY ENABLE

256K ROM

NORMAL MODE

LOW : SD[0..7]
HIGH : GPIO[0..7] or FIR/USB function
REFER AP NOTE

(1-2) : NO HOTKEY, FOR M1543

(2-3) : HOTKEY, FOR M1543C

PENTIUM CPU

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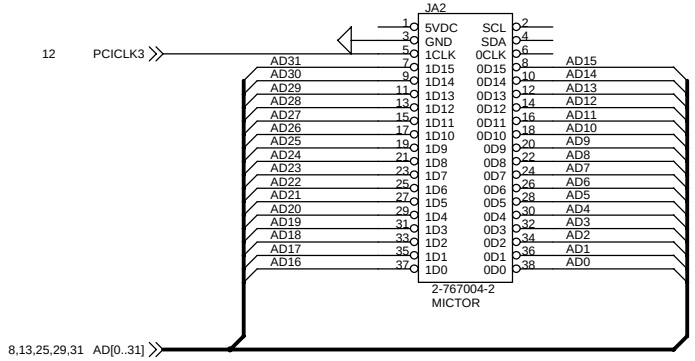
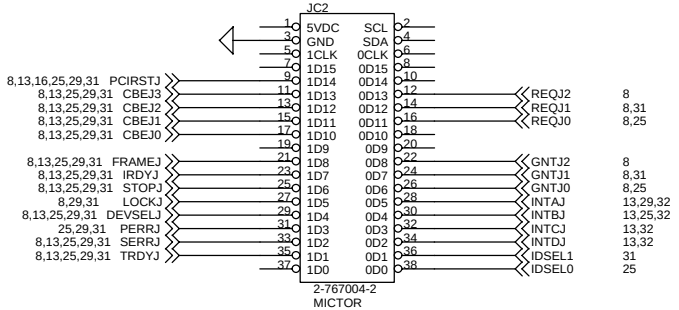
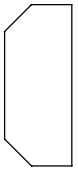
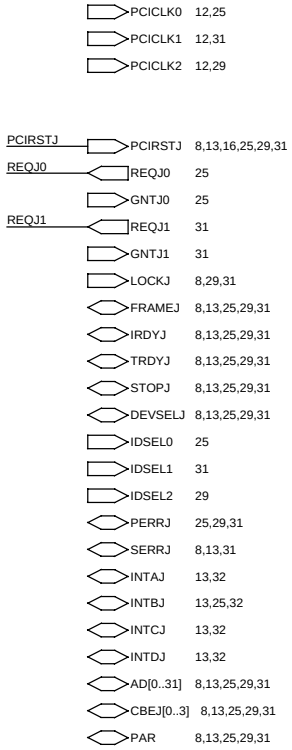


NOTE: GND MICTOR MOUNTING HOLES

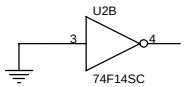


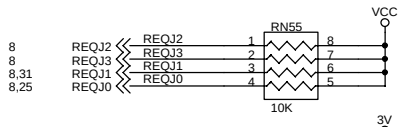


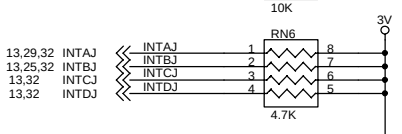


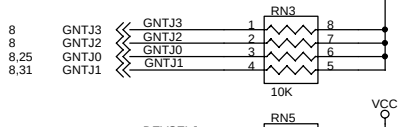
INTERRUPT	DESCRIPTION	1543 CONFIG PIN
IRQ0	SYSTEM TIMER	
IRQ1	KB INH	(PU - RTS2J)
IRQ2	PROG INT CTRL	
IRQ3	COM2	
IRQ4	COM1	
IRQ5	CPCI ENUMERATE	
IRQ6	FLOPPY DISK CTRL	
IRQ7	LPT1	
IRQ8	RTC INT	
IRQ9	GEN PURPOSE	
IRQ10	KB DATA	(PU - RTS2J, PU PCSJ)
IRQ11	PCI INT	
IRQ12	MOUSE DATA	(PU - DTR2J)
IRQ13	FP ERROR	
IRQ14	AGP INTA	
IRQ15	AGP INTB	
SIRQI	IDE PRIMARY	
SIRQII	IDE SECONDARY	

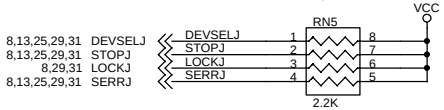
C/BE[3:0]	ADDRESS CYCLE DESCRIPTION
0000	INT ACK
0001	SPECIAL CYCLE
0010	IO READ
0011	IO WRITE
0100	RESERVED
0101	RESERVED
0110	MEM READ
0111	MEM WRITE
1000	RESERVED
1001	RESERVED
1010	CONF READ
1011	CONF WRITE
1100	MEM READ MULTIPLE
1101	DUAL ADDRESS CYCLE
1110	MEM READ LINE
1111	MEM WRITE & INVALIDATE

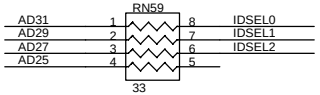




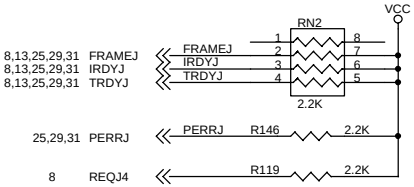


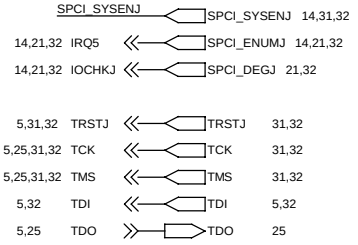


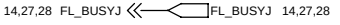




ETHERNET
PCI 2 PCI BRIDGE
S5920 PCI SLAVE







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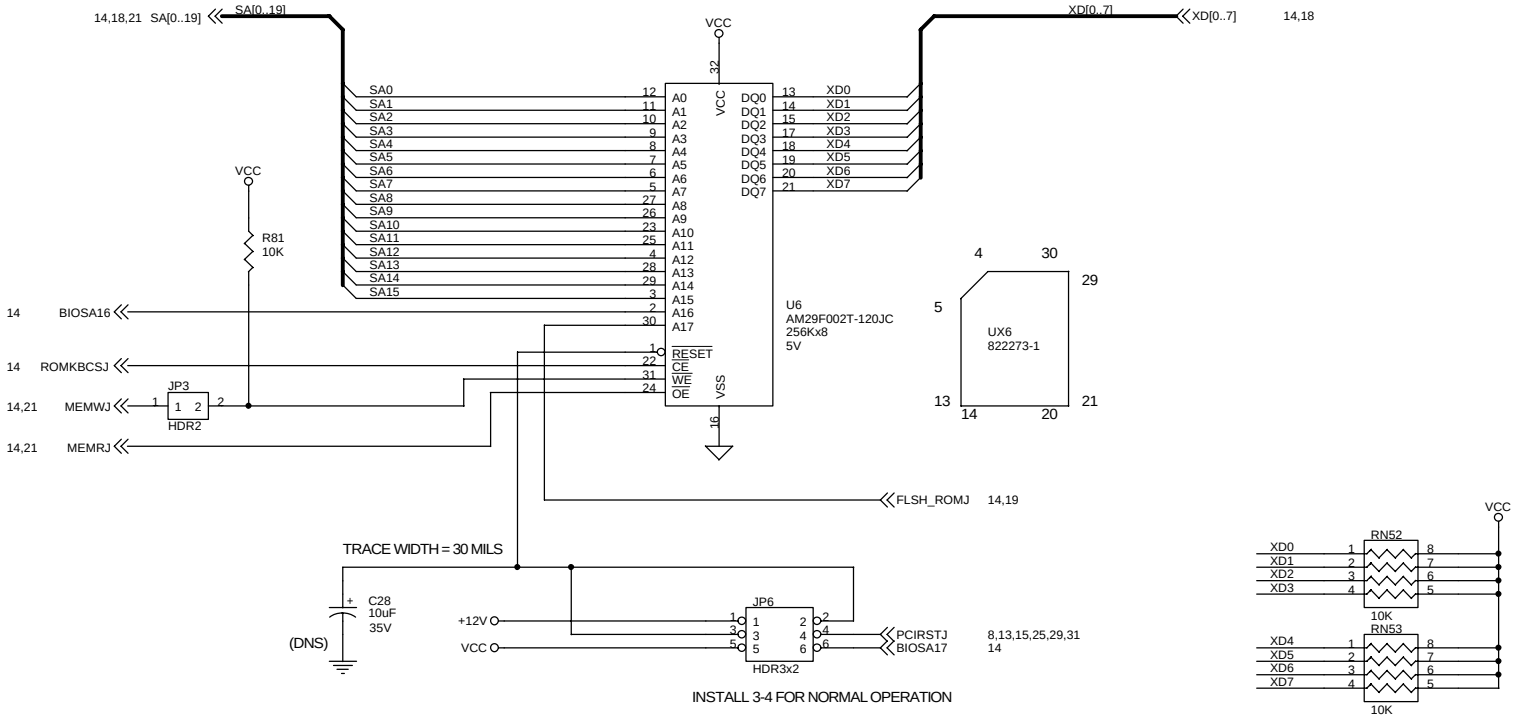
REV B: REMOVED 74LS245 IO BUFFER

INSTALL 32 PIN SOCKET



SX2
2JM-G

VCC
C128
.01uF

FLASH ROM VOLTAGE	MANUFACTURER	SIZE
+5V	AMD, AM29F002T-120P	2MB

AMD

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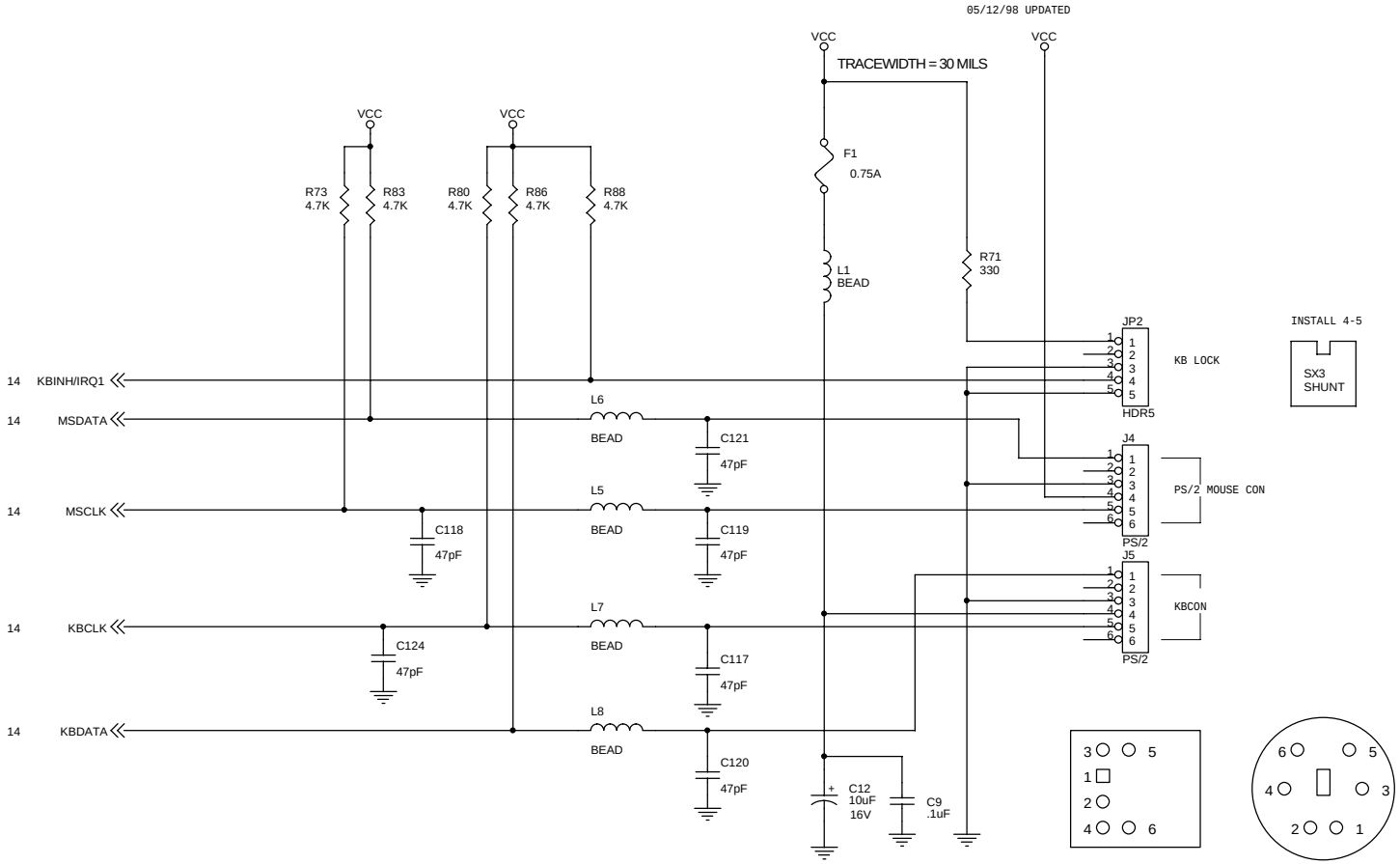
REV B: CHANGED 3V_ON TO 3V, CHANGED 5V_ON TO 5V



VSS

AMD

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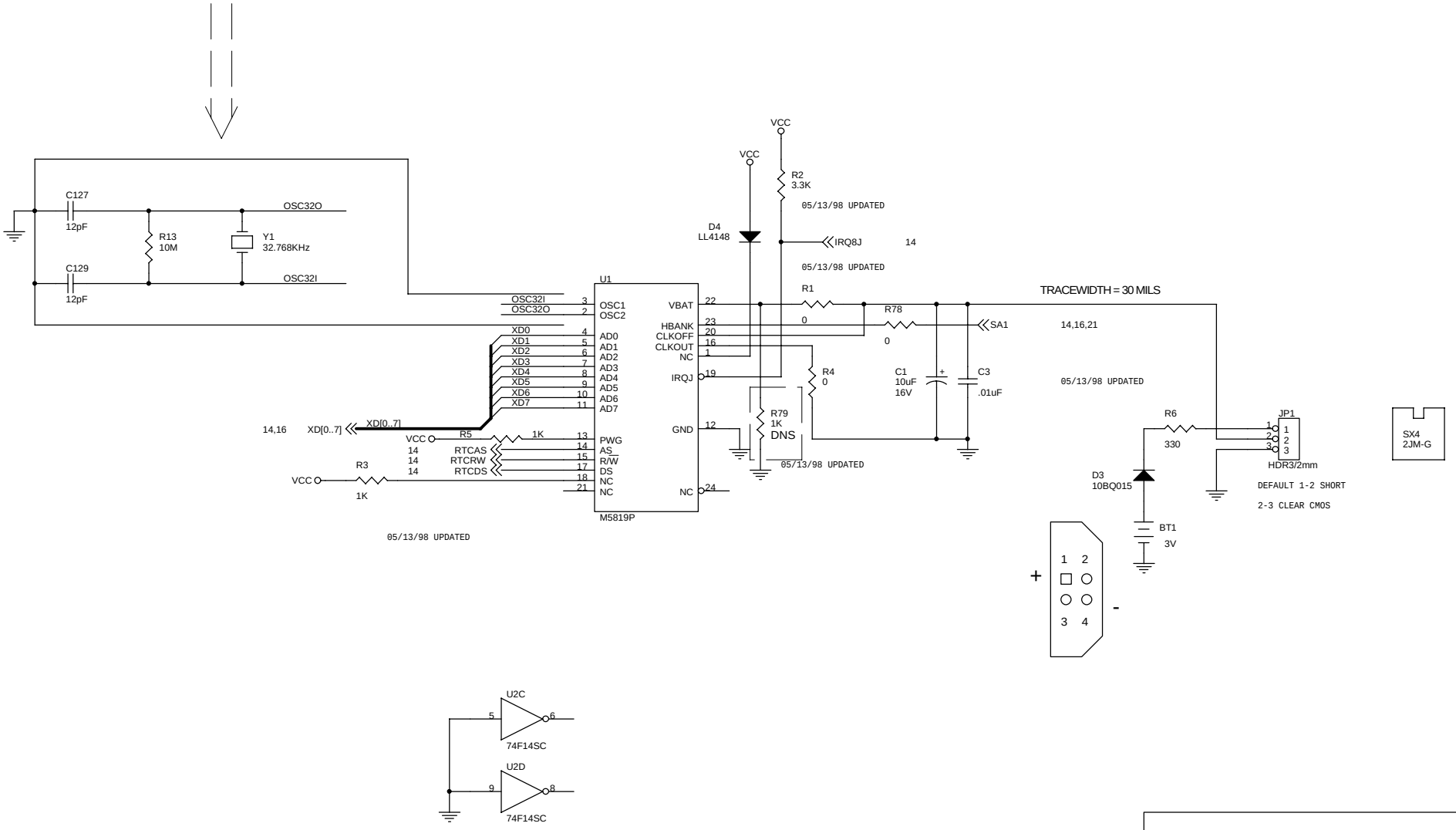
REV B: CHANGED 5V_ON TO VCC

PLACE THIS BLOCK AS CLOSE M5819 AS POSSIBLE

PLACE THIS BLOCK SURROUNDED BY GND LINE AND DO NOT HAVE ANY THROUGH HOLE



AMD		
Title: AMD-K6E CompactPCI		
Size: B	Document Number: <Doc>	AMD-K6E CompactPCI DSN REV C
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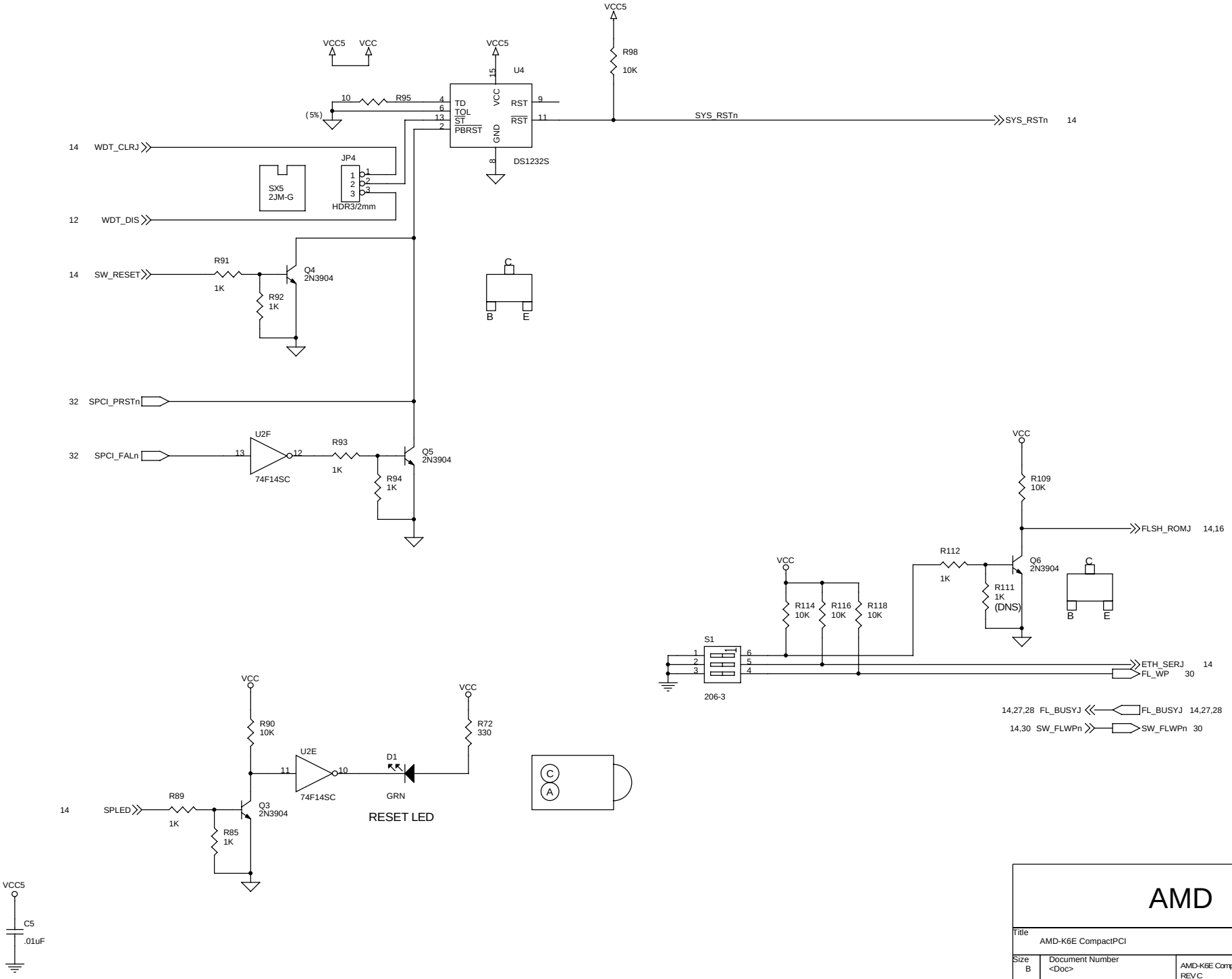
REV B: ADD SYS_RSTn, ADD INVERTER TO SPLED, CHANGED 5V_ON TO 5V

REV C: ADD SW_FLWPn



AMD

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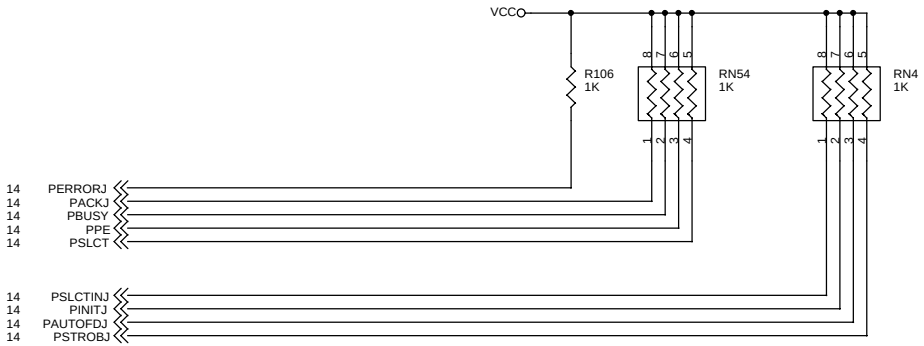
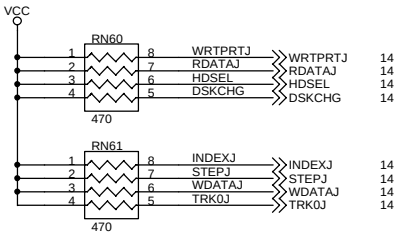
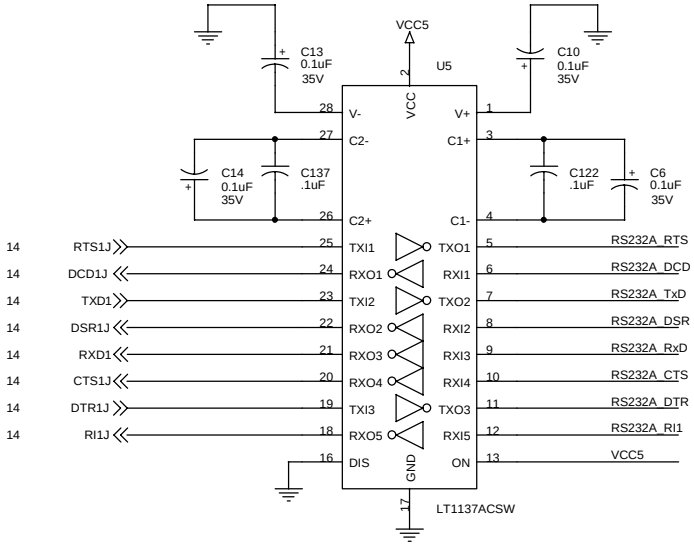
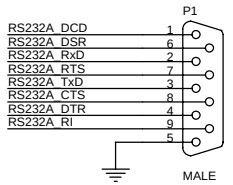
REV B: CHANGED 5V_ON TO 5V

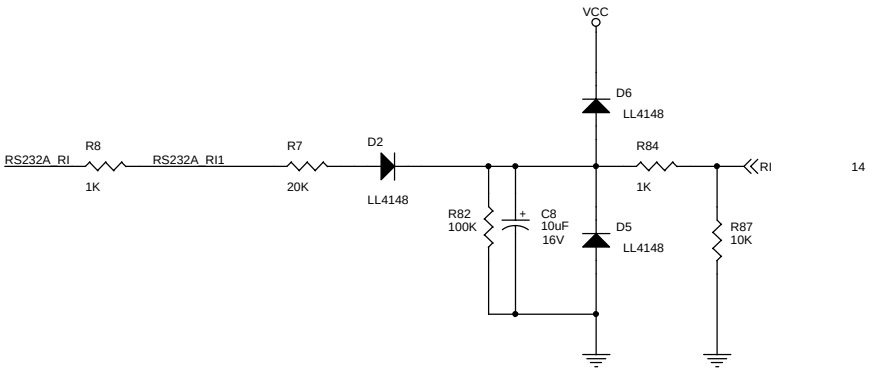






DEBUG SERIAL





AMD

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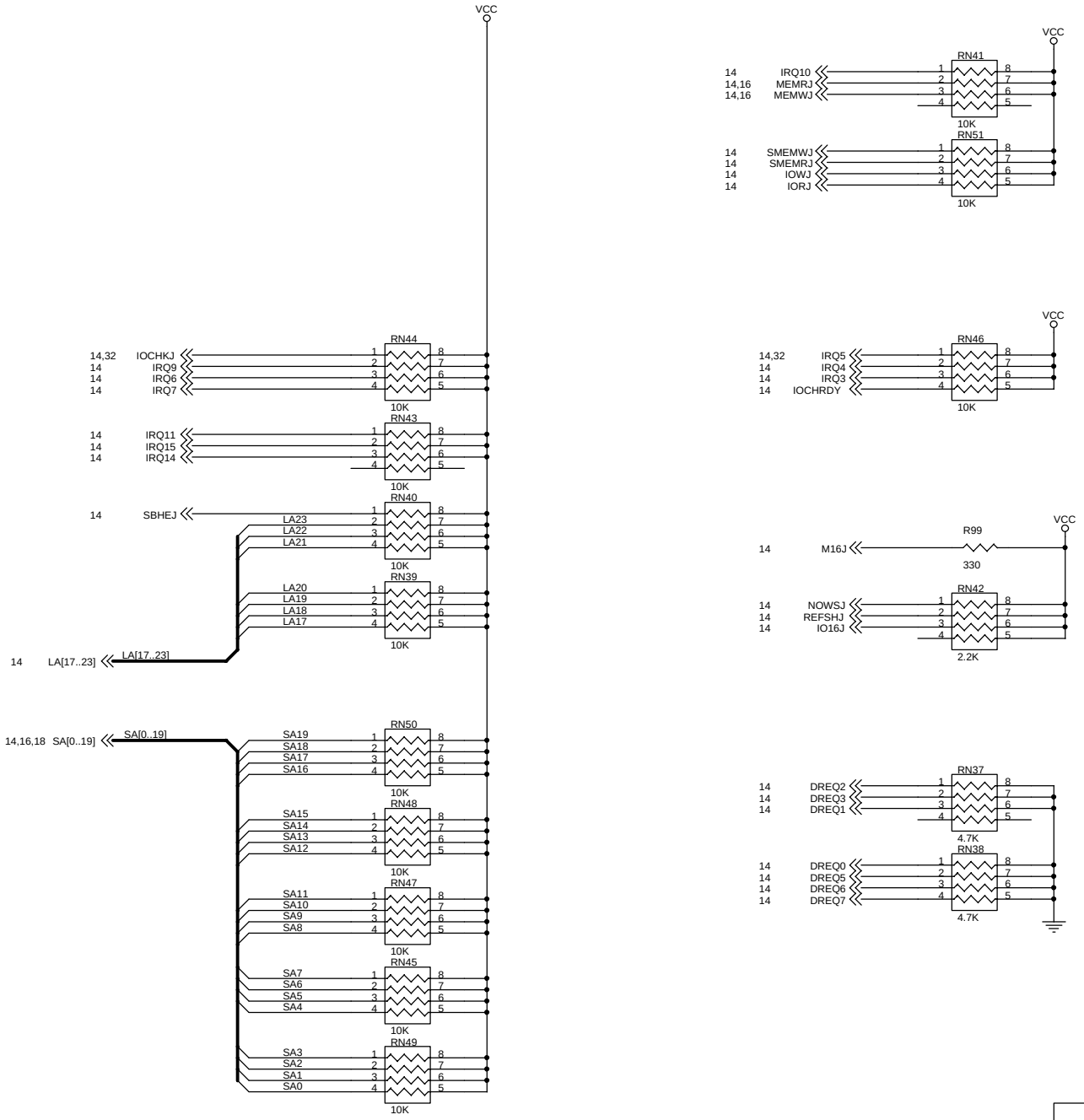

AMD

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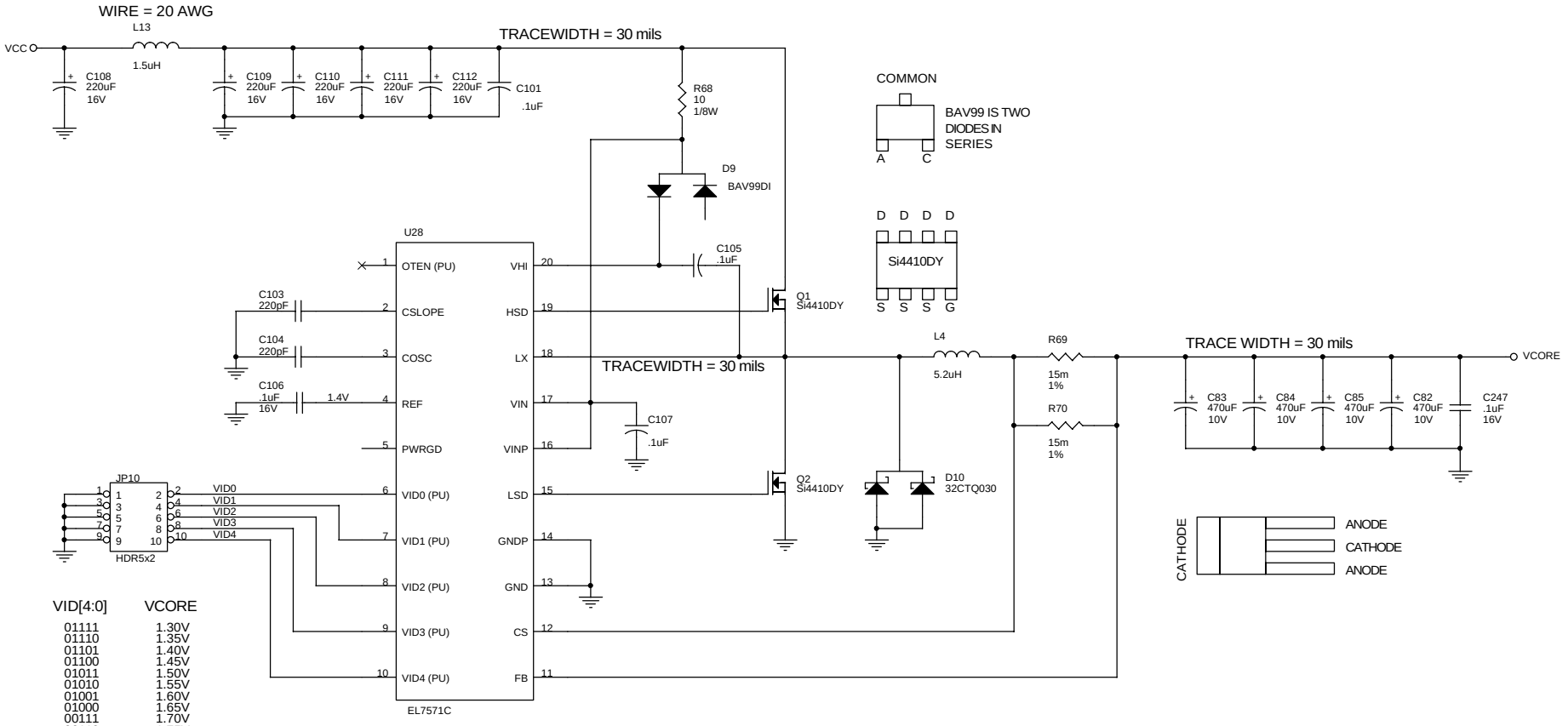
REV B: REPLACED SWITCHING POWER SUPPLY



VID[4:0]	VCORE
01111	1.30V
01110	1.35V
01101	1.40V
01100	1.45V
01011	1.50V
01010	1.55V
01001	1.60V
01000	1.65V
00111	1.70V
00110	1.75V
00101	1.80V
00100	1.85V
00011	1.90V
00010	1.95V
00001	2.00V
00000	2.05V
11111	NO CPU
11110	2.10V
11101	2.20V
11100	2.30V
11011	2.40V
11010	2.50V
11001	2.60V
11000	2.70V
10111	2.80V
10110	2.90V
10101	3.00V
10100	3.10V
10011	3.20V
10010	3.30V
10001	3.40V
10000	3.50V

AMD

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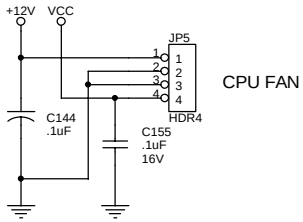
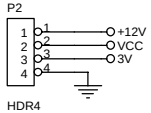
REV B: REMOVE 3V_ON, 5V_ON, 5V_SB CIRCUIT

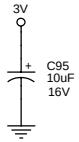
USE FAT TRACES TO DRIVE FAN POWER

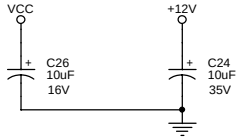


CPU FAN

USE LARGE THROUGH HOLE







PLACE NEAR CPU FAN CONNECTOR

AMD

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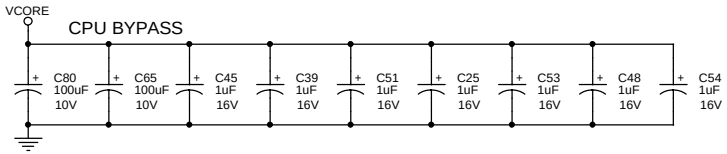

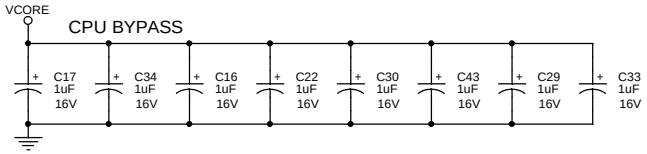

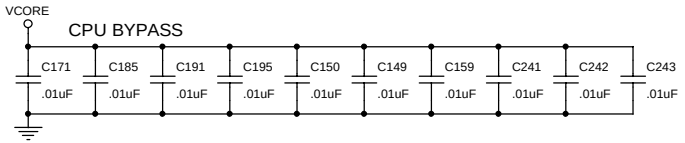

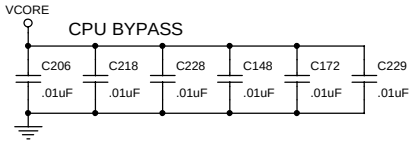

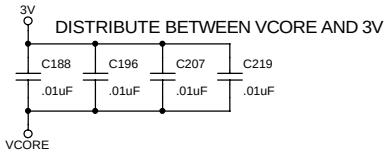

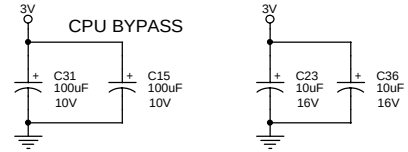

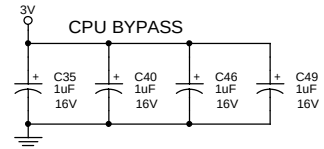

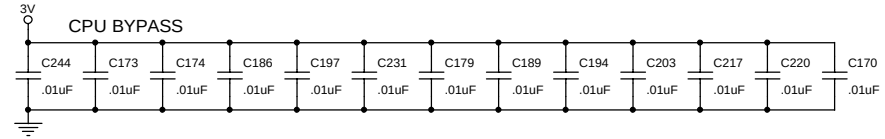

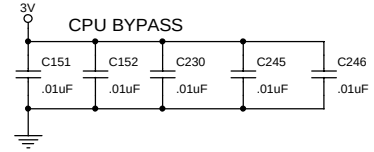

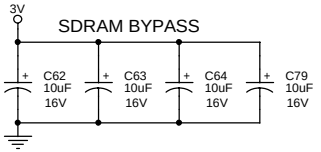

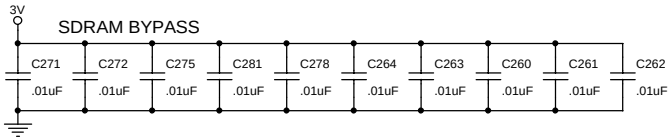

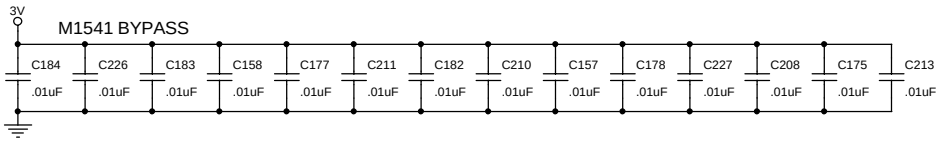

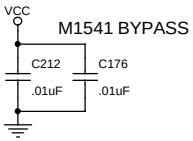

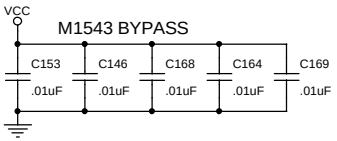

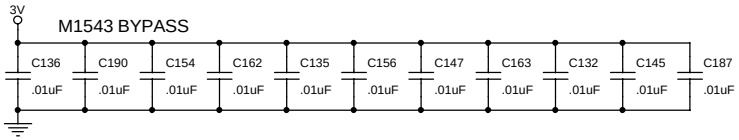

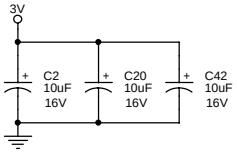

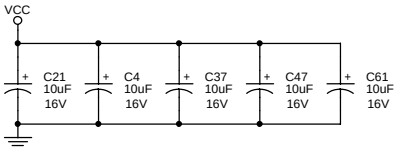

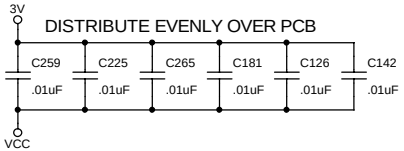

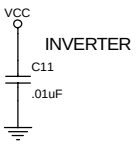

AMD

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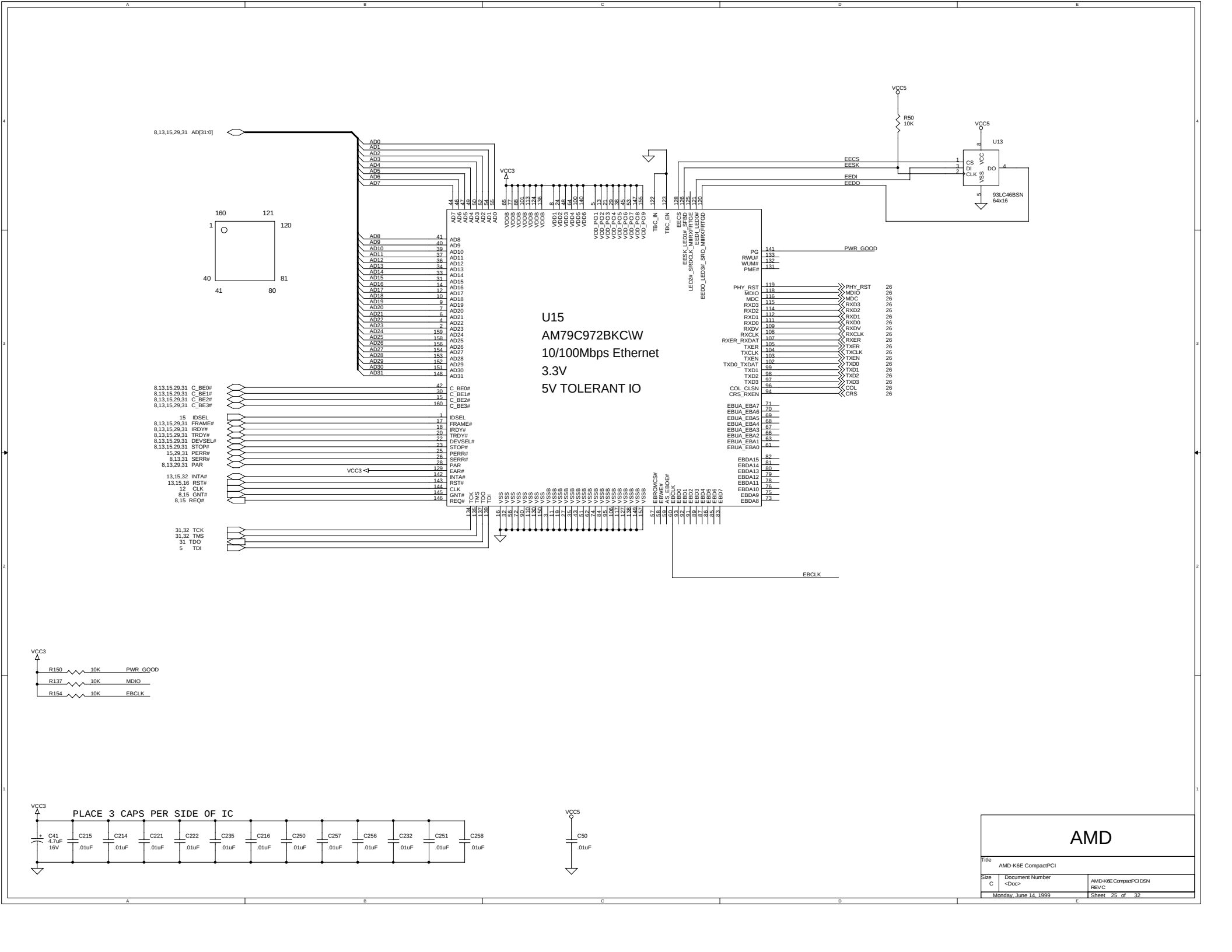
U15
AM79C972BKC\W
10/100Mbps Ethernet
3.3V
5V TOLERANT IO
8,13,15,29,31 AD[31:0]
VCC3
VCC5
R50
10K
U13
93LC46BSN
64x16
EECS
EESK
EEDI
EEDO
PWR_GOOD
PHY_RST
MDIO
MDC
RXD3
RXD2
RXD1
RXD0
RXDV
RXCLK
RXER
TXER
TXCLK
TXEN
TXD0
TXD1
TXD2
TXD3
COL
CRS
EBCLK
8,13,15,29,31 C_BE0#
8,13,15,29,31 C_BE1#
8,13,15,29,31 C_BE2#
8,13,15,29,31 C_BE3#
15 IDSEL
8,13,15,29,31 FRAME#
8,13,15,29,31 IRDY#
8,13,15,29,31 TRDY#
8,13,15,29,31 DEVSEL#
8,13,15,29,31 STOP#
15,29,31 PERR#
8,13,31 SERR#
8,13,29,31 PAR
13,15,32 INTA#
13,15,16 RST#
12 CLK
8,15 GNT#
8,15 REQ#
31,32 TCK
31,32 TMS
31 TDO
5 TDI
R150 10K PWR_GOOD
R137 10K MDIO
R154 10K EBCLK
PLACE 3 CAPS PER SIDE OF IC
C41 4.7uF 16V
C215 .01uF
C214 .01uF
C221 .01uF
C222 .01uF
C235 .01uF
C216 .01uF
C250 .01uF
C257 .01uF
C256 .01uF
C232 .01uF
C251 .01uF
C258 .01uF
C50 .01uF
AMD
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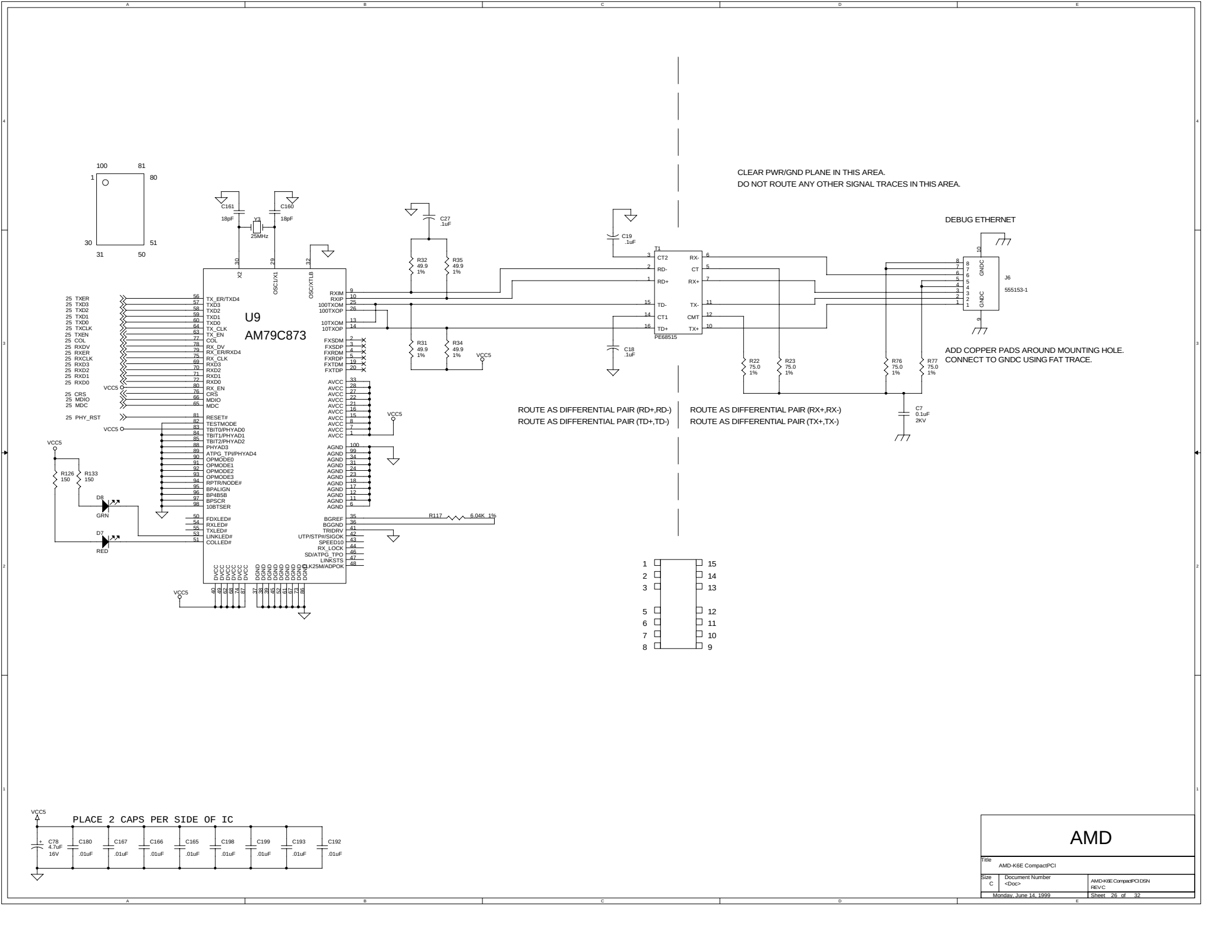
CLEAR PWR/GND PLANE IN THIS AREA.
DO NOT ROUTE ANY OTHER SIGNAL TRACES IN THIS AREA.
DEBUG ETHERNET
ADD COPPER PADS AROUND MOUNTING HOLE.
CONNECT TO GNDC USING FAT TRACE.
U9
AM79C873
PE68515
J6
555153-1
ROUTE AS DIFFERENTIAL PAIR (RD+,RD-)
ROUTE AS DIFFERENTIAL PAIR (TD+,TD-)
ROUTE AS DIFFERENTIAL PAIR (RX+,RX-)
ROUTE AS DIFFERENTIAL PAIR (TX+,TX-)
PLACE 2 CAPS PER SIDE OF IC
AMD
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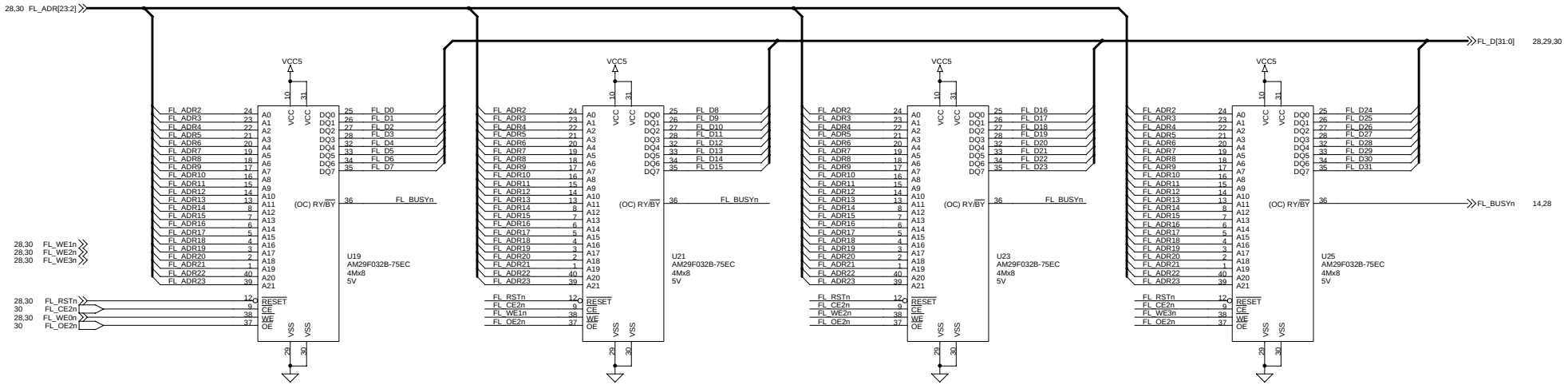

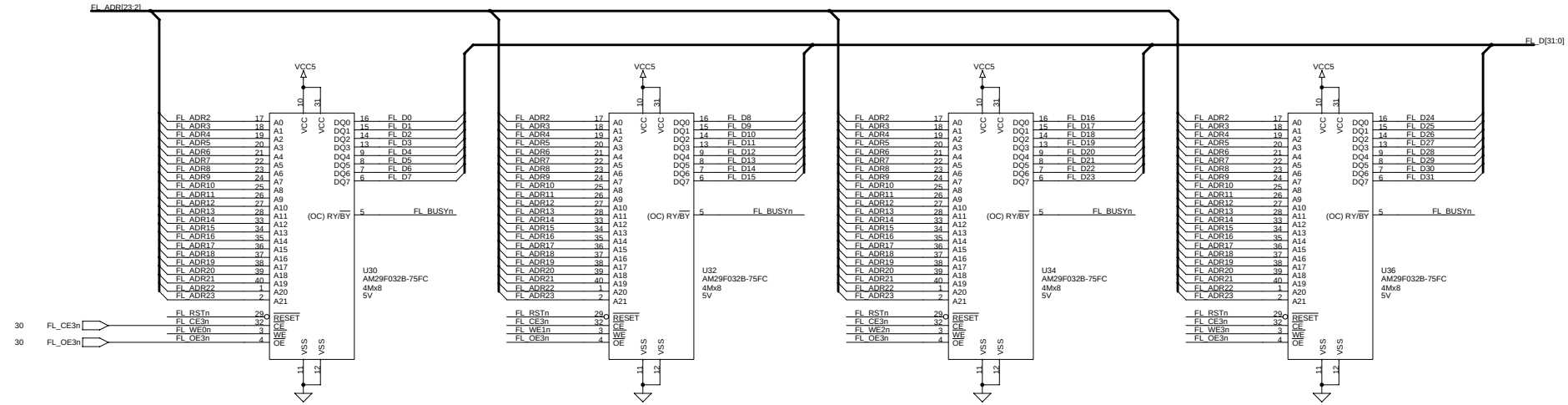

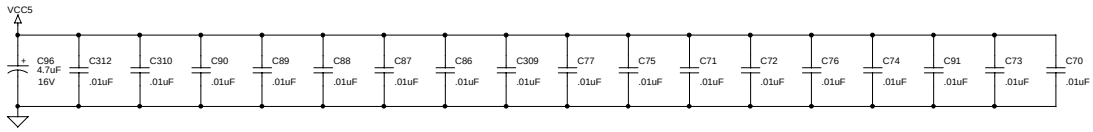

AMD

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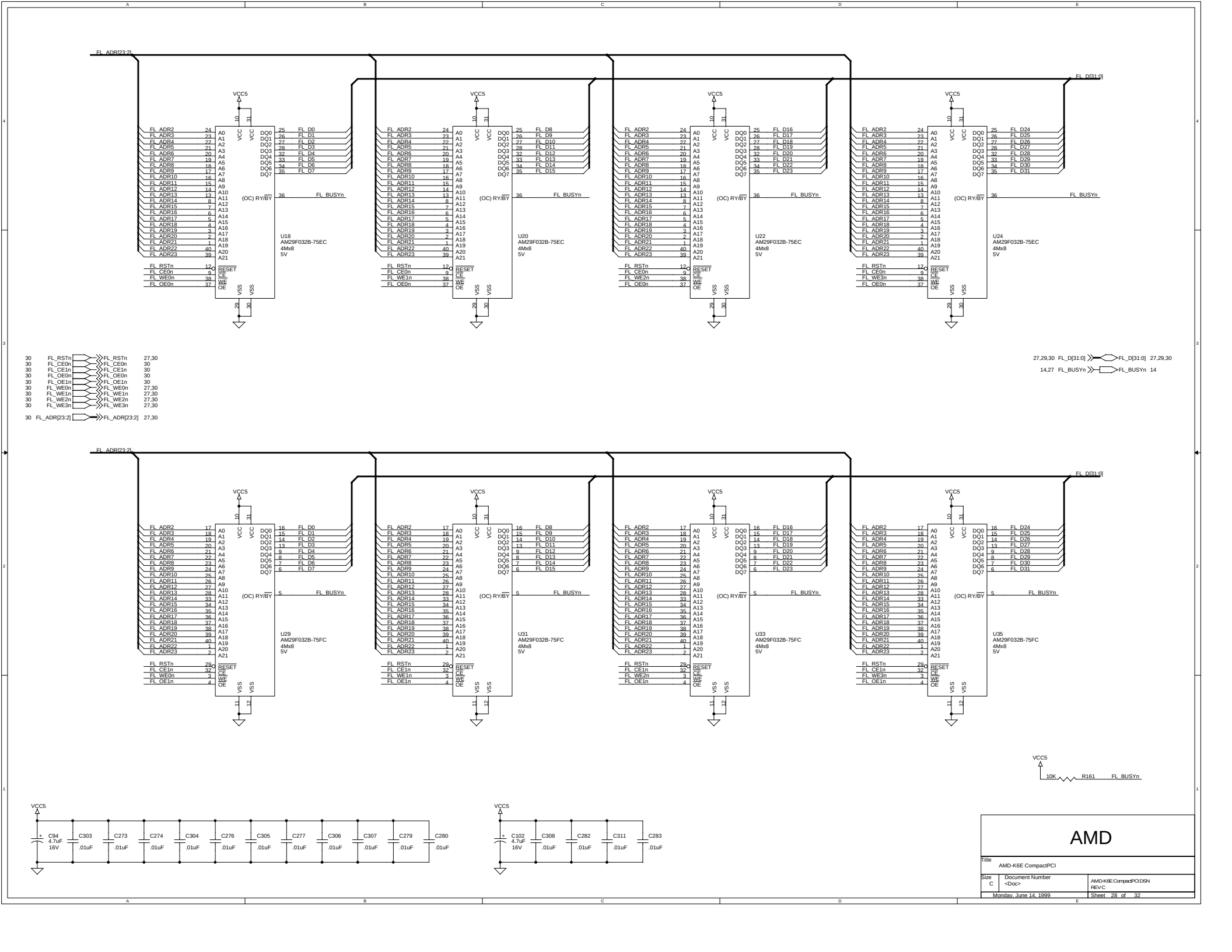
FL_ADR[23:2]
FL_D[31:0]
VCC5
U18
AM29F032B-75EC
4Mx8
5V
U20
AM29F032B-75EC
4Mx8
5V
U22
AM29F032B-75EC
4Mx8
5V
U24
AM29F032B-75EC
4Mx8
5V
(OC) RY/BY
FL_BUSYn
FL_RSTn
FL_CE0n
FL_WE0n
FL_OE0n
FL_WE1n
FL_WE2n
FL_WE3n
FL_CE1n
FL_OE1n
30 FL_RSTn FL_RSTn 27,30
30 FL_CE0n FL_CE0n 30
30 FL_CE1n FL_CE1n 30
30 FL_OE0n FL_OE0n 30
30 FL_OE1n FL_OE1n 30
30 FL_WE0n FL_WE0n 27,30
30 FL_WE1n FL_WE1n 27,30
30 FL_WE2n FL_WE2n 27,30
30 FL_WE3n FL_WE3n 27,30
30 FL_ADR[23:2] FL_ADR[23:2] 27,30
27,29,30 FL_D[31:0] FL_D[31:0] 27,29,30
14,27 FL_BUSYn FL_BUSYn 14
U29
AM29F032B-75FC
4Mx8
5V
U31
AM29F032B-75FC
4Mx8
5V
U33
AM29F032B-75FC
4Mx8
5V
U35
AM29F032B-75FC
4Mx8
5V
10K R161 FL_BUSYn
C94 4.7uF 16V
C303 .01uF
C273 .01uF
C274 .01uF
C304 .01uF
C276 .01uF
C305 .01uF
C277 .01uF
C306 .01uF
C307 .01uF
C279 .01uF
C280 .01uF
C102 4.7uF 16V
C308 .01uF
C282 .01uF
C311 .01uF
C283 .01uF
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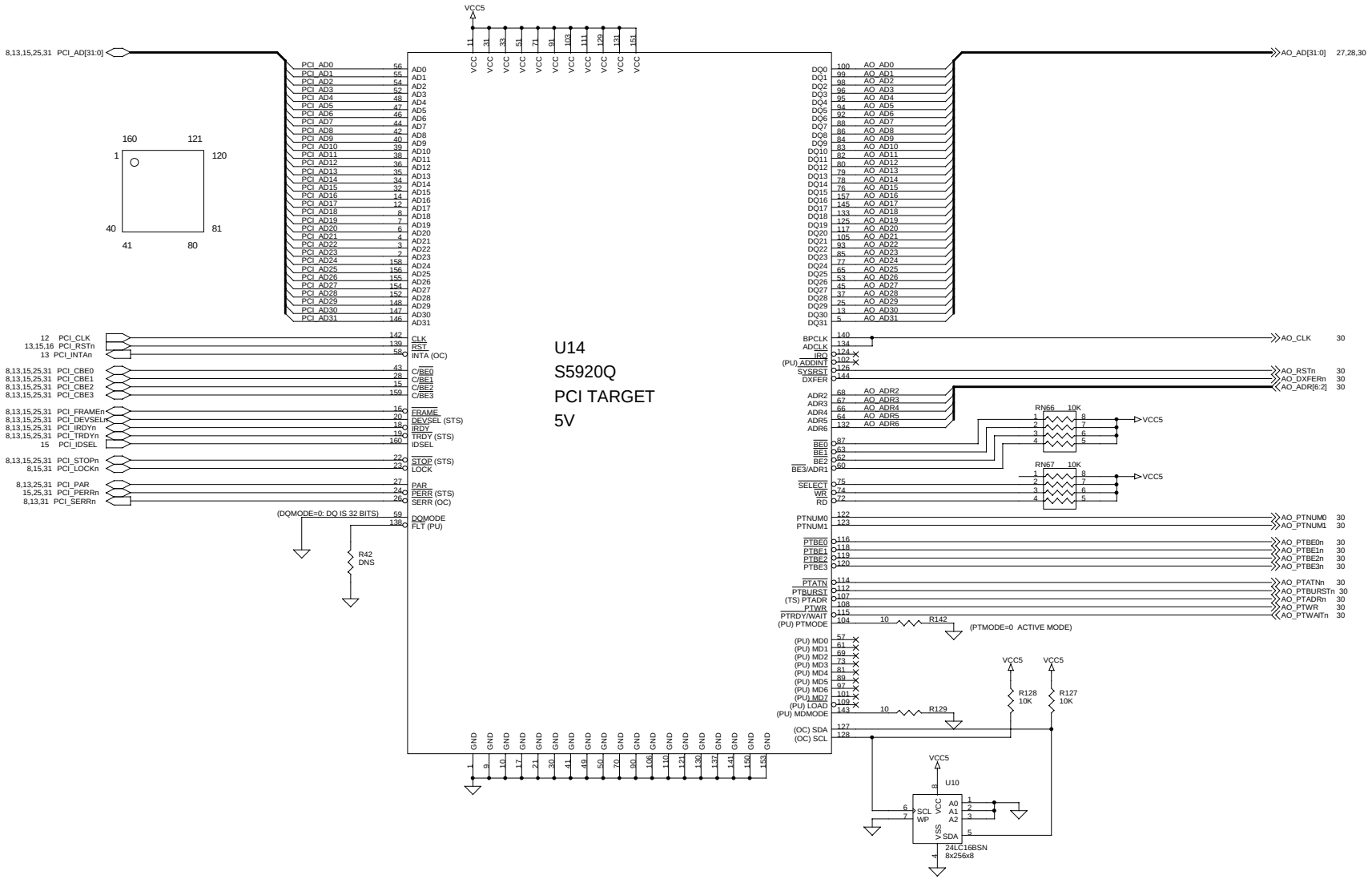
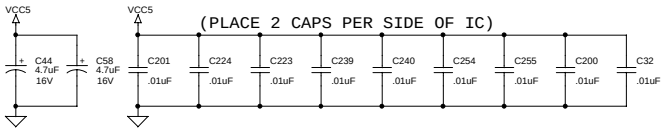
PCI BUS

ADD ON BUS





AMD

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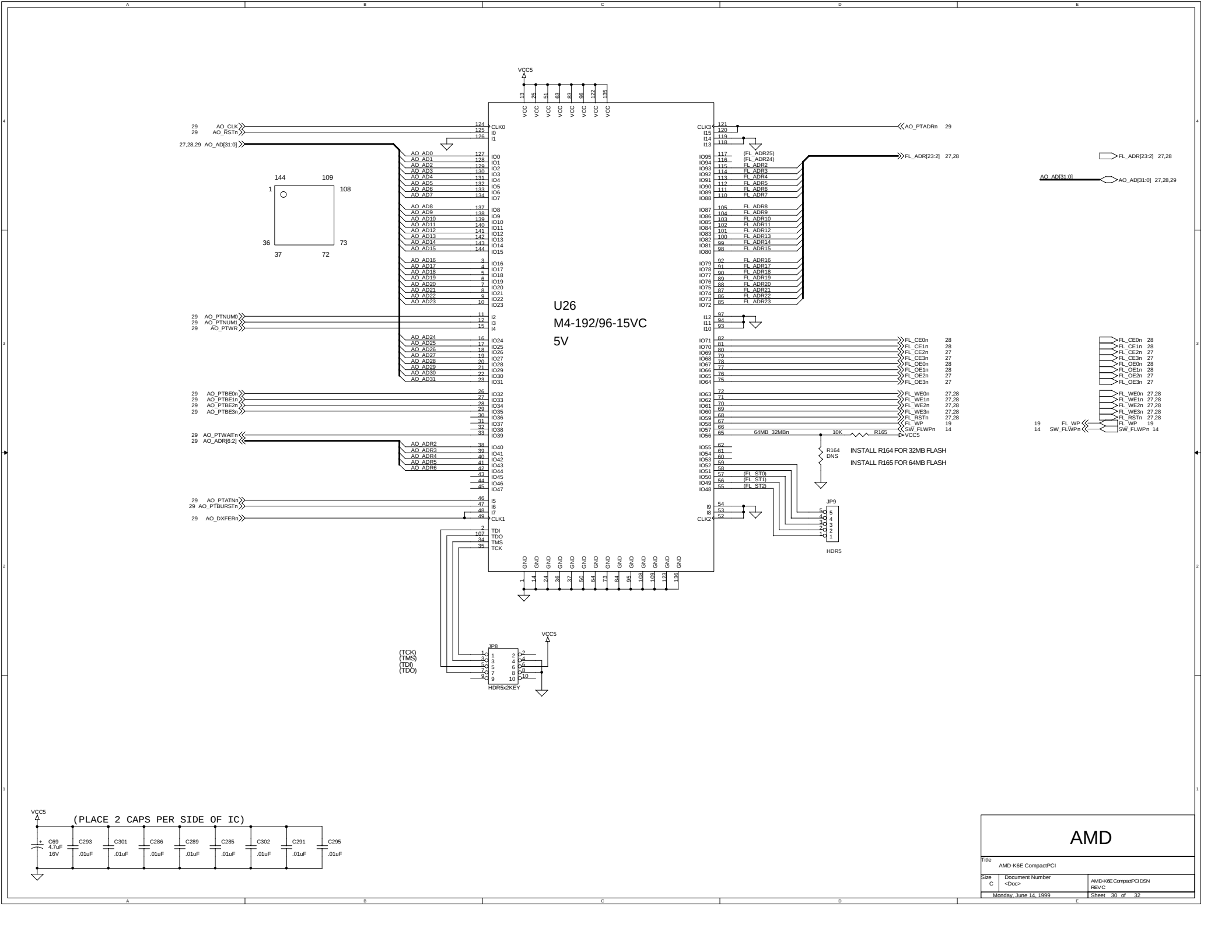

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REV C: ADDED PULLUPS TO SPCI_REQXn

U17
21150-AB
PCI TO PCI BRIDGE
3.3V
3V OR 5V IO

CLOCK LENGTH OF SPCI_CLKO7 MUST BE
6.5" PLUS LENGTH OF SPCI_CLKOX.

DISABLE SPCI_SCLK[6..0] IN SW
FOR SLAVE OPERATION

(PLACE 3 CAPS PER SIDE OF IC)

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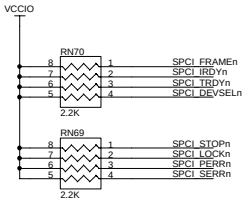
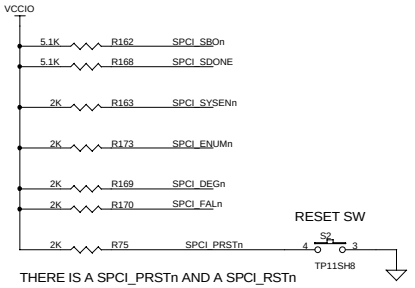
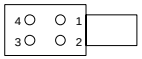
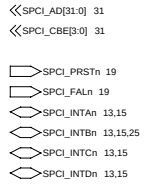
REV C: ADD PU/PD ON CPCI JTAG SIGNALS.





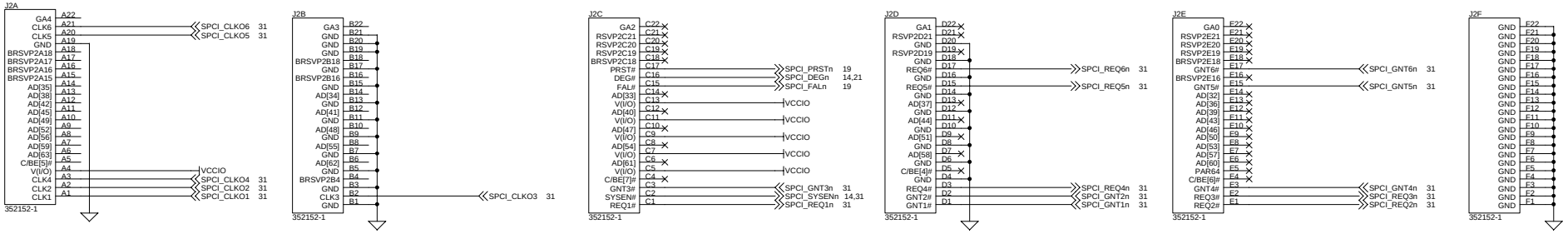
THERE IS A SPCI_PRSTn AND A SPCI_RSTn

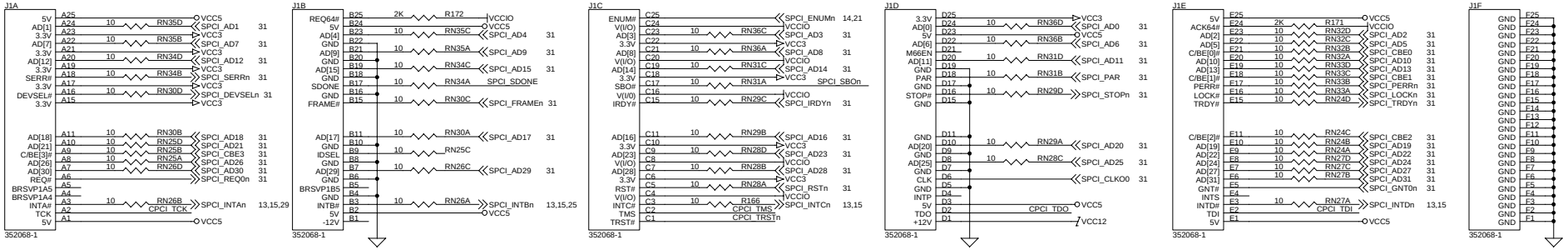


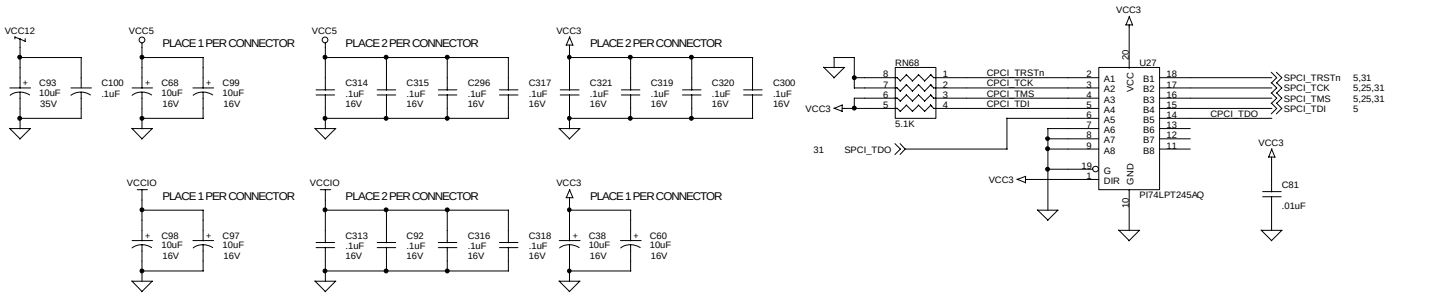


NOTE: CONNECTOR NUMBERING AND COMPACTPCI NUMBERING IS REVERSED!
SERIES RES TO BE PLACED WITHIN 15.2mm (0.6") OF SIGNAL CONNECTOR PIN
ROUTE CLKO[6..0] WITH MATCHED LENGTH TRACES TO WITHIN 0.5"

NOTE: SPCI INTERRUPTS GO INTO LOCAL PCI BUS.
NOTE: SPCI INTERRUPTS PULLED UP ON LOCAL PCI BUS.







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