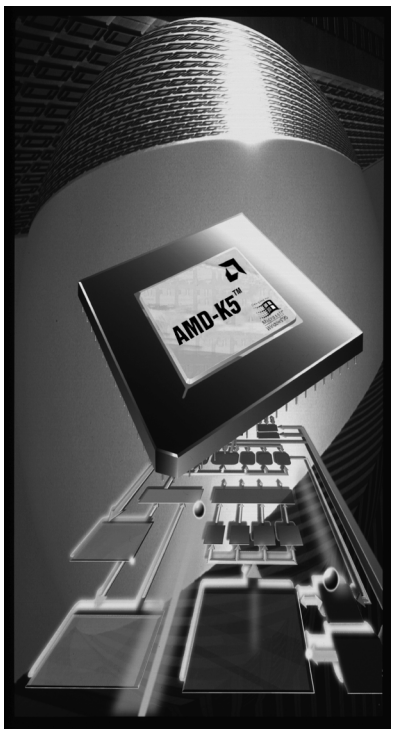
AMD



AMD-K5™ PROCESSOR

Software Development Guide Amendment

Publication # **20007** Rev: **D** Amendment/**1**
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Amendment Contents

The following changes and updates are included in this amendment to the *AMD-K5™ Processor Software Development Guide*:

- Global Pages
  - TLB flushing behavior is described
- Model-Specific Registers
  - Write allocate registers are added
- CPUID Instruction
  - Model 2 and model 3 are added
- RDMSR and WRMSR Instructions
  - Write allocate registers are added
- Hardware Configuration Register
  - Write allocate enable bit defined
  - Option 100 removed from the debug control field
- Table 4-5, Test Access Port (TAP) ID Code
  - Manufacturer location changed to bits 11–1
  - Least-significant bit defined as set to 1
- The Hardware Debug Tool section is modified
- Appendix A.3, AMD-K5 Model 1 Array Data Formats
  - Change the heading to Model 1, 2, and 3
- Implementation of Write Allocate
  - A description of write allocate
  - Programming details for write allocate

The following paragraph should be inserted on page 9 at the end of the Global Pages section that begins on page 8.

TLB Flushing

In models 1, 2, and 3 of the AMD-K5 processors with stepping level of 4 or greater, the processor flushes both the 4-Kbyte TLB and the 4-Mbyte TLB (including global entries) whenever the GPE bit in CR4 is set or reset. Model 0 and models 1, 2, and 3 with stepping level less than 4 do not flush the TLBs when the GPE bit is set or reset.

It is not necessary to load CR3 with the base address of the page directory in order to flush the TLBs on models 1, 2, and 3 of the AMD-K5 processors with stepping level of 4 or greater.

The following two sections on write allocate registers should be inserted after the section titled *Hardware Configuration Register (HWCR)* on page 28.

Write Allocate Top-of-Memory and Control Register (WATMCR)

The Write Allocate Top-of-Memory and Control Register (WATMCR) contains bits that enable write allocate range controls and a field to specify the top-of-memory address limit for write allocate operations. The WATMCR can be written or read with the WRMSR or RDMSR instruction when the ECX register contains the value 85h.

For details on the WATMCR, see "Implementation of Write Allocate in the AMD-K5 Processor" in this amendment.

Write Allocate Programmable Memory Range Register (WAPMRR)

The Write Allocate Programmable Memory Range Register (WAPMRR) contains fields that specify the top and bottom addresses of the programmable memory range. The WAPMRR can be written or read with the WRMSR or RDMSR instruction when the ECX register contains the value 86h.

For details on the WAPMRR, see "Implementation of Write Allocate in the AMD-K5 Processor" in this amendment.

Table 1-8 appears on page 29 in the section on the CPUID instruction. It has been updated to include information regarding model 2 and model 3 of the AMD-K5 processor.

Table 1-8A. CPU Clock Frequencies, Bus Frequencies, and P-Rating Strings

Family Code	Model Code	CPU Frequency (MHz)	CPU Bus Frequency (MHz)	P-Rating String ("PRxxx")[1]
5	0	75	50	PR75
		90	60	PR90
		100	66	PR100
	1	90	60	PR120
		100	66	PR133
	2	116.7	66	PR166
	3	133	66	PR200

Notes:

1. *The CPUID instruction does not return a P-Rating string.*

– *This table does not constitute product announcements. Instead, the information in the table represents possible product offerings. AMD will announce actual products based on availability and market demand.*

The following two bulleted items should appear at the end of the list on page 34.

- *85h*: Write Allocate Top-of-Memory and Control Register (WATMCR). This register contains bits that enable write allocate range controls and a field to specify the top-of-memory address limit for write allocate operations. For details on the WATMCR, see "Implementation of Write Allocate in the AMD-K5 Processor" in this amendment.
- *86h*: Write Allocate Programmable Memory Range Register (WAPMRR). This register contains fields that specify the top and bottom addresses of the programmable memory range. For details on the WAPMRR, see "Implementation of Write Allocate in the AMD-K5 Processor" in this amendment.

Figure 4-1 on page 71 is updated to include the write allocate enable bit, bit 4. Option 100 has been removed from the debug control field.

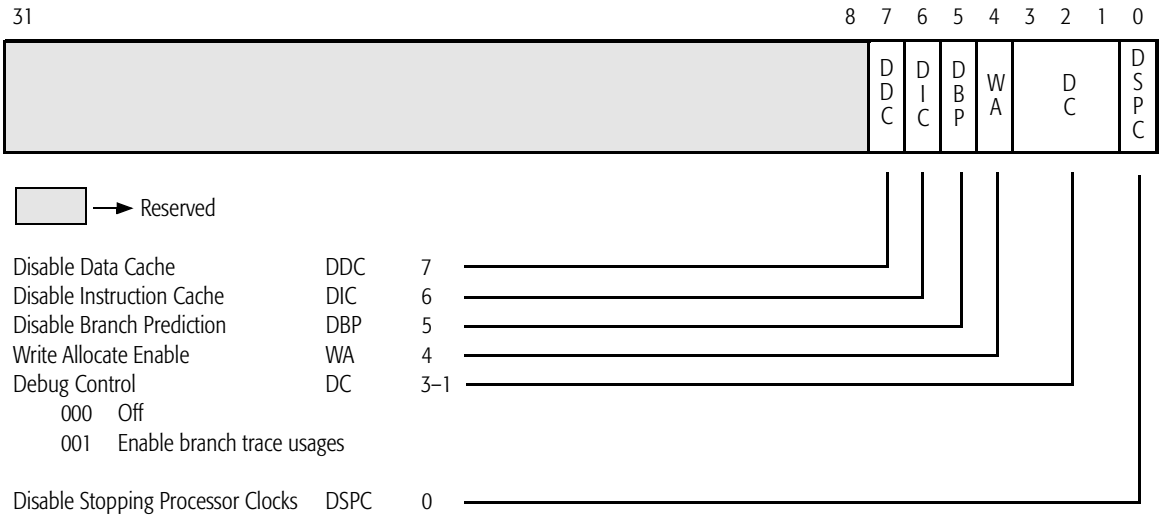

Figure 4-1. Hardware Configuration Register (HWCR)

Table 4-1 on page 72 is updated for bit 4, the write allocate enable bit, and for changing the HDT trap option in the debug control bits to reserved. A note regarding HDT is also removed from the table.

Table 4-1. Hardware Configuration Register (HWCR) Fields

Bit	Mnemonic	Description	Function
31–8	–	–	*reserved*
7	DDC	Disable Data Cache	Disables data cache. 0 = enabled, 1 = disabled.
6	DIC	Disable Instruction Cache	Disables instruction cache. 0 = enabled, 1 = disabled.
5	DBP	Disable Branch Prediction	Disables branch prediction. 0 = enabled, 1 = disabled.
4	WA	Write Allocate Enable	Enables write allocate. 0 = disabled, 1 = enabled
3–1	DC	Debug Control	Debug control bits: 000 Off (disable HWCR debug control). 001 Enable branch-tracing messages. See "Branch Tracing" on page 85. 010 *reserved* 011 *reserved* 100 *reserved* 101 *reserved* 110 *reserved* 111 *reserved*
0	DSPC	Disable Stopping Processor Clocks	Disables stopping of internal processor clocks in the Halt and Stop Grant states. 0 = enabled, 1 = disabled.

Table 4-5 on page 92 is updated to show that the least-significant bit (bit 0) is always set to 1.

Table 4-5. Test Access Port (TAP) ID Code

Version (Bits 31–28)	Bond Option (Bit 27)	Unused (Bits 26–24)	Part Number (Bits 23–12)	Manufacturer (Bits 11–1)	LSB (Bit 0)
Xh	Xb	000b	50Xh = Model 0 51Xh = Model 1 52Xh = Model 2 53Xh = Model 3	00000000001b	1b

Remove the second paragraph from the Hardware Debug Tool section on page 112.

Hardware Debug Tool (HDT)

The Hardware Debug Tool (HDT)—sometimes referred to as the debug port or Probe Mode—is a collection of signals, registers, and processor microcode that is enabled when external debug logic drives R/$\overline{S}$ Low or loads the processor's Test Access Port (TAP) instruction register with the USEHDT instruction.

The *AMD-K5 Model 1 Array Data Formats* section on page A-5 is changed to the *AMD-K5 Models 1, 2, and 3 Array Data Formats* section. The titles of all the tables in this section are also changed to reflect the addition of models 2 and 3.

A.3 AMD-K5 Models 1, 2, and 3 Array Data Formats

Table A-15. AMD-K5 Models 1, 2, and 3 ICACHE Physical Tags

Bits 31–21	Bit 20	Bits 19–0
0	Valid Bit	Tag (Physical Address 31–12)

Table A-16. AMD-K5 Models 1, 2, and 3 DCACHE Physical Tags

Bits 31–23	Bits 22–21	Bits 20–0
0	MESI (00=invalid, 01=shared, 10=modified, 11=exclusive)	Tag (Physical Address 31–11)

Table A-17. AMD-K5 Models 1, 2, and 3 DCACHE Data

Bits 31–0
Data

Table A-18. AMD-K5 Models 1, 2, and 3 DCACHE Linear Tag

Bit 28	Bit 27	Bit 26	Bit 25	Bit 24	Bit 23	Bit 22	Bit 21	Bits 20–0
WB	PCD	PWT	Dirty Bit	User/Supervisor Bit	R/W Bit	0	Linear Valid Bit	Tag

Table A-19. AMD-K5 Models 1, 2, and 3 ICACHE Instructions

Bit 25	Bit 24	Bit 23	Bit 22–21	Bit 20–13	Bit 12	Bit 11	Bit 10	Bit 9–8	Bit 7–0
prefix 1				byte (n + 8)	prefix 0				byte (n)
start bit	end bit	opcode bit	map (rops/mrom)	byte (n + 8)	start bit	end bit	opcode bit	map (rops/mrom)	byte (n)

Table A-20. AMD-K5 Models 1, 2, and 3 ICACHE Linear Tag

Bit 22	Bit 21	Bit 20	Bits 19–0
D	Linear Valid Bit	User/Supervisor Bit	Linear Address 31–12

Table A-21. AMD-K5 Models 1, 2, and 3 ICACHE Valid Bits

Bits 31–0
byte-valid bits

Table A-22. AMD-K5 Models 1, 2, and 3 ICACHE Branch Prediction

Bits 31–19	Bit 18	Bits 17–14	Bits 13–12	Bits 11–4	Bits 3–0
0	predicted taken	byte offset within block of last byte of predicted branch instruction	column of predicted target	index of predicted target	target byte

Table A-23. AMD-K5 Models 1, 2, and 3 TLB 4-Kbyte Linear Tag

Bits 31–20	Bit 19	Bit 18	Bit 17	Bit 16	Bit 15	Bits 14–0
0	global valid bit	dirty bit	user/supervisor bit	read/write bit	valid bit	tag (linear address 31–17)

Table A-24. AMD-K5 Models 1, 2, and 3 TLB 4-Kbyte Physical Page Frame

Bits 31–22	Bit 21	Bit 20	Bit 19–0
0	PCD bit	PWT bit	Page frame address (physical address 31–12)

Table A-25. AMD-K5 Models 1, 2, and 3 TLB 4-Mbyte Virtual Tag

Bits 31–15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9–0
0	Global valid bit	dirty bit	user/supervisor	read/write bit	valid bit	tag (linear address 31–22)

Table A-26. AMD-K5 Models 1, 2, and 3 TLB 4-Mbyte Physical Page Frame

Bits 31–12	Bit 11	Bit 10	Bits 9–0
0	PCD bit	PWT bit	Page frame address (physical address 31–22)

Implementation of Write Allocate in the AMD-K5 Processor

The AMD-K5 processor implements write allocate by providing a global write allocate enable bit and two memory range registers supporting up to three ranges. The write allocate enable bit is accessed using the hardware configuration register (HWCR), and the memory range registers are programmed via read/write model-specific register (MSR) instructions.

What is Write Allocate?

Write allocate is an operating mode of the AMD-K5 processor that causes cache write misses either to proceed as normal write misses or to be converted to data cache line fills followed by cache write hits. Use of the write allocate feature provides improved performance on repeat accesses to write-allocated data cache lines. The load/store unit in the processor determines whether each cache write miss is write-allocatable by whether it falls in or out of the ranges specified in the memory range registers.

A write allocate occurs when the processor has a pending memory write cycle to a cacheable line and the line does not currently reside in the L1 data cache. In this case, the processor performs a burst read cycle to fetch the data-cache line addressed by the pending write cycle. The data associated with the pending write cycle is merged with the recently-allocated data-cache line and stored in the processor's L1 data cache.

During the write allocate, a 32-byte burst read cycle is executed in place of a non-burst write cycle. While the burst read cycle generally takes longer to execute than the write cycle, performance gains are realized on subsequent write cycle hits to the write-allocated cache line. Due to the nature of software, memory accesses tend to occur within proximity of each other (principle of locality). The likelihood of additional write hits to the write-allocated cache line is quite high.

BIOS Programming Details

The steps required for programming write allocate on the AMD-K5 processor are as follows:

1. Check for the correct revision of the processor.
2. Setup the MSRs.
3. Enable write allocate.

Check for the Correct Revision of the Processor

Write allocate is supported only on Models 1, 2, and 3, with a Stepping of 4 or greater. Use the CPUID instruction (see the *AMD-K5 Processor Recognition* application note, order# 20734) to determine if the proper revision of the processor is present.

Setup the MSRs

Two new MSRs are defined to support write allocate. The MSRs are accessed using the RDMSR and WRMSR instructions (see "RDMSR and WRMSR" on page 34 of the *AMD-K5 Processor Software Development Guide*, order# 20007). The following index values in the ECX register access the new MSRs:

- *85h*: Write Allocate Top-of-Memory and Control Register
- *86h*: Write Allocate Programmable Memory Range Register

Three non-write-allocatable memory ranges are defined for use with the write allocate feature—one fixed range and two programmable ranges. The fixed memory range is 000A0000h–000FFFFFh and can only be enabled or disabled. One programmable memory range is xxxx0000h–yyyyFFFFh, where xxxx and yyyy are defined using bits 15–0 and bits 31–16 of MSR 86h respectively. The other programmable memory range is the top of memory. Top of memory is equal to or greater than zzzz0000h, where zzzz is defined using bits 15–0 of MSR 85h. The processor treats cache write misses that hit in any of these memory ranges as normal write misses and does not allocate a data cache line for them.

Bits 18–16 of MSR 85h control the enabling or disabling of the three write allocate memory ranges as follows:

- Bit 18: Top-of-Memory Control bit.

  0 = disabled (default)
  1 = enabled

- Bit 17: Programmable Range Enable bit
  0 = disabled (default)
  1 = enabled
- Bit 16: Fixed Range Enable bit
  0 = disabled (default)
  1 = enabled

Figure 1 and Figure 2 show the bit positions for these two new registers.

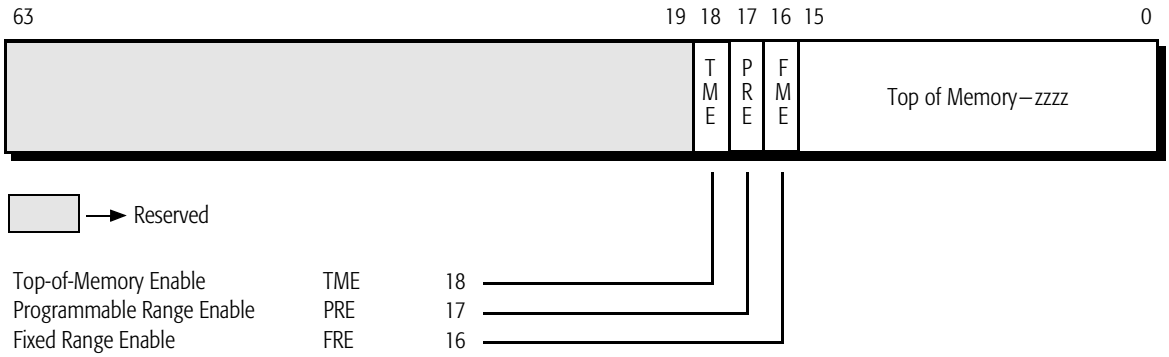

Figure 1. Write Allocate Top-of-Memory and Control Register

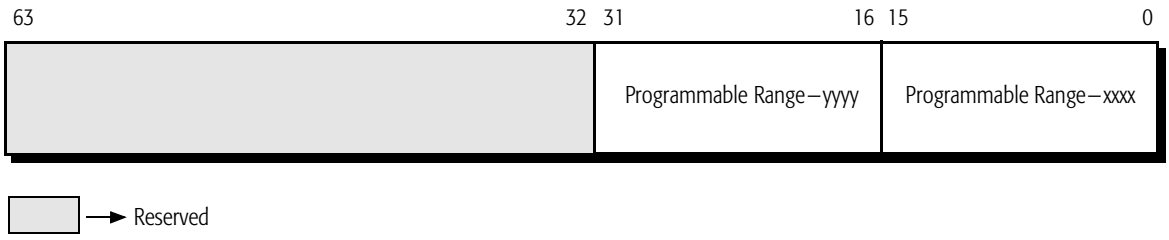

Figure 2. Write Allocate Programmable Memory Range Register

Enable Write Allocate Write allocate is enabled by setting bit 4 (WA) of the HWCR to 1. For more information on the HWCR, see the *AMD-K5 Processor Software Development Guide*, order# 20007. Figure 3 shows the revised definition of the Hardware Configuration Register.

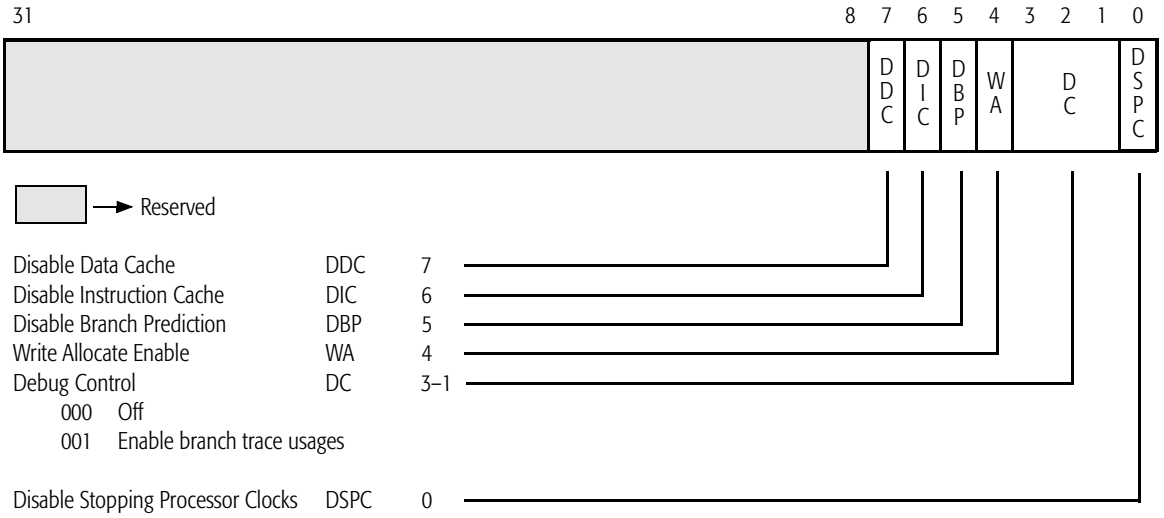

Figure 3. Hardware Configuration Register (HWCR)

For more information or to order literature, write to or call:

TOLL FREE: (800)222-9323
(512)602-5651
Advanced Micro Devices, Inc.
5204 East Ben White Blvd.
Mail Stop 604
Austin, Texas 78741
http://www.amd.com