E86 FAMILY

AMD Am486®DX Microprocessor

AMD

The AMD Am486DX Microprocessor Combines x86 Compatibility with Enhanced Performance

The AMD Am486DX microprocessor family are embedded versions of the enhanced Am486 microprocessor. Driven by development in the desktop PC market, these microprocessors are now available with support and lifetimes appropriate for the embedded market. The Am486DX enhances performance by incorporating a 16-Kbyte write-back cache implementation, flexible clock control, and enhanced SMM.

The Am486DX microprocessor cache allows write-back configuration through software and cacheable access control. On-chip cache lines are configurable as either write-through or write-back.

The CPU may be stopped under controlled conditions, allowing reduced power consumption during system inactivity. The SMM function is implemented with an industry standard two-pin interface.

PRODUCT HIGHLIGHTS

High Performance Design
- Improved cache structure supports industry-standard write-back cache
- Frequent instructions execute in one clock
- .35-micron CMOS process technology
- Dynamic bus sizing for 8-,16-, and 32-bit buses

High On-Chip Integration
- 16-Kbyte unified cache
- Floating-point unit
- Paged, virtual memory management

Enhanced System and Power Management
- Stop clock control for reduced power consumption
- Industry-standard 2-pin System Management Interrupt (SMI) for power management independent of processor operating mode and operating system
- Wide range of chipsets supporting SMM available to allow product differentiation
- Hardware compatibility with 66-, 100-, and 133-MHz operating frequencies

Complete 32-Bit Architecture
- Address and data buses
- All registers
- 8-, 16-, and 32-bit data types

Standard Features
- 3-V core with 5-V tolerant I/O
- Binary compatible with all Am486 family microprocessors
- Wide range of tool support available through the AMD FusionE86™ program

IEEE 1149.1 JTAG Boundary-Scan Compatibility
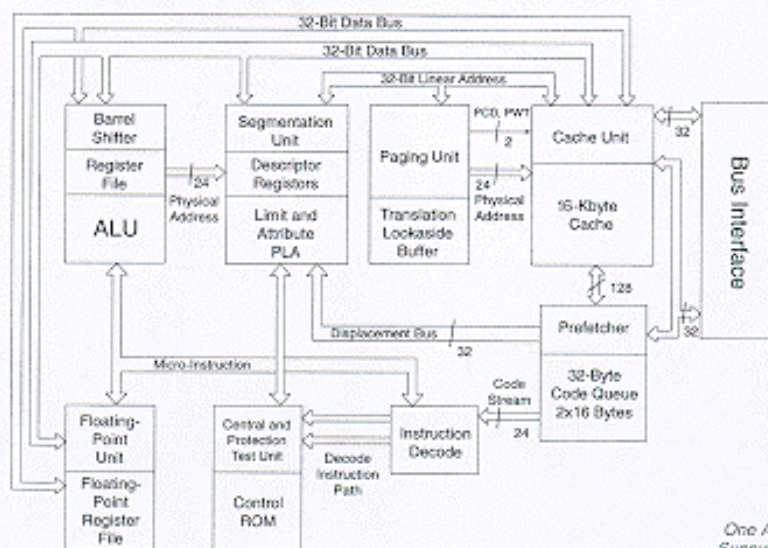
168-Pin PGA and 208-Pin SQFP Packaging

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The Am486DX microprocessor uses a 32-bit architecture with on-chip memory management and cache memory units. The instruction set includes the complete 486 microprocessor instruction set along with the extensions to serve the new extended applications. All software written for the 486 microprocessor and previous members of the x86 architectural family can run on the Am486DX microprocessor without modification.

The on-chip Memory Management Unit (MMU) is completely compatible with the 486 MMU. The MMU includes a segmentation unit and a paging unit. Segmentation allows management of the logical address space by providing easy data and code relocatibility and efficient sharing of global resources. The paging mechanism operates beneath segmentation and is transparent to the segmentation process. Paging is optional and can be divided into one or more 4-Kbyte segments. To implement a virtual memory system, the Am486DX microprocessor supports full restartability for all page and segment faults.

Am486DX Embedded Microprocessor

Related Literature:

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